Phase Locked-Loop with Decaying DC Transient Removal for Three-Phase Grids

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Abstract

Frequency and phase of the power grid, which are critical for reliable control and protection of grid-tied devices, are generally detected by the closed-loop phase locked-loop (PLL). In highly inductive high-voltage transmission systems, decaying DC (DDC) components with large amplitude can be easily introduced by load disturbances and/or grid abnormalities, leading to severe performance degradation of the PLL during the transient. Focusing on this issue, in this paper, modifications to the conventional synchronous reference frame (SRF)-PLL have been made to address the short-term disturbances including the DDC component, and the system operation is divided into the normal state and the DDC-transient state. The SRF-PLL is only adopted for the normal state where the DDC component is negligible. In the presence of a significant DDC component, as well as disturbances including negative-/zero-sequence components and harmonics, the weak effectiveness of the conventional SRF-PLL is proved, and an efficient DDC component extraction method, with a detection time of 0.5 grid cycle, is introduced for the three-phase system. The real-time amplitude and phase of the positive-sequence component can be efficiently extracted via the proposed scheme, by exploiting the transient signal properties in the dq-frame and assuming a constant grid frequency during the short transient. Finally, a proper design of switching logic has been proposed to allow for the fast and precise transition between the normal and the DDC-transient state, thereby ensuring high steady-state accuracy as well as short-term DDC transient immunity.

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Hardware-in-the-loop based experiments have been used to verify the effectiveness of the proposed PLL technique.

Keywords: decaying DC component, phase locked-loop, transient signal, unbalanced grid, harmonics

1. Introduction

Fast and accurate detection of grid amplitude and phase is of paramount importance for power system applications, including the control of electrical machines [1], measuring power quality phenomena and indices [2], islanding detection [3], and especially, high-performance control of grid-tied converters [4]. This is usually done by means of phase locked-loops (PLLs), [5, 6], either in the form of open-loop or closed-loop schemes. Over the past decades, there has been a rapid development of PLL techniques. Among many possibilities, the synchronous reference frame (SRF) based PLL, i.e., SRF-PLL, has been widely adopted in practice, owing to its simple implementation and satisfactory detection accuracy in many scenarios.

However, the traditional PLLs are insufficient to deal with several extreme cases in practice, e.g., when a significant decaying DC (DDC) component is present during the transient. The DDC component is introduced to the grid quantities by the fast switching of circuit topology (such as the grid fault and load shedding) in a highly inductive environment, such as the high-voltage overhead lines, high power generators, large transformers, and distribution networks with large inductive loads, since the non-negligible grid inductance hinders the sudden change of current [7]. In the event of a DDC transient, the phase detected by the traditional PLL is inaccurate with the presence of undesired oscillations, and an accurate detection requires a long dynamic response time.

There are several works in the literature attempting to achieve a fast phase synchronization in the event of a DDC transient. These methods, according to their implementations, can be either modification to a conventional PLL scheme, e.g., the modified enhanced PLL in [8], or specifically designed to remove the DDC component during transient, e.g., [7, 9]. Theoretically, the former has a more general structure and easier implementation, yet the detection speed or accuracy is not optimized. Conversely, owing to the embedded algorithm specifically tailored for DDC component detection, the latter has the potential to achieve faster and more precise detection re-

sults at the expense of slightly increased computational complexity, which can be anyway effectively addressed by the real-time controller.

Several methods are available in the literature as long as the accurate detection of the DDC component is the target. However, many methods, e.g., [10, 11, 12, 13, 14, 15], are not suitable for real-time control applications, which require not only a high detection performance in terms of precision and speed, but also a light computational burden limited by the controller performance. Indeed, these DDC detection methods, among many other alternatives, were developed and applied with the aim to facilitate grid fault analysis, relay design, and power system protection. Unlike these works, several attempts in the last few years provide simple yet feasible DDC component detection solutions optimized for the embedded controller. [16, 17] use analysis of empirical formula to derive detection methods based on high-order time-derivatives, which are highly susceptible to random noise. [18] and [19] designed an active power filter to eliminate the DDC current from the source based on detection results, realizing a response time of roughly one grid cycle. Based on mathematical analysis and time integrals, [20] realized DDC component detection within half grid cycle. These methods are easy to be digitally implemented, and can be calculated in real time with the common embedded controller, which is generally a digital signal processor (DSP).

Based on the aforementioned works, [9] proposed an open-loop amplitude-phase detection scheme for grid voltage considering the transient DDC component and harmonics, and has a response time of one grid cycle. An improved amplitude-phase detection scheme is proposed in [7] based on a variable integral length of the DDC detection algorithm, thereby allowing for a fast initial detection speed within half grid cycle and gradually increased detection precision. In that work, the grid unbalance is also considered, by decomposing the grid quantity into positive-, negative-, and zero-sequence components, and assuming non-zero negative- and zero-sequence components. Indeed, this consideration is more practical in the high-voltage transmission and distribution networks, where the X/R ratio is large to produce a significant DDC component, yet the harmonics are usually negligible. In a recent work [19], an open-loop detection scheme is developed to address the DDC transient with the possible presence of a DC offset. Since the addition of the DC offset will invalidate the half-wave symmetry of the DDC-free signal component, the developed algorithm requires slightly increased detection time. However, in the aforementioned works, the steady-state accuracy of

grid frequency and phase in the absence of the DDC transient cannot be guaranteed, due to the use of an open-loop detection scheme that presumes a fixed grid frequency. Indeed, this is an issue to be addressed if a DDC component detection algorithm is to be used in practice.

Focusing on the aforementioned limitation, this work presents a comprehensive solution for phase synchronization that deals with both the normal state operation and DDC transient event; also, the transition between the two states has been addressed. To this end, in this work, the conventional SRF-PLL scheme is served as the starting point for accurate phase detection, but is then integrated with the amplitude-phase detection algorithm that is able to quickly separate the DDC component during the transient. Detailed implementation of the two schemes and the proper switching logic that enables seamless transition are discussed. The proposed strategy allows for efficient phase detection in the possible presence of negative- and zero-sequence components, harmonics, and most importantly, DDC transients with a notable amplitude. Hardware-in-the-loop based experiments, considering the aforementioned disturbances and the frequency sudden change, have been used to show the effectiveness of the proposed method.

2. Normal-State Phase Detection based on SRF-PLL

2.1. Basic Principle

When the utility grid is operating in the ideal condition, the three-phase grid quantities (voltages/currents) are balanced. In this case, considering only the presence of positive-sequence components, the three-phase quantities can be formulated as

$$\mathbf{X}^{+}(t) = \begin{bmatrix} x_a^{+}(t) \\ x_b^{+}(t) \\ x_c^{+}(t) \end{bmatrix} = X^{+} \begin{bmatrix} \sin(\phi^{+}) \\ \sin(\phi^{+} - 2\pi/3) \\ \sin(\phi^{+} + 2\pi/3) \end{bmatrix} \tag{1}$$

$$\phi^{+} = \omega t + \theta^{+} \tag{2}$$

where $\mathbf{X}^{+}$ is the general grid quantity whose phase is to be detected, and the superscript + represents the positive-sequence quantity hereinafter. X^{+}, ϕ^{+}, and θ^{+} are the amplitude, real-time phase, and initial phase of the grid quantity, respectively, and $\theta^{+} \in [0, 2\pi)$. $\omega = 2\pi f$ (with f being the frequency in Hz) is the angular frequency of the grid in rad/s.

To obtain the phase (ϕ^+) and frequency (ω) information of the grid quantity, the SRF-PLL scheme can be adopted. With reference to the control diagram in Fig. 1, k_p and k_i are the proportional and integral gains of the PI controller, respectively. mod is the modulo operation that calculates the remainder after division; in this case, the phase is divided by 2π to obtain the final value within $[0, 2\pi)$. ω_s is the synchronous angular frequency of the grid. The *abc*/*dq* transformation matrix is given by

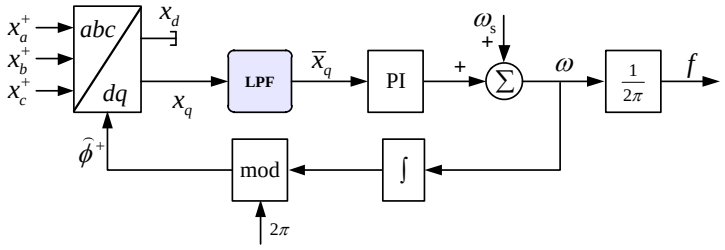

Figure 1: Structure of the traditional closed-loop SRF-PLL.

$$\mathbf{T}_{abc/dq} = \frac{2}{3}\begin{bmatrix} \sin\widehat{\phi^+} & \sin\left(\widehat{\phi^+} - 2\pi/3\right) & \sin\left(\widehat{\phi^+} + 2\pi/3\right) \\ \cos\widehat{\phi^+} & \cos\left(\widehat{\phi^+} - 2\pi/3\right) & \cos\left(\widehat{\phi^+} + 2\pi/3\right) \end{bmatrix} \tag{3}$$

During the closed-loop phase synchronization process, the PLL dynamically adjusts its output phase ($\widehat{\phi^+}$) through the PI controller, and tracks the time-variant phase of the grid quantity [see ϕ^+ in (2)] in real time. When $\widehat{\phi^+} = \phi^+$, the phase is synchronized, and the phase and frequency of the PLL output are those of the grid quantity.

By properly designing the low-pass filter in the PLL (see LPF block in Fig. 1), the grid imbalance (negative-/zero-sequence components) and harmonics can also be effectively addressed, at the expense of increased dynamic response time. However, the DDC transient possibly present in the grid will have a significant impact on the PLL performance, as will be discussed in the following.

2.2. Limitation of SRF-PLL during DDC Transient

Due to the large X/R ratio of the middle-/high-voltage grid system, a significant DDC component can be generated during the transient [7]. In

this section, a general grid quantity decomposition considering the presence of the DDC component is performed as the starting point.

Considering a general grid transient encompassing positive-, negative-, and zero-sequence components, harmonics, as well as DDC components, in compact form, the three-phase grid quantities $\mathbf{X}(t) = [x_a(t), x_b(t), x_c(t)]^{\mathrm{T}}$ can be written as

$$\mathbf{X}(t) = \mathbf{X}^{+}(t) + \mathbf{X}^{-}(t) + \mathbf{X}^{0}(t) + \mathbf{X}^{\mathrm{h}}(t) + \mathbf{X}^{\mathrm{ddc}}(t) \tag{4}$$

where the positive-sequence component $\mathbf{X}^{+}(t)$ is given by (1) and (2). The superscripts $-$ and 0 represent the negative- and zero-sequence components, respectively. $\mathbf{X}^{\mathrm{h}}(t)$ and $\mathbf{X}^{\mathrm{ddc}}(t)$ represent the harmonic and DDC components, respectively. These components can be expressed as

$$\mathbf{X}^{-}(t) = \begin{bmatrix} x_a^{-}(t) \\ x_b^{-}(t) \\ x_c^{-}(t) \end{bmatrix} = X^{-} \begin{bmatrix} \sin(\omega t + \theta^{-}) \\ \sin(\omega t + \theta^{-} + 2\pi/3) \\ \sin(\omega t + \theta^{-} - 2\pi/3) \end{bmatrix} \tag{5}$$

$$\mathbf{X}^{0}(t) = \begin{bmatrix} x_a^{0}(t) \\ x_b^{0}(t) \\ x_c^{0}(t) \end{bmatrix} = X^{0} \begin{bmatrix} \sin(\omega t + \theta^{0}) \\ \sin(\omega t + \theta^{0}) \\ \sin(\omega t + \theta^{0}) \end{bmatrix} \tag{6}$$

$$\begin{aligned} \mathbf{X}^{\mathrm{h}}(t) = \sum_{n=3,5,7,\ldots} \mathbf{X}_n(t) = \sum_{n=3,5,7,\ldots} X_n^{+} \begin{bmatrix} \sin(n\omega t + \theta_n^{+}) \\ \sin\left[n\left(\omega t - \frac{2\pi}{3}\right) + \theta_n^{+}\right] \\ \sin\left[n\left(\omega t + \frac{2\pi}{3}\right) + \theta_n^{+}\right] \end{bmatrix} \\ + \sum_{n=3,5,7,\ldots} X_n^{-} \begin{bmatrix} \sin(n\omega t + \theta_n^{-}) \\ \sin\left[n\left(\omega t + \frac{2\pi}{3}\right) + \theta_n^{-}\right] \\ \sin\left[n\left(\omega t - \frac{2\pi}{3}\right) + \theta_n^{-}\right] \end{bmatrix} \end{aligned} \tag{7}$$

$$\mathbf{X}^{\mathrm{ddc}}(t) = \begin{bmatrix} x_a^{\mathrm{ddc}}(t) \\ x_b^{\mathrm{ddc}}(t) \\ x_c^{\mathrm{ddc}}(t) \end{bmatrix} = \begin{bmatrix} X_a^{\mathrm{ddc}} e^{-\sigma_a t} \\ X_b^{\mathrm{ddc}} e^{-\sigma_b t} \\ X_c^{\mathrm{ddc}} e^{-\sigma_c t} \end{bmatrix} \tag{8}$$

where X^{-} and X^{0} are negative- and zero-sequence amplitudes, respectively. θ^{-} and θ^{0} are negative- and zero-sequence initial phases, respectively. $X_n^{\pm}$ and $\theta_n^{\pm}$ are the positive-/negative-sequence amplitude and phase of nth order harmonic, respectively. In accordance with the general case in practice, only odd harmonics are considered here for simplicity. X_k^{ddc} and σ_k are the amplitude and decay coefficient of the DDC component in phase k, respectively, and $k = a, b, c$.

In a more general situation, multiple DDC components with different amplitudes/decay coefficients can be simultaneously present. As proved by mathematical induction [7], these components can be anyway simplified into a single equivalent DDC component, thereby reducing the analysis and computational complexity.

If the same transformation (3) is applied to the compound transient signal (4), it is obvious that the DDC component in the physical domain cannot be converted into the form of constants or standard trigonometric functions in the *dq*-frame. Indeed, its counterpart appears in the *dq*-frame as the decaying AC component, which cannot be effectively mitigated by the LPF in Fig. 1. In this case, the detected phase will exhibit significant oscillations for several grid periods, until the effect of the DDC component is notably reduced, i.e., when the amplitude of the DDC component decays below a certain level. This result should be improved by using a more efficient detection scheme.

3. Amplitude-Phase Detection during DDC Transient

3.1. DDC Component Separation

During the DDC transient, the primary target is to achieve a fast detection speed of transient components to support the converter control, fault detection, grid protection, etc., thereby ensuring the safety and stability of converters and power grids. Accordingly, the grid frequency is assumed to be constant during this procedure, and the accurate frequency and phase detection using the traditional PLL scheme will be delayed to the normal condition, where the DDC component is negligible.

In the transient signal model (4), sequence components are in the form of sinusoidal waves. Hence, the DDC quantities with unaltered polarities can be extracted by utilizing the half-wave symmetry of sinusoidal waves, i.e.,

$$\begin{cases} \mathbf{X}^{+}(t) + \mathbf{X}^{+}(t - T/2) = 0 \\ \mathbf{X}^{-}(t) + \mathbf{X}^{-}(t - T/2) = 0 \\ \mathbf{X}^{0}(t) + \mathbf{X}^{0}(t - T/2) = 0 \\ \mathbf{X}^{\mathrm{h}}(t) + \mathbf{X}^{\mathrm{h}}(t - T/2) = 0 \end{cases} \tag{9}$$

where T is the grid period, which is the inverse of grid frequency f.

An intermediate variable $\mathbf{X}^{r}$ is defined as the summation of the three-phase signal and its half-grid-period delay, as

$$\mathbf{X}^{r}(t) = \mathbf{X}(t) + \mathbf{X}(t - T/2) \tag{10}$$

Then, by combining (4), (8), (9), and (10), the sequence components in $\mathbf{X}$ can be eliminated. Accordingly, the three-phase DDC component in the compound signal $\mathbf{X}$ can be obtained as

$$\mathbf{X}^{\mathrm{ddc}}(t) = \left(\mathbf{E} + e^{\frac{T}{2}\boldsymbol{\sigma}}\right)^{-1} \mathbf{X}^{r}(t) \tag{11}$$

where $\boldsymbol{\sigma}$ is the intrinsic parameter matrix of the DDC component given by $\boldsymbol{\sigma} = \mathrm{diag}\left(\begin{bmatrix}\sigma_{\mathrm{a}} & \sigma_{\mathrm{b}} & \sigma_{\mathrm{c}}\end{bmatrix}\right)$, and $\mathbf{E}$ is the 3-by-3 identity matrix.

Calculation of the DDC component by (11) requires the information on decay coefficients matrix, $\boldsymbol{\sigma}$. This can be obtained phase-by-phase using the time integral method, [20, 7]. For phase k ($k = a, b, c$) element of $\mathbf{X}^r$, definite integrals over time L and $2L$ ($L > 0$) are performed, giving rise to

$$A_{k1} = \int_{t-L}^{t} x_k^r(t)\,\mathrm{d}t = \frac{X_k^{\mathrm{ddc}}}{\sigma_k}\left(1 + e^{\frac{\sigma_k T}{2}}\right)\left(e^{\sigma_k L} - 1\right)e^{-\sigma_k t} \tag{12}$$

$$A_{k2} = \int_{t-2L}^{t} x_k^r(t)\,\mathrm{d}t = \frac{X_k^{\mathrm{ddc}}}{\sigma_k}\left(1 + e^{\frac{\sigma_k T}{2}}\right)\left(e^{2\sigma_k L} - 1\right)e^{-\sigma_k t} \tag{13}$$

Combination of (12) and (13) gives the phase-k DDC decay coefficient as

$$\sigma_k = \frac{1}{L}\ln\left(A_{k2}/A_{k1} - 1\right) \tag{14}$$

A suitable selection of the integral length L is of paramount importance for DDC detection speed and accuracy. A short integral period is conducive to achieving a fast response, yet a long period enhances suppression of the random sampling noise. A variable integral solution [7] can be used to optimize both the transient and steady-state performances. Specifically, at the beginning of transient, this solution achieves a rough yet fast detection speed based on the allowable minimum interval, with the aim to quickly determine the subsequent critical actions (e.g., performing active compensation or converter fault ride-through); the integral interval is then extended in real time until its upper limit, reducing the random noise in long-term operation.

Besides, although the proposed solution presumes a fixed frequency before and after the disturbance, the effect of frequency change on the detected phase is generally negligible during the transient due to the twofold effect that the grid frequency fluctuates within a narrow range limited by the grid code, and that the slight frequency change will have an insignificant impact on the signal constitutes excluding the DDC component. The effectiveness of the proposed solution in the case of sudden frequency change will be proven in Section 5.

3.2. Positive Sequence Component Extraction

To separate the positive-sequence component, the Park's transformation is first applied to the three-phase transient signal, giving rise to

$$\mathbf{X}_{dq}(t) = \mathbf{T}^{+}_{3\mathrm{s}/2\mathrm{r}}\mathbf{X}(t) \tag{15}$$

where $\mathbf{X}_{dq}(t) = \begin{bmatrix} x_d(t) & x_q(t) \end{bmatrix}^{\mathrm{T}}$

$$\mathbf{T}^{+}_{3\mathrm{s}/2\mathrm{r}} = \frac{2}{3}\begin{bmatrix} \sin\omega t & \sin(\omega t - 2\pi/3) & \sin(\omega t + 2\pi/3) \\ \cos\omega t & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \end{bmatrix}$$

Here, the grid angular frequency ω in the steady state is used to generate the reference phase of the dq-frame. The transformation is different from the previous case in (3), where the detected grid phase is used directly as the reference phase of transformation. After this *abc-dq* transformation, $\mathbf{X}(t)$ in positive-sequence dq-frame is decomposed as

$$\begin{aligned} x_d(t) &= X^{+}\cos\theta^{+} - \; x_d^{\mathrm{even}}(t) \quad + \; x_d^{\mathrm{ddc}}(t) \\ x_q(t) &= \underbrace{X^{+}\sin\theta^{+}}_{\mathrm{DC}} + \; \underbrace{x_q^{\mathrm{even}}(t)}_{\text{even harmonics}} \quad + \; \underbrace{x_q^{\mathrm{ddc}}(t)}_{\text{decaying AC}} \end{aligned} \tag{16}$$

where (with $m = 0, 1, 2, \ldots$)

$$\begin{aligned} x_d^{\mathrm{even}}(t) = {} & X^{-}\cos\left(2\omega t + \theta^{-}\right) \\ & - \sum_{n=6m+1} X_n^{+}\cos\left[(n-1)\,\omega t + \theta_n^{+}\right] + \sum_{n=6m-1} X_n^{+}\cos\left[(n+1)\,\omega t + \theta_n^{+}\right] \\ & + \sum_{n=6m+1} X_n^{-}\cos\left[(n+1)\,\omega t + \theta_n^{-}\right] - \sum_{n=6m-1} X_n^{-}\cos\left[(n-1)\,\omega t + \theta_n^{-}\right] \\ x_q^{\mathrm{even}}(t) = {} & X^{-}\sin\left(2\omega t + \theta^{-}\right) \\ & + \sum_{n=6m+1} X_n^{+}\sin\left[(n-1)\,\omega t + \theta_n^{+}\right] + \sum_{n=6m-1} X_n^{+}\sin\left[(n+1)\,\omega t + \theta_n^{+}\right] \\ & + \sum_{n=6m+1} X_n^{-}\sin\left[(n+1)\,\omega t + \theta_n^{-}\right] + \sum_{n=6m-1} X_n^{-}\sin\left[(n-1)\,\omega t + \theta_n^{-}\right] \end{aligned} \tag{17}$$

$$\begin{aligned} x_d^{\mathrm{ddc}}(t) = {} & \frac{2}{3}\left[X_a^{\mathrm{ddc}}e^{-\sigma_a t}\sin\omega t + X_b^{\mathrm{ddc}}e^{-\sigma_b t}\sin(\omega t - 2\pi/3)\right. \\ & \left. + X_c^{\mathrm{ddc}}e^{-\sigma_c t}\sin(\omega t + 2\pi/3)\right] \\ x_q^{\mathrm{ddc}}(t) = {} & \frac{2}{3}\left[X_a^{\mathrm{ddc}}e^{-\sigma_a t}\cos\omega t + X_b^{\mathrm{ddc}}e^{-\sigma_b t}\cos(\omega t - 2\pi/3)\right. \\ & \left. + X_c^{\mathrm{ddc}}e^{-\sigma_c t}\cos(\omega t + 2\pi/3)\right] \end{aligned} \tag{18}$$

In (16), the DC components are counterparts of positive-sequence components in the *abc*-frame, the even harmonics are counterparts of the negative-sequence base-frequency component and positive-/negative-sequence odd harmonics in *abc*-frame, and the decaying AC waves correspond to DDC components in *abc*-frame. The correspondence of these quantities is illustrated in Fig. 2.

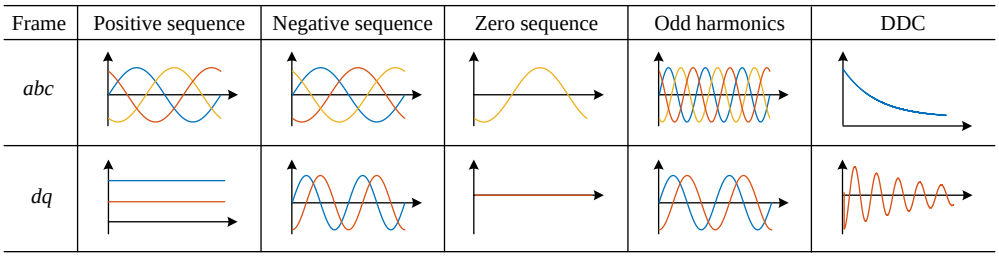

Figure 2: Correspondence of *abc*- and *dq*-frame quantities.

The even harmonics in *dq*-frame can be canceled via full-wave symmetry of the sinusoidal signal, i.e., their time integral over half grid period is zero. However, as previously discussed, the decaying AC component cannot be simply removed by a moving average filter, thus causing detection errors when the traditional PLL schemes are used. Conversely, if this component can be precisely determined during the transient, specific countermeasures can be taken to alleviate its effect. To this end, the decaying AC components in (16) are analytically calculated first as [7]

$$\begin{aligned}\int_{t-\frac{T}{2}}^{t} x_d^{\mathrm{ddc}}(t)\,dt &= -\mathbf{H}\left(\boldsymbol{\sigma}\mathbf{T}_{\sin}+\omega\mathbf{T}_{\cos}\right)\mathbf{X}^r\\ \int_{t-\frac{T}{2}}^{t} x_q^{\mathrm{ddc}}(t)\,dt &= -\mathbf{H}\left(\boldsymbol{\sigma}\mathbf{T}_{\cos}-\omega\mathbf{T}_{\sin}\right)\mathbf{X}^r\end{aligned} \tag{19}$$

where $\mathbf{H}=\frac{2}{3}\begin{bmatrix}\frac{1}{\omega^2+\sigma_a^2} & \frac{1}{\omega^2+\sigma_b^2} & \frac{1}{\omega^2+\sigma_c^2}\end{bmatrix}$

$$\mathbf{T}_{\sin}=\mathrm{diag}\left(\begin{bmatrix}\sin(\omega t) & \sin(\omega t-2\pi/3) & \sin(\omega t+2\pi/3)\end{bmatrix}\right)$$

$$\mathbf{T}_{\cos}=\mathrm{diag}\left(\begin{bmatrix}\cos(\omega t) & \cos(\omega t-2\pi/3) & \cos(\omega t+2\pi/3)\end{bmatrix}\right)$$

Hence, the DC component in (16) is calculated as

$$
\begin{aligned}
X^{+}\cos\theta^{+} &= \frac{2}{T}\left[\int_{t-\frac{T}{2}}^{t} x_d\left(t\right)dt - \int_{t-\frac{T}{2}}^{t} x_d^{\mathrm{ddc}}\left(t\right)dt\right] \\
&= \frac{2}{T}\left[\int_{t-\frac{T}{2}}^{t} x_d\left(t\right)dt + \mathbf{H}\left(\sigma\mathbf{T}_{\sin} + \omega\mathbf{T}_{\cos}\right)\mathbf{X}^{r}\right] \\
X^{+}\sin\theta^{+} &= \frac{2}{T}\left[\int_{t-\frac{T}{2}}^{t} x_q\left(t\right)dt - \int_{t-\frac{T}{2}}^{t} x_q^{\mathrm{ddc}}\left(t\right)dt\right] \\
&= \frac{2}{T}\left[\int_{t-\frac{T}{2}}^{t} x_q\left(t\right)dt + \mathbf{H}\left(\sigma\mathbf{T}_{\cos} - \omega\mathbf{T}_{\sin}\right)\mathbf{X}^{r}\right]
\end{aligned}
\tag{20}
$$

This gives the positive-sequence component of $\mathbf{X}$ as

$$
\begin{aligned}
\mathbf{X}^{+} &= \mathbf{T}_{\mathrm{2r/3s}}^{+}\begin{bmatrix} X^{+}\cos\theta^{+} \\ X^{+}\sin\theta^{+}\end{bmatrix} \\
&= \frac{2}{T}\mathbf{T}_{\mathrm{2r/3s}}^{+}\left(\int_{t-\frac{T}{2}}^{t}\mathbf{X}_{dq}dt + \begin{bmatrix}\mathbf{H}\left(\boldsymbol{\sigma}\mathbf{T}_{\sin} + \omega\mathbf{T}_{\cos}\right)\mathbf{X}^{r} \\ \mathbf{H}\left(\boldsymbol{\sigma}\mathbf{T}_{\cos} - \omega\mathbf{T}_{\sin}\right)\mathbf{X}^{r}\end{bmatrix}\right)
\end{aligned}
\tag{21}
$$

where

$$
\mathbf{T}_{\mathrm{2r/3s}}^{+} = \begin{bmatrix} \sin\omega t & \cos\omega t \\ \sin\left(\omega t - 2\pi/3\right) & \cos\left(\omega t - 2\pi/3\right) \\ \sin\left(\omega t + 2\pi/3\right) & \cos\left(\omega t + 2\pi/3\right)\end{bmatrix}
$$

Here, the extraction of the positive-sequence component is shown as an example for further phase detection. However, the negative-sequence component can be similarly extracted if the pertinent transformation is applied to the compound signal followed by proper processing. The zero-sequence component can be simply extracted by subtracting the DDC component from the compound signal, [7], owing to the symmetry of AC signals.

3.3. Amplitude-Phase Detection

Once the sequence components are detected, the amplitude and phase can be calculated accordingly, [7]. For brevity, only the phasor calculation of the positive-sequence component is illustrated here as an example. During the calculation, the grid frequency is considered to be constant; however, it will be shown in Section 5 that the effect of frequency change on the

detected phase is negligible in practice. The amplitude and phase of $\mathbf{X}^+$ can be obtained based on the DC component result in (20) as

$$\begin{cases} X^+ = \sqrt{\left(X^+\cos\theta^+\right)^2 + \left(X^+\sin\theta^+\right)^2} \\ \theta^+ = \arctan\left(\dfrac{X^+\sin\theta^+}{X^+\cos\theta^+}\right) \end{cases} \tag{22}$$

The block diagram of the amplitude-phase detection scheme is summarized in Fig. 3. With this parallel structure, the positive-sequence component can be extracted in nearly half the grid period ($T/2$). Hence, for the results in (20) to be fully valid, a response time of half grid period is required, i.e., 10 ms for a 50 Hz grid.

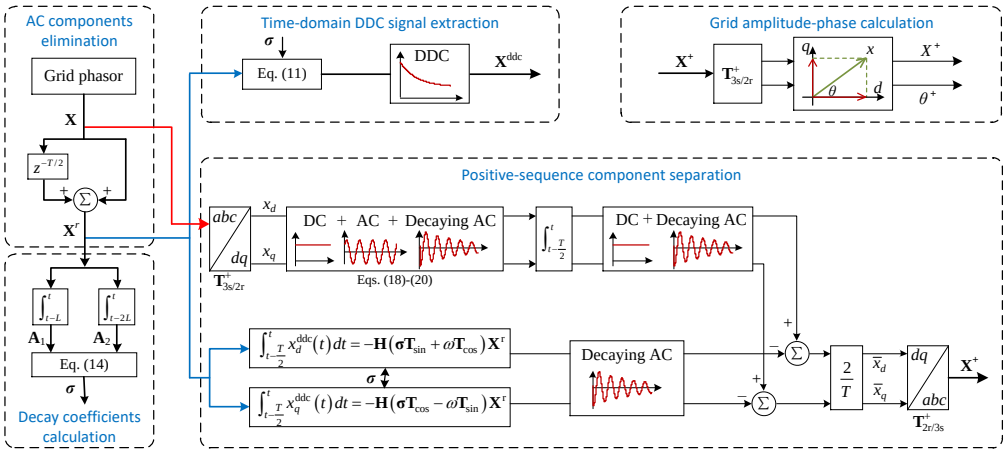

Figure 3: Schematic diagram of positive-sequence component detection in the presence of a DDC transient.

4. Compound Phase Detection considering State Transition

As previously discussed, the DDC-transient state algorithm considers the grid frequency to be constant in order to effectively simplify the calculation and shorten the detection time. When the system resumes the steady-state operation, the detection algorithm should be switched to the conventional PLL algorithm according to the zero-error requirement on steady-state performance. To this end, the reliable detection criterion for a DDC transient

is established first in this section, followed by the development of a suitable switching logic that enables a seamless transition between two phase detection schemes.

4.1. DDC Transient Detection Criterion

DDC components only exist during the transient. If the calculation results of (12) and (13) approach zero simultaneously, the system is in steady state, and the pertinent detection algorithm does not need to consider the influence of DDC components; otherwise, the DDC influence should be considered for accurate amplitude-phase detection.

The aforementioned condition can be equivalently converted to the comparison between the current sample and the sampled values obtained before half and one grid cycle. Indeed, if the steady-state condition is nearly satisfied, the half-wave symmetry and full-wave symmetry conditions of the detected signal are valid. To identify a DDC transient event for phase k, the pertinent state signal S_k can be defined as (with $X_{k,\mathrm{th}}$ being a predefined detection threshold)

$$S_k = \begin{cases} 0, & if \ \ |x_k(t) - x_k(t-T)| < X_{k,\mathrm{th}} \\ & and \ \ |x_k(t) + x_k(t-T/2)| < X_{k,\mathrm{th}} \\ 1, & otherwise \end{cases} \tag{23}$$

The DDC transient is detected if the state signal S_k is 1, and vice versa. This value should be properly chosen to compromise between detection speed and accuracy, namely, it should be large enough to avoid possible misoperations caused by random noise, meanwhile the value should be within a certain range to retain the detection sensitivity towards the desired level of the DDC component to be detected (so that its effect can be considered). A practical design of $X_{k,\mathrm{th}}$ considering the presence of fundamental frequency positive-sequence component, noise signal, and DDC transient signal can be performed as follows.

In industrial sites, appropriate measures must be taken to reduce noise interference and assure a large signal-to-noise ratio (SNR). This gives

$$\eta_k = \frac{X^+_{\mathrm{RMS}}}{X^{\mathrm{noise}}_{k,\mathrm{RMS}}} \geq \eta_{k,\min} \tag{24}$$

where $X^+_{\mathrm{RMS}} = X^+/\sqrt{2}$ is the RMS value of the fundamental frequency sinusoidal component, which is identical for all three phases since only the

positive-sequence component is considered; $X_{k,\mathrm{RMS}}^{\mathrm{noise}}$ is the RMS value of the noise signal in phase k, η_k is the SNR of phase k, and $\eta_{k,\min}$ is the lowest allowable value of SNR in phase k given by relevant regulations of the industrial system.

The noise tolerance range can be converted into the form of energy. To this end, we firstly assume that the energy of the random noise signal is absorbed by an equivalent resistance R. Without loss of generality, the ohmic loss is calculated by assuming the signal to be a current quantity. Accordingly, the associated noise energy in period Δt is

$$E_k^{\mathrm{noise}} = \left(X_{k,\mathrm{RMS}}^{\mathrm{noise}}\right)^2 R\Delta t \tag{25}$$

Substituting (24) into (25) gives

$$E_k^{\mathrm{noise}} = \left(\frac{X_{\mathrm{RMS}}^{+}}{\eta_k}\right)^2 R\Delta t \leq \left(\frac{X_{\mathrm{RMS}}^{+}}{\eta_{k,\min}}\right)^2 R\Delta t \triangleq E_{k,\max} \tag{26}$$

Therefore, in order to satisfy the condition given by (24), the equivalent energy of the random noise signal must not exceed the maximum energy limit $E_{k,\max}$ allowed by the system. Indeed, cumulative energy is a fundamental driving force for heating issues of several electrical devices and further issues of system stability. Analogously, the principle of energy equivalence can be adopted to determine the presence of a DDC transient, namely, the DDC interference can be considered relatively large if its equivalent energy E_k^{ddc} satisfies

$$E_k^{\mathrm{ddc}} \geq E_{k,\max} \tag{27}$$

where the equivalent energy of the DDC component in phase k, E_k^{ddc}, can be evaluated as

$$E_k^{\mathrm{ddc}} = \int_0^{\Delta t} \left[x_k^{\mathrm{ddc}}(t)\right]^2 R\mathrm{d}t = R\int_0^{\Delta t} \left(X_k^{\mathrm{ddc}} e^{-\sigma_k t}\right)^2 \mathrm{d}t = \frac{R\left(X_k^{\mathrm{ddc}}\right)^2}{2\sigma_k}\left(1 - e^{-2\sigma_k \Delta t}\right) \tag{28}$$

(26) and (28) suggest that: E_k^{ddc} and $E_{k,\max}$ both increase with time, but the increase rates differ; with the elapse of time, the increase rate of E_k^{ddc} gradually slows down, yet the growth rate of $E_{k,\max}$ is constant. To highlight the adverse influence of the DDC component, the evaluation period Δt should be as short as possible. Since the response time of the presented

DDC detection scheme consumes at least half the grid cycle, here the detection threshold $X_{k,\mathrm{th}}$ is designed based on $\Delta t = T/2$. To this end, by combining (26), (27), and (28), the DDC component amplitude X_k^{ddc} that triggers the proposed detection algorithm can be obtained, yielding

$$X_k^{\mathrm{ddc}} \geq \frac{X_{\mathrm{RMS}}^{+}}{\eta_{k,\min}} \sqrt{\frac{\sigma_k T}{1 - e^{-\sigma_k T}}} \tag{29}$$

Since the DDC component cannot be directly measured, the DDC transient criterion is based on $X_k^r(t)$ which is given by

$$X_k^r(t) = x_k(t) + x_k(t - T/2) = x_k^{\mathrm{ddc}}(t) \left(1 + e^{\frac{\sigma_k T}{2}}\right) \tag{30}$$

Let t be $T/2$, then the corresponding value can be obtained as

$$X_k^r(T/2) = x_k^{\mathrm{ddc}}(T/2) \left(1 + e^{\frac{\sigma_k T}{2}}\right) = X_k^{\mathrm{ddc}} \left(1 + e^{-\frac{\sigma_k T}{2}}\right) \tag{31}$$

Therefore, when evaluating the energy and influence of the DDC component by half grid cycle, the pertinent threshold can be expressed as

$$X_{k,\mathrm{th}} = \frac{X_{\mathrm{RMS}}^{+}}{\eta_{k,\min}} \sqrt{\frac{\sigma_k T}{1 - e^{-\sigma_k T}}} \left(1 + e^{-\frac{\sigma_k T}{2}}\right) \tag{32}$$

In practice, the product $\sigma_k T$ is usually very small. Therefore, (32) can be simplified by approximating the exponential term with Taylor series expansion as

$$X_{k,\mathrm{th}} \approx \frac{X_{\mathrm{RMS}}^{+}}{\eta_{k,\min}} \left(2 - \frac{\sigma_k T}{2}\right) \approx 2 \frac{X_{\mathrm{RMS}}^{+}}{\eta_{k,\min}} = \frac{\sqrt{2} X^{+}}{\eta_{k,\min}} \tag{33}$$

Therefore, if the positive sequence signal amplitude X^{+} is large, the detection threshold of the DDC component can be appropriately increased. Besides, if the system requirement on SNR is not stringent (i.e., $\eta_{k,\min}$ is small), the system allows a large level of signal other than the positive sequence component, and the detection threshold of the DDC component can also be increased.

4.2. DDC Transient State Synthesis and Latching

After obtaining the state signal of each phase, the global state signal can be simply synthesized by using either an *and* ($\wedge$) or *or* ($\vee$) logic. Namely,

$$S = \begin{cases} S_a \wedge S_b \wedge S_c, \ \textit{and logic} \\ S_a \vee S_b \vee S_c, \ \textit{or logic} \end{cases} \tag{34}$$

The effect of the two methods differs when used in various systems. Specifically, the *and* logic is more conservative in the detection of the DDC transient since it requires all the three signals to satisfy the pertinent requirement. Conversely, when the *or* logic is used, the global DDC transient is identified once a single-phase signal exhibits significant half-/full-wave asymmetry. Since the DDC components in three phases have different amplitudes in general, the signal in one phase can reach the threshold level easier, hence the *or* logic is preferred in practical situations. Indeed, considering the same noise level in all phases, this gives the most reliable detection result, and the subsequent positive sequence component extraction can be more accurate.

To increase the system reliability, especially at the final stage of a DDC-existing transient, the latching mechanism is used to process the DDC state signal (see Fig. 4). This conditioning is needed to avoid the issue caused by possible jitters. At the end of the DDC transient, the amplitude of the DDC component becomes low, and the presence of random noise can lead to jitters in the detected state signal before it steadily reaches low.

With reference to Fig. 4, the DDC state signal is latched once it reaches low according to (23). This state is locked for a period, which is predefined to guarantee the coverage of jitters in the state signal. Afterward, the DDC transient detection is enabled again, to allow for the processing of successive transient events.

4.3. Compound Phase Detection Scheme

By combining the conventional PLL scheme in normal state and the amplitude-phase detection method in the case of a DDC transient, the complete control diagram of grid frequency and phase detection can be obtained in Fig. 5. The DDC state signal S is used for switching the output variables. When the DDC transient is detected, i.e., $S = 1$, the phase-amplitude detection algorithm that resists the DDC transient is effective, and vice versa. At one specific moment, the control system works with one path only, while bypassing the other path. Accordingly, the real-time complexity of the proposed scheme is equal to that of the single path, either the traditional PLL or the DDC-transient state algorithm, and is fully acceptable due to the high efficiency of both methods.

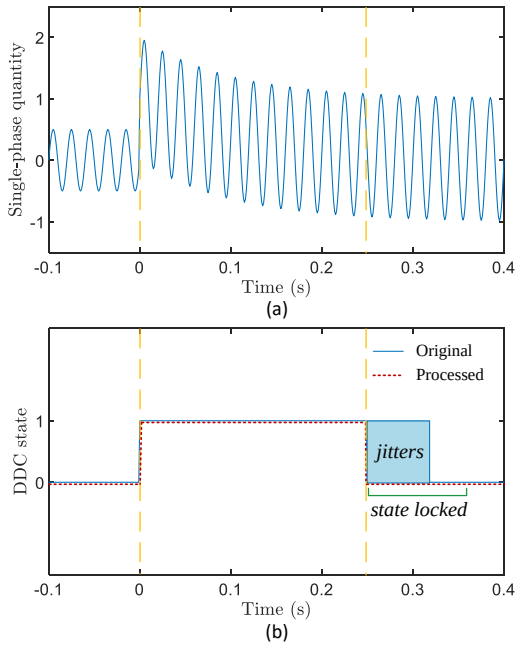

Figure 4: (a) Simulated single-phase signal considering DDC transient (starting at $t = 0$), and (b) processed state signal with the latching mechanism.

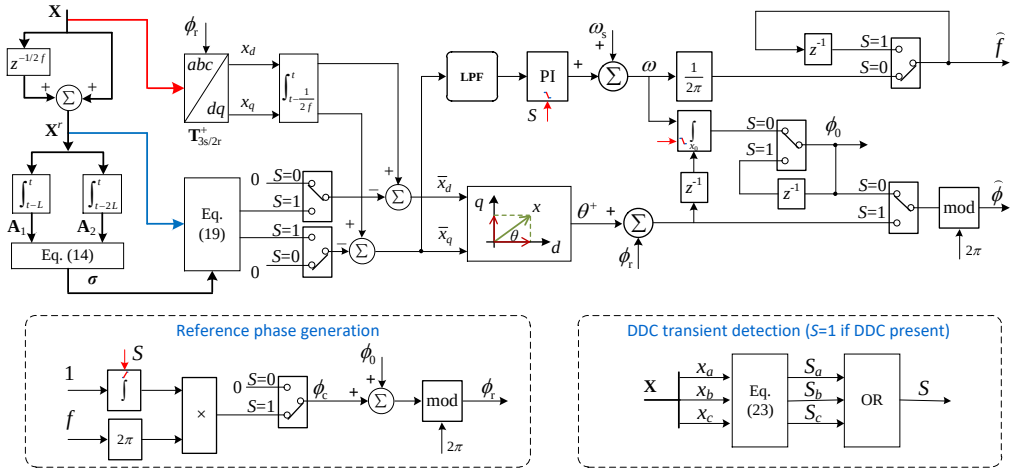

Figure 5: Complete control diagram for grid phase locking considering the DDC transient.

Specific efforts have been taken to enforce the smooth transition between the two paths. When the system transitions from the normal state to a DDC-

existing transient, the previously detected grid frequency and phase are used as the fixed initial condition, by using the latching modules implemented by connecting the pertinent output and a delay block. Also, in order to generate the real-time phase during the transient, a real-time reference phase ϕ_{r} is added to the initial phase calculated by (22). Specifically, ϕ_{r} considers both the aforementioned initial phase given by the normal steady-state control and the time-varying part ωt, as shown by the Reference phase generation block in Fig. 5.

Additionally, when the system transitions from the transient state to the normal state, the initial status of the integrator needs to be properly set. At the end of the DDC transient, the previous output phase, which was detected by the DDC transient path, is used as the initial phase output (i.e., the integrator value) of the normal state path. Meanwhile, the internal integrator output of the PI controller is reset to zero. These settings are achieved based on the DDC state signal S, and the falling edge of S is used to trigger the value resetting. Otherwise, the output phase signal will exhibit an undesired transient response when the DDC component approaches zero (i.e., when S transitions from 1 to 0), as will be shown in the following section.

5. Verification

In this work, the effectiveness of the proposed method is verified by hardware-in-the-loop (HIL) experiments, where the algorithm is embedded into the DSP controller TMS320F28335 commonly used for a grid-tied converter, and the three-phase grid signals containing the DDC component are generated by a real-time simulation target machine with the main step size of 8 μs. The grid signals are suitably scaled to output via the embedded multifunctional I/O card of the target machine, and are then sampled by the peripheral circuit of the DSP control board for further processing. Finally, an oscilloscope is used for real-time monitoring and logging of signals, which are output by the digital-to-analog-converter circuit of the control board. The sampling frequency is 10 kHz for the PLL control system. Two disturbance scenarios are considered, namely, without and with sudden frequency change at the instance of disturbance. In both cases, the non-ideal grid signal also includes harmonics and negative-/zero-sequence components.

5.1. Scenario A: Without Frequency Change

Before the disturbance, the system is three-phase symmetric with only the positive-sequence component, whose amplitude and phase are 0.25 p.u. and $-\pi/2$, respectively, and harmonics (see Table 1). The three-phase parameters after the disturbance, pertinent to positive-, negative-, and zero-sequence components, are shown in Table 2, and the DDC component during transient is determined based on (6) in [7], i.e.,

$$\mathbf{X}^{\mathrm{ddc}} = -\begin{bmatrix} \left(X^{+}\sin\theta^{+} - X\right)e^{-\frac{R^{+}}{L^{+}}t} + X^{-}\sin\theta^{-}e^{-\frac{R^{-}}{L^{-}}t} + X^{0}\sin\theta^{0}e^{-\frac{R^{0}}{L^{0}}t} \\ \left[X^{+}\sin\left(\theta^{+} - \frac{2\pi}{3}\right) + \frac{X}{2}\right]e^{-\frac{R^{+}}{L^{+}}t} + X^{-}\sin\left(\theta^{-} + \frac{2\pi}{3}\right)e^{-\frac{R^{-}}{L^{-}}t} + X^{0}\sin\theta^{0}e^{-\frac{R^{0}}{L^{0}}t} \\ \left[X^{+}\sin\left(\theta^{+} + \frac{2\pi}{3}\right) + \frac{X}{2}\right]e^{-\frac{R^{+}}{L^{+}}t} + X^{-}\sin\left(\theta^{-} - \frac{2\pi}{3}\right)e^{-\frac{R^{-}}{L^{-}}t} + X^{0}\sin\theta^{0}e^{-\frac{R^{0}}{L^{0}}t} \end{bmatrix} \tag{35}$$

Table 1: Scenario A - Harmonics of Testing Signal

Order	Before disturbance		After disturbance	
	Amplitude (p.u.)	Phase (deg)	Amplitude (p.u.)	Phase (deg)
3rd	0.2	70	0.1	30
5th	0.3	20	0.2	-60
7th	0.1	-50	0.05	-5

Table 2: Scenario A - Main Parameters of Testing Signal

Parameter	Value	Parameter	Value	Parameter	Value
X^{+}	0.5 p.u.	θ^{+}	$\pi/3$	L^{+}/R^{+}	0.06 s
X^{-}	0.3 p.u.	θ^{-}	$-\pi/2$	L^{-}/R^{-}	0.08 s
X^{0}	0.1 p.u.	θ^{0}	$\pi/5$	L^{0}/R^{0}	0.07 s

The result of test signal is shown in Fig. 6. After a short time, the disturbance occurs, and the three-phase DDC component is characterized by a large amplitude and a short duration during the transient. Indeed, based on the overall DDC state signal obtained by using the OR logic, as shown by the green curve in Fig. 6, the DDC components are only significant within 0.3 s after the disturbance. This impulsive transient inevitably leads

to inaccuracy of the detected phase, if the traditional SRF-PLL scheme is used.

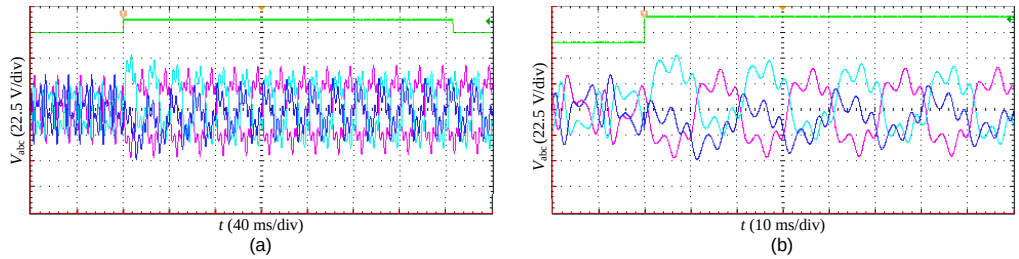

Figure 6: Experiment results of three-phase signals in scenario A. (a) Overall view, and (b) zoom-in at the transient beginning. Green curve: DDC transient state S.

This is specifically obvious at the beginning of transient [see Fig. 7, the cyan curve]. This result, if applied to converter control and protection, will lower the converter performance in terms of disturbance suppression and fault ride-through. Conversely, with the proposed detection scheme, the grid phase can be synchronized within a short period, i.e., 10 ms for the 50 Hz system, as shown by the magenta curve in Fig. 7.

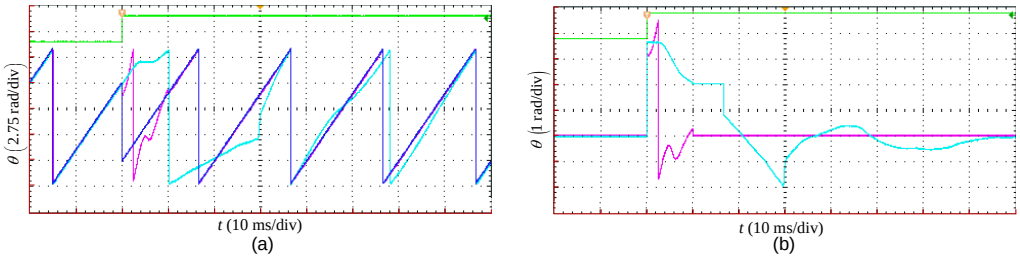

Figure 7: (a) Detected phases, and (b) phase errors at the beginning of the DDC transient in scenario A. Green curve: DDC transient state S. Blue curve: ideal phase output. Cyan curve: Traditional PLL result. Magenta curve: Proposed PLL result.

At the end of the DDC transient, the DDC status signal returns to zero according to the judgment criterion. If the zero phase is used as the initial output of the PLL integrator, a dynamic process is needed [see Fig. 8(a)] in order to achieve accurate phase detection. Conversely, the proposed method has a significantly quicker transient process [see Fig. 8(b)], and the phase difference is negligible in this case owing to the suitable transition logic that is being used.

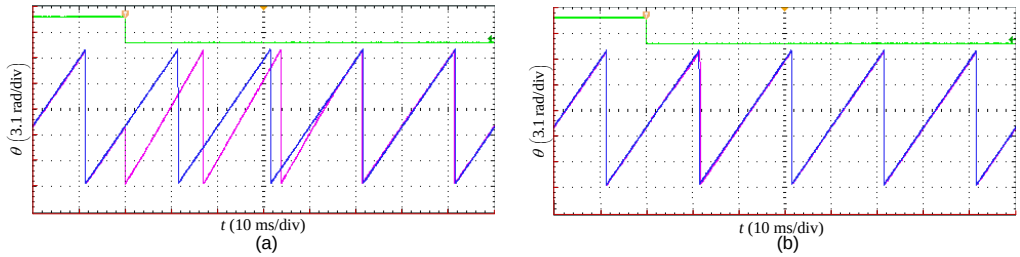

Figure 8: Detected phases at the end of the DDC transient in scenario A. (a) When the initial condition of the integrator is zero. (b) When the integrator is properly initialized. Green curve: DDC transient state S. Blue curve: ideal phase output. Magenta curve: PLL result.

5.2. Scenario B: With Frequency Change

In this scenario, the system is again three-phase symmetric with only a positive-sequence component (with amplitude being 0.25 p.u and phase being $-\pi/2$) and harmonics before the disturbance. The harmonics and three-phase parameters are shown in Tables 3 and 4, respectively. Besides, a sudden frequency increase of 1 Hz is imposed at the disturbance instant, in order to exacerbate the test case and verify the proposed method.

Table 3: Scenario B - Harmonics of Testing Signal

Order	Before disturbance		After disturbance	
	Amplitude (p.u.)	Phase (deg)	Amplitude (p.u.)	Phase (deg)
3rd	0.125	30	0.075	-40
5th	0.075	100	0.025	20
7th	0.025	50	0.0125	100

Table 4: Scenario B - Main Parameters of Testing Signal

Parameter	Value	Parameter	Value	Parameter	Value
X^+	0.75 p.u.	θ^+	$\pi/4$	L^+/R^+	0.04 s
X^-	0.50 p.u.	θ^-	$\pi/12$	L^-/R^-	0.02 s
X^0	0.25 p.u.	θ^0	$-\pi/6$	L^0/R^0	0.03 s

The result of the test signal is shown in Fig. 9. Analogous to the previous case, the transient is characterized by a three-phase DDC component with a large amplitude and a short duration. The detected phase with the conventional PLL is inaccurate specifically at the beginning of transient [see Fig. 10, the cyan curve]. Such an issue is overcome by the proposed detection scheme, with which the grid phase can be approximately detected within 10 ms, as shown by the magenta curve in Fig. 10. In this case, though a certain error will be present due to the frequency shift, the detection result provides satisfactory accuracy for converter control and protection considering the ongoing critical situation. Also, it is noted that the proposed switching logic enables the smooth transition at the end of the DDC transient compared to the hard switching without proper initial value setting, as shown in Fig. 11.

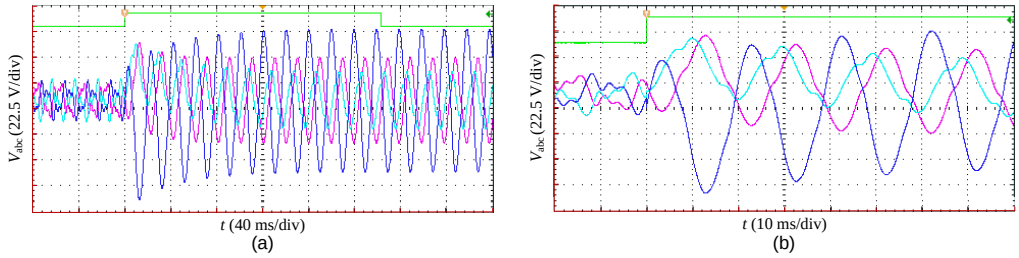

Figure 9: Experiment results of three-phase signals in scenario B. (a) Overall view, and (b) zoom-in at the transient beginning. Green curve: DDC transient state S.

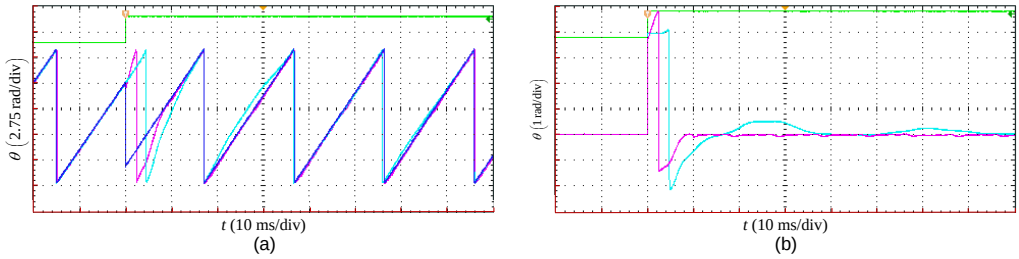

Figure 10: (a) Detected phases, and (b) phase errors at the beginning of the DDC transient in scenario B. Green curve: DDC transient state S. Blue curve: ideal phase output. Cyan curve: Traditional PLL result. Magenta curve: Proposed PLL result.

Finally, the detected grid frequency signal using different methods under both scenarios are compared in Fig. 12. Proper post-processing (including a rate limiter and a low-pass filter) was adopted to smooth the output

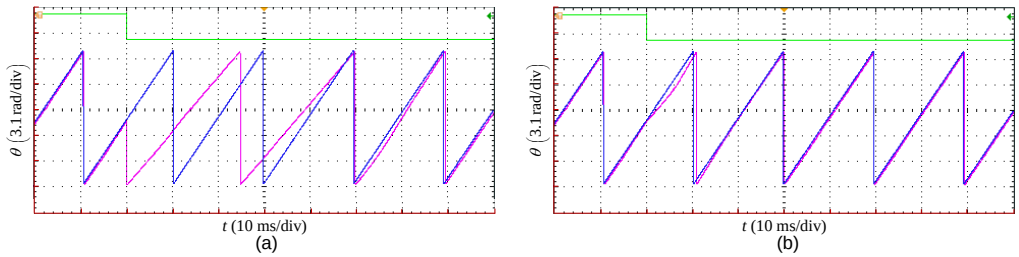

Figure 11: Detected phases at the end of the DDC transient in scenario B. (a) When the initial condition of the integrator is zero. (b) When the integrator is properly initialized. Green curve: DDC transient state S. Blue curve: ideal phase output. Magenta curve: PLL result.

frequency for both PLL schemes. Besides, due to the constant frequency assumption of the proposed PLL scheme during the DDC transient, the accurate frequency detection is deferred to the transient end. In scenario A, the detected frequency fluctuates around the nominal value (50 Hz) with both methods due to the influence of the DDC component, and the oscillation amplitude is smaller with the proposed method. In scenario B, the detected frequency of both schemes will reach the actual value; the proposed method takes a longer overall duration yet a shorter dynamic response time.

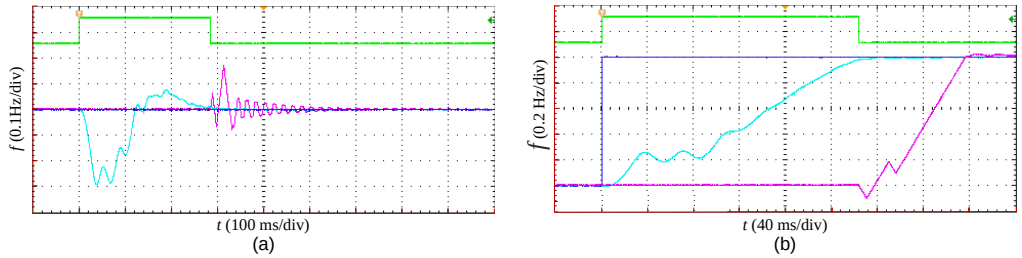

Figure 12: Detected frequencies using different methods. (a) Scenario A. (b) Scenario B. Green curve: DDC transient state S. Blue curve: ideal frequency output. Cyan curve: Traditional PLL result. Magenta curve: Proposed PLL result.

6. Conclusion

Power grids with large X/R ratios are easy to have large-amplitude DDC components in transient electrical quantities, when major disturbances such as faults and heavy load switching occur. Their presence greatly affects the

normal function of conventional PLL, which is critical for converter control. Focusing on this issue, in this paper, improvements to the traditional SRF-PLL are made, by embedding a specific algorithm that enables quick and efficient DDC component detection. This method accurately extracts the DDC component within approximately 0.5 grid cycle, and provides the per-sequence amplitude and phase information. As the DDC component becomes insignificant, the conventional PLL with proper initial condition setting is adopted. The effectiveness of the proposed method is verified by experiment results.

This work aims to present a general scheme for phase detection in the presence of DDC-existing transients. Though the SRF-PLL scheme is used in this paper as an example, more advanced closed-loop PLL schemes with better performance can be used, as long as the switching logic and initial conditions are properly designed. Besides, the DC offset can also be considered during the transient process by using alternative DDC detection approaches, e.g., the method in [19], at the expense of a slight increase in dynamic response time.

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