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Memtransistor Devices Based on MoS_2 Multilayers with Volatile Switching due to Ag Cation Migration

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In the recent years, the need for fast, robust, and scalable memory devices have spurred the exploration of advanced materials with unique electrical properties. Among these materials, 2D semiconductors are promising candidates as they combine atomically thin size, semiconductor behavior, and complementary metal–oxide-semiconductor compatibility. Here a three-terminal memtransistor device, based on multilayer MoS_2 with ultrashort channel length, that combines the usual transistor behavior of 2D semiconductors with resistive switching memory operation is presented. The volatile switching behavior is explained by the Ag cation migration along the channel surface. An extensive physical and electrical characterization to investigate the fundamental properties of the device, is presented. Finally, a chain-type memory array architecture similar to a NAND flash structure consisting of memtransistors is demonstrated, where the individual memory devices can be selected for write and read, paving the way for high-density, 3D memories based on 2D semiconductors.

1. Introduction

In the last twenty years, a broad range of novel emerging memory technologies, such as the resistive switching random-access memory (RRAM)[1,2] and the phase change memory (PCM),[3,4] have been proposed as storage class memory (SCM) toward bridging the gap between high-performance memory and low-cost storage devices.[5] Despite the strong research efforts, none of these emerging memory devices have reached industrial maturity due to reliability issues or insufficient performance/cost metrics in terms of power consumption and integration density. It appears thus that further progress in the development of robust, scalable memory technologies requires the exploration of alternative materials and device concepts. 2D semiconductors, such as transition metal dichalcogenides (TMDs), are promising thanks to their atomic-scale thickness and their strong potential for 3D integration.[6] RRAMs based on 2D semiconductors as active switching layer have been demonstrated,[7,8] although the advantages of these memory devices over conventional RRAM in terms of scaling or reliability are not clear yet. MoS_2-based transistors have been reported as selector devices for conventional oxide-based RRAM in one-transistor/one resistor (1T1R) structures,[9,10] although their low-current operation might represent a major limitation over their Si-based counterparts. Charge-based Flash memories have also been developed with 2D semiconductors,[11] although the fundamental issues of Flash in terms of single-electron phenomena and charge retention still represent a concern. Recently, memtransistor devices, combining transistor structure and functionality with memristive, or resistive, switching behavior, have been presented.[12–15] The memtransistor switching mechanism has been attributed to field-induced dislocation migration in the polycrystalline MoS_2 channel[12,13] or the dynamic tuning of the Schottky barrier at the metal-semiconductor contact.[14] Memtransistor devices based on direct cation migration from the electrodes on the surface of a 2D semiconductor have also been reported,[16,17] however displaying an asymmetric structure with different source/drain electrode materials. Memtransistors appear promising as they may combine the best properties of transistors, i.e., field-controlled transport and ideal digital switching, with the unique performance of memristors, i.e., nonvolatile or volatile memory behavior and the ability for electrical reconfiguration.

This work presents a memtransistor device based on multilayer MoS_2 with ultrashort channel length in the range of few tens of nm. The device shows excellent transistor characteristics with a subthreshold swing exceeding 5 orders of magnitude, limited by the measurement sensitivity. The volatile memristive switching is explained by the Ag cation migration along the channel surface, where the conductive bridge is first formed by field-induced migration, then disconnects within a retention time below 1 s due to spontaneous atomic rediffusion. We show that the ON and OFF states of the memtransistor device can be independently controlled via the compliance current and the gate bias, respectively, contrary to the 2-terminal memristor devices.[18,19] Finally, we demonstrate a chain-type memory array

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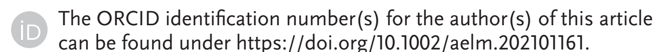
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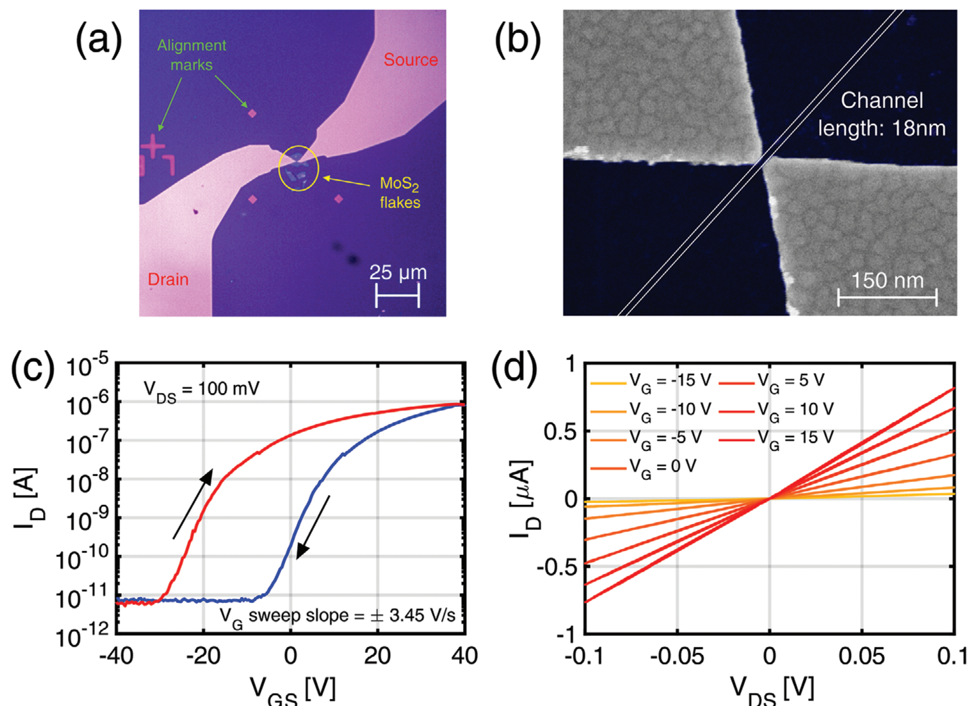

Figure 1. Memtransistor device structure and characteristics. a) Optical image of the MoS_2 memtransistor. Source and drain electrodes are deposited by thermal evaporation on a MoS_2 flake. Alignment marks are used for the alignment of lithography masks during source/drain patterning. b) Scanning electron microscopy (SEM) image of the source/drain electrodes and the channel region with a channel length of 18 nm. c) Measured drain current I_D as a function of the gate-source voltage V_{GS} for a constant drain-source voltage V_{DS} = 100 mV. The gate voltage was increased from –40 V to +40 V, then decreased back to –40 V. d) Measured I_D–V_{DS} characteristics at increasing V_{GS}.

architecture where the individual memory devices along the chain can be selected for write and read, thus paving the way for high-density, 3D memories based on 2D semiconductors.

2. Device Characteristics

Figure 1a shows the MoS_2-based memtransistor, consisting of a three-terminal device with a back-gate structure.[20–22] Source and drain contacts are obtained by thermal evaporation of Ag on an exfoliated MoS_2 flake with a thickness of few atomic layers (see Figure S1 in the Supporting Information). Note that, unlike other memtransistor devices based on Ag migration,[16,17] the device has a symmetric structure, where the source and drain electrodes can be fabricated within the same lithography and metal deposition process steps. Figure 1b shows a SEM image of the channel region of a memtransistor device. The typical channel length $L_{channel}$ of the memtransistor is in the range between 10 and 40 nm. Source and drain contacts are patterned with triangular shape to minimize the channel width in the gap region and to reduce proximity effects in the channel region during exposure.

Figure 1c shows the measured drain current I_D as a function of the back-gate voltage V_{GS}, where the gate voltage was first increased from –40 V to +40 V and then decreased to –40 V, while the source was grounded, and the drain-source voltage V_{DS} was kept equal to 100 mV. The relatively large gate voltage is necessary due to the thick gate oxide with thickness t_{ox} = 285 nm. Regardless of the thickness of the MoS_2 flake, all the devices show n-type characteristics with negative threshold voltage, indicating the intrinsic n-doping of the MoS_2 channel.[20] The I_D–V_G characteristic displays a relatively large hysteresis[23] due to the presence of trapping centers in the MoS_2 film,[24] at the oxide-semiconductor interface,[25,26] or within the oxide layer itself.[27,28] These defects might originate from oxygen vacancies in the oxide, or sulfur vacancies in the MoS_2, or water molecules that interact with the semiconductor.[29,30] Figure 1d shows the I_D–V_{DS} characteristics at increasing V_{GS} at relatively small V_{DS} from –100 mV to +100 mV. The linearity of the curves indicates ohmic-like contacts between Ag and MoS_2.[31]

Increasing V_{DS} to a relatively large voltage across the channel induces resistive switching as shown in **Figure 2**a. The I_D–V_{DS} characteristic in the figure indicates a steep transition from the transistor characteristics to a low resistance state (LRS) at V_{DS} = 1.8 V. This event is referred to as forming process, in analogy with RRAM devices.[32] The forming voltage V_{form} was generally smaller than 3 V with a dependence on the channel length of the device (see Figure S2 in the Supporting Information). In particular, V_{form} was found to increase for increasing channel length. Note that the current spontaneously collapses to the transistor characteristic as V_{DS} is decreased below a holding voltage of about 0.2 V. During the forming process in the figure, the current was limited to below the compliance value I_C = 0.8 µA, to prevent the destructive breakdown of the device. We will refer to the transistor characteristics as high resistance state (HRS) in the following, in analogy with RRAM.

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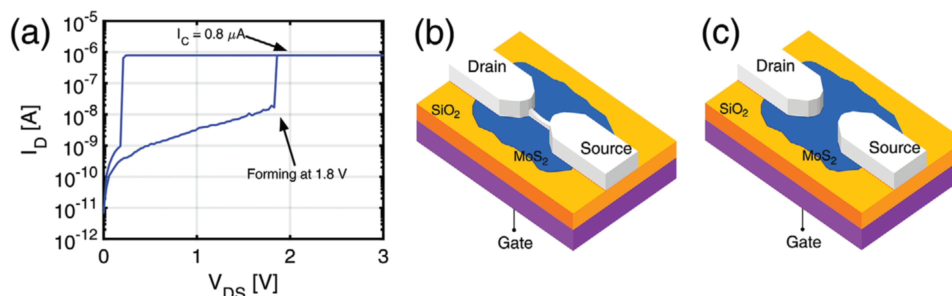

Figure 2. Forming operation in the memtransistor device. a) Measured I_D–V_{DS} characteristic of the device during the forming process. Forming is evidenced by the steep increase of current at V_{DS} = 1.8 V. A current limitation to I_C = 0.8 μA was adopted to prevent destructive breakdown. b) Schematic of the MoS_2 memtransistor switching mechanism. For small V_{DS} the metallic electrodes are physically separated and the current is confined in the semiconductor channel region. c) After forming or the set transition, a CF is formed between the two electrodes, thus enhancing conductance. The CF is then spontaneously dissolved as V_{DS} is decreased below a holding voltage.

The resistive switching behavior in Figure 2a is attributed to the formation of a conductive filament (CF) on the surface of the MoS_2 channel. As schematically illustrated in Figure 2b, the large electric field along the channel during forming results in cation migration between the Ag electrode, similar to the electrochemical memory (ECM) class of RRAM, also known as the conductive bridge random access memory (CBRAM).[33] The CF might form by neutralized ions piling up at the source side, after traveling across the channel.[15] Alternatively, the CF might originate from the direct growth from the drain electrode along a localized path.[34] In both cases, the dependence of V_{form} on the channel length in Figure S2a in the Supporting Information can be understood by the existence of a critical electric field to induce the cation migration.[32] Forming characteristics for increasing channel length are reported in Figure S2b in the Supporting Information. As V_{DS} is reduced below the holding voltage, atomic diffusion leads to the dissolution of the CF, which is evidenced by the sudden drop of conductance in Figure 2a. Figure 2c illustrates the device in the transistor mode, after the dissolution of the CF, where the current flow is controlled by V_{GS}-dependent channel conductance. Similar to the switching process in CBRAM devices,[35,36] the volatile memory behavior might originate from diffusion at the surface of the CF and/or MoS_2, thus benefitting from the lower energy barrier for surface diffusion.[19] The spontaneous dissolution can be explained by surface re-diffusion of Ag atoms constituting the CF. The holding voltage V_{hold} after the forming was found to decrease at increasing channel length, hence increasing V_{form} (see Figure S3a in the Supporting Information). The decreasing V_{hold} might reflect the longer retention time, resulting from high V_{form} stabilizing the CF. As a result, the CF dissolution time is longer for large V_{form}, thus resulting in a lower V_{hold}. In few extreme cases, we even found that the forming led to an irreversible breakdown at high V_{form}, where the device ends up in a short circuit state after forming (see Figure S2b in the Supporting Information).

After the forming process, the device shows a set transition at the characteristic voltage V_{set} which is typically smaller than V_{form}. **Figure 3**a shows measured *I–V* characteristics at variable V_{GS} for I_C = 4 μA, indicating set transition at a V_{set} of about 0.8 V and recovery of the off state at V_{hold}. The decreased value of V_{set} with respect to forming can be explained by the presence of a preferential path for ionic migration possibly including Ag nanocrystals on the MoS_2 surface, as a result of the original forming process.[37] Bidirectional set events can also be obtained by applying negative voltage sweeps of V_{DS} (see Figure S4 in the Supporting Information), thanks to the symmetric source/drain materials in the device. The switching characteristics display a negligible dependence on V_{GS}, which can be explained by the ionic drift being only sensitive to the lateral field along the channel, with negligible impact of the vertical field and the channel current I_D. Figure 3b shows the measured V_{set} and V_{hold} for several switching cycles as a function of V_{GS}, again confirming that set and recovery transitions are constant. This is further confirmed by the distributions of measured V_{set} and V_{hold} in Figure 3c. Unlike V_{form} and the first V_{hold} (i.e., the one measured immediately after the forming event), V_{set} and V_{hold} did not show any clear dependence on the channel length.

The memtransistor allows for an independent control of the HRS and LRS conductance, thanks to the three terminal structure. Figure 3d shows the measured HRS resistance as a function of V_G, where the decrease of HRS resistance at high V_G is due the increasing electron concentration in the MoS_2 channel. Figure 3e shows the measured LRS as a function of the compliance current I_C, where the decrease of LRS resistance at high I_C is due to the increasing cross section area of the filament.[38] Note that conduction in the LRS results from the parallel transport in the semiconductor channel and the metallic filament, although the latter provides the dominant contribution due to the high conductivity of the Ag filament (see also Figure S5 in the Supporting Information). Figure 3f illustrates the parallel conduction in the 2D MoS_2 channel and the 1D Ag filament. The separate control of HRS and LRS resistance, which is a unique feature of the memtransistor device in contrast to typical 2-terminal RRAM and CBRAM, allows to achieve extremely large resistance window, approaching 7 orders of magnitude for the highest I_C and lowest V_{GS}.

The recovery process taking place at V_{hold} in Figure 3a reveals the metastable nature of the CF, which can be characterized by a retention time t_{ret}. **Figure 4**a shows the voltage waveform for the pulse stimulation at V_D = 3 V for 1 s with I_C = 3 μA, followed by read at V_{read} = 0.1 V for characterizing t_{ret}. The gate voltage was maintained constant at –15 V during both stimulation and read phases of the experiment. Figure 4b

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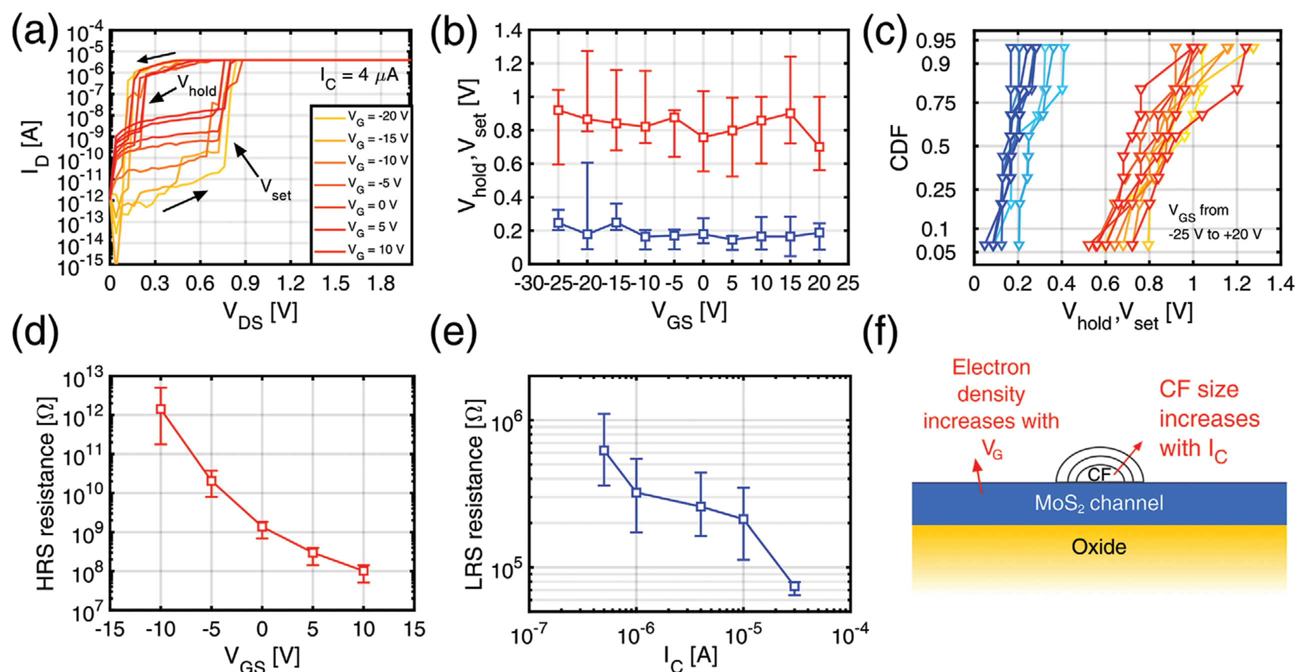

Figure 3. Volatile switching characteristics of the memtransistor device. a) Measured *I*–*V* curves showing the set transition at increasing V_{GS}, with I_C fixed at 4 µA. The set voltage V_{set} and holding voltage V_{hold} remain approximately constant, indicating no dependence on V_{GS}. b) Measured V_{set} (red) and V_{hold} (blue) for the same device as a function of V_{GS}. c) Cumulative distribution function (CDF) of V_{set} and V_{hold}, indicating a cycle-to-cycle variation with negligible dependence on V_{GS}. d) Measured HRS resistance as a function of V_{GS}, showing that the HRS resistance can be reduced by increasing V_{GS} due to the MoS_2 inversion at increasing vertical field. The maximum resistance (corresponding to $V_{GS} = -10$ V) is limited by the current sensitivity in our measurement setup. e) Measured LRS resistance as a function of I_C. As I_C is increased, the LRS resistance decreases due to the formation of a larger CF. f) Schematic of the HRS and LRS control mechanisms. In the LRS (ON state), the formation of the metallic filament between the source and drain terminals dominates the conduction, which can be controlled by the applied I_C. In the HRS (OFF state), the current flows only in the MoS_2 channel, which can be controlled by changing the V_{GS}.

shows the measured response I_D indicating a drop at $t = 0$, corresponding to the transition from stimulation to read, and a second drop for $t_{ret} > 0$, which reveals the CF dissolution time.[19,33] Multiple current drops may also occur, as the device switches to intermediate conductance levels before eventually collapsing to the HRS. The retention time t_{ret} was always characterized as the time where the read current drops to 1% of the initial value. Similar to CBRAM devices, t_{ret} shows a relatively wide dispersion, as also indicated by the cumulative distributions in Figure 4c.[39] The median time of the retention time is about 0.1 s with a weak dependence on I_C where a higher I_C results in slightly longer retention. This type of behavior was previously observed in CBRAM devices and can be explained by the dependence of diffusion rate on the surface curvature.[19] Variation of the CF shape can result in largely variable surface curvature, hence a large spread of the retention time.

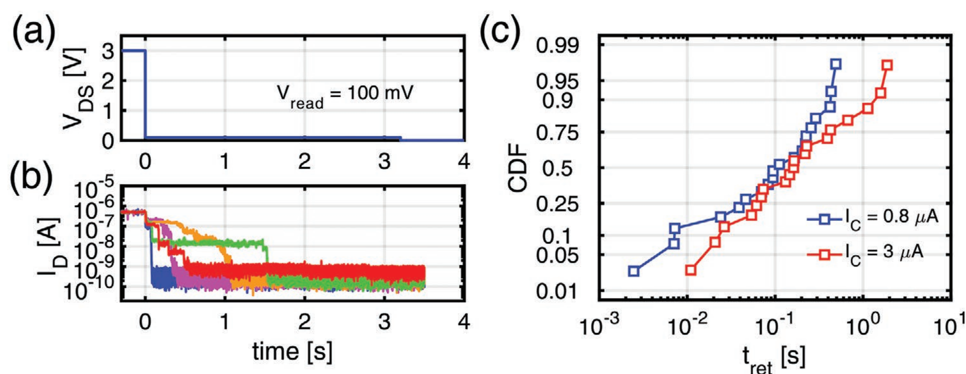

Figure 4. Retention time of the memtransistor device. a) Voltage waveform applied across the drain-source terminals for the retention experiments. A rectangular pulse with 3 V amplitude is applied followed by a read phase at 100 mV. b) Read currents for selected retention experiments, indicating the large variability of the dissolution dynamics. c) Cumulative distribution functions (CDF) of retention time t_{ret} for two different I_C.

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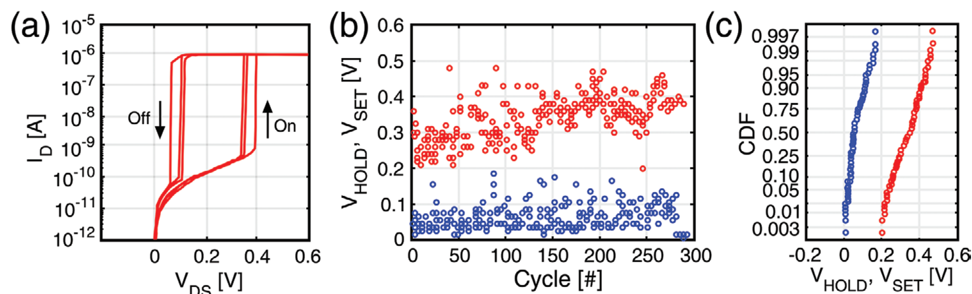

Figure 5. Cycling endurance of the memtransistor device. a) Measured *I–V* curves over 300 DC cycles at $V_{GS} = -5$ V performed on a device with a channel length $L = 20$ nm with $I_C = 1$ µA. b) Measured V_{set} (red) and V_{hold} (blue) as a function of the number of cycles. c) Cumulative distribution function (CDF) of V_{set} and V_{hold}.

3. Cycling Degradation

Figure 5a shows the $I - V$ curves of repeated switching cycles for a device with a channel length $L = 20$ nm. Note that, compared to Figure 4, this device is characterized by a relatively low V_{set} of about 0.35 V and V_{hold} of about 0.1 V, possibly because of a different surface microstructure after the forming process. Despite the extremely high repeatability of the transistor characteristics, V_{set} shows some variation. This is also visible in Figure 5b, showing the measured V_{set} (red) and V_{hold} (blue) of the device during 300 cycles at $V_{GS} = -5$ V, and in Figure 5c, showing their cumulative distributions. While the variation of V_{set} can be explained by the variable concentration of residual Ag along the channel in the off state, the variation of V_{hold} reflects the stochastic spread of t_{ret} in Figure 4. In fact, the longer the retention time, the lower is the voltage V_{hold} at which the device displays the transition to the off state while returning to zero voltage during the *I–V* characterization. The cycling endurance of the device strongly depends on the I_C applied, as typically observed for oxide-based filamentary switching RRAM devices.[40] As I_C is increased, the cycling endurance decreases (see Figure S6 in the Supporting Information), which might be explained by the larger degradation of the MoS_2 surface in the channel region. The value of I_C should thus be optimized in view of the best tradeoff between energy consumption, resistance window and endurance.

For a better understanding of the device failure mechanism, the channel region of the memtransistor was observed by SEM before and after the forming operation (see Figure S7 in the Supporting Information). After forming, some devices showed a longer gap length and the formation of Ag clusters within the MoS_2 region between the source and drain electrodes, suggesting that the repeated ionic migration results in a displacement of Ag from the source/drain reservoir to the channel region. Extensive cycling usually leads to an increase of V_{set}, thus resulting in the device remaining in the HRS under the application of set voltage pulses with fixed amplitude (see Figure S8a in the Supporting Information). We attribute the permanent HRS to an increase of the channel length, as supported by the SEM in Figure S4b in the Supporting Information. The increase of the channel length is equivalent to a decrease of the electric field at a given voltage, thus resulting in a lower driving force for the migration of Ag ions. At this point, if a larger V_{DS} of about 5.5 V is applied to force the device to form again, the devices switch to a permanent LRS without the usual spontaneous relaxation to the HRS. Atomic force microscopy (AFM) observations of the broken device in short circuit shows extensive degradation in the channel region, with relatively large clusters attributable to residual Ag (see Figure S8b in the Supporting Information).

4. Memtransistor Switching in a Chain-Type Circuit

The 3-terminal device structure is suitable to implementation of a chain-type memory array circuit as shown in **Figure 6**a. Here, several memtransistor devices are connected along a

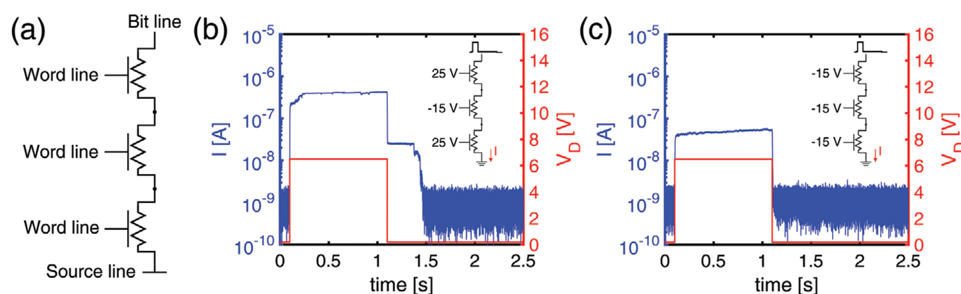

Figure 6. Implementation of a chain-type memory array architecture with three memtransistor devices. a) Schematic of the circuit with three memtransistors. A write pulse followed by a read phase is applied at the top terminal, while the gate terminals are biased in pass mode (positive bias) or select mode (negative bias). b) When the two devices used as selectors are biased in pass mode, the applied bitline voltage drops across the selected device with negative gate bias, thus resulting in the switching. c) When the two devices used as selectors are biased at negative voltage, the bitline voltage drops approximately equally across the devices in the string, thus resulting in no change of state.

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string between a bit line and a source line. The gate terminals of devices in separate strings are instead shared along the wordline, while source terminals can be shared among the whole array or sub-array. Chain-type memory circuits, previously reported for ferroelectric random-access memory[41] and PCM,[42] allow for a small area and a high density, by connecting all devices in a string fashion similar to NAND flash.[43] To select a device during program or read, the gate terminal of the selected device is biased to negative voltage, while the gate terminals of all other devices along the string are biased at positive voltage, also referred to as pass voltage. This ensures that all the unselected devices in the same string display a low resistance, irrespective of their programmed state. As a result, the programming voltage applied between bit and source lines drops almost entirely across the selected device. During the read operation, the resistance between bit line and source line is dictated by the selected device, all the unselected devices being in low-resistance pass state.

To support the concept of chain array structure with the memtransistor, we connected three devices in series with independent gate terminals. Figure 6b shows the applied bit-line voltage V_D and the measured string current for the case where the middle device was selected with gate bias $V_G = -15$ V, while the top and bottom devices were unselected with positive pass voltage $V_G = 25$ V at the gate. The applied V_D drops entirely across the selected cell, thus resulting in a set transition as revealed by the device increasing to about 0.5 µA. Note that the device current was limited by the series resistance due to the top and bottom memtransistors in pass mode, with no need for any external compliance. After the programming pulse, a small $V_D = 0.1$ V was applied to read the string, thus evidencing a retention time t_{ret} of about 0.5 s. Figure 6c shows the case where the top and bottom devices were biased with $V_G = -15$ V, instead of pass condition. During the applied programming and read pulse, the selected device is biased in deep subthreshold mode, however the bitline voltage drops almost uniformly across the three devices in the string, thus being insufficient to induce any switching transition. In fact, the response current does not indicate any switching process in the string. Compared to chain memory arrays with PCM and FeRAM, where the select transistor is in parallel to the memory element, the chain in Figure 6a only includes memtransistors, thanks to their twofold operation where the same device can operate both as a transistor and a memristor. The atomic thickness of the MoS_2 channel, combined with its suitability for 3D integration, makes the memtransistor chain structure a very promising architecture for ultrahigh-density memory.

5. Conclusion

This work presents a memtransistor device based on multilayer MoS_2 with ultrashort channel length. The device shows transistor characteristics with a large resistance ratio between LRS and HRS (typically more than 5 orders of magnitudes) and a memristive switching characteristic for source-drain voltages around 0.8 V. The observed switching behavior is volatile, which is attributed to Ag surface diffusion across the channel region. The HRS and LRS resistances can be independently controlled by the applied V_{GS} and the compliance current I_C, respectively. The endurance failure is interpreted by the displacement of Ag clusters from the source/drain electrodes. The potential of the memtransistor device is finally demonstrated with a chain-type memory array architecture demonstrating select/unselect properties during program and read. These results pave the way for high-density, 3D memtransistor arrays based on 2D semiconductors.

6. Experimental Section

Device Fabrication: The memtransistors were fabricated by mechanical exfoliation and lithographic patterning. Memtransistor devices were fabricated on top of a p-doped Si substrate covered with a SiO_2 layer with a thickness of 285 nm, grown by chemical vapor deposition (CVD). Alignment marks made of Au were deposited on top of the SiO_2 surface for the definition of the source and drain electrodes. The SiO_2 surface was then cleaned with sonication in acetone, dried with isopropanol (IPA) and finally treated with O_2 plasma with a power of 200 W for 1 minute, to remove organic residues. After the cleaning process, MoS_2 flakes were deposited via mechanical exfoliation, thus allowing the deposition of thin mono-crystalline flakes of semiconductor with high level of purity.[44,45] The optical contrast with the SiO_2 layer was used for identifying and selecting the flakes for memtransistor fabrication. Due to the thickness of the SiO_2 layer, thin MoS_2 flakes appear with blue color, while thicker flakes tend to show a white color. The accurate characterization of the MoS_2 thickness was carried out by a Keysight 5600LS atomic force microscope (AFM). In general, the MoS_2 flakes consisted of generally less than 6 monolayers (see Figure S1 in the Supporting Information). Source and drain contacts were patterned by electron beam lithography using PMMA 200k spin at 4000 rpm for 1 minute. Finally, Ag was thermally evaporated with a thickness of 40 nm at a deposition rate of 0.02 nm/s.

Electrical Characterization: All the electrical characterizations were carried out at room temperature using the Keithley 4200-A SCS parameter analyzer. All the DC and retention experiments were carried out in a probe station, while the memory-chain experiments are realized using bonded devices in a custom printed-circuit board with ad-hoc design.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

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Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D semiconductor, memory physics, memristor, memtransistor, MoS_2

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