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Abstract. We use thin layers of exfoliated black phosphorus to realize back-gated field-effect transistors in which the Si/SiO_2 substrate is exploited as gate electrode. To prevent the detrimental effect of the air exposure the devices are protected by Poly(methyl methacrylate). We report the observation of an improved contact resistance at the interface between the layered material and the metal contact by electrical conditioning. We also demonstrate the existence of a hysteresis in the transfer characteristics that improves by increasing the gate voltage sweep range. Finally, we prove the suitability of such transistors as memory devices.

1. Introduction

The discovery of graphene [1] in 2004 has opened the way to a huge research effort in the field of two-dimensional (2D) materials, characterized by several interesting properties related to the very small thickness of the materials [2]. Initially, great excitation came from the extremely high mobility of graphene, however it was soon clear that the lack of bandgap is a severe limitation towards its exploitation as channel in field-effect transistors [3–5], preventing a complete switch-off of the device. Different solutions have been proposed in order to open a sizeable bandgap by substituting a carbon atom with nitrogen to break the in-plane symmetry of the carbon hexagonal lattice [6], or by breaking the symmetry along the vertical direction creating a graphene bilayer [7], or by the quantum confinement in nanoribbons and graphene quantum dots [8], or by complete oxidation of graphene [9]. However, it is now recognized that several 2D semiconducting layered materials are more suitable for electronic applications as field-effect transistors, such as the transition metal dichalcogenides (TMDs) family that includes MoS_2, WS_2, PdS_2, PtS_2, etc. and the corresponding diselenides [10–20]. Indeed, an on/off ratio up to 10^8, and a subthreshold slope close to 60 mV/decade have been reported for TMDs based FETs [21]. However, the contact resistance is one of the major limitation [22,23] to the best performance of electronic devices: contacts on 2D materials often have a large Schottky barrier due to interfacial effects such as Fermi-level pinning [24,25].

Black phosphorus (BP) is a 2D layered material in which layers are vertically stacked by van der Waals forces, allowing easy exfoliation from bulk samples [26–28]. A BP layer has puckered honeycomb structure in which each atom is covalently bonded with other three atoms (as shown in figure 1a). When in bulk form BP has a small bandgap of about 0.3 eV. Reducing the thickness to few layers causes an increase of the bandgap until a direct bandgap of about 2 eV for monolayer BP. Consequently, BP is attracting growing interest for electronic and optoelectronic applications, in particular as 2D channel in FETs, considering that the direct bandgap (thickness-dependent) can favour the development of photodetectors in the infrared region. It has also been reported that hole mobility at room temperature can reach 650 $cm^2 V^{-1} s^{-1}$ and 1000 $cm^2 V^{-1} s^{-1}$ at 120 K. Moreover, differently from TMDs that have indirect bandgap in the form of multi-layers, the BP is characterized by direct bandgap, independently from the thickness. The conduction type in BP is mostly hole-dominated transport due to a lower activation energy for p-type BP than for n-type and to a higher hole effective mass originated by the material anisotropy. Actually, anisotropic charge transport has been reported with a much larger hole mobility in the a direction with respect to the perpendicular one. It has also been demonstrated that increasing the number of layers of the BP channel in FETs causes a reduction of the on/off ratio due to a reduction of the Schottky barrier for both holes and electrons.

In this paper, we report the electrical characterization of field-effect transistors in back-gated configuration, in which multilayer BP is used as the channel while source and drain electrodes are realized by Cr/Au leads. The FETs are protected by Poly(methyl methacrylate) (PMMA) in order to prevent the degradation due to air exposure.

2. Experiment

Multilayer BP nanosheets were obtained by standard scotch-tape mechanical exfoliation from bulk BP single crystals. The BP flakes were then transferred on p-Si/SiO_2 substrates (with oxide thickness of about 90 nm). Metal electrodes contacting the BP were realized by standard photolithography and electron beam evaporation of Cr (10 nm) as adhesion layer and Au (100 nm). In order to use it as back-gate, the silicon substrate was scratched on the back-side and covered with silver paint to favour ohmic and low resistance electrical contact. A schematic of the BP based FET is shown in figure 1b, while a real image taken by an optical microscope is reported in figure 1c. The thickness of the BP flake was measured by atomic force microscope (at the end of the experiment after removing the PMMA) and it resulted about 9 nm (line profile is reported in figure 1d).

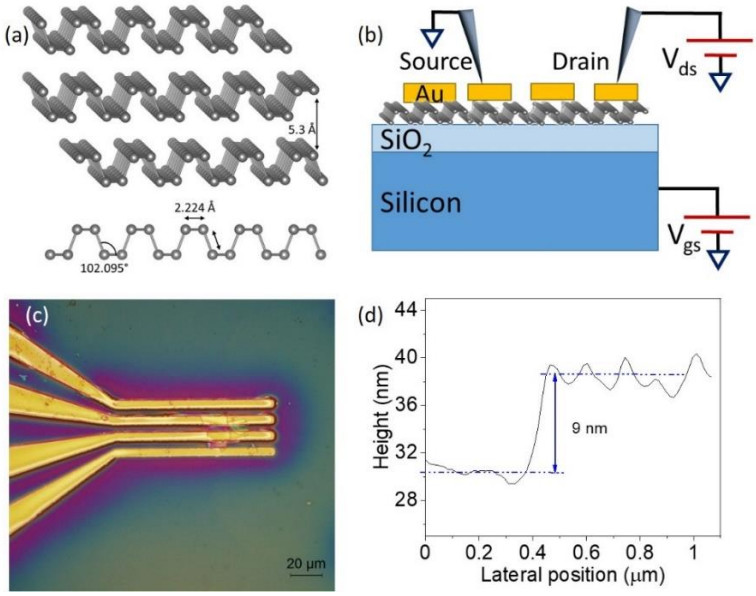

Figure 1. (a) Schematic of black phosphorus crystal structure with puckered honeycomb layers having an interlayer distance of about 0.5 nm. (b) Schematic of the back gated field-effect transistor with the channel realized by a BP flake. (c) Optical image of the real device. (d) Step profile of the BP flake measured by atomic force microscope.

We performed the electrical characterization of the transistors inside a cryogenic probe station (ST-500 by Janis) working under controlled pressure in the range from 10^3 mbar down to 10^{-6} mbar. The nanomanipulated probes were connected (via triaxial feedthroughs) to a semiconductor parameter analyzer (4200-SCS by Keithley) that can be operated as a source-measurement unit with high current resolution (better than 1pA). For these devices, it has been already demonstrated elsewhere [29] that the Cr/Au electrodes form ohmic contacts with low resistance so that the characterization can be correctly performed in a standard two-probe configuration. In figure 2 we report the electrical measurements between the two lower contacts (as shown in figure 1c). We notice that initially the device is characterized by a higher resistance (black curve in figure 2a). However, after a few repetitions the overall resistance is significantly improved and stabilized (blu curve in figure 2a). The positive conditioning effect on the device stability is also confirmed by the comparison of the transfer curves, i.e the channel current I_d versus the bias voltage applied on the gate electrode, while keeping a constant voltage between the source and drain $V_{ds} = 0.01$ V. Indeed, in figure 2b (upper plot) we observe that the transfer curve corresponding to the initial state of the device is noisier, with a lower channel current and a lower and a very limited on/off ratio of about 5%. Vice versa, after the electrical conditioning (several repeated current-voltage characteristics at higher current), the transfer curve (figure 2b, lower plot) shows a channel current improved of about one order of magnitude, the current noise is strongly reduced, and the on/off ratio is improved up to 40%.

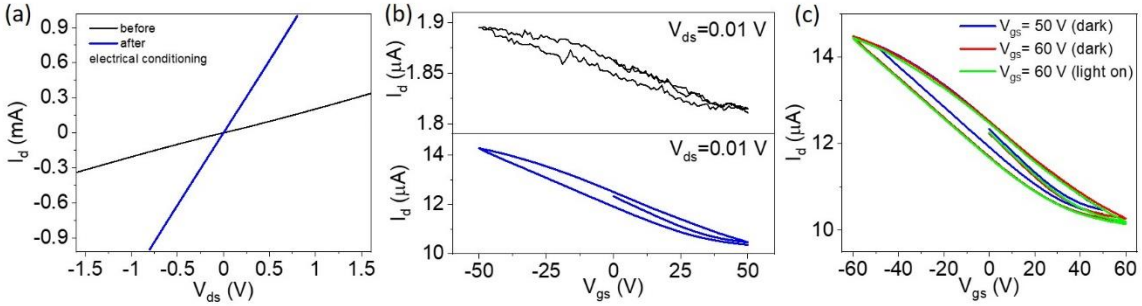

Figure 2. (a) I-V curves measured before and after electrical conditioning. (b) Upper plot: I_d-V_{gs} curve measured before electrical conditioning; Lower plot: I_d-V_{gs} curve measured after electrical conditioning. (c) I_d-V_{gs} curves measured for different V_{gs} range and under illumination.

We observe an increase of the channel current when a negative gate bias is applied, corresponding to a p-type transistor. We notice that performing a complete loop in the voltage sweep applied on the gate electrode, the transfer curve is characterized by an hysteresis, often observed in the FETs based on TMDs [30–34]. We also increase the gate voltage range up to 60 V. As a result, the width of the hysteresis in the transfer curve is increased (figure 2c). To prevent damages to the gate dielectric we did not increase further the gate voltage range, and we did not reach a complete switch off of the transistor. We also illuminated the device by means of a white LED light, but we did not observe significant modification of the current level. The reported hysteresis is probably caused by the existence of intrinsic (such as phosphorus vacancies or grain boundaries) and/or extrinsic (such as environmental adsorbates) trap states and the charge transfer from/to them during the gate voltage sweeps [35–40].

We also tested the same BP flake by contacting a different pair of contacts corresponding to a longer channel. The electrical measurements are reported in figure 3. The output curves, i.e the I_d-V_{ds} curves for different V_{gs} values ($-60V < V_{gs} < +60$ V, step of 10 V) are shown in figure 3a. The curves are linear and we also notice that the application of the V_{gs} affects the overall conductance of the transistor without modifying the $I_d - V_{ds}$ linearity, with the channel current reducing for increasing V_{gs}. The transfer curve (figure 3b) is measured in dark and under illumination, confirming the p-type behavior, the on/off ratio of the order of 40% and no evidence of current increase due to the light.

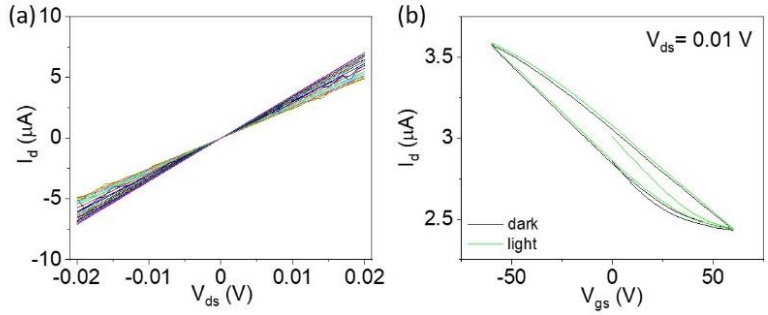

Figure 3. (a) Output curves I_d-V_{ds} for different V_{gs} values (from -60V to +60V with a step of 10 V). (b) Transfer curves I_d-V_{gs} measured in dark and under white LED illumination.

Finally, we investigated the effect of gate bias pulses on the electrical properties. In figure 4a we compare the transfer curves measured before and soon after the application of a prolonged gate bias pulse at V_{gs} = -60 V (for about 250 s). We observe that the curve is slightly shifted after the pulse, that corresponds to a change of threshold voltage as well as of the channel current. In figure 4b, by repeating a series of successive pulses at V_{gs}= +60 V (write), 0 V (read), -60 V (erase), 0V (read), we exploit the BP based FET as a memory device. We observe that the two different states (at 0 V) remain well separated. In figure 4c we enhance the current evolution in the reading time (V_{gs}= 0 V) for both the on-state (upper plot) and the off-state (lower plot). In both cases, the experimental data are well fitted by an exponential behavior with similar time constant of about 12 s (for raising current) and 14 s (for decreasing current). The similar time constants are indicative of similar electron and hole capture/emission times.

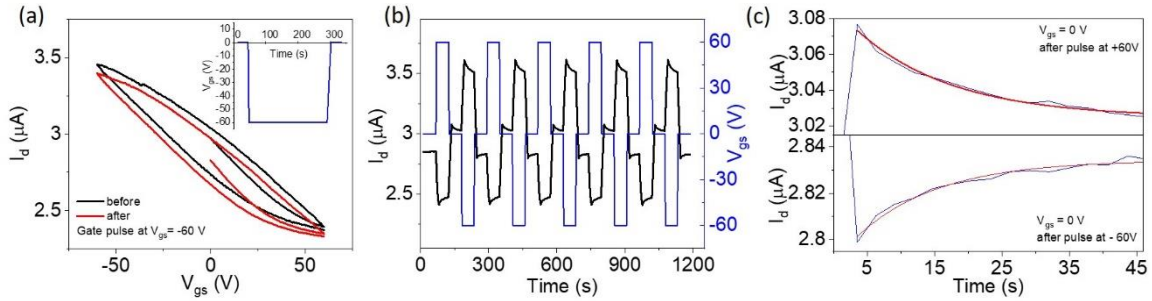

Figure 4. (a) Transfer curves measured before and after a prolonged gate pulse at V_{gs} = -60V. Inset: Gate pulse (V_{gs} versus time). (b) Series of gate pulses V_{gs} = +60 V, 0 V, -60 V, 0 V and corresponding channel current behavior. (c) Enhancement of the experimental data (and exponential fit) of the current behavior for V_{gs} = 0V after the pulse at +60 V (upper plot) and after the pulse at -60 V (lower plot). Time has been normalized for graphical purposes.

3. Conclusions

We realized field-effect transistors in which the conductance channel is realized by thin black phosphorus flakes. The electrical characterization confirms ohmic contacts and current modulation in the device under gate bias along with p-type conduction. We reported a hysteresis in the transfer characteristics growing with the gate sweep range and we demonstrated that it can be exploited to realize memory devices.

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