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Electrical and Thermal Characterisation of β-Ga_2O_3 Devices

Breakdown, Self-Heating, Electrical Performance and Electron Trapping

By

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A dissertation submitted to the University of Bristol in accordance with the requirements of the degree of DOCTOR OF PHILOSOPHY in the Faculty of Physics.

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Abstract

Beta-gallium oxide (β-Ga_2O_3) is a promising wide-bandgap semiconductor for high power applications, such as high-voltage DC converters and low frequency power switches. Such applications require devices that exhibit stable output characteristics under bias stress and that can routinely handle high electric fields. The operating temperatures of such devices have to be minimised in order to maximise their lifetimes. Despite reaching a number of key research milestones, several unresolved problems continue to hinder the commercialisation of β-Ga_2O_3. The degradation of devices at high-voltages and a high degree of self-heating both limit the reliability of β-Ga_2O_3 devices, while deep-level states have been observed to increase device on-resistance and induce threshold voltage instabilities. The investigation of these effects is the focus of this thesis.

High-bias stressing of trench-MOS Schottky-barrier diodes was used to investigate device breakdown. Analysis of the reverse bias leakage current of these diodes revealed two distinct leakage regimes, a low bias leakage current dominated by leakage over the Schottky-barrier, and a high bias leakage dominated by leakage paths through the Al_2O_3 dielectric. Breakdown of the diodes was attributed to the high-bias degradation of the dielectric.

Self-heating in thin-channel β-Ga_2O_3 MOSFETs was then investigated using Raman nanothermography. These measurements revealed an absence of hot-spots for operating powers up to 0.9 W/mm. This was attributed to distributed heating effects in the MOSFET, with the resistive heating in the channel being comparable to that of heating in the high-field region at the drain-side of gate. A comparison of these measurements to a pulsed IV method for extracting averaged channel temperatures, previously reported in the literature, demonstrated a high degree of agreement between the two methods. 3D simulations of the channel temperature profile support this conclusion. Potential anisotropy in the electrical performance of β- Ga_2O_3 MOSFETs was then investigated using pulsed IV characterisation. A large anisotropy in device on-resistance was observed as a function of device orientation relative to the substrate. Raman measurements of the substrate orientation demonstrated that this anisotropy did not correlate with the underlying substrate orientation across two sample sets. The variation in on-resistance was attributed to artifacts in the fabrication of the device.

Electron trapping at a Al_2O_3/Ga_2O_3 interface was investigated using capacitance-voltage characterisation of a MOS-CAP structure. The presence of a distinct ledge in the up-sweep of the capacitance-voltage characteristic, after high bias stressing of the device, was attributed to the presence of an interface trapping state. TCAD simulations demonstrated that the presence of such a state is sufficient to explain the ledge and an observed hysteresis in the capacitance-voltage characteristic. An upper bound of 2.3 eV for the trap state conduction band offset was determined.

Finally, bulk trapping in β- Ga_2O_3 MOSFETs was investigated using deep-level transient current spectroscopy. The presence of a trapping state with an activation energy of 120 meV was consistent with a previously reported trapping state in β-Ga_2O_3. Thermal stressing of the device lead to

the emergence of a new device behaviour, with activation energy of 510 meV. This new behaviour was suppressed after a 350K anneal of the substrate, with a semi-permanent reduction in the drain-current observed. This behaviour was attributed to the charging of electrically isolated regions in the device. The deep-level transient current spectroscopy method is not well suited to the investigation of such charging effects, with a conductive substrate required to separate the impact of buffer trapping from surface trapping. The fabrication of β-Ga_2O_3 devices on a conductive substrate is necessary to model this behaviour.

Dedication and acknowledgements

First I would like to thank Martin Kuball and Michael Uren for their supervision, patience and support throughout the PhD. Their experience and interest in my work has made it a thoroughly rewarding experience. I would also like to thank my collaborators, without whom this thesis would not have been possible. In particular, I would like to express my gratitude to Huili Grace Xing from Cornell University, Andrew Green from the Air Force research Laboratory, and Masataka Higashiwaki from NICT Japan for the samples they have provided and for their feedback on my work. I would also like to give special thanks to Manikant Singh, Stefano Dalcanale, James Pomeroy and Abhishek Mishra for their guidance and training over the past four years, and for the many fruitful discussions we have had.
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Author's declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

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List of Acronyms and Initialisms

- 2DEG - Two Dimensional Electron Gas
- ALD - Atomic Layer Deposition
- BFOM - Baliga Figure of Merit
- CV - Capacitance-voltage
- CVD - Chemical Vapour Deposition
- CVU - Capacitance Voltage Unit
- DFT - Discrete Fourier Transform
- DLTS - Deep-level Transient Spectroscopy
- DUT - Device Under Test
- FE - Field Emission
- FET - Field Effect Transistor
- FIB - Focused Ion Beam
- FN - Fowler-Nordheim
- FOM - Figure of Merit
- FWHM - Full-width Half Maxima
- GND - Ground
- GSG - Ground-signal-ground
- HEMT - High-electron-mobility Transistor
- HV - High Voltage
- HVDC - High-voltage Direct Current

- HVPE - Halide Vapour Phase Epitaxy
- IV - Current-voltage
- JFOM - Johnson Figure of Merit
- MBE - Molecular Beam Epitaxy
- MESFET - Metal–semiconductor Field-effect Transistor
- MOCVD - Metal Organic Chemical Vapor Deposition
- MOS - Metal-oxide-semiconductor
- MOS-CAP - Metal-oxide-semiconductor Capacitor
- MOSFET - Metal-oxide-semiconductor Field-effect Transistor
- MTTF - Mean-time-to-failure
- NNC - Normalised Noise Current
- NQ - Non-quiescent
- PLD - Pulsed Laser Deposition
- Q - Quiescent
- RESURF - Reduced Surface Field
- RF - Radio-frequency
- RIE - Reactive Ion Etching
- SB - Schottky-barrier
- SBD - Schottky-barrier Diode
- SIMS - Secondary Ion Mass Spectrometry
- SMU - Source Measure Unit
- TE - Thermionic Emission
- TFE - Thermionic Field Emission
- TLM - Transmission Line Measurement
- UID - Unintentionally Doped

Chapter 1

Introduction

In 2019 global CO_2 emissions were approximately 32Gt, with almost 13Gt being directly related to electricity generation [1][2]. Network transmissions losses equate to 8% of electricity generation in the UK, and as much as 18% in some regions globally [3]. In total, these transmission losses are responsible for approximately 1Gt of global CO_2 emissions [4]. Therefore, there is a pressing need for high efficiency, high power electronic components for improving grid efficiency and for aiding with the integration of renewable energy with existing power grids. This has spurred interest into components such high-voltage direct current (HVDC) converters for flexible grid operation, electric vehicle power trains, high-voltage wind farm components and photovoltaic inverters [5]. The commercialisation of such components has the potential to significantly impact global electricity demand and its associated CO_2 emissions.
Research into power electronics over the past 30 years has focused on improving the efficiency of silicon power devices [6]. However, as a mature technology, further optimisation of silicon power devices offers diminishing returns, with only another factor of two improvement in 30V FETs thought to be economically feasible [6]. Furthermore, in the area of high power electronics, silicon is limited by its relatively low breakdown field of 0.3 MV/cm [7]. These limitations have initiated the search for new wide-bandgap semiconductors for high-power applications, which will require voltage ratings that are beyond the practical limits of silicon [8]. In particular, research into wide bandgap semiconductors over the past few decades has focused on gallium nitride (GaN) and silicon carbide (SiC). Both of these semiconductors have significantly larger bandgaps than silicon (1.1eV): 3.2eV for 4H-SiC and 3.4eV for GaN. The wider bandgaps afford these materials several key advantages in the design of power devices. Firstly, the bandgap of a semiconductor (E_g) is directly related to its intrinsic breakdown field (E_{br}), with an increase in E_g leading to an increase in E_{br}. The power-law relationship between E_g and E_{br}, ($E_{br} \propto E_g^{\alpha}$), depends on the breakdown

mechanism of the semiconductor, and on whether it has a direct or an indirect bandgap, with the value of α being determined empirically [9]. α is approximately 3 in the case of direct bandgap semiconductors, and between 2.5 and 3 in the case of indirect bandgap semiconductors [10]. As such, the breakdown fields of GaN and SiC are significantly higher than silicon, allowing for devices with higher voltage ratings. In addition, the aggressive scaling down of the device dimensions, in comparison to an equivalent silicon device with the same voltage rating, is made possible by the high breakdown fields of GaN and SiC; both GaN and SiC are capable of handling the higher electric fields associated with a reduction in device dimensions. This scaling down of dimensions leads to a reduction in carrier transit times in a device channel and a reduction in the intrinsic capacitances of the device, both of which are critical for radio-frequency applications. Finally, a wider bandgap is related to a reduced on-resistance (R_{on}) of devices, as thinner drift regions and higher levels of doping can be achieved without triggering device breakdown [11]. The ability to fabricate GaN HEMTs with a 2DEG helps to further reduce the typical R_{on} of power devices [12]. This lower R_{on} leads to lower conduction losses, critical for efficient high-power device operation. The rapid progress in the field of wide bandgap semiconductors has been such that both GaN and SiC power devices are now commercially available [13][14].

As the power ratings of GaN and SiC power devices have increased, so has interest in high-voltage applications that will be difficult to achieve with commercially available devices. In particular, it will be difficult to push GaN and SiC device voltage ratings beyond 3kV and 20kV, respectively [5]. As such, research has shifted over the past decade to (ultra)wide-bandgap semiconductors, with potential voltage handling capabilities in excess of both that of GaN and SiC. By far, the most progress has been made in the field of β-gallium oxide (β-Ga_2O_3) power electronics. The bandgap of β-Ga_2O_3 (4.9eV) is significantly larger than that of the competing wide-bandgap materials, corresponding to an intrinsic breakdown field of 8 MV/cm, (far in excess of SiC and GaN). β-Ga_2O_3 has the added advantage that high-quality, large area crystals can be fabricated from the melt, using the inexpensive Czochralski method [15] [16]. This is in contrast to SiC and GaN; SiC substrates continue to be expensive, while GaN devices suffer from trapping effects associated with heterointerfaces in the substrate epitaxy [17]. Currently, melt grown β-Ga_2O_3 wafers remain expensive, however, a 20-fold decrease in the cost per wafer is expected by 2027 if production volumes reach 1 million wafers per year [18].

The first β-Ga_2O_3 devices, reported by Higashiwaki *et al.*, were single-crystal β-Ga_2O_3 MESFETs [19]. The high breakdown voltage and well behaved DC IV characteristics of these MESFETs spurred research into more sophisticated lateral β-Ga_2O_3 devices. A range of lateral MOSFET devices have been achieved, with Al_2O_3 now used as the standard insulator, due to its wide-bandgap (8.82eV), and ability to alloy with gallium oxide for lattice parameter matching [20][21]. MOSFETs with breakdown voltages as high as 750V were quickly achieved [22], and by 2018 breakdown voltages >1.8 kV had been reported [23]. As of 2022, lateral MOSFETs with breakdown voltages >8kV have been demonstrated [24]. β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HEMTs have

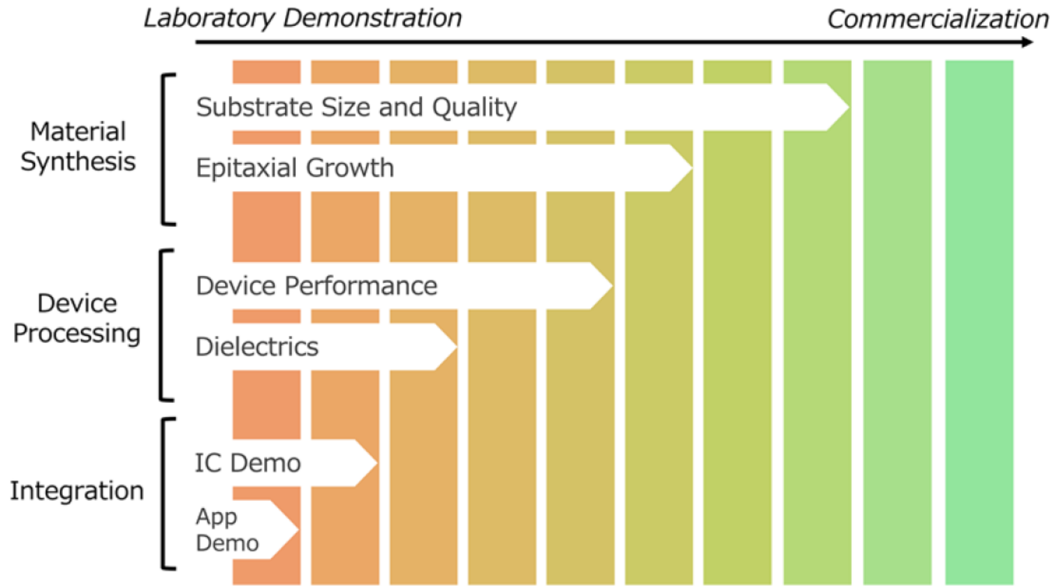


Figure 1.1: The current progress towards the commercialisation of β-Ga_2O_3 devices. Figure reproduced from [18].

been successfully fabricated by Zhang *et al.*, utilising a delta-doping architecture [25]. Interest in vertical devices has also grown over the last few years, as such devices can achieve higher breakdown voltages than lateral MOSFETs and HEMTs (due to their larger channel widths, and the associated lower electric fields). Vertical MOSFETs with breakdown voltages >1kV have been reported [26], with Mg-doped and N-doped charge blocking layers also having been successfully implemented in such devices [27][28][29]. Progress has also been made in the realisation of β-Ga_2O_3 Schottky-barrier diodes (SBDs) for low-frequency power switching applications. A number of different structures have been reported, with the most common being planar SBDs with field-plates, small-angle beveled field-plated SBDs, and trench-MOS SBDs [30]. A breakdown voltage of 1kV has been reported for the planar field-plated SBD structure [31], with a breakdown voltage of 1.1kV reported for beveled SBD structures [32]. Breakdown voltages >2.4 kV have been realised in the trench-MOS SBD architecture [33]. Despite the rapid progress made over the last few years, β-Ga_2O_3 power electronics remain a long way from commercialisation, as shown in Fig.1.1. The growth of β-Ga_2O_3 substrates are nearing commercial viability, with the epitaxial growth of β-Ga_2O_3 device channels not far behind. In contrast, device performance reported in the literature and the fabrication of dielectrics is lacking the quality and consistency required for industrial applications. Without resolving these key issues, a realisation of β-Ga_2O_3's potential is not possible at the system level. Several unresolved problems currently hinder device performance and reliability in β-Ga_2O_3. Arguably the most significant of these is the low thermal conductivity of β-Ga_2O_3. With a maximum thermal conductivity 10 times smaller than that of

GaN, and 6 times smaller than that of SiC, self-heating is a critical design consideration [34]. Self-heating of power devices in the on-state can seriously degrade device performance, and lead to premature device failure [35]. Several thermal management solutions have been suggested in the literature, with heat sinking using metal layers, or the integration of β-Ga_2O_3 with diamond being the most promising [36][37]. However, adequate thermal management in power devices is yet to be demonstrated.
Even if the problem of self-heating is addressed, reliability would still be currently limited by the high-voltage operation required of β-Ga_2O_3 devices. This problem is ubiquitous to power devices, but is particularly acute in β-Ga_2O_3; its breakdown field of 8MV/cm is close to that of the insulating materials used for device dielectric layers and passivisation. As such, the fields that β-Ga_2O_3 devices are routinely expected to handle will pose a particular problem for device reliability, as the degradation of dielectric layers often trigger premature device failure. The degradation of device dielectrics has already been attributed to the premature failure of trench-MOS diodes [38], while the presence of interface states at an Al_2O_3/β-Ga_2O_3 interface has been demonstrated to degrade device performance in the form of an increased on-resistance [39]. Addressing the problem of dielectric reliability remains a key aim of β-Ga_2O_3 research.
Finally, the wide bandgap of β-Ga_2O_3 presents its own problem, in the form of deep-level trapping states. While the (ultra)wide-bandgap of β-Ga_2O_3 is indisputably an asset for high power applications, it also allows for large (>1eV) conduction and valence band offsets for defect and impurity states. The lifetime of such states can be arbitrarily long, and can easily exceed the lifetime of the device. Therefore, the charging of deep-level states can result in significant, semi-permanent, changes in device behaviour. The problem of deep-level trapping states is by no means unique to β-Ga_2O_3, having previously been addressed in the case of C-doped GaN buffers [40]. However, GaN has benefited from two decades of research, over which the understanding of deep-level trapping states and modelling of their impact on device behaviour was refined. A similar effort is now required if β-Ga_2O_3 device reliability is ever to be of a high enough standard for industrial applications.

1.1 Thesis Outline

Investigating and understanding some of the unresolved issues that will hinder the commercialisation of β-Ga_2O_3 devices is the aim of this thesis. Both vertical and lateral devices are used to explore electrical and thermal issues that affect device performance, with device breakdown, self-heating, anisotropic electrical effects and trapping states all covered in the subsequent results chapters. A brief outline of the structure and content of the thesis follows.
Chapter 2 provides the necessary theoretical background required to understand the subsequent results chapters. This chapter begins with a discussion of β-Ga_2O_3's structure, and its resulting band diagram, phonon modes, and phonon dispersion. The electrical and thermal properties of

the material are then outlined, with particular attention paid to the parameters that impact device performance. The potential applications of β-Ga_2O_3 are then discussed, with a comparison to other commonly cited (ultra)wide-bandgap semiconductors. The relevant device physics is then discussed, with an overview of metal-semiconductor contacts and metal-oxide-semiconductor (MOS) interfaces presented. The physics of these interface are then used to describe the operation of MOS field-effect-transistors. The applications and operation of Schottky barrier diodes (SBDs) is then introduced, along with the reduced surface field (RESURF) effect in trench-MOS SBDs: a critical technique for achieving breakdown voltages >1kV in β-Ga_2O_3. The fabrication of β-Ga_2O_3 devices is then outlined. Finally, some critical problems with β-Ga_2O_3 device reliability are discussed: instabilities in the electrical performance of devices are presented in the context of electron trapping and leakage current, and the lifetime limiting effect of device self-heating is reviewed.
Chapter 3 details the experimental methods used throughout this thesis. The typical measurement environment used during the electrical characterisation of devices is introduced. The impact of different probe tips and cabling on the resolution of measurements is then discussed. Electric characterisation techniques are then discussed in detail. The DC characterisation and pulsed characterisation are explained, with the former used to measure device output characteristics and the latter to investigate self-heating and electron trapping. An overview of low-voltage capacitance-voltage measurements is then given. All three of the electrical characterisation techniques covered in chapter 3 can be integrated with a cryogenic probe station. The layout and the specifications of this probe station are briefly discussed. The functioning of a Raman spectrometer is then outlined, along with the resolution limits imposed by the choice of microscope objective, with this being relevant for the thermal characterisation of devices in later chapters. This chapter ends by detailing the simulation techniques used to support and corroborate measured data. Electrical simulations are performed using the Silvaco ATLAS drift-diffusion simulator and thermal simulations performed using the 3D ANSYS simulator. The models and meshing techniques relevant to both the the simulators are outlined.
Chapter 4 focuses on the breakdown mechanisms in vertical trench-MOS β-Ga_2O_3 Schottky-barrier diodes (SBD). These diodes employ a RESURF effect in order to achieve reverse bias operation far in excess of a planar Schottky-barrier diode architecture. The reverse leakage characteristics of these devices exhibited soft-breakdown events, in which a sharp increase in the leakage current is observed. A novel noise technique, developed by Dalcanale *et al.* [41], is applied to analyse the leakage current noise of these devices. A comparison of this noise data with that of planar Schottky-barrier diodes and planar MOS-CAP structures reveals a transition in the dominant leakage path of the trench-MOS diodes, from the Schottky barrier interface to oxide leakage. This change in leakage path is attributed to degradation of oxide layers in these diodes. The architecture of the trench etched inherently leads to high fields over the oxide layers, and so the observed device failure due to oxide degradation poses a significant problem to the

commercialisation of such devices. Optimising the barrier height of the Schottky interface, to allow for a less aggressive RESURF effect, is the key to extending the lifetime of the trench-MOS Schottky-barrier diode structure.

Chapter 5 details potential issues in lateral β-Ga_2O_3 MOSFETs. Initially, device self-heating is characterised using the Raman nanothermography technique, with a direct measurement of channel temperature profiles performed. This data is compared to values of channel averaged temperature extracted using a pulsed IV technique, previously reported by Blumenschein *et al.* [42]. A high degree of agreement is observed between the Raman nanothermography technique and the pulsed IV technique. The agreement between these two techniques is attributed to the lack of thermal hotspots in the device channel. The anisotropy in device self-heating, with respect to gate orientation on the β-Ga_2O_3 substrate, is then investigated using 3D finite element thermal simulations. For simulated devices on a [010] orientated substrate, no significant anisotropy in the channel temperature is observed as a function of gate orientation. This is despite the anistropic thermal conductivity of β-Ga_2O_3. Potential electrical anisotropy in device behaviour is then investigated, with low-field values of device R_{on} extracted across a number of MOSFETs with varying gate orientations. A large anisotropy is observed across two sample sets, however, Raman spectroscopy measurements demonstrates that this anisotropy is not correlated any underlying crystalline direction in the β-Ga_2O_3 substrate. As such, the anisotropy is attributed to the process and fabrication of these devices. Variations in device processing appear to dominate over any intrinsic anisotropy in the properties of β-Ga_2O_3. This highlights the continuing problem of device quality in β-Ga_2O_3; as a relatively novel material, considerations such as thermal and electrical anisotropies should be secondary to optimising device quality.

Finally, chapter 6 is concerned with electron trapping in β-Ga_2O_3 devices and its impact on device performance. Trapping at an Al_2O_3/β-Ga_2O_3 interface is explored using CV measurements of a MOS-CAP device after high-bias stressing. A distinct trapping ledge is attributed to the presence of interface traps and a model is proposed to explain the hysteretic effects observed in the CV characteristics. By considering the behaviour of the surface potential during the measurements, and by considering background charging effects, an upper bound of 2.3eV for the conduction band offset of the interface trap level is determined. Bulk traps in β-Ga_2O_3 MOSFETs are then investigated using deep-level transient current spectroscopy measurements. Two large transitions in trapping behaviour are observed after thermally cycling the devices, with semi-permanent changes in device behaviour induced. A conclusive model of this behaviour could not be proposed, but it is likely that it is related to the charging of electrically isolated regions in the device. These problems are similar to those initially faced by other (ultra)wide-bandgap semiconductors, such as GaN, and highlights the importance of further research into the location and behaviour of deep-level trapping states in β-Ga_2O_3 devices. Chapter 7 presents the conclusions drawn from the results chapters of this thesis.

Chapter 2

Background

The focus of this chapter is to provide the theory and background required in the subsequent results chapters. This chapter will also discuss some relevant growth techniques, semiconductor physics and the background to some key measurement techniques. A key aim of this chapter is to benchmark the properties of β-Ga_2O_3 against some other commonly cited (ultra)wide-bandgap semiconductors, as β-Ga_2O_3 remains a relatively novel material.

2.1 Gallium Oxide

Gallium oxide is a compound semiconductor with six distinct polymorphs; α, β, γ, δ, ϵ and κ. The α-phase has a rhombohedral structure, the β-phase a monoclinic structure, the γ-phase a cubic structure and the ϵ-phase an orthorhombic structure [43][44][45]. These four phases constitute the bulk of research into Gallium Oxide, with the κ and the δ phase being the least studied [46][47]. The three principle phases targeted by device research are the α, β and the ϵ phase. Of these phases, only the β phase is thermally stable, with all other phases being metastable. The formation free energies of the phases varies between phases in the following way: $\beta < \epsilon < \alpha < \delta < \gamma$ [48]. The α phase is stable up to growth temperatures of 800^oC and has the corundum structure common to other oxides, e.g. Al_2O_3 [46]. Therefore, this phase is well suited for integration with with other wide-bandgap semiconductors, e.g. the formation of heterojunctions. The ϵ phase has an intrinsic polarisation due to crystal symmetry [49], and so is potentially of interest for the fabrication of gallium oxide high-electron-mobility-transistors (HEMTs) [50]. However, the vast majority of research into gallium oxide has focused on the β-phase. This thesis focuses exclusively on β-Ga_2O_3 devices, and as such, the rest of this chapter will focus on the properties of this phase.

The unit cell of β-Ga_2O_3 is shown in Fig.2.1. This cell contains 20 atoms (8 Ga and 12 O) and belongs to the space group C2/m. There are two inequivalent gallium sites, one with an octahedral

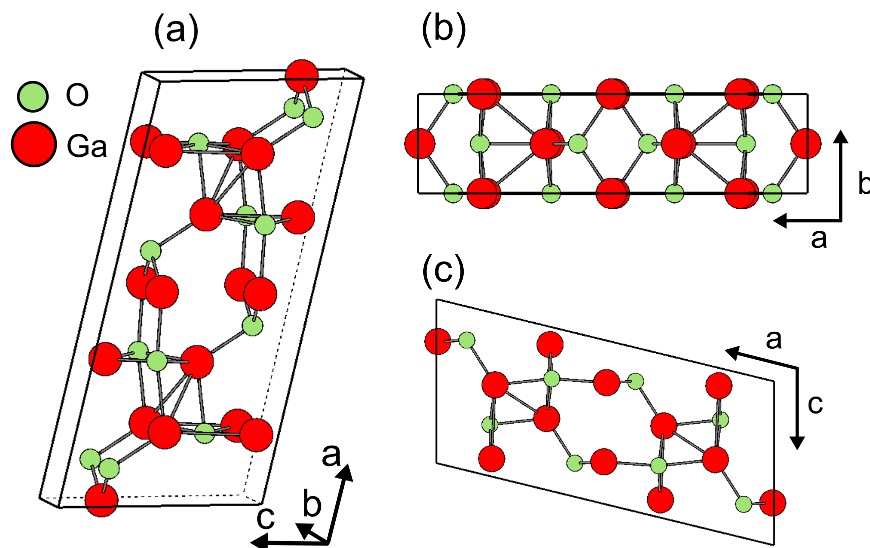


Figure 2.1: (a) The monoclinic structure of β-Ga_2O_3, with the black lines marking the outline of the unit cell. The angle between the a and the c axes is 103.7^o, with the a and b axes being orthogonal. (b) The unit cell viewed down the c direction (c) and the b direction.

coordination and the other with a tetrahedral coordination. The oxygen atoms sit in a distorted cubic structure, with three inequivalent sites. Two of these sites have a three-fold coordination and one site has a fourfold coordination.

The first Brillouin zone of β-Ga_2O_3's monoclinical crystal is required to understand its electronic properties. The Brillouin zone is defined as the reciprocal space Wigner-Seitz cell. A Wigner-Seitz cell is a primitive cell (a cell containing exactly one lattice point) around a lattice point. The points inside the cell are closer to the enclosed lattice point than any lattice points outside the cell [52]. While any number of primitive cells can be defined for a given lattice in reciprocal space, the Wigner-Seitz cell is unique [53]. Fig.2.2(a) shows the first Brillouin zone of β-Ga_2O_3. The point Γ at the centre of the cell represents zero momentum state, with other points of high-symmetry labelled on across the cell. It can be shown that any reciprocal space momentum point outside of the first Brillouin zone is equivalent to a corresponding point within the zone. Therefore, the first Brillouin zone is all that is required to describe the energy-momentum relationship of carriers in the lattice [52]. This relationship is key to understanding the dynamics of carriers in a crystal, and is determined by the band structure of the material. Conventionally, the band structure is obtained by solving the Schrödinger equation for a single electron in the crystal [52],

$$\left[\frac{\hbar^2}{2m_e^*}\nabla^2 + V(\mathbf{r})\right]\Psi(\mathbf{r},\mathbf{k}) = E(\mathbf{k})\Psi(\mathbf{r},\mathbf{k}), \tag{2.1}$$

where m_e^* is the effective mass of the electron, $V(\mathbf{r})$ is the electronic potential of the lattice, $E(\mathbf{k})$ is the electron energy and $\Psi(\mathbf{r},\mathbf{k})$ is the electron wave function. The Bloch theorem states that, if

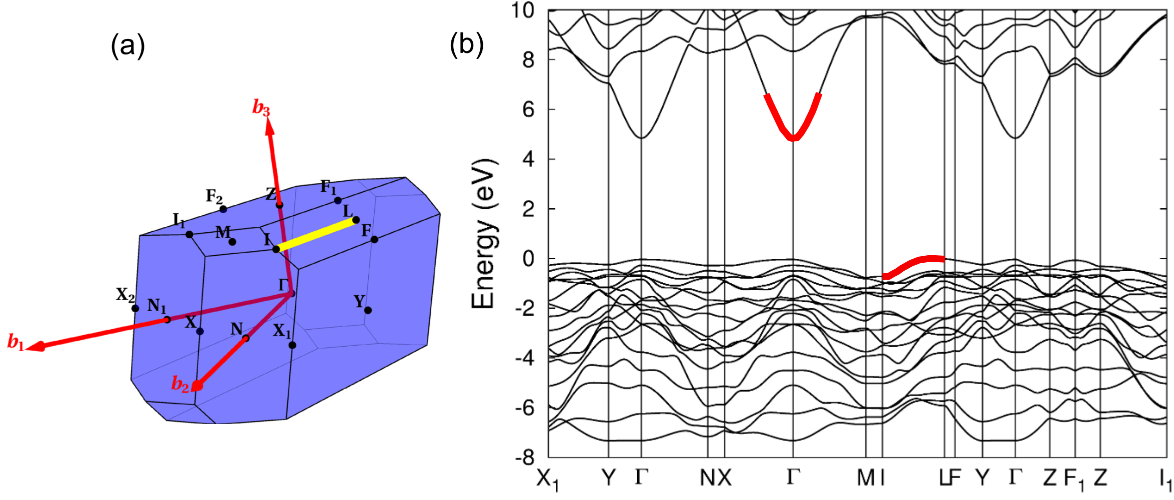


Figure 2.2: (a) The first Brillouin zone of β-Ga_2O_3, with the high-symmetry points labelled. The yellow line between the I and L point indicates the position of the valence band maxima. (b) The corresponding band structure, with the conduction band minia and valence band maxima outlined in red. Figure reproduced from [51].

$V(\mathbf{r})$ is periodic, then the solution to Eqn.2.1 will take the form of a Bloch function,

$$\Psi(\mathbf{r},\mathbf{k}) = e^{(j\mathbf{k}.\mathbf{r})}U_b(\mathbf{r},\mathbf{k}), \tag{2.2}$$

where $U_b(\mathbf{r},\mathbf{k})$ is a function with the same periodicity as the lattice; the Bloch function takes the form of an electron plane wave [54]. By solving Eqn.2.1 for each momentum state, the electronic band structure can be determined. Fig.2.2(b) shows the band-structure of β-Ga_2O_3, with the high symmetry points labelled. Both the conduction band minima and the valence and maxima are highlighted in red, with the corresponding position of the valence band maxima indicated in Fig.2.2(a) by the yellow line. The key feature of this band structure is the approximately flat valence band. While β-Ga_2O_3 is an indirect bandgap semiconductor, the small variation in the valence band means that the direct bandgap at Γ, and the indirect bandgap between Γ and L, have approximately the same energies (4.88eV and 4.84eV respectively) [51]. Low indirect bandgap transition probabilities, and the small energy difference between the direct and indirect bandgaps, means that β-Ga_2O_3 effectively acts as a direct bandgap semiconductor [15].

The flat valence band also has a strong impact on the carrier dynamics. The effective mass of carriers in a semiconductor are, to first order, determined by the curvature of the bands. In the vicinity of a band minia or maxima, the energy-momentum relationship can approximated using the quadratic expression:

$$E(k) = \frac{\hbar^2 k^2}{2m^*}, \tag{2.3}$$

where m^* is the effective mass of the carrier. The conduction bands minima at Γ gives rise to an effective electron mass of 0.27m_e [15], while the approximately flat valence band leads to

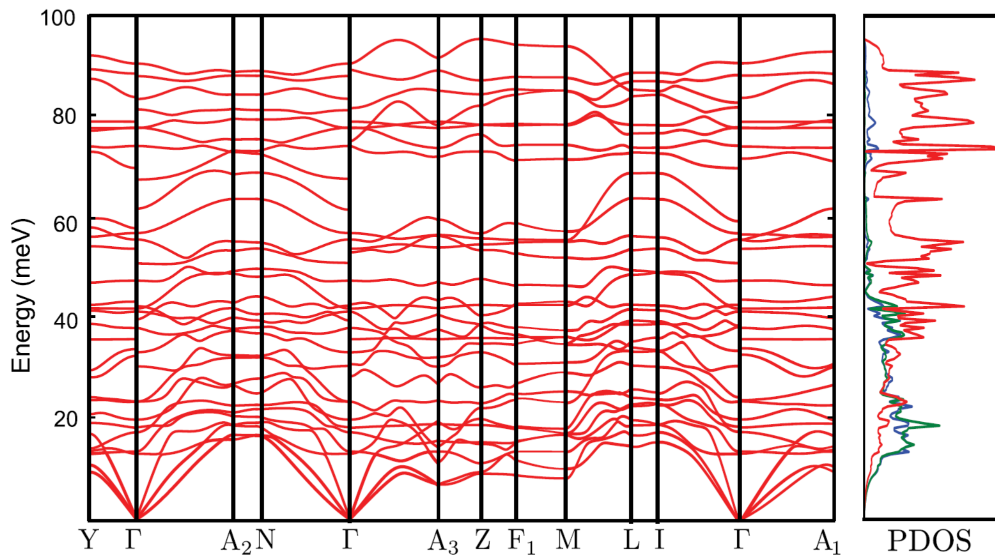


Figure 2.3: The phonon dispersion and phonon density of states for β-Ga_2O_3. Figure adapted from [61].

an incredibly high effective hole mass. This behaviour can be explained with reference to the hybridisation of electron orbitals. The conduction band is mainly composed of delocalised Ga 4s derived states, while the valence band is mainly formed by occupied O $2p^6$ derived states with minor hybridization of the Ga 3d, 4p, and 4s orbitals [55] [56]. The tightly bound O 2p states give rise to the high effective hole mass, in common with other oxides [57]. It has been observed that holes are effectively static in β-Ga_2O_3, as the result of the formation of static polaron states [58]. As such, β-Ga_2O_3 is a unipolar material, and only semiconductor devices exploiting n-type mobility are thought to be achievable [59].

2.1.1 Raman Scattering and Phonon Dispersion in the Monoclinic Structure

In order to understand thermal transport in β-Ga_2O_3 it is necessary to understand the vibrational modes of the lattice, with these modes being primarily responsible for the storage and transport of heat. For a unit cell with N atoms, there are $3N$ degrees of freedom, with each degree of freedom giving rise to a vibrational mode. Of these $3N$ modes, $3N$-3 are optical modes, and 3 are acoustic [54]. The acoustic modes represent collective vibrations that are in phase across the unit cell, while the optical modes represent out of phase vibrations.

The vibrational modes of a lattice can represented as quantised bosonic excitations, or as phonon modes. β-Ga_2O_3 has 30 phonon modes (27 optical and 3 acoustic), as its primitive cell contains 10 atoms with three translational degrees of freedom. The dispersion and density of states of these modes is shown in Fig.2.3, with the high-symmetry points of the Brillouin zone labelled. The 27 optical modes can be represented by irreducible representations at the Γ-point [60],

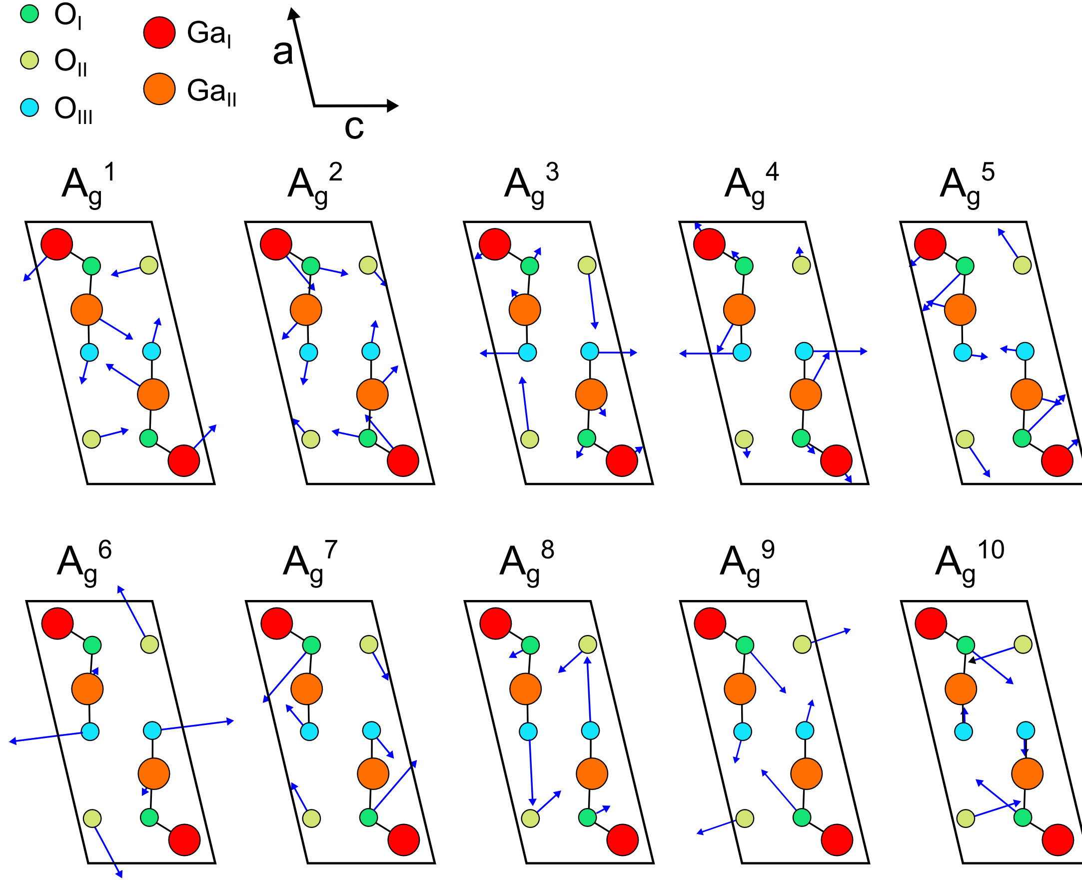


Figure 2.4: The displacement of atoms in the primitive cell of β-Ga_2O_3 for the Raman-active modes with A_g symmetry. The primitive cell is viewed down the [010] direction. The relative size of the arrows indicates the relative amplitude of the atomic displacements, with values taken from [62].

$$\Gamma^{opt} = 10A_g + 5B_g + 4A_u + 8B_u, \tag{2.4}$$

where the A_g and B_g modes are Raman active, and the A_u and B_u modes are IR active. A and B correspond to a symmetry of the mode, with the A modes being symmetric with respect to principal axis of symmetry, and the B modes being antisymmetric. Fig.2.4 shows the physical displacement of atoms in the primitive cell for each of the 10 A_g modes, with the primitive cell viewed down the [010] direction. The relative amplitude of each displacement is represented by the relative size of each arrow.

The scattering of light can be used to measure the properties of a crystal, such as the lattice temperature, the degree of atomic disorder present in the crystal and the presence strain fields. One such process is Raman scattering, in which the interaction between light and phonon modes leads to the inelastic scattering of photons. Raman scattering can be modelled both classically

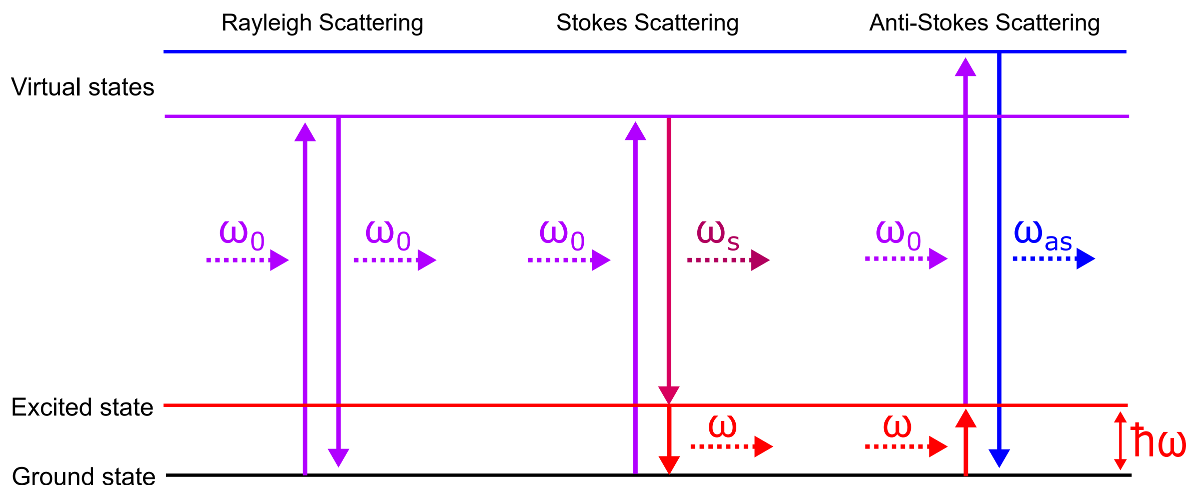


Figure 2.5: Energy transitions relevant to Raman scattering. Rayleigh scattering correspond to an elastic scattering event, whereas Raman scattering is an inelastic process. Stokes and anti-Stokes scattering are both types of Raman scattering.

and using quantum mechanics. A treatment of the classic view of Raman scattering is present by Ferraro *et al.* [63], while a quantum mechanical picture is detailed by Szymanski *et al.* [64]. In this section, the quantum mechanical picture will be outlined.

Raman scattering can be explained with reference to a simplified energy level system, with three scattering schemes shown in Fig.2.5. Initially the system exists in the zero-vibration ground state. If a photon energy $\hbar\omega_0$ is incident on the crystal, it can be elastically scattered (Rayleigh scattering). The system is excited to a virtual energy state and then relaxes, emitting a photon of the same energy. This process accounts for the vast majority of all scattering events, with only 1 in 10^6-10^8 photons scattered inelastically [65]. Raman scattering consists of two inelastic processes: Stokes scattering and anti-Stokes scattering. In the case of Stokes scattering, the incident photon excites the system from the ground state to a virtual energy state. The system then relaxes to the ground state through the generation of photon, energy $\hbar\omega_s$, and a phonon with energy $\hbar\omega$, with a net transfer of energy from the photon to the lattice. In the case of anti-Stokes scattering, the lattice is initially excited to an excited state via the absorption of lattice phonon with an energy of $\hbar\omega$. The incident photon is then absorbed, promoting the system to a higher energy virtual state. Relaxation to the ground state leads to an emission of a photon with energy $\hbar\omega_{as}$, with a net transfer of energy from the lattice to the photon. The energies of the Stokes and the anti-Stokes photons are given by the following expressions,

$$Stokes : \hbar\omega_s = \hbar(\omega_0 - \omega) \tag{2.5}$$

$$anti-Stokes : \hbar\omega_{as} = \hbar(\omega_0 + \omega). \tag{2.6}$$

The relative intensities of the two Raman scattering processes is determined by the ground state configuration of the system. At finite temperature T, the population of states will be distributed

between the ground state and higher energy vibration states. As phonons are bosons, the relative population of the ground state and higher energy states is determined by Bose-Einstein statistics. In the case where $\omega \ll \omega_0$, the Bose-Einstein distribution can be simplified to a Boltzmann factor, yielding a relationship between the Stokes intensity (I_s) and anti-Stokes intensity (I_{as}) of the form [66]:

$$\frac{I_{as}}{I_s} \approx exp\left(-\frac{\hbar\omega}{kT}\right). \tag{2.7}$$

At room temperature, the majority of vibration modes will have an energy greater than the Boltzmann factor, and so the Stokes scattering intensity will be greater than that of the anti-Stokes scattering intensity. This disparity increases with increasing phonon mode energy. As such, the contribution of the anti-Stokes component to the Raman scattering intensity can often be discounted.

The Raman scattering intensity is also dependent on the polarisation of the incident photons relative to the lattice. The scattering intensity can be expressed in the form,

$$I \propto |\hat{e}_0 \cdot \mathscr{R} \cdot \hat{e}_s|, \tag{2.8}$$

where $\hat{e}_0$ is the polarisation of the incident photon, $\hat{e}_s$ the polarisation of the scattered photon and $\mathscr{R}$ the Raman tensor. The Raman tensor is a second order tensor whose elements are determined by the symmetry of the phonon mode. In the case of β-Ga_2O_3, the Raman tensors for the A_g and B_g modes are,

$$A_g : \mathscr{R} = \begin{pmatrix} a & d & 0 \\ d & b & 0 \\ 0 & 0 & c \end{pmatrix}, \quad B_g : \mathscr{R} = \begin{pmatrix} 0 & 0 & e \\ 0 & 0 & f \\ e & f & 0 \end{pmatrix}, \tag{2.9}$$

where a, b, c, d and e are constants. The structure of these tensors leads to selection rules that can result in either set of modes being suppressed, based on the polarisation configuration of the measurement. For instance, B_g modes are forbidden on the (010) plane [67]. Eqn.2.8 is valid when the incident polarisation of the photons is well defined and the scattering can be approximated as point-scattering [67]. In the case of highly anistropic crystals, these assumptions are not valid. A significant degree of birefringence in anistropic crystals leads to a change in polarisation of the incident photons: from linear polarisation to elliptically polarisation [68]. A full treatment of the Raman tensor elements for the anisotropic monoclinic structure is given by Kranert *et al.* [67].

The frequency of Raman modes are temperature dependent, and so can be utilised to study temperature changes in a semiconductor. A decrease in the frequency of modes is observed as temperature increases. Several physical effects induce change in frequency, with damping of phonons, induced strain in the crystal and changes in the crystal volume all contributing. The frequency of a mode at a given temperature ($\omega(T)$) is simply given by subtracting each of these contributions from the harmonic phonon frequency (ω_0):

$$\omega(T) = \omega_0 - \Delta\omega_s(T) - \Delta\omega_d(T) - \Delta\omega_v(T). \tag{2.10}$$

$\Delta\omega_s(T)$ represents the thermal strain generated between materials with different coefficients of thermal expansion, with this term equal to zero for a single crystal. $\Delta\omega_d(T)$ represents damping of phonons with temperature, and $\Delta\omega_v(T)$ represents changes in frequency due to thermal expansion of the crystal volume. Each of these terms has a complex temperature dependence. Cui *et al.* proposed an empirical formula to fit the temperature dependence of phonon frequencies in general [69],

$$\omega(T) = \omega_0 - \frac{A}{e^{(Bhc\omega_0/kT)} - 1}, \tag{2.11}$$

where A and B are fitting parameters. At high temperature this expression can be approximated with the following linear expression,

$$\omega(T) = -\frac{Ak\Delta T}{Bhc\omega_0}. \tag{2.12}$$

2.1.2 Electron Transport in β-Ga_2O_3

High-power electronic applications require semiconductors with high critical breakdown fields and high thermal conductivities. The low symmetry of the monoclinical crystal structure gives rise to strong anisotropies in β-Ga_2O_3's thermal conductivity, and potentially in its electron mobility.

The electron mobility of a semiconductor (μ) in the Drude model is determined by the effective electron mass m_e^*, the electron charge e, and the low-field scattering rate τ [70],

$$\mu = \frac{e\tau}{m_e^*}. \tag{2.13}$$

A comparison of the effective electron masses of some commonly cited compound semiconductors is shown in Fig.2.6(a). A variation of <50% in m_e^* is observed for the semiconductors with bandgaps >3eV. Therefore, the value of τ in Eqn.2.13 is critical for accessing the suitability of a semiconductor for device applications requiring high electron mobilities, as it varies to a far greater degree than m_e^* [71]. The magnitude of τ will be determined by a superposition of many scattering mechanism, each with its own characteristic scattering time constant. Assuming all scattering mechanisms are independent, Matthiessen's rule can be applied to combine all mobility terms into a single term [52],

$$\frac{1}{\tau_{total}} = \sum_{n=1}^{n}\left(\frac{1}{\tau_n}\right), \tag{2.14}$$

where τ_{total} is the electron scattering time constant. From Eqn.2.14 it follows that:

$$\frac{1}{\mu_{total}} = \sum_{n=1}^{n}\left(\frac{1}{\mu_n}\right), \tag{2.15}$$

where μ_{total} is the total electron mobility of the system. Fig.2.6(b) shows the temperature dependence of the electron mobility in β-Ga_2O_3, calculated by summing over the main contributing scattering mechanisms [70]. The scattering mechanisms considered are: acoustic deformation

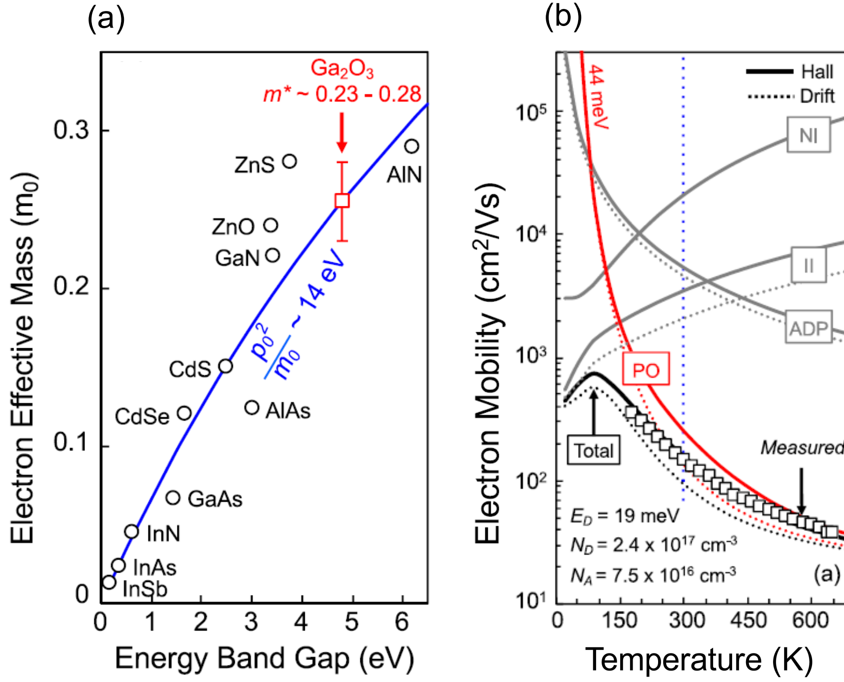


Figure 2.6: (a) A comparison of the effective electron masses of some commonly cited compound semiconductors. (b) The temperature dependence of electron mobility in β-Ga_2O_3. Figure reproduced from [70]

potential scattering (μ_{ADP}); ionized and neutral impurity scattering (μ_{NI} and μ_{II} respectively); and polar-optical (PO) phonon scattering (μ_{PO}). The coupling constant for the PO-phonon-electron interaction is given by the expression provided in [70], and is dependent of the energy of the PO-phonon. In the case of β-Ga_2O_3 the relevant phonon energy is 35–48 meV [72]. While β-Ga_2O_3 has no net polarisation charge, (in contrast to GaN), the PO-phonon coupling constant in β-Ga_2O_3 is three times that of GaN [73][71]. As a result of this large coupling constant, the room temperature electron mobility is limited by the PO-phonon-electron scattering mechanism (Fig.2.6(b)). This severely limits the bulk electron mobility in β-Ga_2O_3 to values <200 $cm^2V^{-1}s^{-1}$, in low doped systems at 300K [70]. PO-phonon scattering limited mobility is also observed in β-$(Al_xGa_{1-x})_2O_3/Ga_2O_3$ HEMTs [25].

The low crystal symmetry of the monoclinic structure in β-Ga_2O_3 hints at a potential anistropic electron mobility. This could be either the result of an anisotropic effective electron mass, or an anisotropy in the electron scattering mechanisms. The effective mass of electrons in β-Ga_2O_3 is predicted to be approximately isotropic, with a variation <4% between crystal axes [74]. However, the scattering mechanisms mediating electron transport are predicted to be anisotropic [75]. For doping levels $n \leq 10^{18} cm^{-3}$ the intrinsic variation in phonon scattering rates is predicted to be <30% [76].

High-field transport is also of interest in β-Ga_2O_3. Fig.2.7 shows simulated velocity-field curves

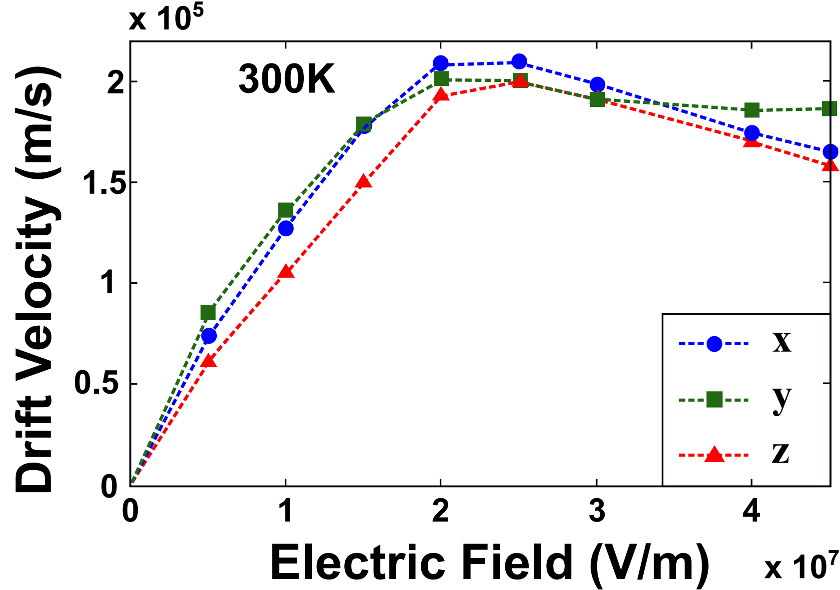


Figure 2.7: Velocity-field relationship for β-Ga_2O_3 calculated using full band Monte Carlo simulations in a Cartesian coordinate system. X corresponds to the [100] direction and Y to the [010] direction. Z does not correspond to a unit vector of the lattice, being orthogonal to both the x and y directions. Figure adapted from [77]

along three orthogonal directions, simulated using a full band Monte Carlo method [77]. No significant variation is observed as a function of direction, with a small reduction in the velocity-field scaling observed along the y direction. There is no significant drop-off in the drift velocity over the range of fields considered, in contrast to other semiconductors such as GaAs and GaN [78][79]. This difference can be attributed to the respective band structures of each semiconductor. In the case of GaN and GaAs, electron velocities are reduced at higher fields by electrons scattering into higher energy valleys in the conduction band. These bands have lower effective electron masses, leading to a reduction in the electron velocity. There is a secondary valley at the Γ point in the band structure of β-Ga_2O_3, (see Fig.2.2). This secondary valley is 2.4eV above the lowest energy conduction band minima, in contrast to GaAs, where the closest satellite valley is 0.3eV above the conduction band minima [80]. Significant intra-band scattering in β-Ga_2O_3 only occurs at higher fields than those considered in Fig.2.7.

2.1.3 Thermal Conductivity of β-Ga_2O_3

The low crystal symmetry, and the resulting anisotropy in phonon modes, also strongly impact the thermal conductivity of β-Ga_2O_3. In many semiconductors, it can be assumed that the contribution of acoustic phonon modes to the thermal conductivity dominates over the contribution of the optical phonon modes. This assumption is justified by the low group velocities and short

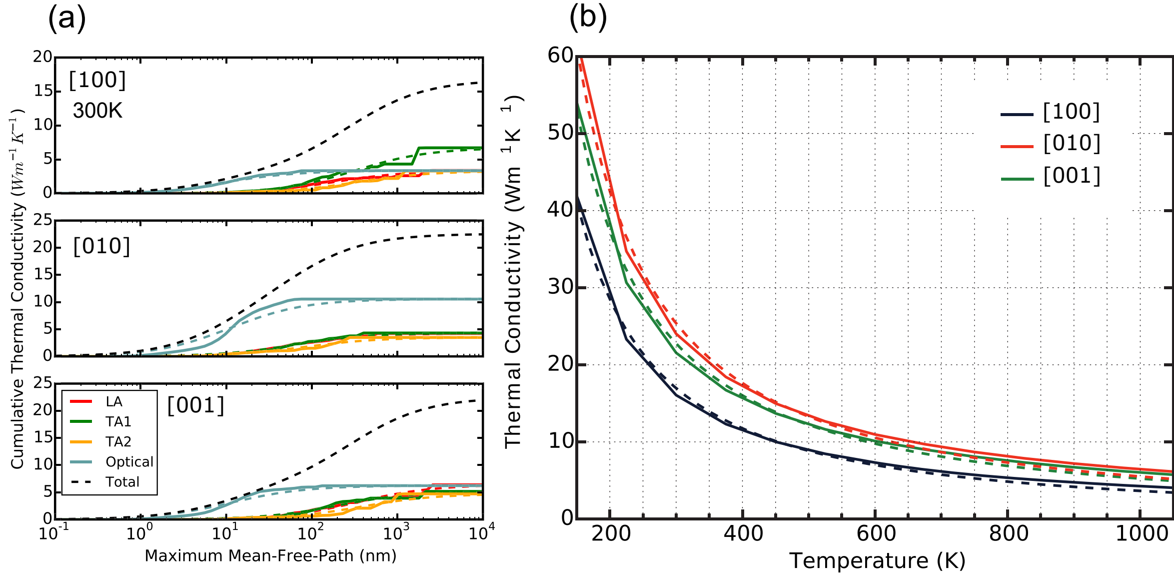


Figure 2.8: (a) The calculated contribution of the three acoustic modes (LA, TA1 and TA2) and the optical modes to the thermal conductivity of β-Ga_2O_3, as a function of mean free path. (b) Calculated thermal conductivity as a function of temperature. Figure adapted from [61].

lifetimes of optical modes [81] [34]. However, this is not the case in β-Ga_2O_3; optical modes contribute up to 25% of the thermal conductivity along the [100] and [001] directions, and up to 44% along the [010] direction [61]. The black dotted lines in Fig.2.8(a) show the calculated thermal conductivity down the three principle crystalline directions, as a function of phonon mean free path (MFP). The contributions of the acoustic modes (LA, TA1 and TA2) and the optical modes are also displayed. It is clear that in bulk β-Ga_2O_3 (MFP = 10^4nm), both sets of modes exhibit an anisotropy as a function of crystal orientation, and both contribute significantly to the total thermal conductivity of β-Ga_2O_3. The temperature dependence of the thermal conductivity in Fig.2.8(b) exhibits an anisotropy, with a maximum in the [010] direction and a minimum in the [100] direction. This trend is in agreement with experimentally measured thermal conductivities, although Fig.2.8(b) underestimates the degree of anisotropy observed in bulk crystals, particularly between the [010] direction and the [001] direction.

The variation in the thermal conductivity as a function of crystal orientation, reported by Guo *et al.*, is shown in Fig.2.9 [34]. The thermal conductivity varies from 27 W/mK in the [010] direction to 10.9 W/mK in the [100] direction. It should be noted that the maximum room temperature thermal conductivity of β-Ga_2O_3 is only around 10% that of GaN [82]. This low thermal conductivity can be explained with reference to the relaxation time of phonons in β-Ga_2O_3. Although β-Ga_2O_3 possesses a similar heat capacity and a similar phonon group velocities to GaN, the phonon lifetimes are far shorter, leading to a lower thermal conductivity overall [34][83].

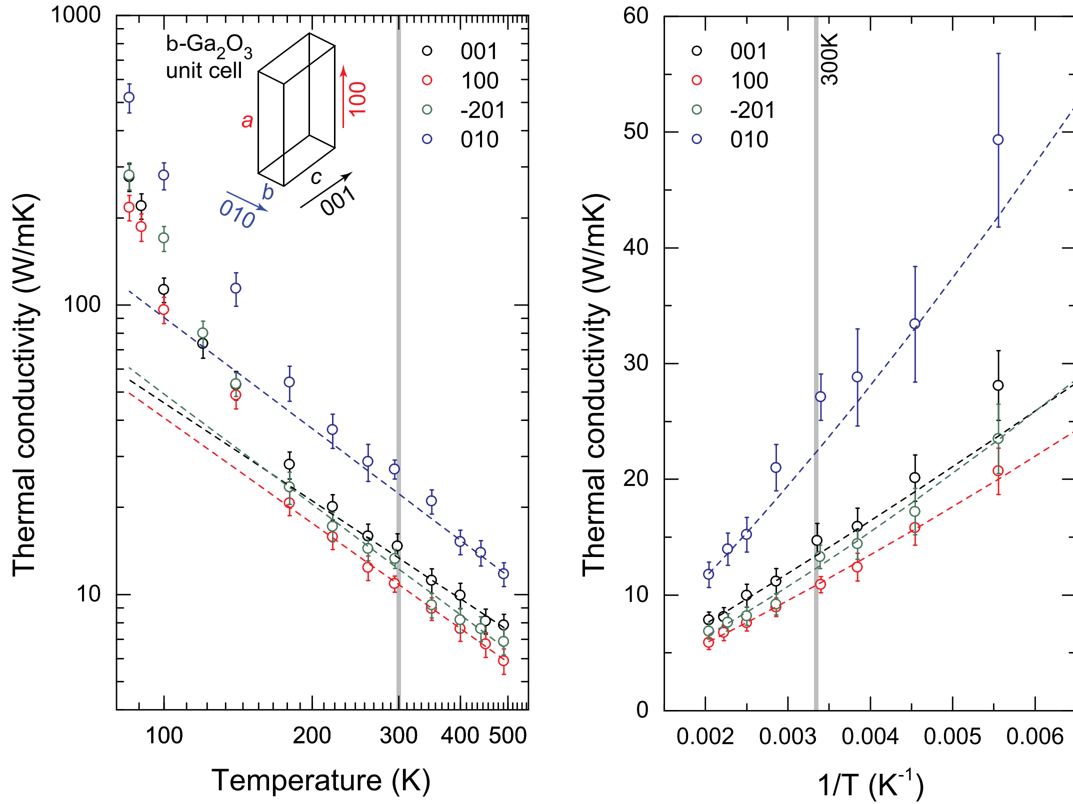


Figure 2.9: The thermal conductivity of β-Ga_2O_3, measured as a function of temperature down four crystal directions using time-domain thermoreflectance. Figure reproduced from [34].

2.1.4 Applications of β-Ga_2O_3

The aim of (ultra)-wide-bandgap research over the past two decades has been twofold; to improve upon the performance of existing devices, and to access applications spaces that semiconductors such as Si and GaAs are intrinsically excluded from by their material properties. There are two important application spaces that beyond-silicon materials have the potential to exploit: radio-frequency (RF) applications and high-voltage (>1kV) applications. Broadly speaking, RF applications require high electron velocities and mobilities, coupled with an aggressive scaling down of device dimensions. High electron velocities reduce the electron transit time in the device channel. The scaling down of device dimensions also reduce the electron transit time, as well as reducing the device's intrinsic capacitances. A reduction in both the electron transit time and the device capacitances are critical for reducing a device's switching time. Power applications also call for the scaling down of device dimensions, but this is largely to reduce the footprint of power circuits, and to reduce the volume/surface area ratio of devices with the aim of improved thermal management. Thermal management is a key consideration for both sets of applications, and particularly for a material such as β-Ga_2O_3, with its low thermal conductivity. Fig.2.10(a) shows the scaling of on-resistance (R_{on}) with breakdown voltage for some widely studied semiconductors,

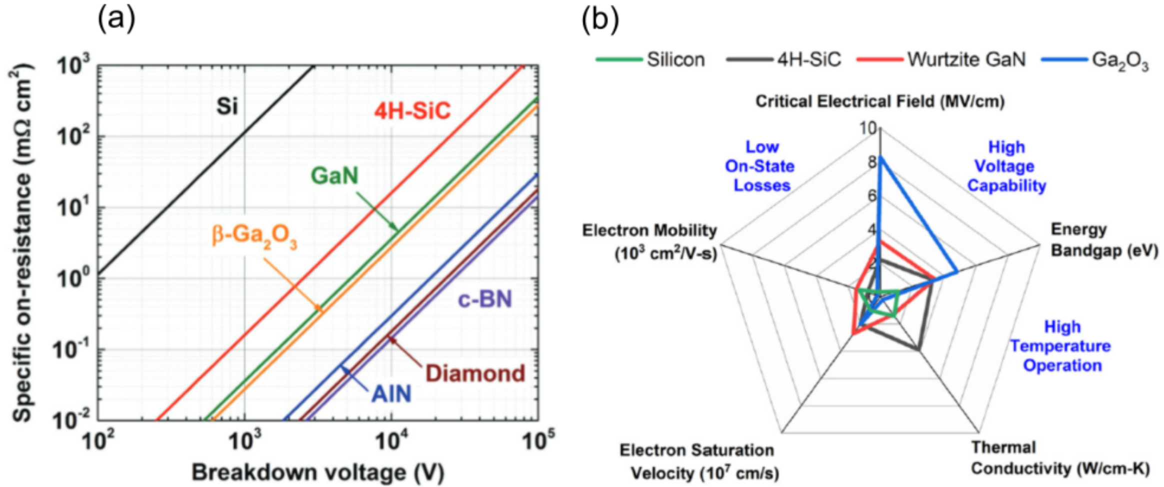


Figure 2.10: (a) The scaling of on-resistance with breakdown voltage for some commonly cited (ultra)wide-bandgap semiconductors. Figure reproduced from [84] (b) A comparison of some key material parameters for some commonly cited (ultra)wide-bandgap semiconductors. Figure reproduced from [5].

assuming the R_{on} vs breakdown voltage scaling reorted by Baliga *et al.* [85]. Fig.2.10(b) shows a comparison of key material parameters of Si and some commonly cited (ultra)wide-bandgap semiconductors. A low R_{on} and a high breakdown field are desirable for power applications; it is clear from Fig.2.10(a) and Fig.2.10(b) that β-Ga_2O_3 has a clear advantage over GaN and SiC. However, it is necessary to make a quantitative comparison of these semiconductors.

When accessing a semiconductor's suitability for an application space, it is instructive to refer to a figure of merit (FOM). An FOM is a metric defined in terms of the intrinsic properties of a semiconductor that are relevant to a particular application space. The two FOMs most relevant to β-Ga_2O_3 are the Johnson's FOM (JFOM) and the Baliga's FOM (BFOM). The JFOM is concerned with RF applications, and attempts to reflect the trade-off between a desire for a high cut-off frequency f_t and the desire for a high breakdown voltage [86]. The cut-off frequency is given by the expression,

$$f_t = \frac{1}{2\pi T}, \tag{2.16}$$

where T is the time taken for an electron to transited the access region of a device. Fundamentally, this is dependent on the device's dimensions and on the electron velocity. While the velocity-field relationship for an electron is an intrinsic property of the material, the device's dimensions can be optimised to maximise the cut-off frequency. However, scaled down devices operated at the same voltages experience higher fields, and so the breakdown voltage is lowered. The JFOM captures this trade-off with the following expression,

$$JFOM = \frac{E_c v_s}{2\pi}, \tag{2.17}$$

	Si	GaAs	4 H-SiC	GaN	Diamond	β-Ga_2O_3
Bandgap (eV)	1.1	1.4	3.3	3.4	5.5	4.8–4.9
Electron Mobility ($cm^2V^{-1}s^{-1}$)	1400	8000	1000	1200	2000	300
Breakdown Field (MV/cm)	0.3	0.4	2.5	3.3	10	8
Relative Dielectric Constant	11.8	12.9	9.7	9.0	5.5	10
JFOM	1	1.8	278	1089	1110	2844
BFOM	1	15	340	870	24664	3444

Table 2.1: A comparison of the material properties and FOMs of some commonly cited semiconductors. All FOM values are normalised to that of Silicon. Values take from [19] [87].

where E_c is the critical breakdown field of the semiconductor and v_s is the electron saturation velocity. While the JFOM is concerned with high-frequency operation, the BFOM is concerned with low-frequency power devices. The BFOM is a measure of conduction losses in a power device, expressed in terms of fundamental semiconductor properties [88]. It is given by the expression [85],

$$BFOM = \epsilon \mu E_g^3, \tag{2.18}$$

where E_g is the bandgap. Eqn.2.18 follows directly from the fact that the device on-resistance (R_{on}) is proportional to the term $\mu^{-1}E_g^{-3}$ [85]. Table.2.1 compares some key material parameters and FOMs across a range of widely studied semiconductors. Despite its low electron mobility, the wide-bandgap of β-Ga_2O_3 means that it's BFOM and JFOM are far higher than that of GaN and SiC. However, these values are valid only for the bulk materials. The JFOM of GaN is comparable to that of β-Ga_2O_3 in the case of a HEMT, as electron mobilities of >2000 $cm^2V^{-1}s^{-1}$ are achievable in an AlGaN/GaN 2DEG [89]. Self-heating effects will also limit the achievable power densities in β-Ga_2O_3 based RF devices. As such, β-Ga_2O_3 is not predicted to have a large advantage over GaN devices in RF applications. In contrast, the high BFOM of β-Ga_2O_3 demonstrates that β-Ga_2O_3 power devices will have higher current and voltage handling abilities than GaN and SiC based devices. As such, the primary application space of β-Ga_2O_3 is that of high-voltage power electronics (>3kV) [5].

2.2 Device Physics

So far, the intrinsic properties and applications of β-Ga_2O_3 have been discussed. This section will explore different aspects of general device physics, including the formation of contacts, the metal-oxide-semiconductor (MOS) interface, the MOS field effect transistor (MOSFET), and the RESURF effect in Schottky-barrier diodes (SBDs). These concepts will be key to understanding the design and the operation of β-Ga_2O_3 devices.

2.2.1 Metal-semiconductor Contacts

All semiconductor devices rely on the formation of heterointerfaces. When a heterointerface between two materials is formed, a discontinuity in the chemical potential is observed. However, a discontinuous chemical potential is not possible in equilibrium; a redistribution of charge results in an equalisation of the Fermi level across the interface. The fundamental interfaces that are utilised for device design are: the interface between a semiconductor and a metal; the interface between a semiconductor and an oxide; and the interface between an oxide and a metal. The metal-semiconductor interface is most commonly used in the formation of contacts, of which there are two types: ohmic and Schottky. The relative positions of the metal workfunction (ϕ_G) and the semiconductor's electron affinity (χ_e) determines which of these contacts is formed. If χ_e>ϕ_G, (as shown in Fig.2.11(a)), electrons are transfered from the metal into the semiconductor, leading to a downward band bending at the interface, (see Fig.2.11(b)). The absence of an energy barrier at the interface means that this contact is ohmic.
If χ_e<ϕ_G, (Fig.2.11(c)), charge redistribution leads to the upwards band bending at the interface, and the formation of a Schottky barrier (SB), with a barrier height (ϕ_B) of $\chi_e - \phi_e$, as shown in Fig.2.11(d). Electrons in the vicinity of the upwards band bending will migrate into the bulk of the semiconductor, forming a depletion region. This depletion region has a depletion width of W_D, which is given to first order by the expression [52],

$$W_D = \sqrt{\frac{2\epsilon_s(V_{bi} - V)}{qN_D}}, \tag{2.19}$$

where V is the voltage bias applied to the metal, N_D is the donor concentration in the semiconductor and V_{bi} is the built-in potential of the junction. This energy barrier acts as a diode, with current flow blocked when reverse biasing the metal with a negative potential. Reverse biasing also leads to an increase in the depletion width, as can be seen from Eqn.2.19. Forward biasing the barrier, with a positive bias on the metal, leads to an electron current flow over the barrier. The magnitude of this current (I) is given by the diode equation,

$$I = I_s\left(exp\left(\frac{V - IR_s}{\eta V_{therm}}\right) - 1\right), \tag{2.20}$$

where I_s is the saturation current in reverse bias, R_s is the resistance of the bulk semiconductor, V_{therm} is the thermal voltage and η is the ideality factor. The term $V - IR_s$ is the effective voltage drop over the barrier, and the ideality factor represents how closely a diode follows ideal behaviour. For an ideal diffusion current across the junction the ideality factor takes a value of η = 1. If a recombination current dominates the ideality factor takes a value of η = 2. When these two currents are comparable the ideality factor has a value of 1 s< η < 2 [52].

2.2.2 The MOS-capacitor

The metal-oxide and oxide-semiconductor interfaces are both found in a metal-oxide-semiconductor (MOS) junction. Fig.2.12(a) shows the band diagram of a MOS junction at zero bias. The key

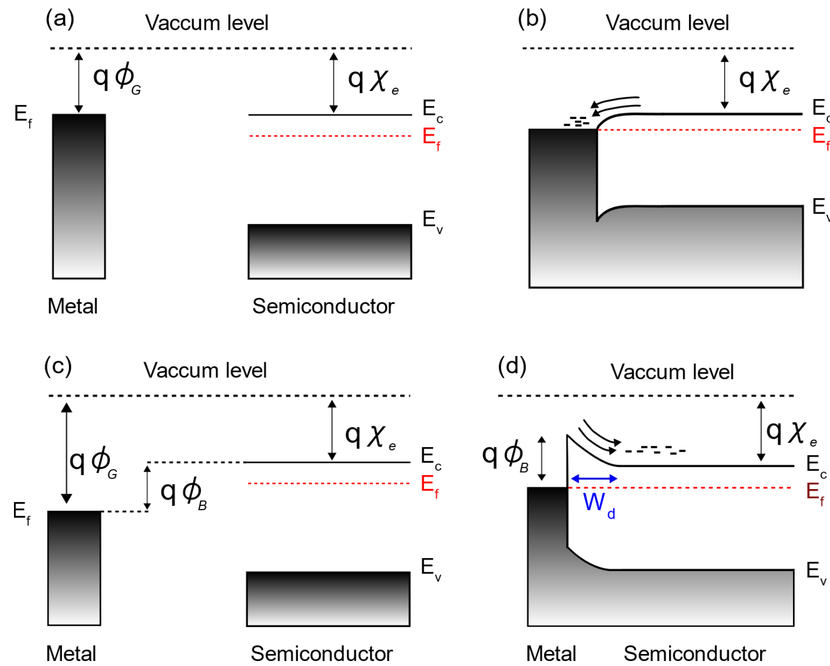


Figure 2.11: Band diagrams demonstrating the formation of ohmic and Schottky contacts. The electron affinity of the semiconductor (χ_e) and the workfunction of the metal (ϕ_G) determines the type of contact formed. (a) Bands for a separated semiconductor and metal where $\chi_e > \phi_G$. (b) An ohmic contact is formed, with a negligible energy barrier. (c) Bands for a separated semiconductor and metal where $\chi_e < \phi_G$. (d) A Schottky contact is formed, with a barrier height of $\phi_B) = \chi_e - \phi_G$.

difference between the MOS structure and a direct metal-semiconductor contact is that there is no charge transfer between the semiconductor and the metal (due to the insulating oxide), with the mismatch in the chemical potentials manifesting as a voltage drop over the oxide layer. Assuming an ideal MOS structure, in which there is no charge inside of the oxide layer, Poisson's equation yields an expression for the spatial variation of the electric potential (ϕ) of $\nabla^2\phi = 0$, implying a linear variation in ϕ over the oxide. This potential drop over the oxide is equal to the difference between the metal's and the semiconductor's work functions. Applying a negative bias to the metal will leads to a negative voltage over the oxide, and a corresponding negative potential at the oxide-semiconductor interface. This leads directly to the formation of a depletion region, as shown in Fig.2.12(b). Fig.2.12(c) shows the effect of a positive bias on the metal, with downward bending of the conduction band leading to the formation of an accumulation region at the oxide-semiconductor interface.

The MOS structure is a capacitor, with the oxide layer acting as a dielectric. The MOS capacitor (MOS-CAP) is a fundamental component of the MOS field-effect transistors (MOSFET). The relevant capacitances present in an n-type MOS-CAP are shown in Fig.2.13(a) and Fig.2.13(b). In the case of Fig.2.13(a), there is no depletion region, and so the capacitance of the conducting

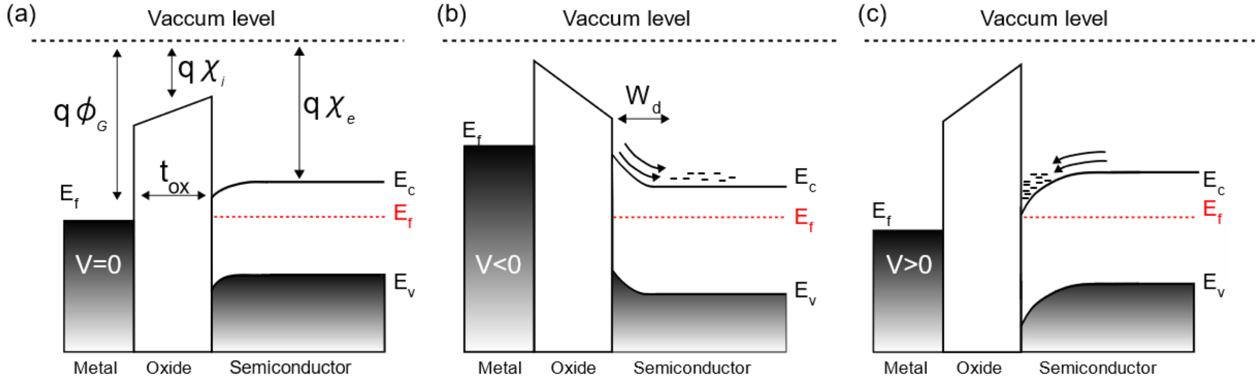


Figure 2.12: (a) A metal-oxide-semiconductor junction in the 0V condition. (b) A negative bias on the metal bends the bands at the interface upwards, creating a depletion region with width W_d. (c) A positive bias on the metal bends the bands at the interface downwards, leading to an accumulation of electrons at the interface.

n-type bulk semiconductor can be disregarded; it is only necessary to consider the capacitance of the oxide. The capacitance of the MOS-CAP (C_{MOS}) will be given by the expression for a parallel plate capacitor,

$$C_{MOS} = C_{ox} = A_{ox}\frac{\epsilon_{ox}}{t_{ox}}, \tag{2.21}$$

where A_{ox} and t_{ox} are the area and thickness of the oxide layer respectively, and C_{ox} is the capacitance of the oxide layer.

In the depletion regime, (Fig.2.13(b)), the region below the contact metal is depleted, and there will be a depletion region capacitance in series with the oxide capacitance. The capacitance over the depletion region is given by the expression,

$$C_D = A_{ox}\frac{\epsilon_{semi}}{W_d}, \tag{2.22}$$

where W_d is the depletion width. The total capacitance of the MOS structure in the depletion regime is,

$$C_{MOS} = \frac{C_{ox}C_D}{C_{ox}+C_D}. \tag{2.23}$$

When the anode bias is sufficiently negative, the MOS enters the inversion regime. In this regime, the concentration of minority carriers, i.e. holes, increases at the metal-semiconductor interface. This happens as the electric field is sufficiently high to separate spontaneously generated hole-electron pairs before recombination occurs. The holes at the interface have the effect of screening any subsequent negative changes in the gate voltage. The depletion region width is now fixed, with its capacitance (C_{Dmin}) given by the expression,

$$C_{Dmin} = A_{ox}\frac{\epsilon_{semi}}{x_{dmax}}. \tag{2.24}$$

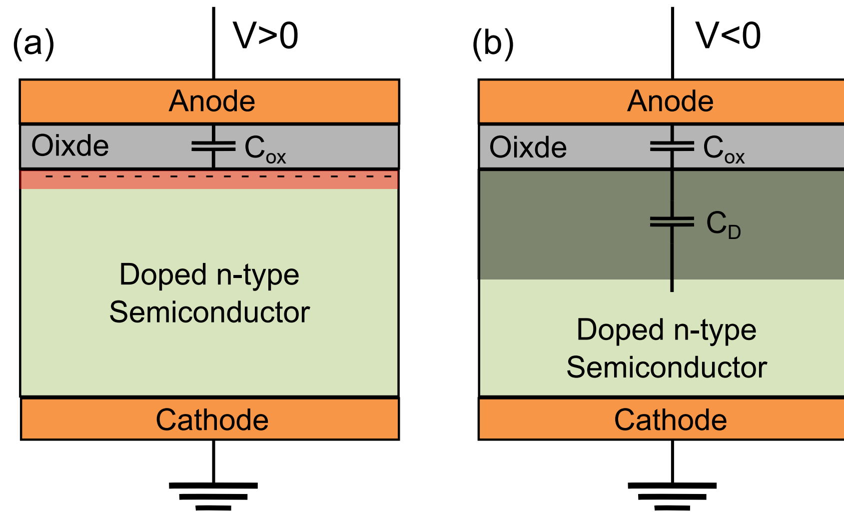


Figure 2.13: Relevant capacitances in a MOS-CAP when the structure is biased into (a) the accumulation regime and (b) the depletion regime.

In the inversion regime the capacitance of the MOS is found by substituting C_D in Eqn.2.23 for C_{Dmin} in Eqn.2.24,

$$C_{MOS} = \frac{C_{ox}C_{Dmin}}{C_{ox} + C_{Dmin}}. \tag{2.25}$$

It is possible to express the maximum depletion width (W_{dmax}) in terms of the donor concentration (N_D) in the bulk semiconductor,

$$W_{dmax} = \sqrt{\frac{4\epsilon_{semi}}{qN_D}|\phi_f|}, \tag{2.26}$$

where ϕ_f is given by the expression,

$$\phi_f = \frac{KT}{q} ln\left(\frac{N_D}{n_i}\right), \tag{2.27}$$

where n_i is the intrinsic carrier concentration of the semiconductor.

2.2.3 MOSFETs

MOSFETs are solid state devices which belong to the family of the field effect transistors (FETs). FETs are named as such as their conductivity is modulated using an electric field. A simplified schematic of an n-type MOSFET is shown in Fig.2.14. These devices have three terminals: drain, source, and gate. Drain and source are ohmic contacts, connected to a bulk conducting semiconducting channel. The gate is a MOS-CAP structure situated above the conducting channel. Two input voltages, the gate-source voltage (V_{GS}) and the drain-source voltage (V_{DS}), modulate the source to drain current of the MOSFET (I_D).

Fig.2.15(a) shows the typical I_D-V_{GS} characteristics of a normally-on MOSFET. For an n-type MOSFET, the channel is in the on-state when V_{GS} = 0V, meaning that the channel is conducting.

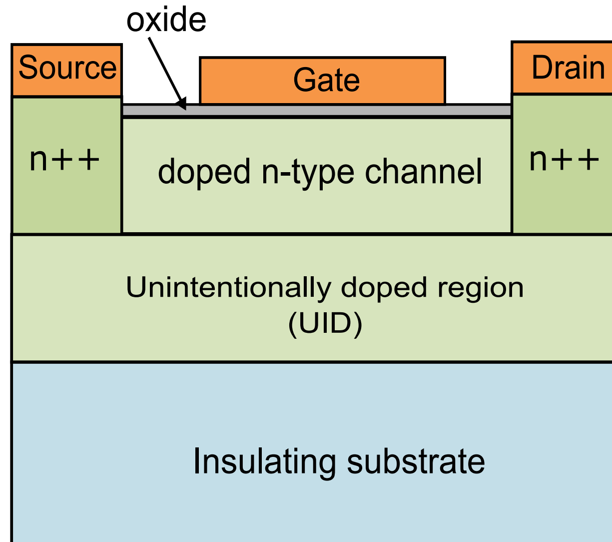


Figure 2.14: A simplified schematic of an n-type MOSFET. Current flows between the source and drain contacts via a doped channel. The channel conductivity is modulated by applying a voltage to the gate contact, separated from the channel by a thin oxide layer.

Varying V_{GS} will transition the region under the gate from the accumulation regime, through depletion regime and into the inversion regime. By modifying the concentration of carriers under the gate, the conductance of the channel between the drain and the source is modulated. As the gate voltage is swept between the depletion and accumulation regions, the device transitions into the sub-threshold region. The channel is still conducting, but small changes in the gate voltage modifies the drain current by orders of magnitude. The gradient of the current with respect to the gate voltage is known as the subthreshold slope S_{th}. The gradient of this slope in an ideal transistor is given by the expression [52],

$$S_{th} = ln(10)\frac{kT}{q}\left(1 + \frac{C_D}{C_{ox}}\right). \tag{2.28}$$

In the limit of an infinitely thin oxide, Eqn.2.28 is only dependent on temperature, with an ideal value of 60 mV/decade at room temperature. Additional capacitance terms are required when there is fixed charge in the oxide or interface traps in the semiconductor, leading to an increase in the value of S_{th}. It is desirable to minimise this value as ideally transistors would act as perfect switches, with a step-like change in I_D, (between the on-state and off-state), at the threshold voltage.

The device is said to be in the off-state when the channel is non-conducting. This occurs when the depletion region under the gate contact reaches the insulating substrate below the channel, effectively cutting off the channel, as seen in Fig.2.15(b). The voltage at which the device transitions from the off-state to the sub-threshold region is the threshold voltage (V_{th}).

The gain of a MOSFET can be defined as the change in I_D induced by a change V_{GS}. It is clear

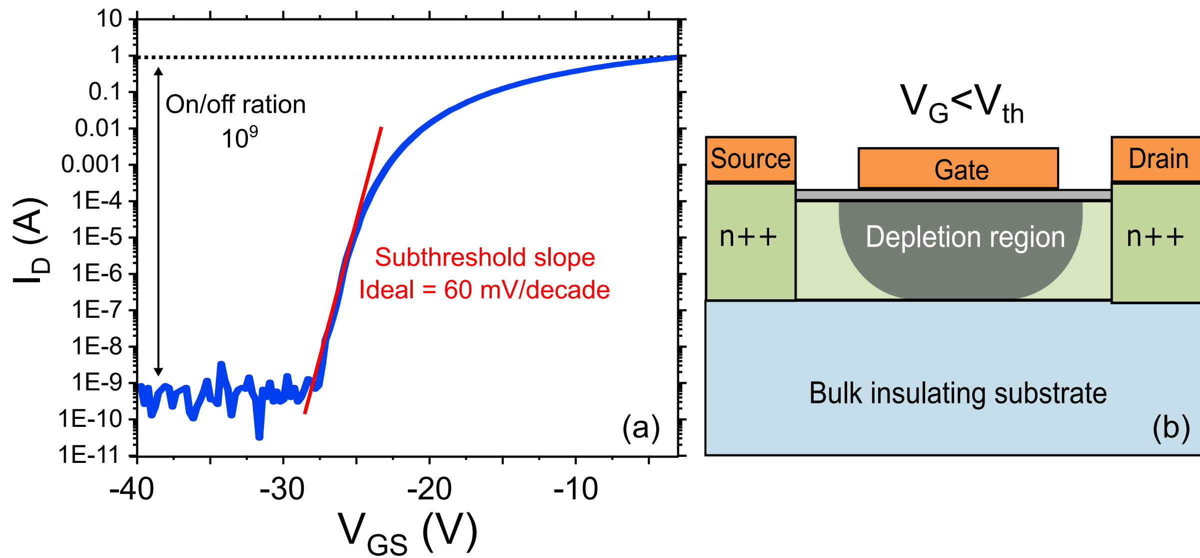


Figure 2.15: (a) An example of a I_D-V_{GS} curve for a normally-on MOSFET. A reduction in the gate voltage sweeps the device from accumulation, to the sub-threshold region, and into depletion. The ideal sub-threshold slope has a gradient of 60 mV/decade.(b) A device in the off-state. The depletion region across the channel retricts current flow in the channel.

from Fig.2.15(a) that the gain of a device will vary significantly as the device transitions from the on-state into the off-state. The transconductance of a device (g_m) is a commonly cited metric of device gain, given by the expression,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{2.29}$$

While V_{GS} modifies the channel conductivity, V_{DS} modifies the output current of the device. Fig.2.16 shows the typical I_D-V_{DS} characteristics of a MOSFET. Three distinct regimes can be identified:

Cut-off region In this region the MOSFET is in the off-state; the gate voltage is less than the threshold voltage. The I_D in this regime consists of leakage currents between the source, gate and drain.

Linear region In the linear region, the channel is conducting, with the channel acting as an ohmic resistor for a fixed V_{GS}. The channel on-resistance (R_{on}) limits the slope of the I_D-V_{DS} characteristic in this region.

Saturation region In this region the drain current is independent of applied drain voltage. The saturation region in a MOSFET occurs when the condition V_{DS} > V_{GS} - V_{th}.

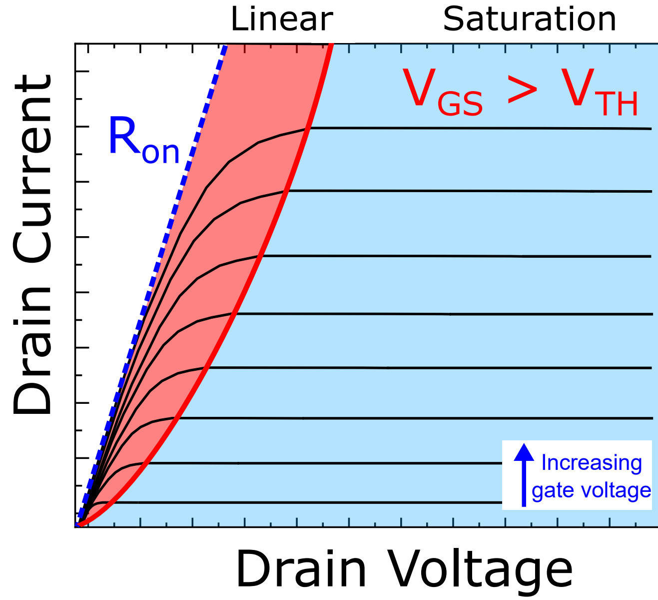


Figure 2.16: Typical I_D-V_{DS} characteristic of a MOSFET.

The current in the linear regime through a device with width W and gate length L_G is given by the expression [90],

$$I_D = \frac{\mu W C_G}{L_G}\left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2}\right] V_{DS} \tag{2.30}$$

where W is gate width, C_G is the gate capacitance. Eq.2.30 can be simplified to the form [91],

$$I_D = \frac{\mu W n_i q}{L_G} V_{DS} \tag{2.31}$$

where $(V_{GS} - V_{th}) >> V_{DS}$. In the saturation regime, Eqn.2.30 reduces to,

$$I_D = \frac{\mu W C_G}{L_G}(V_{GS} - V_{th})^2. \tag{2.32}$$

The behaviour of the device in the saturation region can be explained by the formation of depletion regions. Fig.2.17(a) shows a device where $V_{DS} < V_{GS} - V_{th}$. No depletion regions are present, and the channel should act like an ohmic resistor. A variation in the channel thickness is observed, as the local gate-channel voltage will vary laterally across the channel due to the applied drain bias. Fig.2.17(b) shows the MOSFET with a drain voltage that satisfies the condition $V_D > V_{GS} - V_{th}$. The channel is conducting in the regions where the local gate-channel bias is $>V_{th}$, with the channel voltage increasing closer to the drain. When $V_D > V_{GS} - V_{th}$, the local gate-channel voltage close to the drain contact is $<V_{th}$, and a depletion region is formed. Carriers that enter this region are swept through by the depletion electric field, into the drain contact. As the drain voltage increases, the width of this region increases. The increase in depletion width scales with the increase in drain voltage, fixing the electric field (and the current) across the pinch-off region.

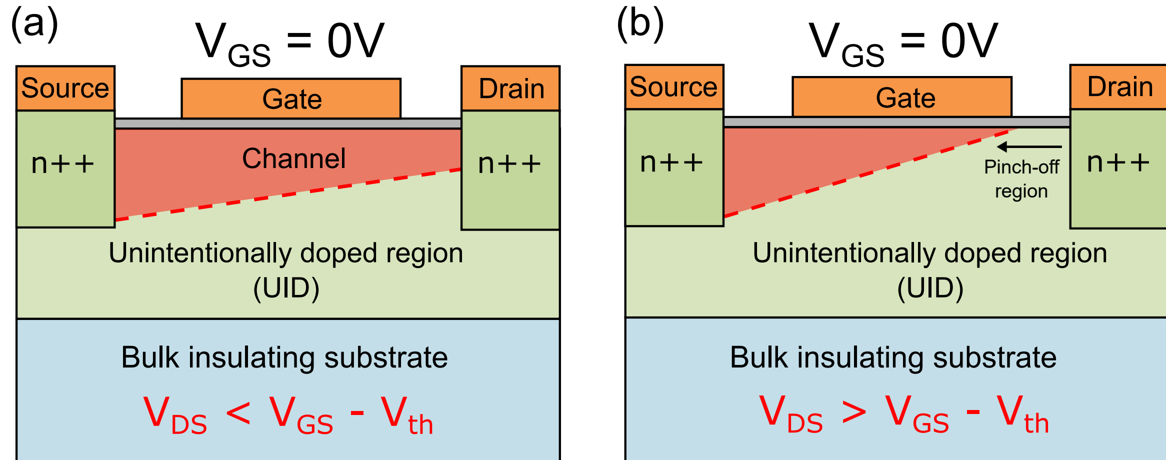


Figure 2.17: (a) For V_{DS} < V_{GS} - V_{th}, a conducting channel is present between the source and the gate contacts. (b) For V_{DS} > V_{GS} - V_{th}, the channel is pinched off, with a small depletion region close to the drain contact. The size of this region increases with increasing drain bias.

2.2.4 Schottky-barrier Diode Devices

The high breakdown field of β-Ga_2O_3 means that it is particularly suited to the fabrication of Schottky-barrier diode (SBD) for power applications. SBDs suffer from no minority carrier storage effects and do not rely on recombination effects when switching between reverse and forward bias. They also have relatively thin drift layers, leading to a lower parasitic capacitance [92]. These two factors allow for a higher switching speed than equivalent pn junction based devices. Coupled with their low turn-on voltage (and the associated lower power losses), SBDs are valuable for lower-frequency power switching applications. However, SBDs generally have higher leakage currents and lower breakdown voltages than pn diodes. β-Ga_2O_3 SBD devices have the potential to mitigate both of these problems, through intrinsically high voltage handling abilities, and through the application of novel device designs.
The layout and the current-voltage characteristics of a typical vertical SBD diode is shown in Fig.2.18. The anode forms a SB with the underlying gallium oxide substrate. The low doping density region in contact with the anode maximises the barrier height, while the highly doped bulk of the substrate reduces R_{on}. The forward bias characteristics are described by Eqn.2.20, and the reverse bias currents are dominated by leakage current across the interface. The leakage current increases with increasing voltage in reverse bias, with a breakdown of the SB interface characterised by a sharp increase in the leakage current at V_{br}. Fig.2.19 shows the three principle leakage mechanisms in a Schottky-barrier diode: thermionic emission (TE), thermionic-field emission (TFE) and field emission (FE). TE is the emission of electrons via thermal agitation, while FE is the field assisted tunneling of an electron through the barrier. TFE is a combination of these two mechanisms. The current density of thermionic emission J_{TE} is exponentially depen-

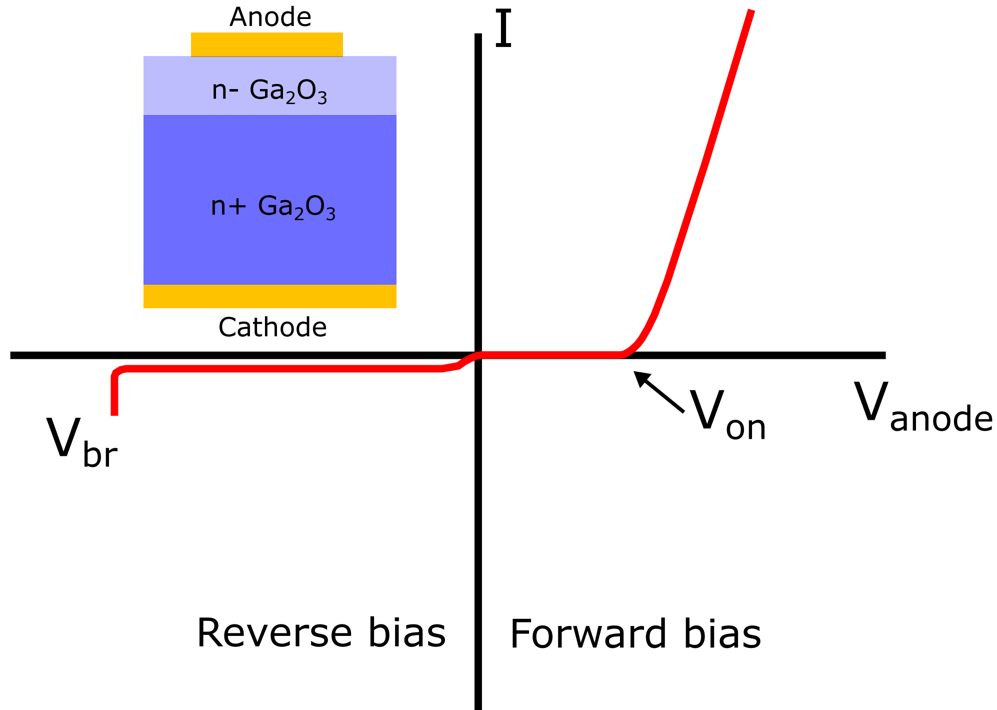


Figure 2.18: Schematic of a typical vertical SBD and its IV characteristic.

dent on the temperature of the device, with the second exponential term accounting for barrier lowering in the device by the diffusion of charge [52]. In contrast, the temperature dependence of J_{TFE} is far weaker, with the current density being strongly dependant on the applied voltage at the interface. The relative impact of J_{TE} and J_{TFE} on the total leakage current dependents on the temperature range considered and on the value of the parameter E_{00}. Padovani *et al.* have previously discussed this in detail, in the case of both GaAs and Si SBDs [93]. FE is strongly dependent on the barrier height and the applied voltage. As the barrier height is fixed by the doping and the anode metal for a given SBD, (typical values lie between 1-1.35 eV [94]), the choice of applied bias determines the magnitude the tunneling current J_{FE}. Li *et al.* reported on the relative importance of these leakage mechanisms in the case of β-Ga_2O_3. The current densities of thermionic emission and barrier tunneling (thermionic field emission and field emission) were calculated, with thermionic emission dominating leakage in the low-field regime and barrier tunneling in the high-field regime. Fig.2.20(a) shows the transition field for the two mechanisms as a function of doping. At 300K, barrier tunneling dominates leakage for fields >0.25 MV/cm, with the transition field value being insensitive to doping. The dependence of the transition field on temperature is shown in Fig.2.20(b), with higher temperatures increasing the relative contribution of thermionic emission relative to barrier tunneling.

The breakdown voltage of planar SBDs can be enhanced by reducing field crowding at the corners of the anodes, through the use of anode field-plates [31][32]. However, field-plates can

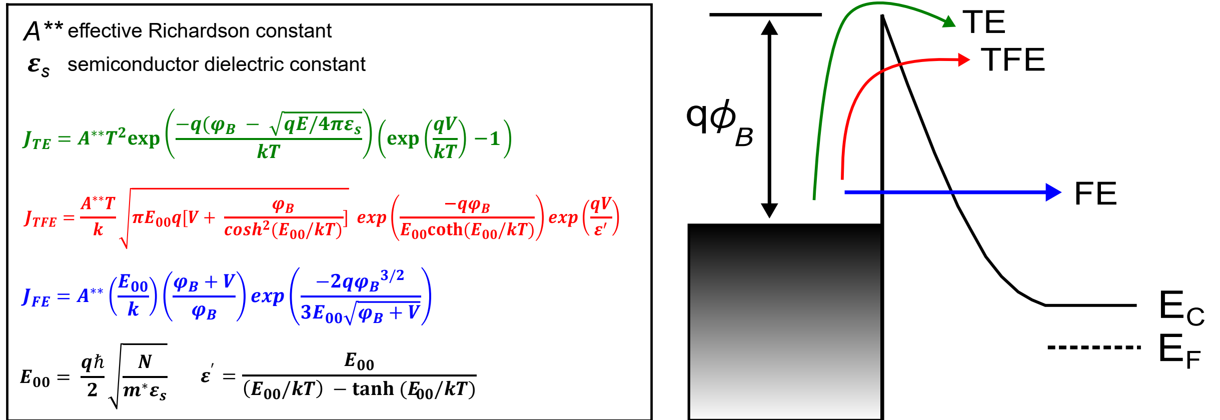


Figure 2.19: The reverse bias leakage mechanisms for a Schottky-barrier. Expressions for the current densities are taken from [95].

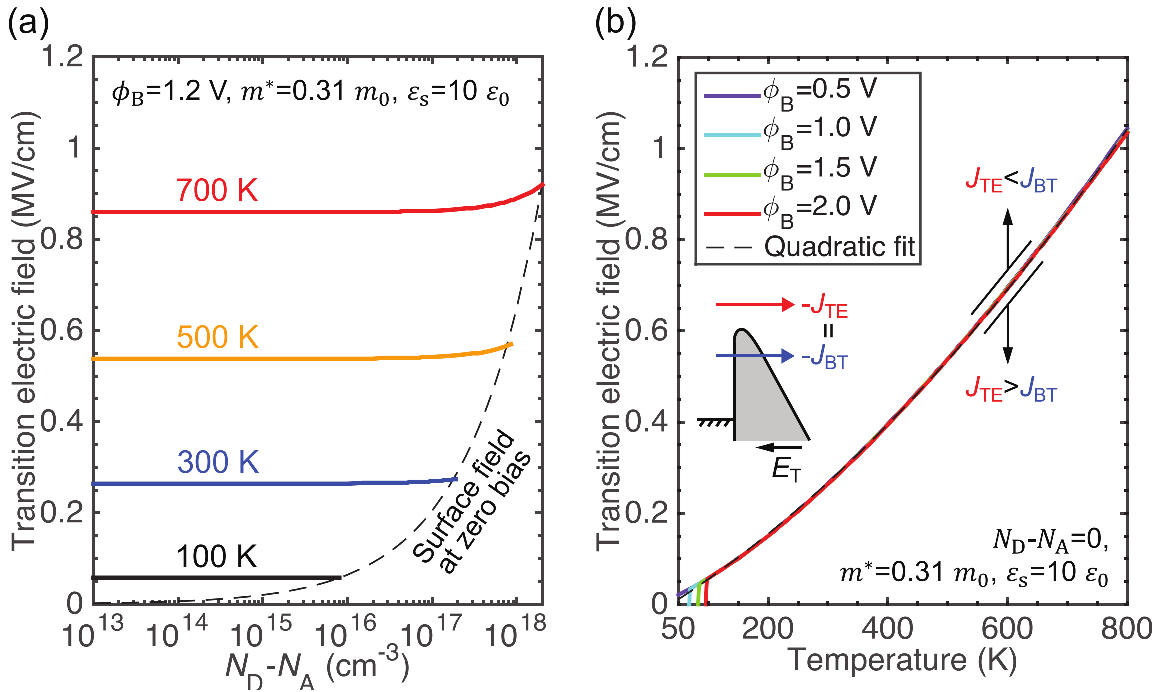


Figure 2.20: The transition field between the two dominant leakage mechanisms in a reverse biased β-Ga_2O_3 SB. In the low-field regime, leakage is dominated by thermionic emission and, in the high field regime, by barrier tunneling. The transition field is shown as a function of (a) doping and (b) temperature. Figure reproduced from [96].

only improve breakdown voltages so far, as the breakdown voltage of the planar SBD structure is intrinsically limited by the surface field at the anode-semiconductor interface. Fig.2.21(a) shows the maximum surface field that can be sustained in β-Ga_2O_3 SBDs as a function of SB height. The same trend is observed across both fixed current densities and temperatures; for barrier heights >1eV, an approximately linear increase in breakdown field with barrier heights is expected. Barrier heights as high as 2.4eV have been reported for oxidised metal contacts on (010) orientated crystals [97]. However, further increases in breakdown voltage will be limited by the breakdown field of β-Ga_2O_3 (8 MV/cm), and other strategies are required to enhance the voltage rating SBDs.
Fig.2.21(b) shows the field profile of a planar SBD under reverse bias. The surface field corresponds to the maximum field observed in the device, with a linear decrease across the drift region. Device failure will be observed over the SB interface, as the SB breakdown field is lower than that of the bulk β-Ga_2O_3. Aside from changing the anode composition, enhanced breakdown voltages can be achieved by exploiting reduced surface field (RESURF) effects. The RESURF effect has been successfully demonstrated in the trench-MOS SBD architecture, as shown in Fig.2.21(b). This structure, first reported by Hu *et al.* [26], consists of a repeating series of trenches and fins, with the anode deposited along the top of the fins, the fin sidewalls, and the trench bottoms. The top of each fin consists of a SB formed at the direct anode/β-Ga_2O_3 interface. The semiconductor is isolated from the anode at the sidewalls and trench bottoms by a dielectric oxide layer. In reverse bias, the anode depletes the fin from the sidewall as well as the SB interface. This has the effect of reducing the surface field, as the potential drop over between any point in the fin and the barrier is reduced. The position of the electric field peak is shifted from the SB interface into the trench-bottom oxide corners, (as shown in Fig.2.21(b)). The RESURF factor (R) can be used to quantify the degree to which the surface field is reduced by the RESURF effect, with R defined as the ratio of the maximum field in the SBD to the surface field (see Fig.2.21(c)). R is related to the R_{on} of a diode by the expression [98],

$$R_{on} = \frac{4V_{br}^2}{\epsilon\mu R^3 E_{surf}^3}, \tag{2.33}$$

where E_{surf} is the surface field at the anode/β-Ga_2O_3 interface. From Eqn.2.33, it is clear that increasing the RESURF factor does not only enhance the breakdown voltage of a SBD, but also decreases R_{on}. Li *et al.* reported trench-MOS diodes that successfully implement the RESURF effect, achieving breakdown voltages of 2.44kV, compared with <1kV for planar SBDs fabricated using the same processing conditions [33]. Breakdown voltages as high as 2.89 kV have since been reported [99].

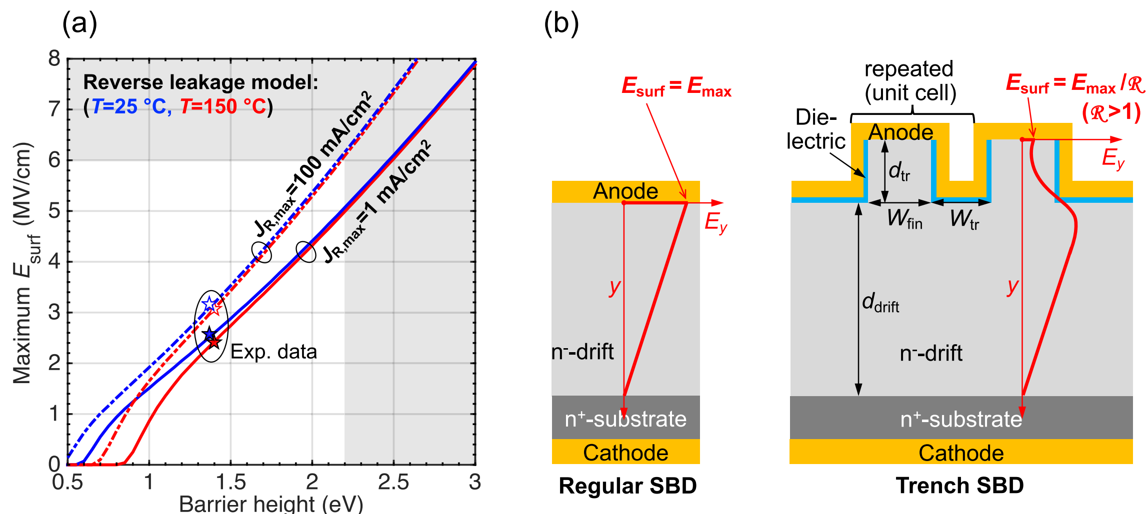


Figure 2.21: (a) The breakdown surface field for a SB interface as a function of barrier height, for two different current densities. Figure reproduced from [100]. (b) A schematic demonstrating the principle of the reduced surface field (RESURF) effect. The maximum field is located at the SB interface for a planar SBD, but is shifted into the oxide corners in a trench-MOS SBD. The reduced surface field enhances the breakdown voltage of the diode [98].

2.3 Growth and Fabrication of β-Ga_2O_3 Devices

This section will discuss key aspects of β-Ga_2O_3 growth and device fabrication. Substrate and channel growth techniques used in the fabrication of the devices investigated in subsequent chapters are discussed, along with the n-type and p-type dopants used to achieve the desired electrical properties of these layers. Strategies for fabricating ohmic and Schottky contact metal stacks are then presented, along with the deposition of gate dielectrics and surface passivisation.

2.3.0.1 Intrinsic and Intentional Doping

The unintentional incorporation of dopants is unavoidable during the growth of device substrates and channels. Crystals with such dopants are referred to as unintentionally doped (UID). Unintentional doping in β-Ga_2O_3 has been observed to be intrinsically n-type. Many impurities could be responsible for this behaviour, with the most likely candidates being precursor elements used in crystal growth, organic contaminates in the growth system, and structural defects such as oxygen vacancies. Varley *et al.* used density functional theory to access the stability of different impurities in the β-Ga_2O_3 crystal [101]. The energy of formation as a function of Fermi energy can be used to access the relative stability of impurities and their relative charge states as a function of the Fermi level position [102]. The energy of formation E^f of an impurity i is given by the expression [101],

$$E^f(i) = E^{tot}(i) - E^{tot}(Ga_2O_3) + \mu_0 + qE_f, \tag{2.34}$$

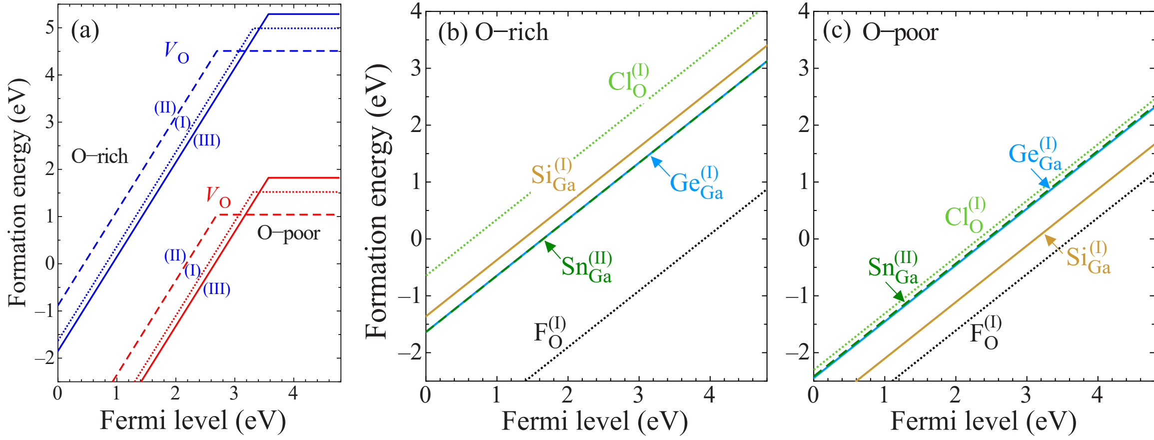


Figure 2.22: The formation energies of (a) oxygen based defects in β-Ga$_2$O$_3$, and shallow donors in (b) oxygen rich and (c) oxygen poor conditions. The zero energy of the Fermi level corresponds to the valence band edge. Figure reproduced from [101].

where $E^{tot}(i)$ is the energy of the crystal containing an impurity, $E^{tot}(Ga_2O_3)$ is the energy of the crystal without an impurity and μ_0 is the chemical potential. μ_0 is impacted by the growth conditions of the crystal e.g. oxygen rich and oxygen poor growth conditions. Fig.2.22(a) shows the energy of formation for an oxygen vacancy in both oxygen and oxygen poor conditions. In both cases, the formation energy exhibits a change in gradient at approximately 1eV below the conduction band edge. This change in gradient is associated with a change in charge state of the vacancy, suggesting that the vacancy acts as a deep donor [102]. As such, it cannot be responsible for the conductivity of UID β-Ga$_2$O$_3$. In contrast, the formation energies of the defects in Fig.2.22(b) and Fig.2.22(c) exhibit no change in gradient as a function of Fermi energy. Therefore, of these impurities act as shallow donors, and therefore can contribute to the conductivity of UID β-Ga$_2$O$_3$. A florine atom on the O(I) site is the most stable of these impurities for both growth conditions.

Intentional doping of β-Ga$_2$O$_3$ is a prerequisite of any device fabrication. Both n-type and p-type doping has been reported in β-Ga$_2$O$_3$: n-type to achieve controllable conductivity of device channels and p-type for electron compensation and the formation of insulating substrates. N-type doping is achievable with any group IV elements, which act as shallow donors [30]. Si, Sn and Ge are the most commonly used shallow donors [103][104], with reported conduction band offsets of 16-50 meV, 7.4–60 meV and 17.5 meV, respectively. Doping with Nb, while less common, has also been reported, with a measured conduction band offset of 30–150 meV [105]. N-type doping with Ta has also been reported [106]. Donor elements are required to not only exhibit shallow conduction band offsets, but are also required to incorporate onto donor sites over a wide range of doping densities. It is also desirable for the donor elements not to exhibit large compensation effects at higher densities, as this will limit the mobility and conductivity of a device channel. Fig.2.23(a) shows the concentration of carriers, extracted using Hall measurements, as a function

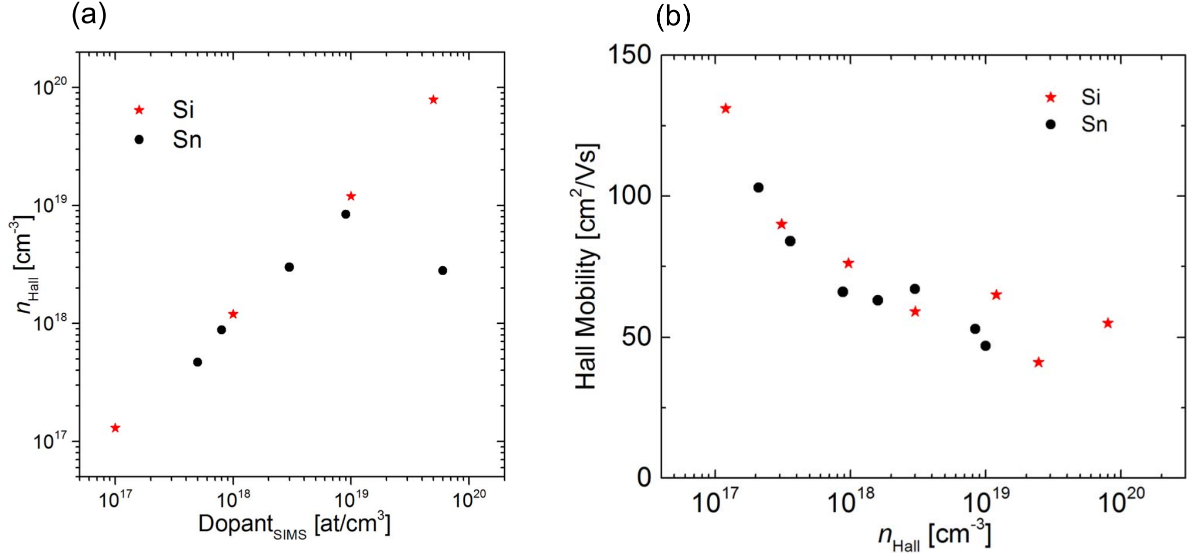


Figure 2.23: (a) Free electron concentration as a function of donor density in both Si and Sn doped β-Ga_2O_3 (001) orientated crystals. (b) Hall mobility of Si and Sn doped crystals as a function of donor density. Figure reproduced from [107].

of both Si and Sn donor density, extracted using SIMS in (001) β-Ga_2O_3 substrates [107]. For donor densities $<10^{19}$ cm^{-3}, both elements exhibit a linear increase in carrier concentration with dopant concentration, indicating minimal compensation effects and good activation of the donors. For donor densities $>10^{19}$ cm^{-3}, Sn exhibits a saturated carrier concentration, indicating some degree of compensation. This will have the effect of degrading the channel mobility, and so means that Sn is not suitable for doping devices that require higher carrier concentrations. Fig.2.23(b) shows the corresponding Hall mobilities as a function of carrier concentration. Both Si and Sn exhibit approximately the same behaviour, with the drop in mobility at higher carrier concentration attributed to an increase in ionised impurity scattering.

P-type doping is primarily used for the purpose of compensating background donors in UID in β-Ga_2O_3. A sufficiently high density of deep-level acceptors have the effect of pinning the Fermi level at the acceptor energy level, suppressing n-type conductivity in the crystal [112]. Therefore, deep-level acceptors are often used to achieve insulting β-Ga_2O_3 substrates. The formation energies of a number of acceptors are shown in Fig.2.24(a). Formation energies are given for both gallium rich and oxygen rich growth conditions. It is predicted that N substitution on the O(II) site and Mg substitution on the Ga(II) site have particularly low formation energies. The position in the bandgap of the most commonly used deep-level acceptors are shown in Fig.2.24(b). Although the formation energy of iron was not included in Fig.2.24(a), it also acts as an acceptor, with an energy level close to the conduction band edge [110]. The range of possible energies for the N and Mg dopants reflects the fact that both can occupy different lattice sites [55][111].

As well as compensating unintentional donors, both Mg and N are used in the formation pn

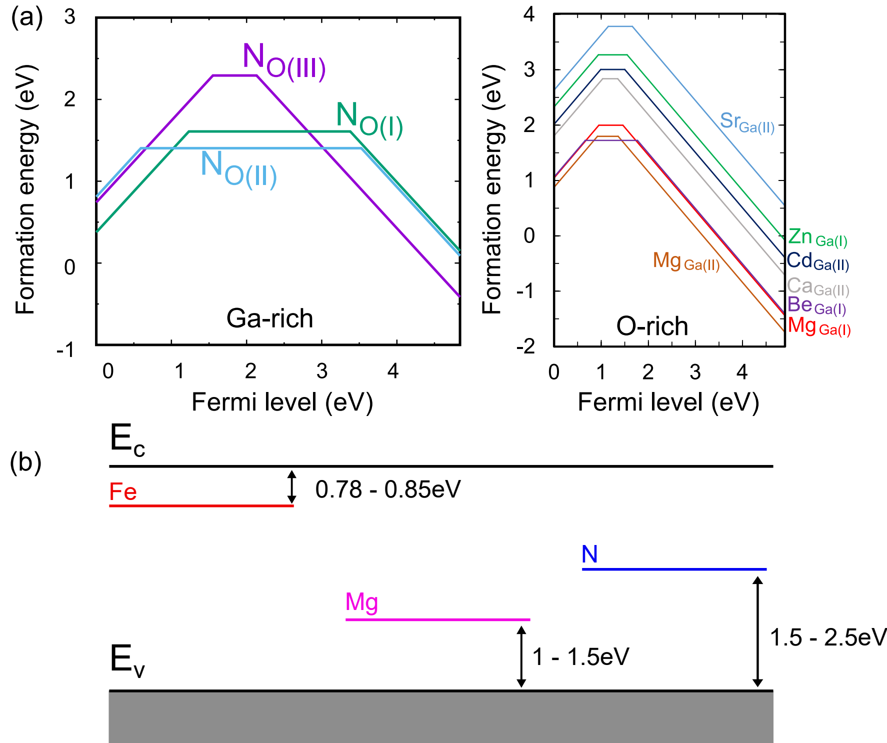


Figure 2.24: (a) The formation energies of different acceptor impurities in both Ga-rich and O-rich growth conditions. Figure reproduced from [108]. (b) The position in the bandgap of some deep-acceptors commonly used to achieve an insulating substrate. Values of the conduction band offset for Fe are reported separately for the same energy level [109][110]. Energy ranges for Mg and N cover a range of possible dopant sites [55][111].

junctions in devices. These junctions exhibit an insignificant hole mobility, but their build-in fields are used as energy barriers for the formation of charge blocking layers. Vertical MOSFETs that exploit the charge blocking action of the pn junction have been reported previously by Wong *et al.* [27][29]. N is the preferred dopant, as it is predicted, and has been demonstrated, that Mg ions diffuse at temperatures as low as 700°C in β-Ga$_2$O$_3$ [108][28]. Annealing temperatures used during the fabrication of devices often exceed this level, leading to the migration of Mg ions from the substrate into the channel, degrading its conductivity.

2.3.0.2 Substrate Growth

One of the key attractions of β-Ga$_2$O$_3$ is the melt growth of large-area crystals [113]. Native substrates are desirable in semiconductor devices, as they eliminate the need for heterointerfaces in the device stack (a potential source of defects and trapping states). Melt growth techniques typically have high-growth rates, scalability, and are inexpensive once optimised. The high melt temperatures used during growth means that melt techniques are only suitable for the

thermodynamically stable β-phase. Techniques such as the Czochralski method, float zone growth and vertical Bridgman growth have all been reported in β-Ga_2O_3 [114]. Since it was first reported by Tomm *et al.*, Czochralski growth has become the most common growth technique for β-Ga_2O_3 substrates [115]. In this process, a rotating crystal is pulled out of a melt contained within a metal crucible. By optimising the rate of rotation, the rate at which the crystal is withdrawn from the melt and the growth atmosphere, high quality single crystals can be produced [116]. Fig.2.25 shows three β-Ga_2O_3 crystals grown using the Czochralski method. The crystal grown along the [010] direction exhibits high crystal quality, with no obvious deformities and an approximately constant radius along its entire length, whereas crystals grown off the [010] direction exhibit lower crystal quality. A preference for growth along the [010] direction leads to the lower crystal quality for other growth directions, through the formation of twin planes in the crystal[117]. As such, the [010] direction is favoured for the growth of β-Ga_2O_3 substrates.

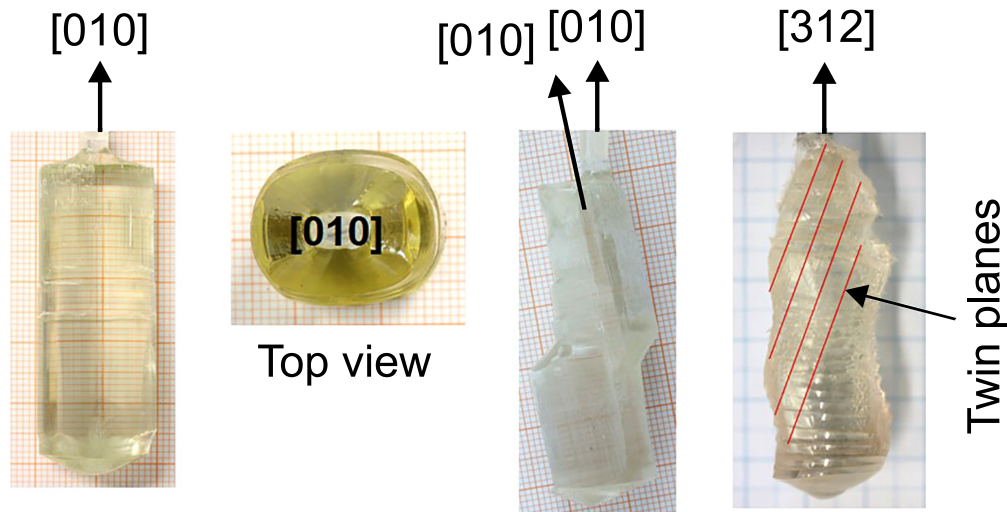


Figure 2.25: β-Ga_2O_3 crystals grown using the Czochralski method along different crystalline directions. Highest quality growth is observed down the [010] direction. Figure reproduced from [117].

2.3.0.3 UID layer and Channel Growth

The availability of melt-grown crystals allows for direct growth of β-Ga_2O_3 layers on the substrate. Two distinct layers of β-Ga_2O_3 are required in a typical lateral device, a UID layer and the doped channel layer. In lateral MOSFETs, an unintentionally-doped (UID) layer of β-Ga_2O_3 is usually grown on the substrate, and then the channel is formed by doping the topmost section of this layer. The UID layer primarily acts as an insulating layer to confine charge to the channel. It has also been reported to have reduced the problem of deep-acceptor diffusion into the channel, with Fe diffusion into the channel during thermal annealing having previously been observed in β-Ga_2O_3

MOSFETs [118][119]. Low background impurity concentrations are required in the UID layer to achieve higher electron mobilities and to suppress trapping/compensation effects in the channel. A range of epitaxial growth techniques have been investigated in the literature for β-Ga_2O_3, including: pulsed laser deposition (PLD), molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), halide vapour phase epitaxy (HVPE), chemical vapor deposition (CVD) and atomic layer deposition (ALD) [120]. MOCVD, MBE and HVPE are the most widely used of these techniques.

- **Molecular beam epitaxy:** MBE is an ultra-high vacuum growth technique in which effusion cells are used to create molecular beams, directed towards a target growth substrate [121]. These beams consist of the constituent elements of the desired growth film [122]. The kinetic energy of the atoms incident on the substrate surface, combined with the thermal energy provided by the heating of the growth substrate, allows for the migration of atoms across the surface of the substrate. Growth of a desired crystal is achieved when the atoms on the surface redistribute to adopt the most thermodynamically stable configuration [123]. MBE growth of β-Ga_2O_3 uses a gallium effusion cell, with the gallium atoms oxidised using either ozone or an oxygen plasma. Film growth is strongly dependent on the Ga/O ratio, and on growth substrate orientation. The highest growth rates are observed for (310) and (010) orientated substrates (130 nm/h) [124]. In-situ doping of the channel during growth is possible during MBE: the opening and closing of additional effusion cells can be used to control the doping profile of the device.

- **Metal-organic chemical vapor deposition:** MOCVD is a thin-film growth technique that relies on metal-organic precursors for crystal growth. The precursors flow across a target substrate, reacting with the surface and resulting in epitaxial growth. Typically, the precursors metal organic trimethyl-gallium (TMG) and oxygen are used for MOCVD growth of β-Ga_2O_3 [125]. MOCVD has been used previously to grow β-Ga_2O_3 films with key dopants, such as Si, Sn and Mg [126][127]. Doping is achieved through the addition of another precursor, (e.g. silane (SiH4)/He gas for Si doping). Room temperature electron mobilities as high as 160 cm^2/Vs have been reported in MOCVD grown β-Ga_2O_3 crystals [128].

- **Halide vapour phase epitaxy:** HVPE is a similar process to MOCVD, in which chlorine based precursors are used for epitaxial growth on the target substrate, as opposed to metal-organic based precursors. In the case of β-Ga_2O_3, a GaCl precursor is used, along with O_2 gas [129]. The advantage of HVPE is both high-growth rates and the suppression of key compensating dopants that are unavoidable in MOCVD, such as carbon and hydrogen [130]. These impurities are always present in MOCVD films due to the presence of

organic precursors during the growth process. In contrast, neither element is present in the precursors used for HVPE.

- **Applications:** MBE is used where high-quality epitaxy and control of the growth process is required. MBE, however, is expensive and suffers from low growth rates [131] [18]. In contrast, MOCVD can achieve high growth rates and scalability of wafer production [132]. HVPE is preferred when low background carrier concentrations ($N_D - N_A$) are required [133].

MBE, MOCVD and HVPE all allow for the in-situ doping of the UID layer for the purpose of channel formation. However, it is not always desirable to introduce dopants in this way, for instance, if a non-uniform doping profile is required in the channel. Dopants can be introduced to form a channel after UID layer growth using implantation doping. Implantation doping is a technique in which dopant ions from a solid or gaseous source are accelerated towards a crystal using an electromagnetic field. These ions then collide with the crystal, scattering off atoms in the lattice. The ion loses kinetic energy with each collision, displacing atoms from their lattice sites in the process, introducing radiation damage in the form of interstitials and vacancies. Once the kinetic energy of the ion is sufficiently low, it will occupy a vacancy site or an interstitial site in the lattice. Thermal annealing is required to reduce the number radiation defects to an acceptable level. In β-Ga_2O_3, implantation doping has been achieved using Si^+, Mg^+, N^+, H^+ and Ar^+ ions [134].

2.3.0.4 Contacts

The wide-bandgap of β-Ga_2O_3 complicates the formation of ohmic contacts, as there are only few metals with a low enough work-function to satisfy the conditions for ohmic contact formation, (outlined in Fig.2.11). As such, Schottky-barriers usually form at a β-Ga_2O_3-metal interfaces. Two main approaches have been adopted to address this problem: workfunction tuning through the fabrication of metal stacks and implantation doping of the contact area.
Fig.2.26(a) shows the two most widely used ohmic contact stacks used in β-Ga_2O_3 devices. Both stacks have a Ti layer in direct contact with the channel. The work function of Ti (4.33eV) is larger than the electron affinity of β-Ga_2O_3, and so a SB should form at this interface. However, thermal annealing of the contact metal stack has been shown to promote the formation of a titanium oxide (Ti_2O_3) layer at the metal-channel interface. The low workfunction of the Ti_2O_3 layer (3.6-3,9eV) allows for the formation of an ohmic contact with the channel [135]. The Au capping layer on the contacts ensures a good electrical connection between the metal stacks and external equipment, (such as probe tips). The Ti/Au stack has been observed to degrade at temperatures >500°C, with an increase in the contact resistance and non-ohmic behaviour reported [136]. In contrast, the Ti/Ni/Al/Au stack has demonstrated resistance to high temperature degradation.
The problem of Schottky barriers can also be avoided by heavily doping the region under the

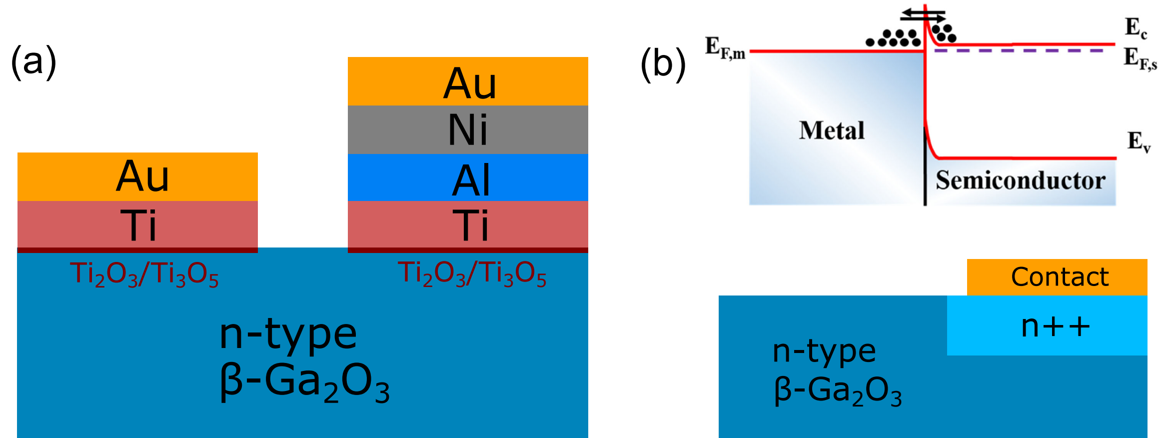


Figure 2.26: (a) Metal stacks used for the formation of ohmic contacts with β-Ga$_2$O$_3$. A titanium oxide layer forms at the gallium oxide interface after thermal annealing. The low workfunction of titanium oxide allows for the formation of an ohmic contact. (b) Heavy doping of contact region reduces the Schottky-barrier width at the metal-semiconductor interface, lowering the contact resistance. Figure adapted from [135].

contact metal stack. Fig.2.26(b) shows the band diagram of the interface between a contact and a heavily doped interface. The heavy doping has the effect of reducing the width of the Schottky barrier (Eqn.2.19). If the barrier is sufficiently thin, electrons will directly tunnel into the contact, significantly reducing the contact resistance and suppressing non-ohmic behaviour [135]. This technique has been previously demonstrated using Si$^+$ implantation doping under contacts [137]. Regrowth techniques, in which the semiconductor under the contact is etched away and regrown with a higher doping density, have also been used to achieve low contact resistances [138].
The main consideration when fabricating Schottky contacts on β-Ga$_2$O$_3$ is the barrier height. This dependents on both the metal workfunction and the orientation of the crystal β-Ga$_2$O$_3$ channel. Reported barrier heights for commonly used Schottky metals on (010) β-Ga$_2$O$_3$ are 1.27 V for Pd, 1.54 V for Ni, 1.58 V for Pt and 1.71 V for Au [139]. Values have been also reported for a range of metals on (100) β-Ga$_2$O$_3$ and for Pt on (001) β-Ga$_2$O$_3$ [140][141].

2.3.0.5 Gate Dielectric and Passivation Layers

High-quality gate dielectric layers are required for the fabrication of device gates, to reduce gate leakage currents and to minimise the density of trapping centres that could affect device behaviour. Passivation is required to reduce surface leakage in devices [142] and to suppress surface states close to the channel [143]. These states could consist of surface oxygen vacancies, defect states, and surface absorbents. Passivation has been demonstrated to enhance device breakdown and to reduce surface depletion [144]. Non-dispersive RF output characteristics have also been attributed to high-quality passivation in β-Ga$_2$O$_3$ devices [22]. Several insulators

have been investigated in the literature, for use as gate dielectrics and passivation. The most commonly used are SiO_2 and Al_2O_3, with SiN and HfO_2 also reported [145].
Deposition of dielectric and passivation layers is usually achieved with chemical vapour deposition (CVD) and atomic layer deposition (ALD). MOCVD deposition of Al_2O_3 has also been reported. ALD is a form of CVD, in which a precursors are added in stages to achieve a series of self-limiting half reactions. This allows for the deposition of single layer materials. In general, ALD is preferred over CVD for the deposition of gate dielectrics, as thin-films grown by this technique exhibit high-quality, lower defect densities and a high degree of uniformity [146]. CVD is generally preferred for passivation layers due to the slow deposition rate of ALD [147].

2.4 Device Reliability

The equations, band diagrams and output characterises presented in the previous section assumed ideal behaviour. Deviations from ideal behaviour are often observed; leakage currents, electron trapping and device self-heating all impact on the reliability of devices. In this section, some of these challenges and problems will be outlined, and their impact on device behaviour discussed.

2.4.1 Leakage Currents and Device Breakdown

Current leakage in MOSFETs is an intrinsic problem that degrades device performance. The magnitude and voltage scaling of leakage currents is determined by the nature of available leakage paths in a device. Device breakdown is triggered when the electric field over these paths is sufficiently high, as a large leakage current over a resistive leakage path can lead to the formation of hot-spots via hot electron damage [148]. These hot-spots can trigger device failure by inducing irreversible damage across the device. This is a particular problem in (ultra)wide-bandgap semiconductors, where the high breakdown fields allow for significant off-state bias stressing during normal device operation. Fig.2.27 shows the principle leakage paths in the MOSFET structure. Punch-through leakage can occur under the channel, when the device is in the depletion regime. This is often the result of poorly-insulting substrates, and can degrade electrical performance of devices, as it allows for a parallel conduction path in off-state devices [149]. Substrate leakage is the result of poor-quality epitaxy, with the leakage current being observed between a biased drain contact and the electrically grounded device substrate. This leakage current will cause a high off-state leakage current that is independent of the gate voltage. The leakage path that most often triggers device breakdown in (ultra)wide-bandgap MOSFET devices is leakage through the gate oxide and passivation layer. An increase in the gate leakage current is often indicative of device degradation and usually precedes gate oxide failure [150][151]. Mechanisms such as surface hopping conduction can lead to a leakage current between a biased gate and source contact [152]. This can be suppressed by introducing a suitable passivation layer.

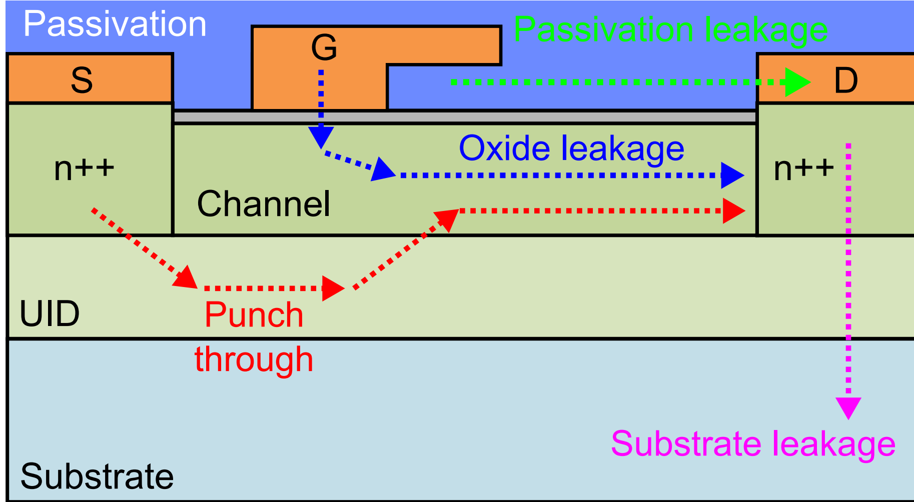


Figure 2.27: Schematic demonstrating the main leakage paths present in a MOSFET.

However, direct leakage between the conducting channel and the gate contact remains a problem. High-fields in the region of the gate-drain edge can enhance the leakage current via the creation of trap states by hot-electrons [153]. The peak field regions of the device, (e.g. the drain-side of the gate), are the critical failure points of a gate dielectric.

There are many possible leakage mechanisms in a gate dielectric, with the most commonly observed ones shown in Fig.2.28. Thermionic and thermionic field-emission are equivalent to the process shown in Fig.2.19 for a reverse biased SB, and have similar expressions for current density. Direct tunneling is observed at low-field, and consists of an electron quantum mechanically tunneling through the oxide potential barrier. A simplified expression for the direct tunneling current density (J_{DT}) is given by the expression [154],

$$J_{DT} \approx exp\left(-\frac{8\pi\sqrt{2q}}{3h}(m_e^*\phi_B)^{1/2}\epsilon_r t_{ox}\right), \tag{2.35}$$

where t_{ox} is the oxide thickness and ϵ_r is the dielectric constant. The exponential dependence of tunneling current on oxide thickness in Eqn.2.35 means that direct tunneling is insignificant for oxide layers with thicknesses >10nm.

Tunneling current densities can be increased with the application of a high electric field. A high field over the oxide modifies its conduction band profile, reducing the effective electron tunneling distance across the potential barrier (see Fig.2.28). Tunneling through this barrier at high-field is known as Fowler-Nordheim (FN) tunneling. Its tunneling current (J_{FN}) has the following field dependence [155],

$$J_{FN} = CE^2 exp\left(-\frac{B}{E}\right), \tag{2.36}$$

where E is the field at the oxide interface and B and C are constants. The presence of this tunneling mechanism across thin film oxides in MOS structures is well established, [156][157][158].

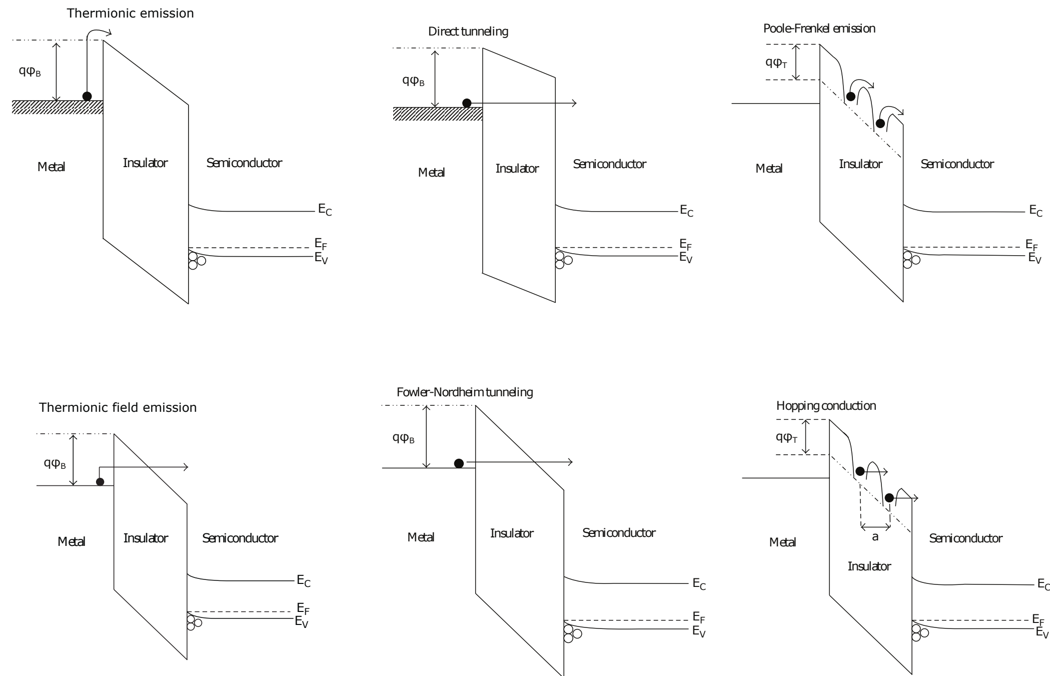


Figure 2.28: Leakage mechanisms across a MOS interface, with a negative bias applied to the metal. Figure reproduced from [154].

Tunneling over the entire oxide width is only possible in thin, high quality oxide films in the absence of defects [159]. When trapping states are present in the oxide layer, electrons tunnel into the states under the application of field, either directly, or via a trap-assisted tunneling mechanism [160][161][162].

The two trap-assisted leakage mechanisms are Poole-Frenkle emission and hopping conduction. Poole-Frenkle emission is a high-field emission process in which the effective depth of the potential well of a trap state is reduced in one direction by an applied voltage. This assists the thermally agitated emission of the electron to the conduction band, leading to a net tunneling current across oxide [163]. The current density is given by the expression [154],

$$J_{PF} = q\mu N_C E exp\left(-\frac{-q(\phi_t - \sqrt{qE/\pi\epsilon_r\epsilon_0}}{kT}\right), \tag{2.37}$$

where ϕ_t is the trap energy level and N_C is the conduction band density of states. In contrast to Poole-Frenkle emission, hopping conduction does not require the emission of an previously trapped electron. Instead, hopping conduction covers a range of mechanisms that rely on the tunneling of electrons between trap states in the oxide. 'Hopping' between these states leads to a net leakage current density across the oxide.

2.4.2 Electron Trapping

2.4.2.1 Trapping States in β-Ga_2O_3

Electron trapping in semiconductor devices has the potential to severely limit their performance and reliability. Fundamentally, electron traps are defects or impurities that form an energy level in a semiconductor's bandgap. What differentiates an acceptor/donor state and a trapping state is their position within the bandgap; any state which is >0.1eV from the conduction/valence band edge can be considered a trapping state [164]. Trapping in (ultra)wide-bandgap semiconductors is a particular problem as deep-level states with an energy offset >1eV from the conduction/valence band edge are common. These states have significant detrapping time constants associated with the capture and emission of an electron. As such, long lived charging effects are common in (ultra)wide-bandgap semiconductors.
A large number of trapping states in β-Ga_2O_3 have already been identified. Fig.2.29 shows the position of a number of previously reported deep-level states in the bandgap of β-Ga_2O_3. The energy range for each state reflects the spread of values reported in the literature, using different growth and measurement techniques. The origin of these trapping states has been attribute to a number of impurities and structural defects. The majority have been linked with gallium vacancies, oxygen vacancies, iron impurity states, native and intrinsic defects and transition metal impurities [165]. The growth conditions and presence of specific impurities will determine the number and density of trap states found in a β-Ga_2O_3 crystal. Fig.2.30 shows a comparison

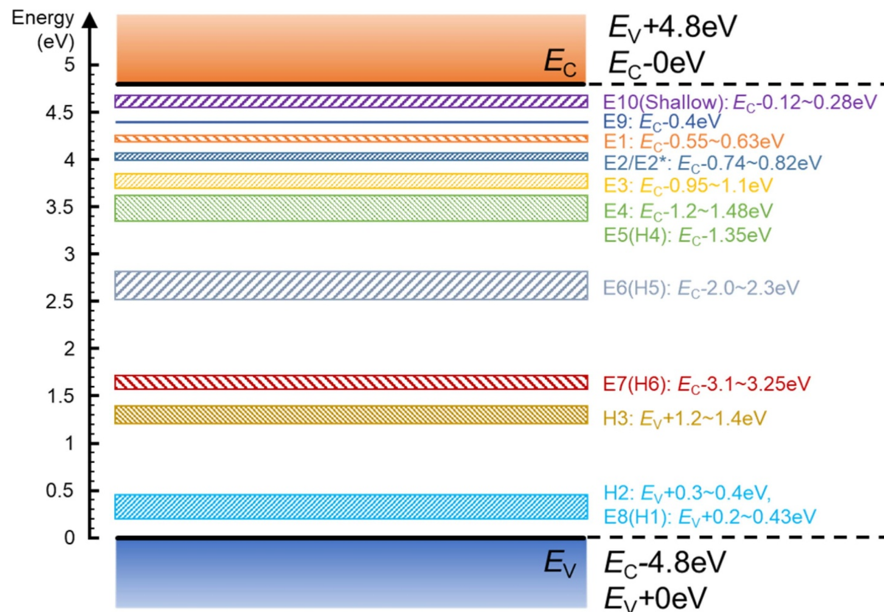


Figure 2.29: The distribution of deep-level traps in the bandgap of β-Ga_2O_3. Figure adapted from [165].

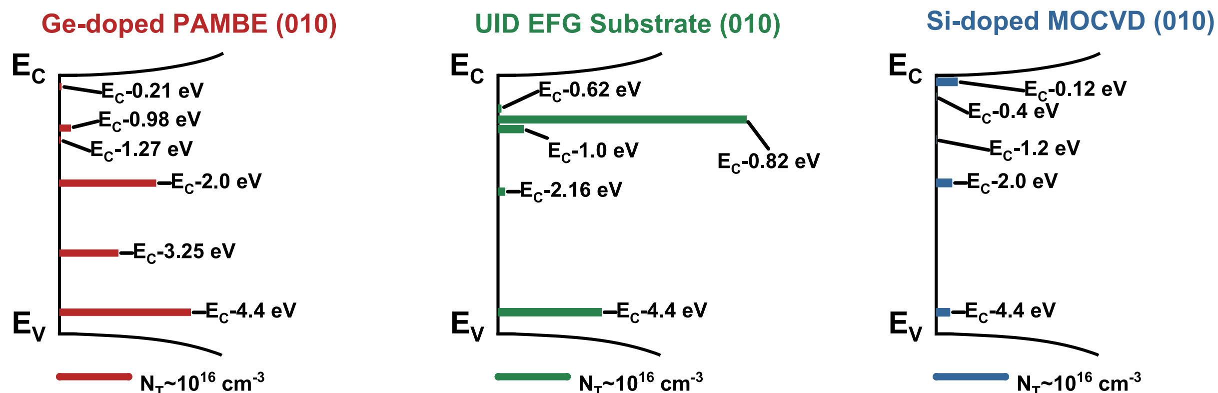


Figure 2.30: Conduction band offsets and densities of deep-level trap states in three β-Ga_2O_3 crystals. The three crystals were grown using plasma-assisted MBE (PAMBE), edge-define film-fed growth (EFG) and MOCVD. Figure adapted from [166].

of the deep-level states present in three crystals grown using different methods, reported by Ghadi *et al.* [166]. The trap energies and densities were extracted using deep-level transient spectroscopy for conduction band offsets < 1eV, and deep-level optical spectroscopy for conduction band offsets > 1eV. Three growth methods were used: plasma-assisted MBE; edge-define film-fed growth [116]; and MOCVD. All three crystals contain a number of the deep-level states, all of which are present in Fig.2.29. The trapping states 2eV and 4.4eV below the conduction band are common to all three growth methods. The presence of other states depends on the growth method employed. It is clear that MOCVD growth is the best method for achieving low densities of deep-level states, with no states having a density $>10^{16}$ cm^{-3}. States that are only seen in the case of a single growth method, such as the trap with a conduction band offset of 0.12 eV observed after MOCVD growth, are mostly attributed to extrinsic defects in the literature [165].

2.4.2.2 Electron Trap Locations

The precise location of trapping states within a β-Ga_2O_3 devices will determine their impact on the device behaviour. There are many potential trap locations in devices such as MOSFETs, such as the substrate, the UID region and the channel. Fig.2.31 shows the position of potential trapping states within the MOSFET structure.
Surface states are not positioned in the conductive channel, and so their charge state can only change via electron transport across the surface of the device, via a field driven hopping mechanism. The field-driven conductivity σ of this effect is given by the expression [167],

$$\sigma = \sigma_o exp(\beta E^{1/2}/K_B T), \tag{2.38}$$

where σ_0 is the low-field conductivity of the material, E is the electric field, T is the temperature and β is a constant. It is clear from Eqn.2.38 that small changes in field will lead to large changes in the conductivity of the surface state, particularly in high-field regions on the surface [168].

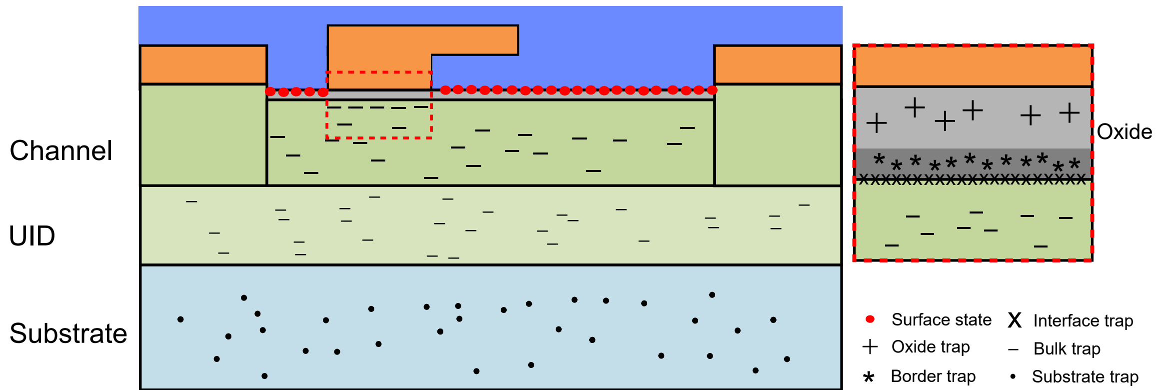


Figure 2.31: The potential positions of trap states in a typical MOSFET. The inset at the top right of the figure shows an enlarged cross-section of the metal-oxide-semiconductor junction.

Under high-voltage operation, there will be a high-field region situated at the drain-side of the gate; surface states close to this region will experience a change in their charge state. If the field at the drain-side of the gate then is removed, the charge states of the surface states will persist. This trapped surface charge introduces a 'virtual gating' effect [169]. The negative charge of the virtual gate has the effect of depleting the underlying channel, effectively extending any depletion regions under the gate further into the channel. This second depletion region is not controlled directly by the applied biases (e.g. V_{GS}), but by the trapping/detrapping mechanism of the surface states. This can introduce current-collapse and frequency dispersion in the drain current [170].

The MOSFET oxide layer can also act as a source of trapping, with bulk oxide traps, border traps in the oxide, and oxide-semiconductor interface traps all observed [171]. There are many potential sources of charge trapping states in oxide layers, e.g. amorphous Al_2O_3 can contain oxygen vacancies, aluminum interstitials and hydrogen interstitials, (provided by impurities in the growth process) [172]. Interface traps differ from border and bulk oxide traps insofar as they are physically situated at the interface between an oxide and semiconductor, whereas border traps and oxide traps are situated within the oxide layer. Border traps and bulk oxide traps are distinguished by the way in which they interact with the semiconductor layer below; electrons are able to tunnel between border traps and the channel in a reasonable amount time [173]. In contrast, tunneling from the channel into bulk oxide traps is suppressed by the exponential distance term in the oxide tunneling current, (see Eqn.2.35).

The charging of bulk oxide trapping states in the oxide layer relies on field-driven conduction to change their charge state, such as FN tunneling and hopping conduction (see Fig.2.28). Fixed oxide charge in the gate dielectric of a MOSFET manifests as a shift in the device threshold voltage; the potential of this fixed charge effectively acts as a voltage offset in the gate voltage.

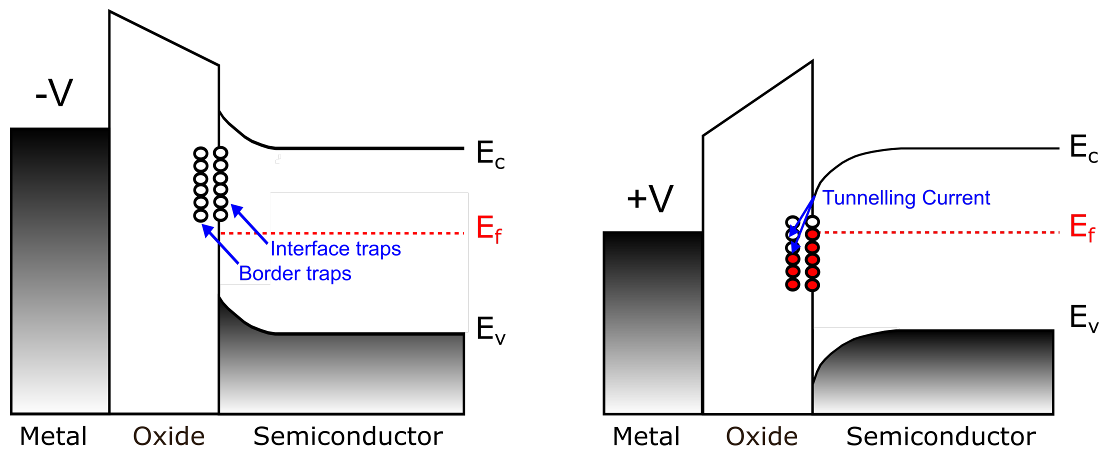


Figure 2.32: The change in interface and border trap occupancy as a function of bias. Traps far above the Fermi energy are unoccupied. As traps cross the Fermi energy, they are occupied by conduction band electrons. Electrons must tunnel through part of the oxide to occupy border traps.

The shift in threshold voltage (δV_{th}) is given by the following expression [174],

$$\delta V_{th} = -\frac{Q_{ox}^{+} - Q_{ox}^{-}}{C_{ox}}, \tag{2.39}$$

where Q_{ox}^{+} and Q_{ox}^{-} are the fixed positive and negative charge trapped in the oxide, respectively. Interface traps do not rely on electron tunneling to change charge state. When a voltage is applied to the gate, the Fermi level at the interface moves up or down with respect to the interface-trap levels. As the Fermi level passes the interface traps, their occupancy will change, as shown in Fig.2.32. Electron emission from these traps is observed when an occupied trap passes above the Fermi level. The behaviour of border traps is similar to that of interface traps, with the response time of the traps also depending on conduction band offset. However, the response time of a border trap is longer than that of interface traps with the same conduction band offset, as electrons must tunnel over a few nms of oxide to change modify its charge state. Both border and interface traps can induce threshold voltage shifts, changes in the subthreshold slope and frequency dispersion in the output characteristics of a device [175]. Bulk oxide traps typically have far longer response times than interface and border traps. Changes in bulk oxide charge state are semi-permanent in the absence of a bias stress, due to the low tunneling probability of electrons across thick oxide layers (>10nm).

Deep-level states and defects in the semiconductor act as bulk traps in the conducting channel. The occupancy of trap states in the bulk of the semiconducting device channel is determined by Shockley–Read–Hall statistics [180]. The rate of electron capture by a trapping state (R_C), with

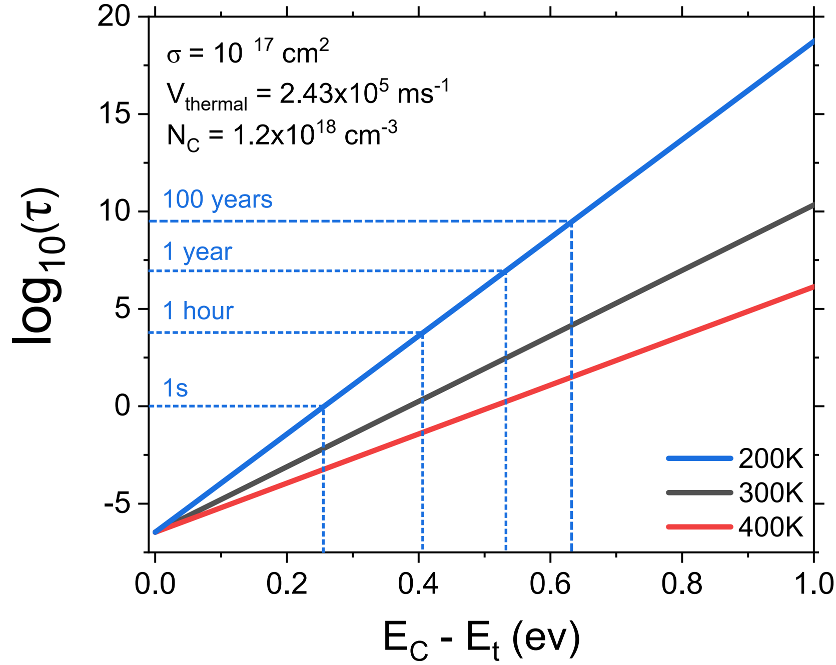


Figure 2.33: The emission lifetimes for a trapping state in GaN, as a function of both temperature and conduction band offset. The cross-section for electron capture is assumed to be 10^{-17} cm^2, a typical value for trapping states in GaN [176]. The thermal velocity of electrons is taken from [177], and the density of states at the conduction band edge from [178]. Treating these parameters as constants has little bearing on the excessive detrapping times of deep-level states, due to the exponential dependence of τ on conduction band offset.

a conduction band offset of E_t is determined by the following expression,

$$R_C = \sigma_n N_t[1 - F(E_t)]n, \tag{2.40}$$

where σ_n is the electron capture cross-section, n is electron concentration, N_t is the density of trapping states and $F(E_t)$ is the Fermi-Dirac distribution. The Fermi-Dirac term of Eqn.2.40 takes the form,

$$F(E_t) = \frac{1}{1 + exp[(E_t - E_F)/kT]}. \tag{2.41}$$

The rate of emission of electrons from the trap state into the conduction band (R_E) is be given by the expression,

$$R_E = E_n N_t F(E_t), \tag{2.42}$$

where E_n is a constant. In equilibrium, the rates in Eqn.2.40 and Eqn.2.42 will be equal, and there will be no net change in the average charge state of the traps. Applying bias stresses to a device will shift the Fermi energy, modifying the value of $F(E_t)$, leading to a net capture or

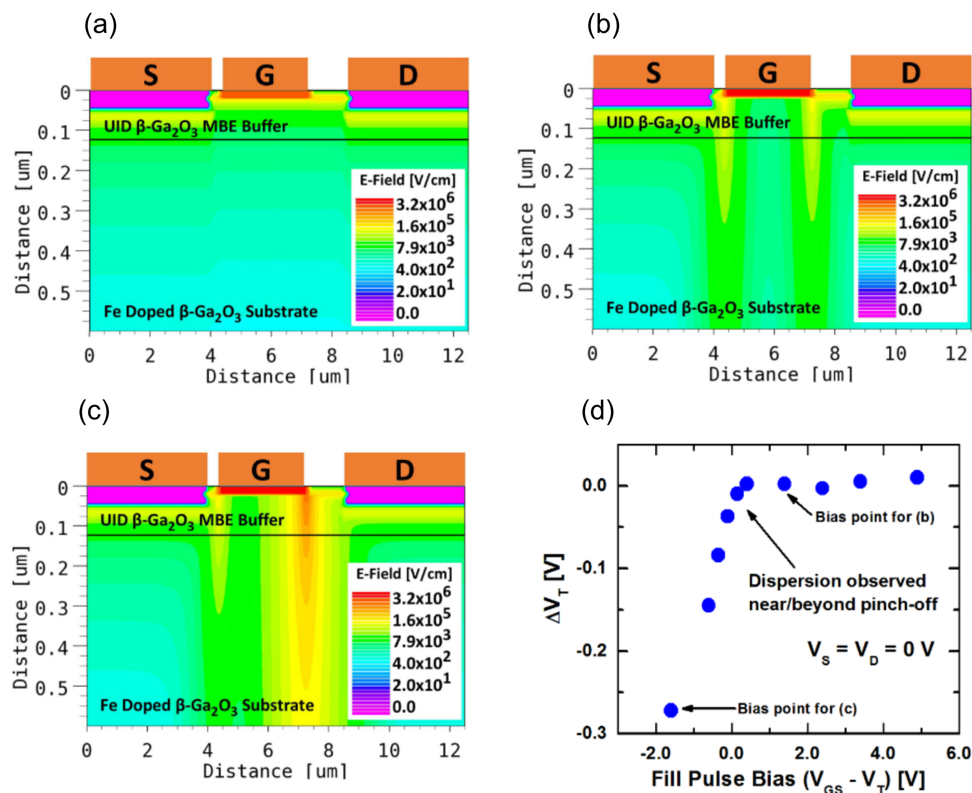


Figure 2.34: (a) Field profile of a delta-doped β-Ga_2O_3 MESFET in the on-state. The channel screens the substrate from the applied field. (b) In the off-state. the gate bias field penetrates into the substrate. (c) Applying a drain bias in the off-state significantly increases the field in the substrate. (d) Threshold voltage shift as a function of applied gate bias. Shifts are only observed when the device is in the off-state, suggesting the filling of traps in the substrate. Figure adapted from [179].

emission of electrons. The emission rate of electrons can be expressed in terms of the electron trap energy level offset from the conduction band [181],

$$R_E = V_{therm}\sigma_n N_C exp\left(\frac{E_t - E_c}{KT}\right), \tag{2.43}$$

where V_{therm} is the thermal velocity of the electrons, N_C is the density of states in the conduction band and E_c is the conduction band energy. It is clear from Eqn.2.43 that the emission rates for trapping states deep in the bandgap (>0.1/0.2 eV), will be suppressed by the exponential term. This implies a large characteristic time constant for electron emission τ, defined by the expression,

$$\tau = \frac{1}{R_E}. \tag{2.44}$$

In (ultra)wide-bandgap semiconductors, the lifetime of such traps can be so large as to exceed any reasonable measurement time. Fig.2.33 shows the lifetimes of a trapping state as a function of both temperature and conduction band offset. The value of the conduction band offset dominates

τ, with increasing offset reducing the electron emission lifetime [182]. Trapping states with conduction band offsets >0.8eV have detrapping time constants >10 days at room temperature. Long-lived trap states in the channel will decrease the channel mobility and increase device R_{on} through ionised impurity scattering (see Fig.2.6).
Buffer traps are situated in the substrate, and so are physically isolated from the device channel. Therefore, occupied buffer traps do not directly act as scattering centres in the channel, but can introduce back-gating effects. This can lead to instabilities in the device on-resistance, drain-current lag, and shifts in the threshold voltage [183][184]. The magnitude and the recovery of these effects heavily depend on the stress bias across the channel-buffer interface. The bias dependence of such effects can be seen in Fig.2.34. McGlone *et al.* reported on threshold voltage instabilities in β-Ga_2O_3 delta-doped MESFETs, after off-state bias stressing of the device [185]. In the on-state, the charge in the device channel screens the substrate from the gate bias, (Fig.2.34(a)). Depleting the channel allows for the gate potential to penetrate into the substrate (Fig.2.34(b)), with the application of an additional drain stress bias significantly increasing the field in the substrate (Fig.2.34(c)). The high-field leads to injection of charge into the substrate, and to the charging of buffer traps. These traps then deplete the backside of the channel, reducing the device's threshold voltage (Fig.2.34(d))). Once charged, these traps pose a particular problem for device performance, as their detrapping time constant can be limited by transport from the buffer into the channel. Electrically isolated traps in a substrate can lead to semi-permanent changes in the device behaviour [40].

2.4.3 Device Self-heating

The output characteristics and transfer characteristics presented in section.2.2.3 assume an ideal device. The impact of electron trapping on these characteristics has been discussed in the previous section. The effect of device self-heating on the device performance needs to also be considered. In the on-state, current flow leads to resistive heating in the channel. In turn, this leads to a drop in the I_D, as the scattering of electrons in the semiconductor by phonons increases with temperature. In equilibrium, the generation of heat in the channel will be balanced by the heat flux out of the channel. As β-Ga_2O_3 devices are fabricated on native substrates, they do not suffer from the problem of thermal boundary resistances at heterointerfaces, as seen for GaN channels grown on Si and SiC substrates [187][188]. However, the low thermal conductivity of β-Ga_2O_3 significantly limits the heat flux out of the channel, leading to a high degree of self-heating. Fig.2.35(a) shows a comparison of the pulsed and the DC characterisation of a lateral β-Ga_2O_3 MOSFET, reported by Singh *et al.* [35]. During pulsed measurements self-heating is suppressed, and in DC measurements self-heating is present, leading to a significant reduction in the drain current, (pulsed and DC measurements will be explained in detail in section.3.2.3 and section.3.2.2, respectively). Fig.2.35(b) shows a simulation of the time taken for the channel to reach thermal equilibrium, with the peak temperature of the device plotted. For a relatively

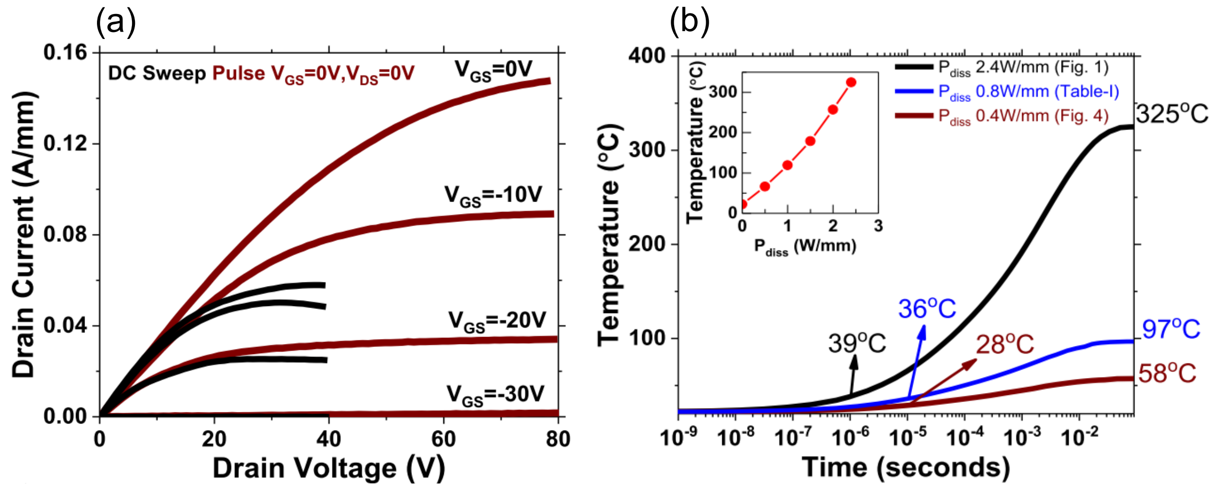


Figure 2.35: (a) The effect of self-heating on the I_D-V_{DS} characteristics on a β-Ga_2O_3 MOSFET. The pulsed measurement suppresses self-heating, which is present in the DC measurement. (b) Simulated peak channel temperature as a function of time. Inset: Simulated transient peak channel temperature as a function of power dissipation. Figure reproduced from [35].

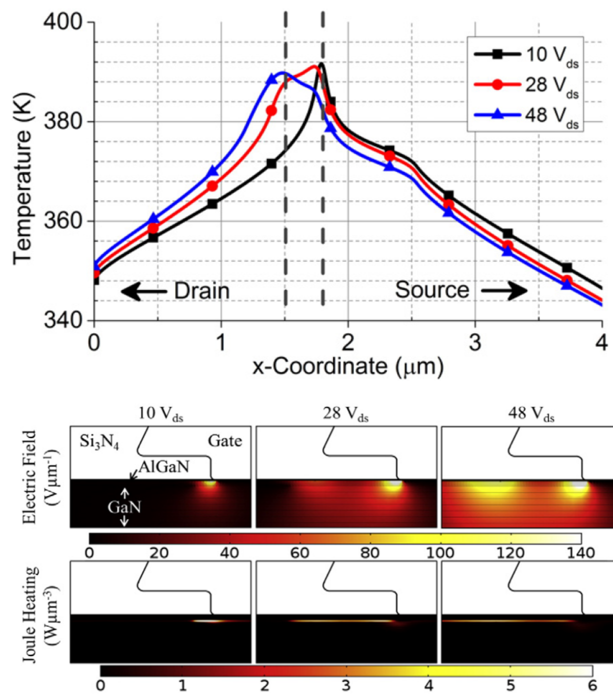


Figure 2.36: Simulated bias dependence of device self-heating for a GaN HEMT. The drain bias is varied, with the gate bias adjusted to ensure a constant power dissipation. Increasing drain bias leads to elongation of the self-heating profile, which can be attributed to the more distributed electric field and Joule heating in the channel. Figure reproduced from [186].

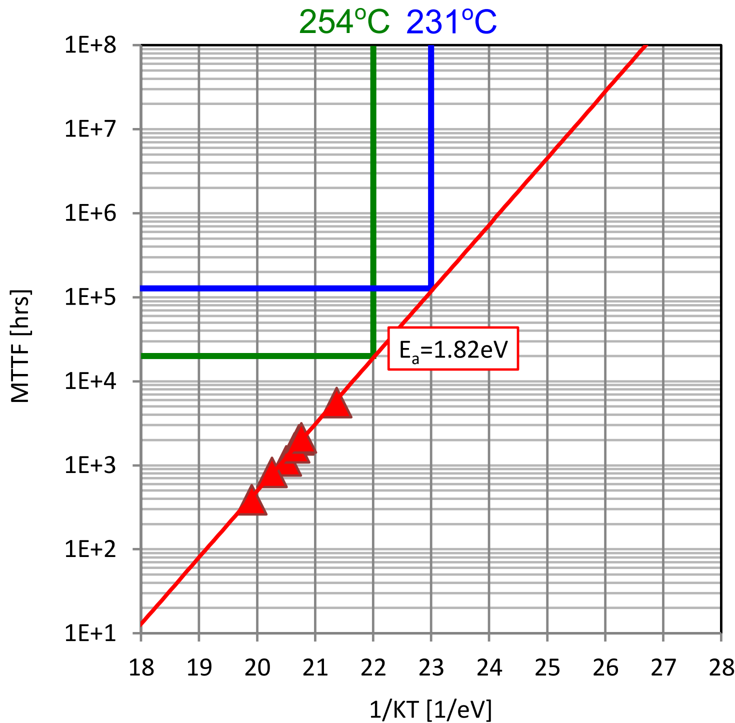


Figure 2.37: The results of high temperature operation life testing of several GaN HEMTs under DC bias stress. The lifetime of the devices is measured as a function of temperature. The lifetimes are then used to extrapolate an activation energy of 1.82eV for the breakdown process. The linear fit to this data can be used to predict the MTTF for a given channel temperature. Figure adapted from [189].

low power dissipation of 1 W/mm, significant self-heating is observed, with the channel reaching temperatures >100°C.

The position of the peak temperature in device channel will depend on the precise electric field profile in the device. Peaks in electric field can lead to a higher degree of localised self-heating. Fig.2.36 shows the simulated self-heating profiles for a GaN HEMT, reported by Jones *et al.* [186]. For each drain voltage, the gate voltage was varied to ensure a constant power dissipation. As the drain bias is increased, an elongation of the temperature profile is observed, with an increased width in the peak temperature hot spot and a shift of the hot spot position towards the drain. This behaviour can be explained with reference to the electric field and the Joule heating profiles. At low drain biases, a single peak in the field is observed at the drain-side of the gate. A second peak emerges at the drain side of the field-plate at higher biases. The delocalisation of the peak field results in a more distributed Joule heating profile at the drain-side of the gate, leading to more uniform heating under the field plate. It is clear from Fig.2.36 that the bias conditions used when investigating self-heating in a device must be carefully considered.

As well as reducing the performance of β-Ga_2O_3 devices, self-heating also significantly reduces device lifetimes. The mean-time-to-failure (MTTF) of a device is often modelled using a Arrhenius relationship, with respect to the peak channel temperature in the device [190]. There is an exponential dependence of the MTTF on the peak channel temperature, and so even a small increase in channel temperature can lead to a large decrease in device reliability. Fig.2.37 shows an example of a MTTF Arrhenius plot for a set of GaN HEMTs, reported by Lambert *et al.* [191]. Measurements of device lifetimes under DC bias stress, over a range of temperatures, allow for a MTTF-temperature relationship to be extrapolated. The MTTF-temperature relationship can be described with an activation energy, with the value depending on the breakdown mechanisms of the device [192]. It is clear that small changes in channel temperature can significantly impact a device's lifetime, with an increase from 231°C to 254°C leading to an order of magnitude reduction in the MTTF.

Chapter 3

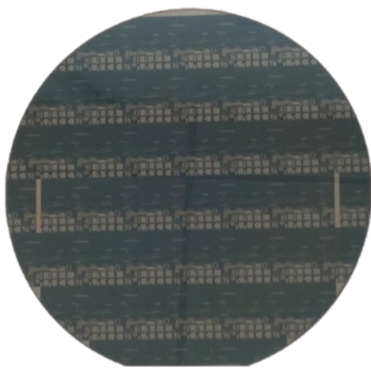
Characterisation Techniques

The experimental characterisation of devices is key to understanding their behaviour and physics. This is especially true of devices that utilise novel materials, such as β-Ga_2O_3. The behaviour of such devices is not fully understood, and often deviates from theoretical models. This chapter will outline the characterisation techniques that will used in subsequent results chapters to understand and investigate the behaviour of various device architectures. These techniques will cover electrical and thermal characterisation, along with simulation based methods.

3.1 Measurement Environment

All devices characterised in subsequent chapters were on-wafer devices, as opposed to packaged devices. As such, all measurements were performed in a probe station environment, using probe tips to allow for on-wafer characterisation. There was a great deal of variation between the required measurements and on-wafer layout of each sample set, and so a range of measurement configurations were required. Each configuration had to be tested carefully for possible leakage paths, ground loops, and parasitics, with particular attention paid to the layout of cabling. Fig.3.1 shows a typical measurement environment for on-wafer device characterisation, and a typical sample wafer. The probe station is situated inside a metal cabinet. This cabinet ensures optical isolation of the system, and screens the wafer from any external electromagnetic interference, both of which can induce changes in device behaviour. During measurements, the wafer sits on the metal chuck, with the probe tips used to contact a single device. The position of the wafer relative to the tips is controlled by moving the chuck using a set micropositioner. The chuck grounding cable ensures that the substrate voltage of the wafer is defined relative to the contact

(1) Cabinet for opitcal isolation
(2) Instrument to device cabling
(3) Probe tip holder
(4) Probe tips
(5) Substrate chuck
(6) Chuck micropositioners
(7) Chuck grounding cable
(8) Probe station door interlock
(9) Microscope



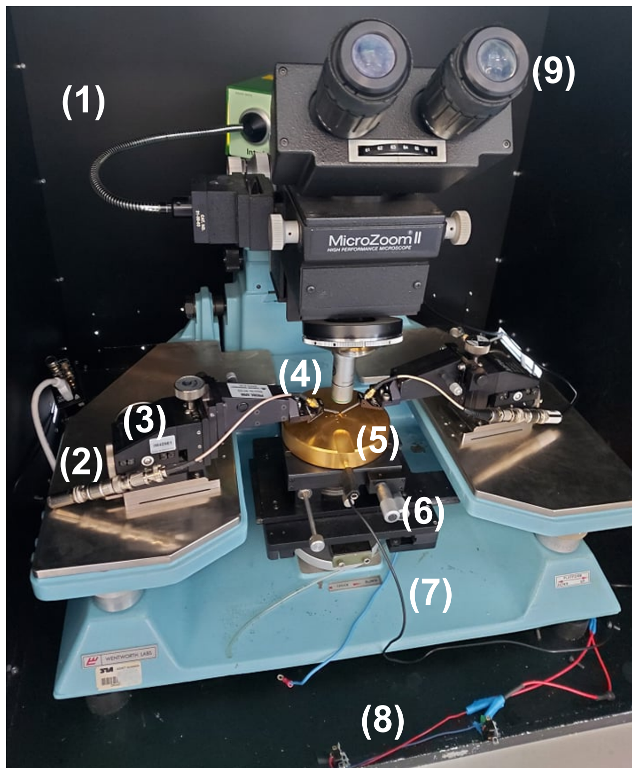


Figure 3.1: A standard probe station used for on-wafer characterisation of devices. The probe station is inside a metallic cabinet, ensuring both optical isolation and screening from external electromagnetic interference. An interlock circuit ensures that no biases are applied while the cabinet doors are open. A typical sample wafer is shown in the bottom left hand corner.

pads of the device. Biases are applied via cabling, running from the probe tips to an external instrument. Careful consideration must be taken when choosing probe tips and suitable cabling for a particular measurement configuration.

A good connection between the device contact pads and the probe tips is critical for on-wafer characterisation. Two types of probe tips were used in the measurements presented in subsequent chapters: DC probe tips and ground-signal-ground (GSG) probe tips. Fig.3.2(a) shows a schematic of a DC tip, which consists of a single metallic signal tip. This tip is unshielded, and so is exposed to parasitic capacitive and inductive paths. Therefore, DC probe tips are only suitable for low-frequency measurements. For high-frequency measurements, and measurements that require periodic functions with rapid rise times (e.g. square waves), ground-signal-ground probe tips are used, as shown in Fig.3.2(b). Here, the signal probe tip runs between two equally spaces grounded tips (on-wafer devices are required to have two source pads for the ground probes). The purpose of the ground tips is to suppress inductive parasitics. During the measurement, the flow of current induces magnetic fields around the signal tip. Any changes in the applied bias will lead

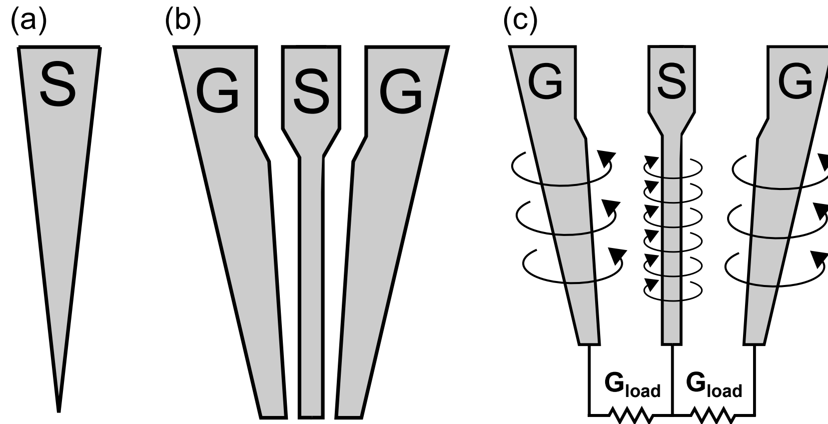


Figure 3.2: Schematics of (a) a DC probe tip and (b) a ground-signal-ground (GSG) probe tip. (c) A schematic of the GSG probe tip parasitics. When in contact with two equally balanced loads (G_{load}), the inductive parasitics across the signal and grounds tips cancel out.

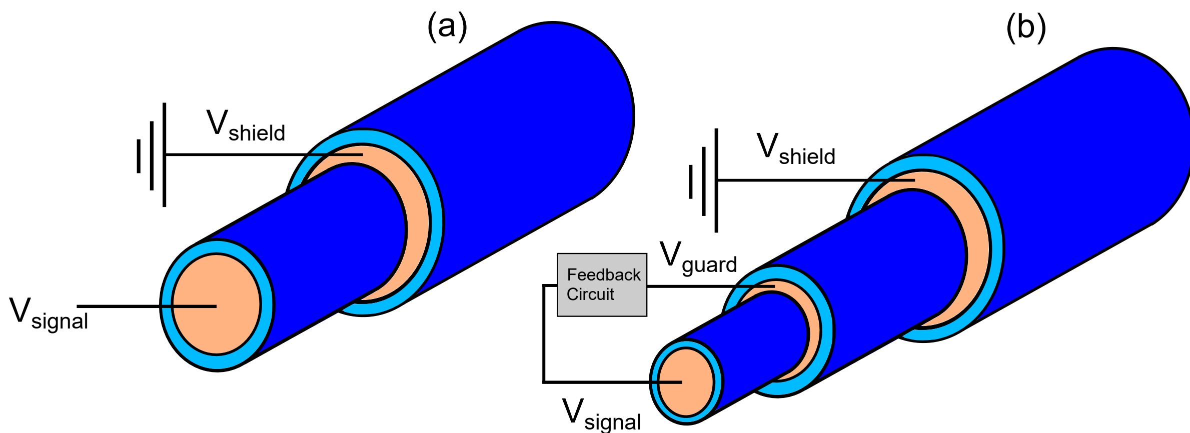


Figure 3.3: Cross-section of (a) a coaxial cable and (b) a triaxial cable. Both cables have an outer metallic shielding layer, with the triaxial cable also having an addition metallic guarding layer between the signal and guard. The feedback circuit ensures that the voltage of the guard is the same as that of the signal.

to changes in this magnetic field. The change in field will back-induce a field in each of the ground tips. If both ground tips are connected to ground pads with equal loads the back-induced fields will have the same magnitude and opposite polarities, (see Fig.3.2(c)). Therefore, the fields around the ground tips will cancel, effectively shielding the signal probe from the wider measurement environment. Often, the loads at each source pad are not be equal, and so some degree of parasitic inductive coupling will still be observed [193].
Suitable cabling is required for accurate measurements, with high current resolution, and low parasitics being desirable. Two types of cabling were used in subsequent chapters, coaxial cables

and triaxial cables. Fig.3.3(a) shows a cross-section of a coaxial cable. The signal line is shielded from external electromagnetic interference by a metallic shielding layer. The current resolution of this cable is limited by the parasitic capacitance between the shield and signal. Fig.3.3(b) shows a cross-section of a triaxial cable, which has an additional guarding layer between the signal and the guard layers. A feedback circuit is used to keep the voltage of the guard equal to that of the signal. This has the effect of reducing the parasitic capacitance across the cable, increasing the current resolution of the measurement system. However, the feedback circuit utilises an op-amp based feedback loop, and so is limited to low frequency operation (<1MHz). As such, triaxial cables are used for low frequency measurements for enhanced current resolution, while coaxial cables are used for high-frequency RF measurements.

3.2 Electrical Characterisation Techniques

3.2.1 Transmission Line Measurements

Before performing in-depth characterisation of a device, it is necessary to quantify key parameters such as the contact resistance. High contact resistances can have a major impact on device performance; a high contact resistance can be the dominant contribution to the transistor's on-resistance, limiting the device's high-power performance. The transmission line measurement (TLM) is a technique used to determine the resistance of a contact pad. The total R_{on} of a device can be modelled by three resistors in series,

$$R_{on} = 2R_M + 2R_C + R_{semi} \tag{3.1}$$

where R_M is the resistance of the metal contacts, R_C is the contact resistance and R_{semi} is the resistance of the semiconductor. The $2R_M$ term can usually be ignored, as the sheet resistance of a metal is typically far smaller than the contact resistance. The resistance of the semiconductor is given by the expression,

$$R_{semi} = \frac{\rho_{semi}}{W} L \tag{3.2}$$

where W and L are the width and length of the semiconductor, and ρ_{semi} is the sheet resistance, with units of Ω/sq . Combining Eqn. 3.1 and Eqn. 3.2 yields the expression,

$$R_{on} = \frac{\rho_{semi}}{W} L + 2R_C. \tag{3.3}$$

Eqn.3.3 provides a simple method by which to determine the contact resistance of a transistor: fabricate a number of contact pads with a variation in their spacing L. The intercept of a plot of R_{semi} vs L will be $2R_C$. It is then straightforward to extract the value of ρ_{semi}, with the gradient of the plot being ρ_{semi}/W.

3.2.2 Current-voltage Characterisation

DC characterisation is the standard way to quantify device performance and reliability. Instruments utilise a source measurement unit (SMU) for this purpose. An SMU can be used as both a voltage source and a current source, with each SMU connected in series with an Ammeter and connected in parallel with a Voltmeter. This configuration allows for the simultaneous application and measurements of a voltage/current. A standard SMU has three output terminals, a force terminal, sense terminal, and a sense low-output terminal. Coupled with the output of a ground terminal, four-point measurements are possible with a single SMU. The resistance of a SMU is high, reducing circuit load when making voltage measurements from high impedance sources. The current resolution and the voltage limits of an SMU varying from instrument to instrument, with current resolutions as low as 10pA, and voltage ratings in excess of 1kV possible. Three instruments were used for the purpose for DC characterisation in the preceding results chapters: a Keithley 4200-SCS SourceMeter; a Keithley 2636B SourceMeter; and a Keithley 2657A High Power System SourceMeter. Below, the current and voltage limits of these instruments are discussed, and the current resolution at 1mA quoted. For a complete overview of the performance of each instrument, consults the relevant data sheets [194][195][196].

The Keithley 4200-SCS SourceMeter has four medium resolution SMUs, with a maximum voltage of 200V and a current resolution as low as 100pA; the current resolution at 1mA is 1nA. Each SMU can be fitted with a 4200-PA (preamp), which increased the current resolution of the instrument to 10fA. However, the addition of the preamp increases the integration time required for each measurement, reducing the time resolution of the measurement. The Keithley 2636B SourceMeter has two medium power SMUs with a maximum operating voltage of 200V, and a maximum current of 0.1A. The maximum current increases to 1.5A for voltages <20V. The time resolution of this instrument is as high as 0.001 number of power line cycles (nplc), where a power line cycle is is the frequency of the mains supply voltage. In the case of a 50Hz supply, this is 20μs. The Keithley 2657A is a single SMU system designed for high-voltage operation. The SMU can apply a maximum voltage of 3kV, with a maximum current of 1mA. Currents as high as 100mA are possible for voltages <100 V. The current resolution at 1mA is 30nA. The time resolution of this instrument is as high as 0.001 nplc, however, this drops to 0.1 nplc at higher voltages.

3.2.3 Pulsed Current-voltage Characterisation

DC IV output characteristics are prone to distortion from both trapping effects and device self-heating. Pulsed IV characterisation is a useful tool for suppressing and investigating these effects. Pulsed measurements involve holding the device in the off-state for an extended period of time, and then pulsing the device briefly into the on-state for the purpose of measurements. The duty cycle of the measurement is define as the ratio of the on-state time to the off-state time. Typical duty cycles used during measurements are between 1% and 0.1%. The applied bias in the on-state

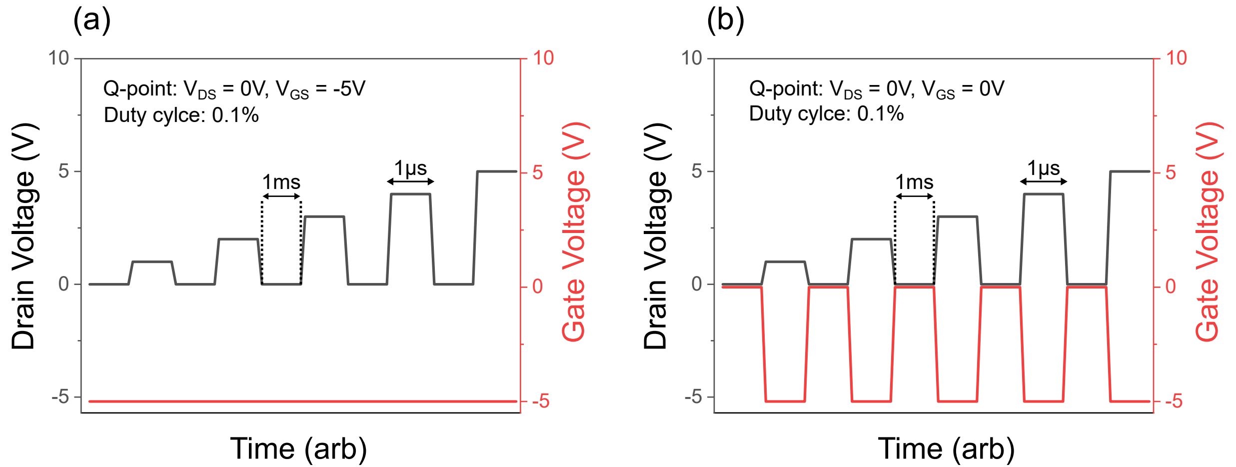


Figure 3.4: Pulse profiles for two pulsed measurements of a single I_D-V_{DS} curve, with a pulsed width of 1μm and a measurement time of 1ms (duty cycle of 0.1%). (a) A measurement with a pulsed drain and a constant bias on gate. (b) A measurement with a pulsed drain and gate.

is referred to the non-quiescent point, or the NQ point, and the bias applied in the off-state is referred to the quiescent point, or the Q-point. Either the gate or drain can be pulsed during a measurement, or both can be pulsed simultaneously.

Fig.3.4(a) shows the voltages used for a pulsed drain measurement, and Fig.3.4(b) the voltages used for a drain and gate pulsed measurement. In both cases, a single I_D-V_{DS} curve is measured, with an NQ gate voltage of -5V. The advantage of the measurement conditions in Fig.3.4(a), when compared to DC characterisation, is that the device spends an insignificant period of time in the on-state. Therefore, device self-heating can often be ignored, and a comparison of the resulting characteristic with the DC case will give quantitative information about its impact on the output characteristics. The underlying assumption here is that device channel does not experience significant heating over the 1μs pulse width. This is material dependent, and the pulse width may need to be modified in different material systems. The drawback of the measurement shown in Fig.3.4(a) is the constant gate voltage. If there are traps close to the gate region, then the applied voltage of -5V will act as stress bias, potentially modifying the device behaviour. Therefore, the measurement shown in Fig.3.4(b) has the added advantage of minimising the impact of trapping on the output characteristics.

When applying a double pulse, some care must be taken to protect the device and the measurement system. Switching both the gate and drain simultaneously can potentially induce large stresses in the device, particularly in the case of power devices with high operating voltages. As such, a pulse delay is normally used, between the gate and the drain pulse, reducing the maximum switching voltage experienced by the device. The stress applied to the device can be further reduced by increasing the rise time of each of the voltages. An example of a double pulsed measurement with a pulse delay is shown in Fig.3.5. The voltage and current in both the NQ

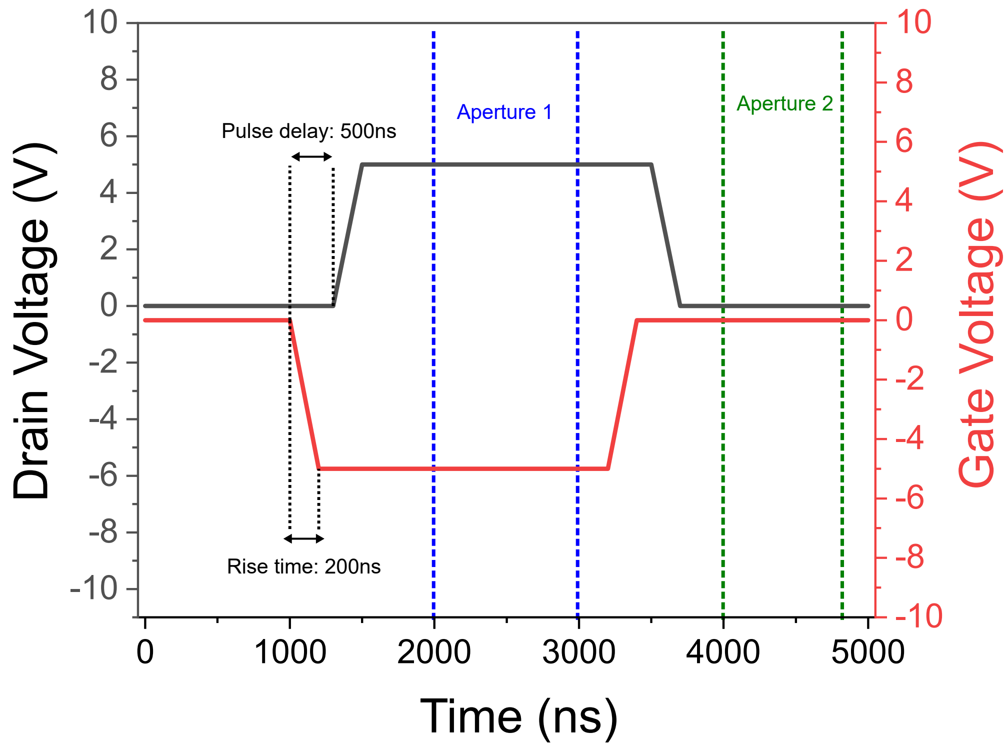


Figure 3.5: A profile of a single pulse period, with a 2μs pulse applied to both the gate and drain. A rise time and pulse delay are specified in the measurement configuration. The integration period used to measure the NQ and Q characteristics are defined by apertures 1 and 2 respectively.

and Q state are measured using an ammeter and a voltmeter, with an integration over some time period. The integration periods are defined by apertures 1 and 2. The width and position of these apertures is determined by the pulse profile: they should be sufficiently far from the edge of either pulse, so that any noise/ringing in the current and voltage at the pulse edge does not affect the measurement.

The presence of trapping in a device, and possible trap state locations, can be explored using different Q biases during a pulsed IV characterisation. An example of such a measurement is shown in Fig.3.6. Two characterisations are performed, one with a Q gate stress of V_{GS} = -40V, and one with a Q gate-drain stress of V_{GS} = -40V, V_{DS} = 40V. The bias stresses will modify the charge state of traps in the device structure, manifesting as changes in the output characteristics. The gate-stress in Fig.3.6 exhibit no significant changes in the I_D-V_{DS} of the device, when compared to the unstressed condition. However, a drop in the drain current is consistently observed after applying a gate-drain stress. This suggests that trapping states are present in the device. To comment on the trapping state location, an understanding of the field/voltage distribution across the device, for both Q conditions, is required. The approach is the same for I_D-V_{GS} characterisation,

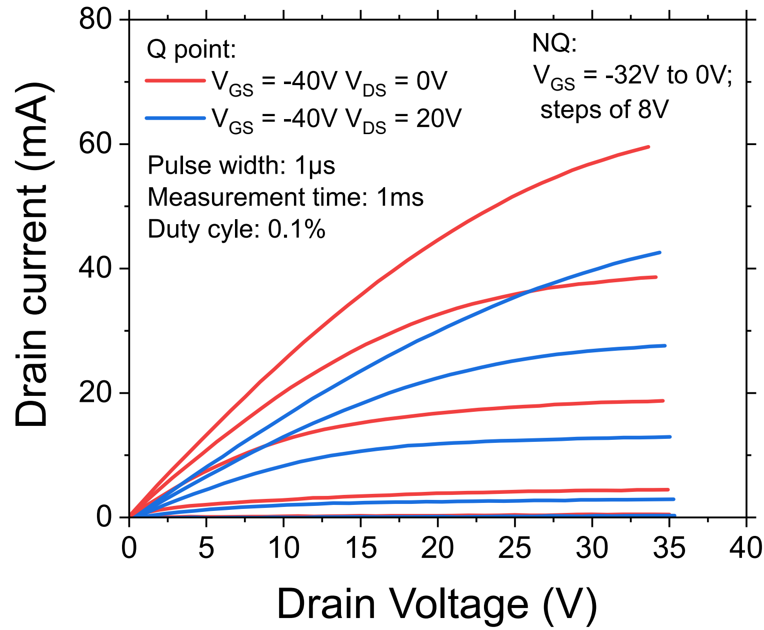


Figure 3.6: Two pulsed I_D-V_{DS} characterisations, with different Q point biases. Comparing a gate stress condition with a gate-drain stress condition can be used to infer the presence of trapping in the device, and to comment on the possible trap state locations.

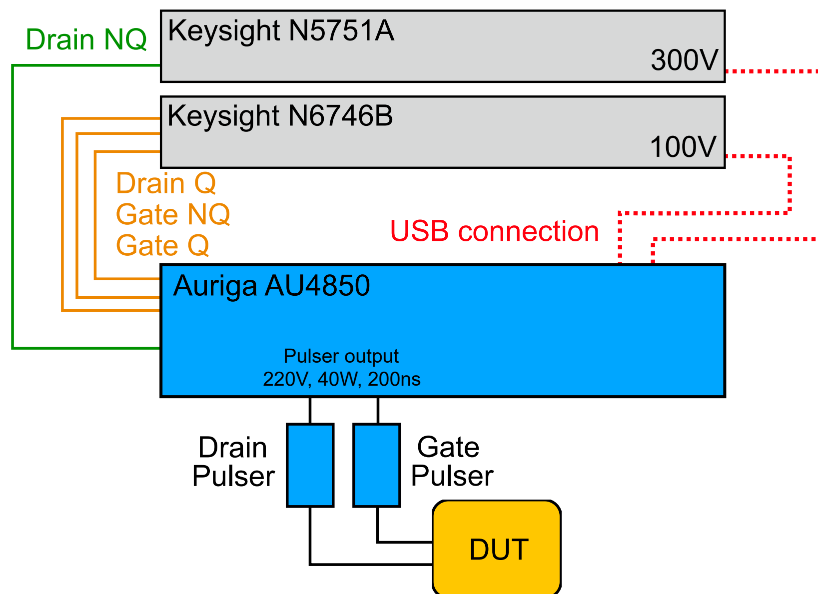


Figure 3.7: A schematic of the system used to perform pulsed IV characterisation. Two power supplies were used to apply voltages, controlled by the Auriga AU4850. Pulse widths as small as 200ns were achieved using a model PHD1020 pulser head on the drain, and a model PHG2020 pulser head of the gate.

with shifts in V_{th} indicating the presence of gate region trapping. Stressed-pulsed measurements are a standard tool for accessing device performance and reliability.
Fig.3.7 shows the measurement configuration used to achieve gate and drain pulsed measurements. The pulsed voltages are controlled using an Auriga AU4850 system [197]. This system controls four external power supplies via USB connections: three Keysight N6746B 100V DC supplies [198] and a Keysight N5751A 300V DC supply [199]. The N5751A supply is used to provide the drain NQ bias, while the other three supplies are used to provide the drain Q bias, the gate NQ bias and the gate Q bias. The Auriga AU4850 is connected to a gate pulser head and a drain pulser head. Each of these pulser heads controls both the NQ and the Q bias of their respective terminals. The pulsers limits the drain NQ bias to 200V, and the the other biases to 40V. Pulse widths as small as 200ns are achievable, with powers as high as 40W. The pulsed biases output of each pulser head are connected directly to the device under test (DUT) via SMA connectors and GSG probe tips.

3.2.4 Capacitance-voltage Characterisation

Capacitance-voltage (CV) measurements are a standard characterisation technique used to extract key material parameters from low leakage structures, such as MOS-CAPs. During a typical CV measurement a DC bias sweep is applied to a contact pad that is electrically isolated from the semiconductor (e.g. the gate), in order to transition the device from accumulation into depletion. A small amplitude AC signal is superimposed with the DC sweep voltage, as shown in Fig.3.8. The AC signal is used to extract a value of capacitance at each step of the DC voltage sweep. This is achieved by measuring any transmitted AC current and AC voltage at a second contact pad (e.g. the drain). Modelling the gate as a leaky capacitor, (using the circuit diagram in Fig.3.8), allows for the extraction the device capacitance. The relationship between the capacitance of the device (C_{DUT}) and the AC current (I_{AC}) of the leaky capacitor is given by the following expression:

$$C_{DUT} = \frac{I_{AC}}{2\pi f V_{AC}}, \tag{3.4}$$

were f is the frequency of the AC signal and V_{AC} is the real and imaginary components of the AC voltage. A measurement of the AC current and AC voltage amplitudes, with the relative phase between the two signals, is sufficient to extract the device capacitance.
The Keithley 4200 SCS SourceMeter was used for CV measurements in subsequent chapters, using a 4200 CVU. A standard CV unit (CVU) has four output terminals: a current low terminal; a current high terminal; a voltage low terminal and a voltage high terminal. The two high terminals and the two low terminals are shorted as close as possible to the device, usually at the probe tip connectors. The high terminal connectors are used to apply the DC and AC biases, and the low terminals are used to measured the transmitted AC signal. The available frequency range of this CVU is 1kHz-10MHz, although frequencies <100kHz are prone to noise. The 4200 CVU is compatible with a range of bias tees: a 3-port circuit that allows for the coupling/decoupling of a

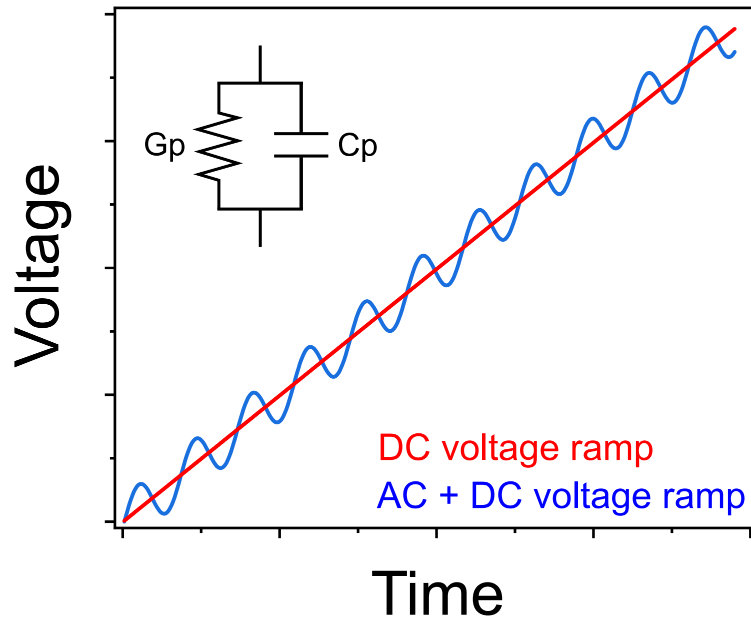


Figure 3.8: The AC and DC voltages applied during a capacitance-voltage measurement. Inset: the circuit model of a leaky capacitor, with a parallel capacitance and a conductance.

DC voltage and an AC voltage. Bias tees can be used to enhance the maximum available voltage during a CV measurement by mixing the AC signal of the CVU with an external DC voltage. The maximum DC voltage that can be applied using a 4200 CVU is 30V, whereas a Keithley 4200 SMU with the CVU and a suitable bias tee allows for a maximum DC voltage of 210V. DC voltages of 3kV can be achieved during a CV measurement by using a suitable high-voltage bias tee with a Keithley 2657A SMU.

3.2.5 Cryogenic Measurements

Many electrical characterisation techniques benefit from access to cryogenic temperatures. Measuring samples at cryogenic temperatures requires a thermally stable, low-pressure environment, which can support a combination of different measurement systems. This was achieved in subsequent chapters using the cryogenic probe station shown in Fig.3.9. This system consists of two chambers: an inner sample chamber and an outer cooling chamber. Samples loaded into the inner chamber can be probed using a combination of four DC probe tips and two RF tips. All tips were electrically connected to external arms with coaxial and triaxial connectors. Liquid nitrogen enters the outer chamber from a dewar via an inlet, cooling the sample in the inner chamber. The temperature of a sample is controlled using a heated baseplate at the bottom of the the inner chamber. The temperature of the baseplate was set using an external PID controller (LakeShore

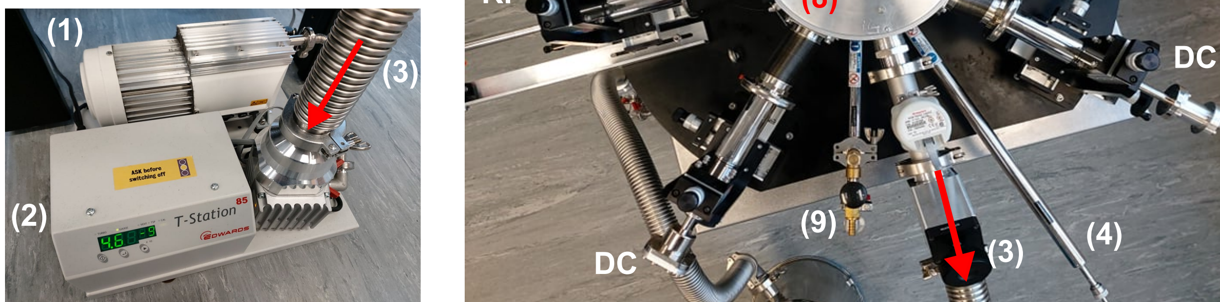


Figure 3.9: The cryogenic probe station used for low-temperature measurements. A high-pressure and low-pressure oil pump are used to evacuate the sample chamber. The samples are cooled using liquid nitrogen, and the temperature is controlled using a thermal base-plate with a PID controller. The sample is loaded into the chamber, and probed using a combination of the four available DC probe arms and the available RF probe arms.

Model 336 Temperature Controller). Both chambers were evacuated using an Edwards T-Station 85 pump system, consisting of high-pressure an oil sealed backing pump and a low pressure nEXT85H turbomolecular pump. This system is capable of achieving pressures as low as 5x10^{-10} mbar, critical for ensuring that there is no residual moisture in the system that could freeze/short contacts at low temperatures.

3.3 Raman Spectroscopy

All thermal measurements were performed using a Renishaw InVia Raman spectrometer. A schematic of the spectrometer is shown in Fig.3.10. A 532nm diode laser is used alongside the spectrometer for the purpose of measurements. The laser beam was first passed through a selectable neutral density filter, in order to attenuate the laser power to a desirable level. Upon entering the spectrometer, the laser is directed to a beam expander by a beam steering mirror. The beam expander consists of two lenses positioned so that their focal points coincide. The beam expander ensures that the laser remains collimated, and increases the diameter of the laser beam.

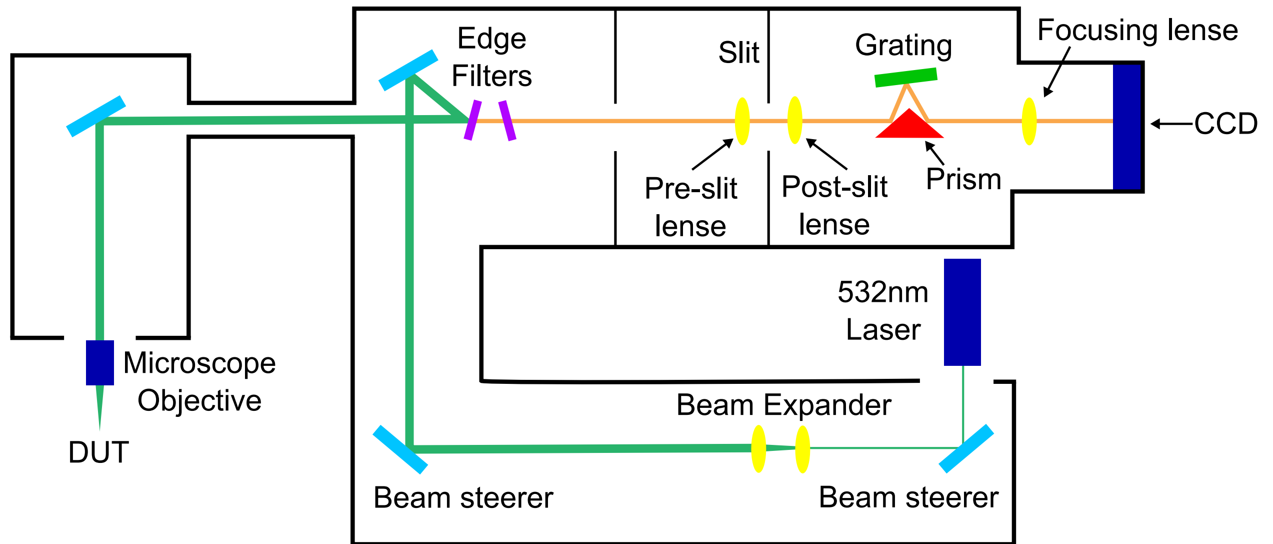


Figure 3.10: A schematic of the Renishaw InVia Raman spectrometer used for thermal measurements. An external 532nm diode laser is passed through the spectrometer to a microscope objective, that focuses the laser onto the device under test (DUT). A CCD camera is used to record the resulting spectra.

This is necessary to ensure that the laser fills the back aperture of the microscope objective lens. Filling of the back aperture ensures that the spot size is minimised on the device, increasing the spatial resolution of the measurement. A second beam steering mirror is then used to direct the laser beam to a edge filter, via a cylindrical lens used to reduce the power density of the laser. The purpose of this edge filter is to reflect wavelengths of light below a cut-off value, while allowing the rest to pass with a high optical efficiency. The edge filter cut-off wavelength was set to the wavelength of the laser diode. The beam is reflected by this filter into a Leica DMLM confocal microscope where is focused onto the device under test (DUT) via a Nikon x50 objective lens, with a numerical aperture NA of 0.5.

Backscattered light from the DUT, consisting of the Raman signal and the reflected laser beam, then passes through the objective lens and into the spectrometer. When this light reaches the edge filter, the laser signal (532nm) is reflected, leaving just the Raman signal. The signal is then focused, using a pre-slit lens, onto a slit with adjustable width. The purpose of this slit is to block any divergent ambient light that originates from outside of the system. The slit can also be used to reduce spectral broadening of the signal, with a narrower slit leading to a decrease in the broadening. The slit width was typically set to 50μm during measurements. A post-slit lens is then used to collimate the beam and direct it towards a prism, which reflects the light onto a grating. The purpose of this grating is to spatially disperse the light, so that different wavelengths can be distinguished. The grating consists of a surface with ridges, with a with a line density of 2400 lines/mm. For a grating with ridges separated by a distance of d, constructive

interference occurs when the Bragg condition is satisfied,

$$\lambda = dsin(\theta), \tag{3.5}$$

where θ is the angle of of the dispersed light, and λ is the wavelength of the light. The beam reflected by the grating becomes spatially dispersed with respect to wavelength. A greater dispersion is achieved with a smaller value of d. This will lead to a greater spectral resolution, but also a corresponding smaller spectral window. The grating is motorised, and can be rotated with respect to the beam, helping to achieve the full spectral range of the system. The dispersed light from the grating is reflected into a lens and focused onto a CCD. Each pixel position is converted into a frequency, based on the dispersion of the grating. The spatial mapping of wavelengths onto pixels has to be calibrated before measurements. This is done using a Silicon calibration wafer, with reference to the wavelength of the 520.3 cm^{-1} spectral line.
During measurements, the DUT was biased using a 2636B Keithley sourcemeter, with tungsten DC tips. By controlling the voltage and current, the desired power dissipation was achieved. Thermal measurements require the substrate of the device to be thermally grounded. A thermo-electrical vaccum chuck, situated directly below the microscope, was used to hold the bottom of sample substrates at a fixed temperature. The position of the device throughout the measurement was controlled using a piezoelectric positioner.
The spatial resolution of the Raman measurement is determined by the resolution of the confocal microscope objective used. The lens focuses the leaser beam to a single spot, with the lateral full-width half maxima ($FWHM_{lat}$) of the beam given by the expression [200],

$$FWHM_{lat} = \frac{0.51\lambda_{laser}}{NA} \tag{3.6}$$

where λ_{laser} is the wavelength of the laser. The axial resolution, or the depth resolution, is given by the expression,

$$FWHM_{axial} = \frac{0.88\lambda_{laser}}{(n - \sqrt{n^2 - NA^2})}, \tag{3.7}$$

where n is the refractive index of the transparent sample.

3.4 Simulations

3.4.1 Silvaco ATLAS

Simulating the electrical characteristics of a device is often necessary to corroborate experimental results. A detailed understanding of the voltage scaling of fields is of particular use in the following chapters. The simulations presented throughout this thesis were implemented using Silvaco ATLAS, a drift-diffusion simulator developed for semiconductor devices. Fundamentally, ATLAS outputs both electrostatic field distributions, and electron transport properties, by solving three sets of equations; the Poisson equation, the carrier continuity equations, and the transport

equations. The Poisson equation is sufficient to obtain static field solutions, in the absence of current,

$$\nabla\phi = \frac{\rho}{\epsilon}, \tag{3.8}$$

where ϕ is the electrostatic potential and ρ is the charge density. To understand the dynamic behaviour in device, e.g. on-state currents, the continuity equations are required:

$$\frac{\partial n}{\partial t} = \frac{1}{q}\nabla\vec{J}_n + G_n - R_n, \tag{3.9}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\vec{J}_p + G_p - R_p. \tag{3.10}$$

Eqn.3.9 is the electron continuity equation, where q is the electron charge, n is the electron density, $\vec{J}_n$ is the electron current density, G_n is the generation rate of electrons and R_n is the electron recombination rate. Eqn.3.10 is the hole continuity equation, with all terms corresponding to those of Eqn.3.9. In order to simulate devices, two transport equations are required to define the terms J_n and J_p, with additional physical models required for G_n, G_p, R_n and R_p. Using the drift diffusion model for the current densities, the drift-diffusion equations can be obtained,

$$\vec{J}_n = qn\mu_n\vec{E}_n + qD_n\nabla n, \tag{3.11}$$

$$\vec{J}_p = qn\mu_p\vec{E}_p - qD_p\nabla p, \tag{3.12}$$

where D_n and D_p are diffusion coefficients and E_n and E_p are the electric fields experienced by both sets of carriers.

Eqn.3.11 and Eqn.3.12 are solved for a 2D cross-section of a device using a predefined mesh. This mesh consists of a grid of triangles, with sizes and aspects ratios that vary based on the local geometry of the 2D cross-section. The numerical convergence of the simulator, and the validity of the output results, relies on the quality of the mesh. Ideally, a high density mesh would be used across the structure, to avoid any potential boundary problems between materials, (resulting from large changes in mesh density). However, this is computationally expensive, and often not practical. Therefore, it makes sense to define a mesh in which the point density is highest in regions with large field gradients, and lowest in regions where the field is approximately constant. For example, a planar interface in a vertical device, (with a periodic boundary condition), will have a constant lateral field. As such, the vertical mesh point density is more critical than the lateral mesh point density. An example of a vertical structure with a typical mesh overlaid is shown in Fig.3.11(a). Here, each region has a set of mesh constraints (maximum triangle height, width and aspect ratio) with areas of high mesh density corresponding to transition regions between two different meshes.

In the case of β-Ga_2O_3 devices, where high-voltage operation is desirable, high field gradients can cause problems with numerical convergence. A prior knowledge of the field distribution in a device would allow for high mesh densities in the critical areas of the device. This is not always

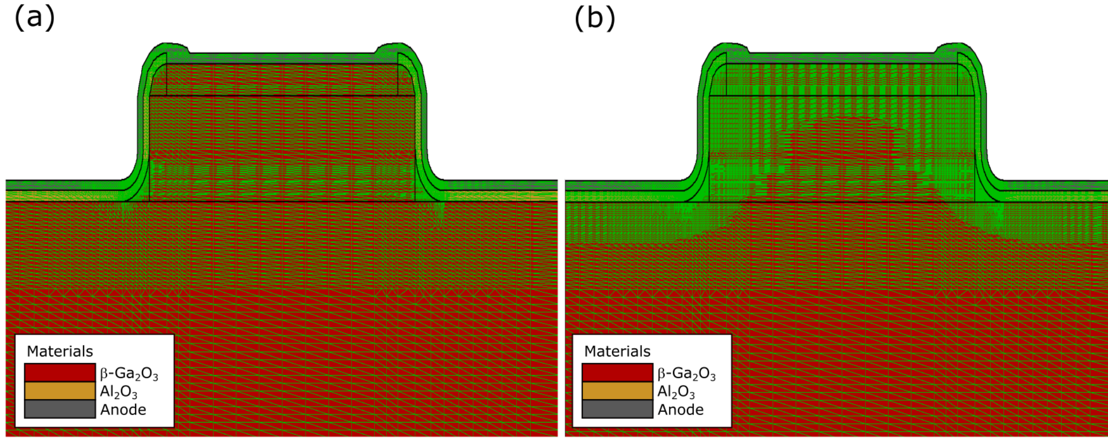


Figure 3.11: (a) Example of a device mesh used for a device simulations in Silvaco ATLAS. (b) The same structure shown in (a), but with the mesh rebuilt so that regions of high field gradient have a corresponding high mesh point density.

achievable with the simple mesh constraints. Instead, a low-field simulation can be performed on the device, and the mesh rebuilt using the outputted field-distribution. The regions with the highest field gradient in the low field simulation will be meshed with a higher density of points. Such a mesh will then be suitable over a large range of voltages and fields. An example of a mesh rebuild, performed on the mesh in Fig.3.11(a), is shown in Fig.3.11(b).

A selection of common of materials are native to ATLAS, with their material parameters well defined. However, implementing simulations of β-G_2O_3 devices presents two major problems. The first, common to all wide-bandgap materials, is the extremely low intrinsic carrier concentration (n_i) at room temperature. Eqn.3.13 gives the expression for n_i,

$$n_i = N_s \exp\left(\frac{-E_g}{2k_B T}\right), \tag{3.13}$$

where N_s is the number of available states per unit volume. The approximate value of n_i for Si at room temperature is 1.5x10^{10}cm^{-3}, [180]. Due to the exponential dependence of n_i on E_g, this value falls to 1.06x10^{-10} cm^{-3} for SiC, and to 1.79x10^{-22} cm^{-3} for β-Ga_2O_3. The small intrinsic carrier concentration introduces convergence problems primarily into low-current simulations.

The absence of mobile holes in β-Ga_2O_3 also needs to be considered carefully when performing electrical simulations. When recombination physics was not required, holes were suppressed during simulations. In simulations where this was not possible, the mobility of holes was set to a low value (<0.1 cm^{2}V^{-1}), and transient ramped simulations were performed. Transient ramping consists of ramping the device biases over a defined time step. A sufficiently small time step was chosen, so that the device did not reach equilibrium: electron redistribution was observed, but not the redistribution of low-mobility holes. This approach successfully models the self-trapped holes in β-Ga_2O_3.

ATLAS can be used to evaluate the internal heat generation of a device under bias. It considers Joule heating due to the flow of current, cooling due to carrier generation and recombination, along with the Peltier effect and the Thompson effect. To achieve this ATLAS uses a differential equation to model the heat flow in the lattice. The change in lattice temperature (T_L) with time is given by,

$$\rho C_p = \frac{\partial T_L}{\partial t} = \nabla(\kappa \nabla T_L) + H, \tag{3.14}$$

where ρ is the density of the material, C_p is the specific heat capacity, κ is the thermal conductivity and H is the internal heat generation. The form of H is dependent on the models for channel heating and cooling implemented in the simulation.

3.4.2 ANSYS

ANSYS is a finite element simulator used to extract 3D temperature profiles of devices under bias. This software allows for both steady state and transient simulations of temperature distributions. It also provides information about the heat flux in the device, e.g. from the channel into the contact pads. Simulations in ANSYS can be coupled with those of ATLAS; internal heat generation profiles in the channel from Silvaco ATLAS loaded directly into an ANSYS model. Models in ANSYS output channel temperature profiles, calculated using internal heat generation profiles, and by considering the diffusion of heat. The first law of thermodynamics can be expressed in the form,

$$\rho C_p \left(\frac{\partial T}{\partial t} + \vec{v} \nabla T \right) + \nabla . \vec{q} = U, \tag{3.15}$$

where $\vec{v}$ is the heat velocity vector, $\vec{q}$ is the heat flux vector and U is the internal heat generation density. ANSYS solves this equation by modelling $\vec{q}$ with Fourier's law,

$$\vec{q} = -k_{ij} \nabla T, \tag{3.16}$$

where k_{ij} is the thermal conductivity tensor. Combining Eqn.3.15 and Eqn.3.16 yields,

$$\rho C_p \left(\frac{\partial T}{\partial t} + \vec{v} \nabla T \right) = \nabla . (k_{ij} \nabla T) + U \tag{3.17}$$

Eqn.3.15 simplifies to the Boltzmann heat transport equation in the case of steady-state thermal simulations, with the full form of Eqn.3.17 only being used in the case of transient thermal simulations. The time differential term represents the rate of heat storage in a material. The specific heat capacity is a temperature dependent parameter; modelling this temperature dependence is required for transient thermal simulations. For simulations in subsequent chapters, the Deybe model of heat capacity is used. This model assumes that the specific heat of the material is dominated by the phonon heat capacity [201]. Einstein proposed a similar model, assuming that all available vibrational modes had the same frequency. The Deybe model, however, assumes a continuous distribution of mode frequencies, with a maximum cut-off frequency of v_D [202]. The

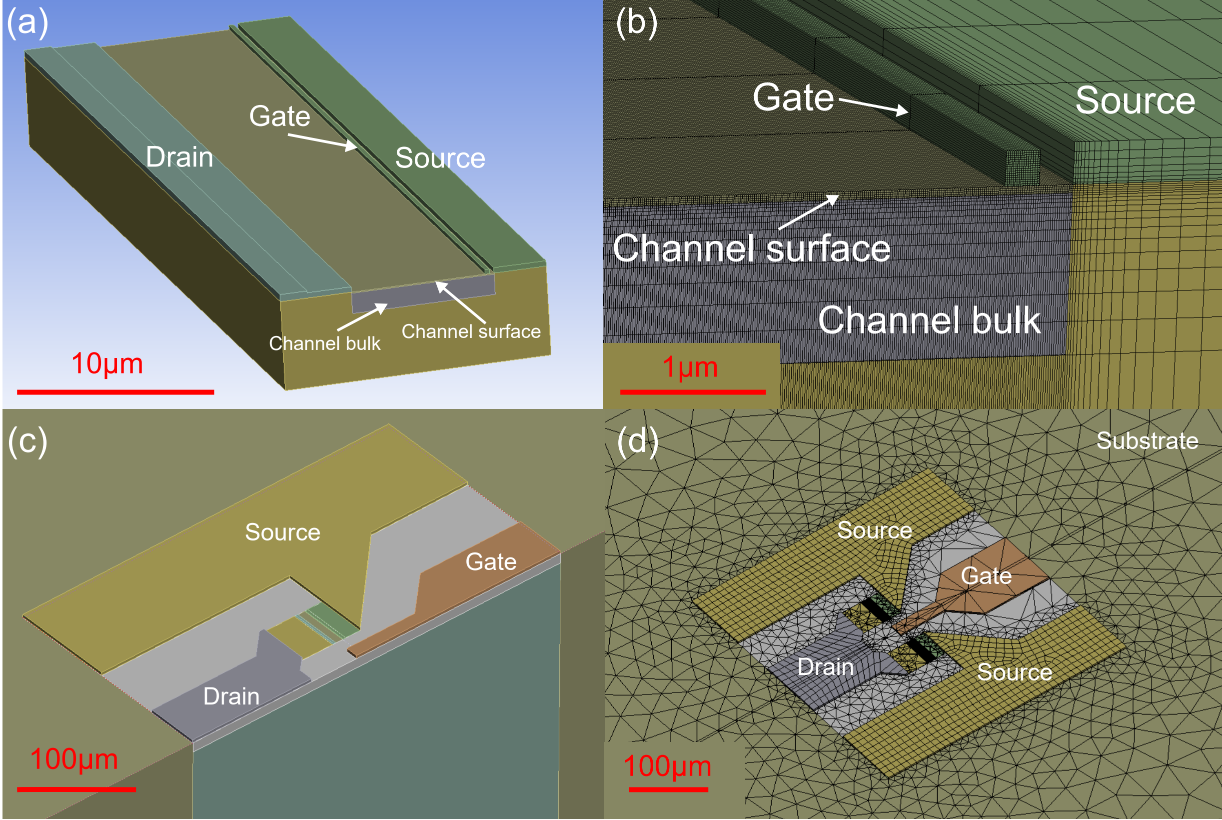


Figure 3.12: (a) A device channel constructed using TCAD software. The channel is divided into two parts, the channel bulk and the channel surface. This allows for different mesh densities over the channel region. (b) Part of the channel region with the mesh overlaid. (c) Half of a transistor constructed using TCAD software. A mirror boundary condition is applied at the plane intersecting the gate and drain contact pads. (d) Mesh overlaid on the full device.

Deybe heat capacity (C_D) is given by the following expression [203],

$$C_D = 9Nk\left(\frac{T}{\theta_D}\right)\int_0^{\theta_D/T}\frac{x^4e^x}{(e^x-1)^2}dx, \tag{3.18}$$

where x = $h\upsilon/kT$, N is the number of atoms in the system and θ_D is the Deybe temperature, given by the expression:

$$\theta_D = \frac{h\upsilon_D}{k}. \tag{3.19}$$

For temperatures $T << \theta_D$, Eqn.3.18 simplifies to [204],

$$C_D = \frac{12\pi^4}{5}Nk\left(\frac{T}{\theta_D}\right)^3. \tag{3.20}$$

ANSYS solves the full or simplified form of Eqn.3.17 numerically using a finite element scheme. In all simulations, the heat capacity, thermal conductivity tensor, and the density of all materials

in the device must be defined. Then, with the internal heat generation profile loaded into the model, the temperature profile of the device can be simulated by solving Eqn.3.17 over a defined mesh. Fig.3.12 shows a typical 3D device structure and mesh. The device structure is constructed using TCAD software, with an example of a device channel shown in Fig.3.12(a). It is useful to separate the device channel into several sections, e.g. channel bulk and channel surface, for the purpose of implementing different mesh densities (see Fig.3.12(b)). Fig.3.12(c) shows half of the transistor constructed in TCAD. A mirror condition is applied on the cut-plane intersecting the gate and drain metal pads. The corresponding mesh is shown in Fig.3.12(d), with the mesh density progressively reduced as the feature sizes increase. The mesh shown in both Fig.3.12(b) and Fig.3.12(d) exhibit both rectangular grids and tetragonal grids. Rectangular grids are preferred where large heat gradients are expected, as they have a higher mesh point density. However, they cannot be mapped arbitrarily onto any three dimensional surface, unlike tetragonal meshes. These tetragonal meshes are preferred where smaller temperature gradients are expected, as they allow for the smooth transition between different mesh densities.

Chapter 4

Breakdown Mechanisms in β-Ga_2O_3 Trench-MOS Schottky-barrier Diodes

A promising device architecture for β-Ga_2O_3 power applications is the trench-MOS Schottky-barrier diode (SBD). This structure exploits the reduced-surface field (RESURF) effect to enhance its breakdown voltage and reduce its reverse bias leakage current. While previous work has identified the primary failure point of these diodes, less work has been done to understand dynamic changes in their dominant leakage mechanism under reverse bias stress. This chapter utilises a novel noise analysis method, outlined by Dalcanale *et al.*, to analyse the leakage currents of a set of β-Ga_2O_3 trench-MOS SBDs, as a function of reverse bias stress [41]. Device test structures were used to characterise potential leakage paths in the trench-MOS SBD structure, and to investigated transitions in the dominant leakage path. The devices used in this study were fabricated by our collaborators at the Department of Materials Science and Engineering, Cornell University (USA). The noise analysis in this chapter is published in IEEE Transactions on Electron Devices; a significant amount of this chapter's content has been reproduced from this publication [38].

4.1 Introduction

One area in which β-Ga_2O_3's high breakdown field is easily exploitable is the fabrication of vertical diodes. Such devices combine a high off-state blocking voltages with low-leakage currents. Vertical devices also avoid some of the design problems presented by lateral devices; increasing breakdown voltages in lateral devices requires a larger device footprint on the substrate. Vertical β-Ga_2O_3 devices offer a path to realising high current densities, with breakdown voltages higher than that of competing wide-bandgap semiconductors.

As a unipolar semiconductor, β-Ga$_2$O$_3$ based pn diodes are not achievable. Integration of n-type Ga$_2$O$_3$ with a suitable p-type oxide has been previously used to demonstrate a pn diode structure [205]. However, this usually requires the metastable α-phase, as few stable oxides share the β-phase's monoclinic structure, and introduces the problem of heterojunction quality. Alternatively, fabrication of β-Ga$_2$O$_3$ Schottky barrier diodes (SBD) offers a path to high-voltage diodes. Planar SBDs with average breakdown fields at the Schottky barrier (SB) of 5.7 MV/cm and corner fields as high as 7MV/cm have been reported previously [206]. However, the planar diode architecture intrinsically limits the maximum operating voltage of such devices; for a fixed doping, the breakdown of a planar structure will be determined by interface field, between a metal anode and the semiconductor (see section.2.2.4).

To circumvent the intrinsic field-handling limit of β-Ga$_2$O$_3$, reduced surface electric field (RESURF) techniques have been successfully applied. Li *et al.* [207][208] have demonstrated the fabrication and enhanced breakdown voltages of the trench-MOS Schottky-barrier diode (SBD) architecture. The trench diode structure utilises a fin structure, with a SB interface at the top of the fin, and a side-wall anode, separated from the fin via an oxide layer. The side-wall anode leads to field clamping within the fin, effectively pinning the interface field at a lower value than would be expected from the interface voltage. The peak fields in the structure are shifted from the Schottky-barrier (SB) interface to the oxide layer, as discussed in section.2.2.4. This has the effect of enhancing the breakdown voltage of the diode, while the reduced surface field helps to reduce the leakage current over the SB interface. Reverse leakage currents can also suppressed by tuning the SB barrier height to a larger value, using different alloys for the anode metal [209]. Trench-MOS β-Ga$_2$O$_3$ SBDs with breakdown voltages as high as 2.44 kV have been previously reported [33]. Field-plates have been demonstrated to reduce field crowding at the device edges; field-plates have been reported to have enhanced the breakdown voltage of a device by approximately 500V [99].

Failure points of trench-MOS diode structures are well understood under bias-swept conditions [33]. However, it is critical to understand how off-state leakage mechanisms evolve under elevated bias stress, as this more accurately mirrors the real-world operation of these devices. In this work, a transition between two distinct leakage mechanisms in a trench-MOS diode, during step-stressed breakdown measurements, is demonstrated. Analysis of the current noise during step-stressed measurements indicates that a leakage across the SB dominates at low-bias. A transition to leakage through the trench-MOS dielectric is observed at higher voltages. Breakdown of these devices is attributed to a degradation of this dielectric layer.

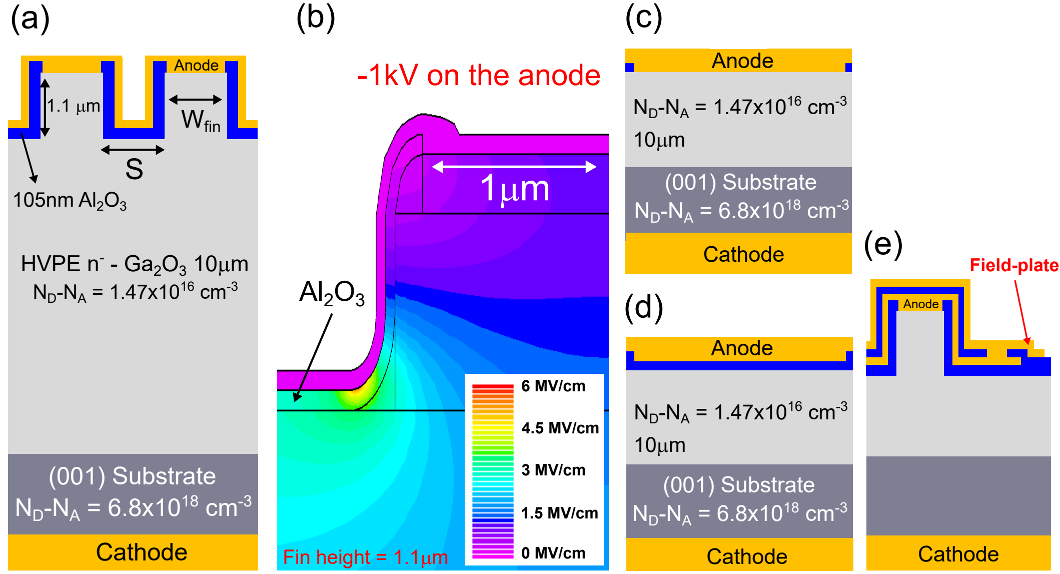


Figure 4.1: (a) Schematic of trench-MOS β-Ga_2O_3 SBDs, with 10µm drift region, and fin width and separation as indicated. (b) Field distribution of a diode oxide corner with -1kV applied to the anode. Peak fields observed at bottom of trench, in the oxide corners. (c) Field-plated Planar SBD, and (d) field-plated MOS-CAP structures. (e) Edge-termination of the trench diode structure, shown in (a). Figure reproduced from [38].

4.2 Experimental Details

4.2.1 Devices

Trench-MOS β-Ga_2O_3 SBDs were studied with fin widths (W_{fin}) and separations (S) ranging from 1µm to 4µm, with a fin height of 1.1 µm and a drift region of 10µm thickness, as shown schematically in Fig.4.1(a). The diode trenches are lined with a 105nm ALD Al_2O_3 layer. A Ti/Au layer at the bottom of the substrate formed a cathode, while a Ni anode was deposited across the fin tops and conformally coated across the oxide in the trenches. A detailed description of the device fabrication can be found in Li *et al.* [33]. The presence of the sidewall metal achieves a RESURF effect within the fins. This RESURF effect is demonstrated by the TCAD simulation shown in Fig.4.2(b), simulated using silvaco ATLAS; the peak field is shifted from the metal-semiconductor interface at the top of the fin to the oxide coated fin corners. The peak fields at the oxide corners will be dependent on the precise geometry of the trench-bottom corners. The radius of curvature used for the trench bottom corners in this simulation were extracted from the FIB cross-section of a device with 1μm fin widths is shown in Fig.4.2(a). A simplistic assumption of 90° terminated corners in the simulation will lead to an overestimate of the peak oxide fields, as will be shown in section.4.3.1. The radius of curvature for the trench corners was set to 200nm for all simulations in this chapter.

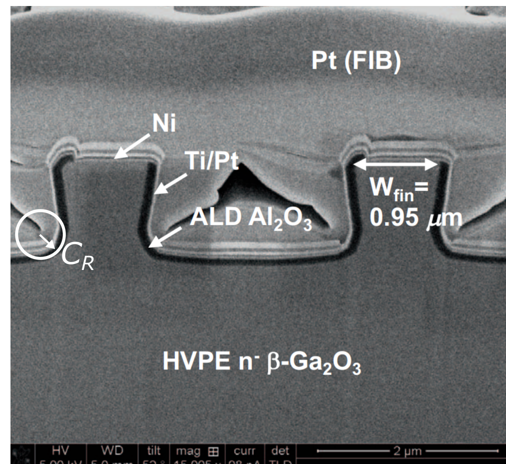


Figure 4.2: FIB cross-section of a diode with a fin width of approximately 1μm. The trench bottom oxide corners are used to extract a radius of curvature for the structure, C_R. Figure reproduced from [33].

The trench-MOS structure can be decomposed into three constituent components, the oxide, the SB interface and the edge-terminated field-plate. The principle structures of interest were the field-plated planar Schottky-barrier (SB) structure, (Fig.4.1(c)), for investigating the SB interface, and the field-plated MOS-CAP structure, (Fig.4.1(d)), for investigating the oxide layers. The field-plated edge-termination of the device is shown in Fig.4.1(e). Non-field-plated structures were not systematically used, due to poor device quality.

4.2.2 Measurement Configuration

In order to investigate the breakdown mechanisms of the trench diodes, two distinct measurement techniques were used. Initially, the breakdown voltages of different trench geometries were investigated using voltage sweep measurements. In these measurements, the back-side cathode was grounded, and the anode was swept from 0V to breakdown for various voltage sweep rates, (between 1 V/s and 10 V/s). These sweep measurements provided a value for the diode breakdown voltage, but little information about the in situ leakage and degradation of the diodes leading up to breakdown. This is as current resolution was limited by the voltage sweep rate of the system; parasitic capacitances lead to displacement currents in the system proportional to the sweep rate. To extract useful information concerning the device degradation under bias stress, voltage step-stressed measurements were performed. In these measurements, a constant anode bias was applied for a period of 120s. The anode bias was then ramped to a new bias, and held there for another 120s. This procedure was repeated for steps of -50V, from 0V up until device breakdown. The voltage ramp between each bias step used a ramp rate of -0.5 V/s for a period of 100s. This slow ramp between voltage steps was found to be essential for avoiding the premature breakdown of the device, with the breakdown voltage limited to a few hundred volts in the case of the

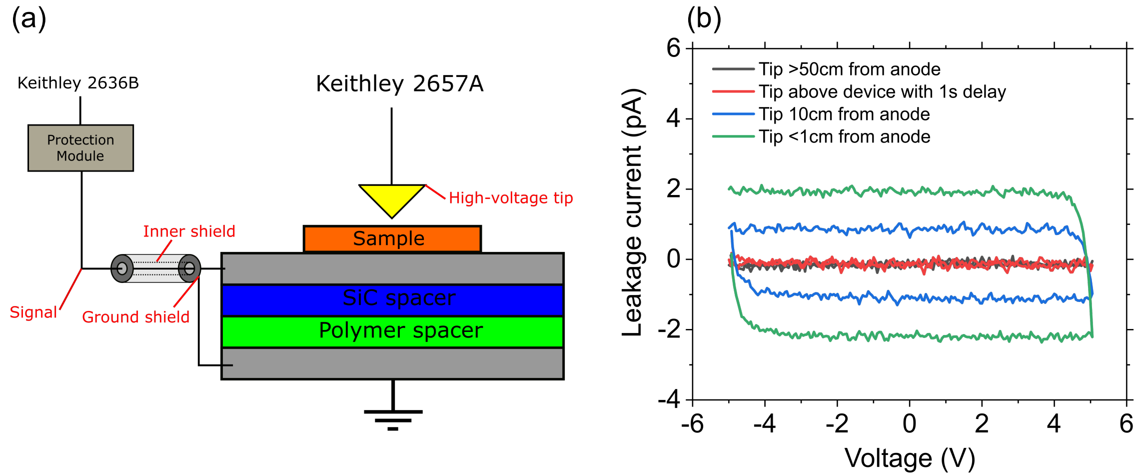


Figure 4.3: (a) Schematic of the measurement configuration used to measure diode leakage currents. Triaxial cables connected a metal chuck and the anode direclty to a Keithley 2636B and a Keithley 2657A, respectively. (b) The noise resolution of the system for various measurement conditions.

stepped-measurement without ramping. For the duration of each voltage step, (with a constant bias on the anode), the leakage current through the cathode was sampled at a frequency of approximately 26 Hz.

Both the voltage sweep breakdown measurements and the voltage step-stressed measurements were performed using the same measurement configuration, as shown in Fig.4.3(a). In this configuration, two Keithley instruments were required. A Keithley 2657A 3kV source meter was used to apply high biases to the anode, while a Keithley 2636B source meter was used to achieve high-frequency/resolution measurements of the diode leakage current. The Keithley 2657A 3kV source meter was connected directly to the top-side anode using a tungsten probe tip. The Keithley 2636B source meter was indirectly connected to the back-side cathode of the sample via a layered chuck. The reason for holding the cathode at a fixed voltage, as opposed to the anode, was that the large area cathode chuck had larger associated parasitic capacitances than the anode probe tip. The Keithley 2636B source meter was used for the current measurements as it has a higher sampling rate and current resolution than the Keithley 2657A 3kV source meter. The cathode chuck consisted of two grounded metal plates, separated using a SiC spacer plate, and a polymer spacer plate. The top plate of the chuck, (in contact with the sample cathode), was used to directly measure the leakage current over the cathode. The bottom plate was in contact with the probe station chuck. The purpose of the plastic spacer and the SiC plate was electrically isolate the top plate from the probe station.

The Keithley 2636B source meter was connected to the cathode chuck via a modified triaxial cable. The triaxial cable ran from the 2636B SMU to a protection module. The purpose of this module was to protect the 2636B source meter from any transient spikes in current, following a

breakdown event. Breakdown of a diode leads to an effective current-short across the sample, exposing the 2636B source meter to voltages and currents outside of its safe operating range. The protection module was then connect via a triaxial cable to the chuck. To connect the cable directly to the chuck, the signal, inner guard and the outer guard of the cable were separated. The inner guard was connect to the lower metal plate, while the signal was connect to the upper metal plate, (in contact with the cathode). This configuration ensures that both plates are held at the same bias, reducing the parasitic capacitance over the chuck.
The current resolution of Keithley 2636B source meter is as low as 1fA. However, in practice, this is not achievable due to noise and interference from other components in the system. These included parasitic displacement currents in the chuck, capacitive coupling between the high-voltage tip and the chuck, background noise in the protection module and exposure of the unprotected signal cable to external sources of interference. The effect of some of these sources of noise on the system resolution is shown in Fig.4.3(b). It is apparent that the capacitive coupling between the high-voltage tip and the chuck had a significant effect on noise floor of the system. Increasing the tip distance from the chuck, or reducing the voltage sweep rate of the tip, reduced the displacements currents measured in the chuck. This is a significant problem in the sweep-voltage breakdown measurements, as the diode leakage current is usually dominated by the displacement currents. For the static step-stressed measurements, the total system current resolution was measured to be 10fA.

4.2.3 Analysis of Leakage Current Noise

The stepped-stress breakdown measurements of trench-MOS SBDs offer a wealth of information, in the form of the high-resolution leakage data. By analysing changes in the leakage current as a function of step-voltage, it is possible to comment on changes in the dominant leakage mechanism and device degradation as the it approaches breakdown. It seems reasonable to focus on the leakage current noise when analysing leakage mechanisms in the diodes, as current noise is intimately related to the modulation of leakage paths via mechanisms including the creation of defects and the charging of trapping centres, [210]. Therefore, quantifying the measured noise of the device as a function of stress-bias should offer insights into the device state.
The noise analysis performed on the leakage current utilises a method developed by Dalcanale *et al.* [41]. Conventional noise analysis relies on averaging over a large number of spectra, taken using a single device. The central limit theorem can then be applied to extract an average noise value, along with a standard deviation in the noise. However, in the case of the diode breakdown measurements, it is not possible to take multiple spectra for a single device. This is as the diodes are observed to permanently degrade between voltage-steps, fundamentally changing the noise behaviour. Furthermore, it is not necessarily possible to average over many devices, due to variations in device processing. The noise method outlined by Dalcanale *et al.* [41], only requires a single spectrum at each stress bias, and will be outlined below.

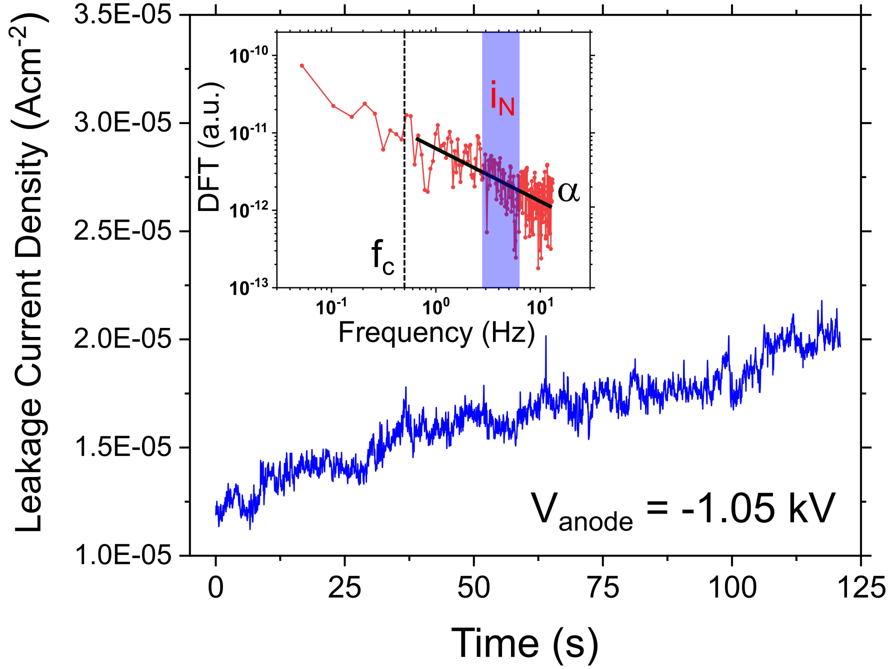


Figure 4.4: Example of leakage current noise trace, (with an anode bias of -1.05 kV), for a trench diode fin width = 1.5 μm and fin separation = 1.5 μm. The discrete Fourier transform of current noise trace is shown in the inset, with the position of the high pass filter, (f_c), and the log-spaced window used to extract i_N marked. A linear fit of the DFT slope is used to extract the spectral power density exponent, α. Figure reproduced from [38].

The leakage current measured during a stepped-stressed breakdown measurement is divided into leakage current traces for each constant bias step. An example of such a leakage current trace is shown in Fig.4.4. A discrete Fourier transform (DFT) of the leakage current is then taken, using a Hann windowing function. A windowing function is necessary as the measured leakage current noise is not a periodic function. The DFT implicitly assumes that the input signal is periodic, repeated temporally over the range of $-\infty < t < \infty$. This assumption results in discontinuous steps at the beginning and end of the non-periodic leakage noise signal, introducing step like frequency artifacts in the DFT. The Hann windowing function is a Gaussian function that is convoluted with the leakage noise signal; effectively pinning the start and end values of the noise signal to zero, and removing the discontinues. Other windowing functions could have been used, for instance: a Tukey window, the Blackman window, the Kaiser window, the Nuttall window, and the flat top window [211]. Dalcanale *et al.* demonstrated, using a dummy function with randomly generated noise, that the Hann windowing function leads to the least spectral leakage and has the smallest impact on the noise signal.
The impact of the Hann windowing function on a dummy function is shown in Fig.4.5. Three

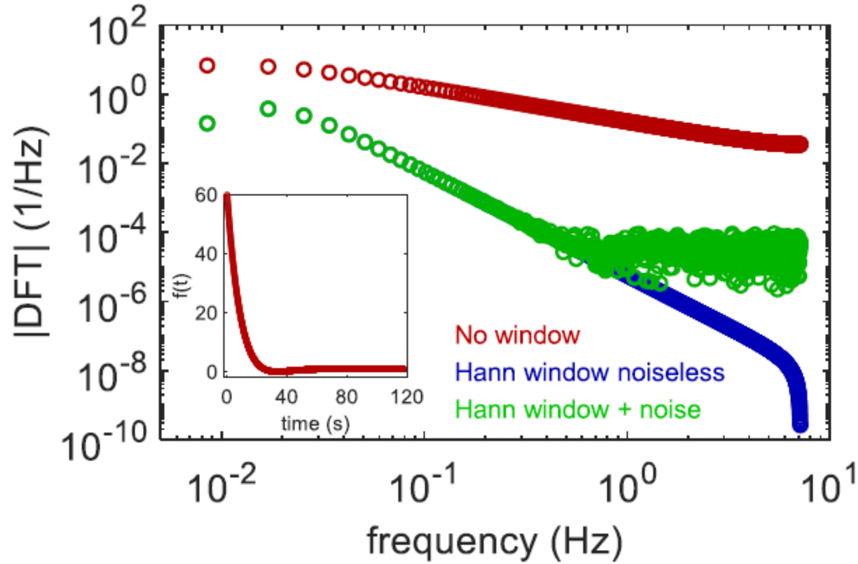


Figure 4.5: The impact of using a Hann windowing function on the DFT of a dummy function. The time-domain test function is shown in the inset. Red: A high noise level is observed without the Hann window, due to spectral leakage. Blue: Noiseless dummy function with a windowing function. Green: DFT of the dummy function with noise. At lower frequency the function's DFT dominates, and at higher frequency the noise signal dominates. Figure reproduced from [41].

DFTs of a dummy function (see inset) are plotted. The no window and the Hann window DFTs are taken directly from the dummy function, while the Hann window and noise DFT is taken for the dummy function with superimposed random noise. Spectral leakage for the windowless DFT is observed, resulting in a high DFT value across all frequencies. The DFT of the dummy function superimposed with noise, taken using a Hann window, shows two distinct regimes. At lower frequencies the DFT of the function dominates, while at higher frequencies the DFT of the superimposed noise dominates. This demonstrates that, when using a Hann windowing function to analyse the leakage current noise of a signal, it is necessary to disregard points below a certain frequency.

Over the frequency range 0.33Hz – 13Hz, the DFT in Fig.4.4 was divided into five log-frequency bins, with equal spacing in log-space. The lower bound of the frequency range was chosen to be 0.33Hz as low-frequency (1/f) noise dominates the signal below this value. In order to extract a qualitative measure of the current noise from the DFT in Fig.4.4, the DFT was divided into 5 windows of equal width in log space. The five windows were, (after dividing the log space equally), 0.33-0.66 Hz, 0.66-1.39 Hz, 1.39-2.9 Hz, 2.9-6.2 Hz and 6.2-13 Hz. The noise power spectral density exponent, α, was extracted by fitting a slope to the averaged values of each bin, (see inset of Fig.4.4). The window covering the range 2.9-6.2 Hz was then used to extract a noise current (i_N), as shown in the inset of Fig.4.4. The distribution of amplitudes around the α baseline, in

this window, were fitted using a Weibull distribution, which takes the form:

$$F(x) = \left(\frac{k}{\lambda}\right)\left(\frac{x}{\lambda}\right)^{k-1} e^{-(x/\lambda)^k} \tag{4.1}$$

where x is a random variable of the Weibull continuous probability density function, k is the shape factor, and λ is the scale factor. The Weibull distribution is only one of many generalised gamma functions that could be used to fit the leakage noise DFT. Dalcanale *et al.* argue that the applied windowing function affects the choice of distribution, with a Hann windowing function yielding a Weibull distribution [41]. The noise current i_N was taken to be the shape factor of the Weibull distribution.
A larger number of windows would have been preferable when fitting the α slope. However, each bin needs to cover the same log space frequency range. As the data points are distributed linearly in frequency space, a larger number of bins would lead to the lowest frequency windows having only a few data points. Based on the number of points and the cut-off frequency of the data sets, five bins were used for the α slope fitting. It was observed that the low-frequency points had a larger impact on the alpha value, as there were fewer points data points per average in the low-frequency windows. As the 'pivot' of the alpha baseline was situated at the low-frequency end of the DFT, the larger variations in i_N were observed in the higher frequency windows, for small changes in α. The third window was chosen to extract i_N in order to balance the requirement for a large number of data points with and the desire for a robust determination of i_N. The i_N is sensitive to both changes in the leakage current noise and to the absolute value of the leakage current. To separate changes in i_N due to device degradation, (which will manifest themselves in the leakage current noise), from increases in leakage current, the normalised noise current (NNC) was used. For each voltage step, the noise factor i_N was normalised to the averaged leakage current (i_{Av}), giving a value for the NNC of i_N/i_{Av} .

4.3 Results

4.3.1 Simulations

Silvaco ATLAS 2D simulations were performed for a range of device dimensions in order to compare the peak fields across different diode geometries. While the 10μm of n-type β-Ga_2O_3 below the anode has a low donor concentration, the bulk drift-region in the substrate is highly doped, (>10^{18} cm^{-3}). As such, the substrate's conductivity will be far higher, and the corresponding voltage drop over this region will be insignificant. For simplicity, this region is ignored in the simulations, and is assumed to be a continuation of the cathode. The aim of the simulations was to make direct comparisons of the breakdown across each of the structures shown in Fig.4.1. Each structure will exhibit a different field-voltage scaling, and so the simulations provide the means to compare the field scaling of each device. Leakage currents were not simulated, owing to the difficultly posed to ATLAS by β-Ga_2O_3's low intrinsic carrier concentration.

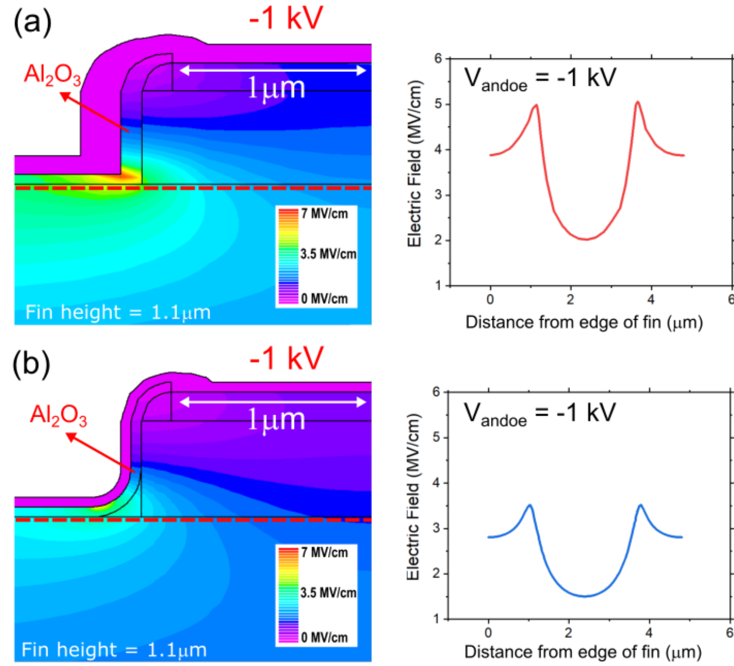


Figure 4.6: Comparison of the peak fields observed in two different fin structures, both with fin widths and separations of 2μm. 2D field profiles of a single trench bottom corner and half of the fin are shown on the left, with a -1kV bias on the anode. Field profile cut-lines for the full fin are shown on the right. The cut-line is take 10nm below the oxide-semiconductor interface, as indicated on the 2D field profiles by the red dotted lines. (a) A trench-MOS diode with 90° terminated corners in the trench bottoms. (b) Round corners in the trench bottom, with the radius of curvature extracted from Fig.4.2.

The bandgap at 300K of β-Ga$_2$O$_3$ was set to 4.8eV and the dielectric constant to 10. The Al_2O_3 layer had a dielectric constant of 12. The models used in the simulations were Fermi–Dirac and Shockley–Read–Hall statistics. Two approaches were used to handle the absence of mobile holes in gallium oxide. The first was simply consider only electrons in the simulation, disabling holes in the TCAD input file. The second was to include holes in the simulation, and to perform a transient ramped simulation, extracting the field profile on a time scale small enough that hole redistribution would not occur (as discussed in section 3.4). In any structure with a direct semiconductor-anode contact (trench-MOS diodes and the planar SBD), the two methods were equivalent. For the MOS-CAP structure, the transient method was the only one to produce convergence. Extracted peak field values for the planar MOS-CAP and the planar SBD matched the calculated analytical values.

Previous reported simulations of these devices used a 90° termination for the oxide in the trench-bottom corners [33]. This leads to an upper bound for the peak field values; overestimating the field compared to the real corner geometry. The impact of using rounded corners in the simulations, with a radius of curvature extracted from Fig. 4.2, is shown in Fig. 4.6. The 2D

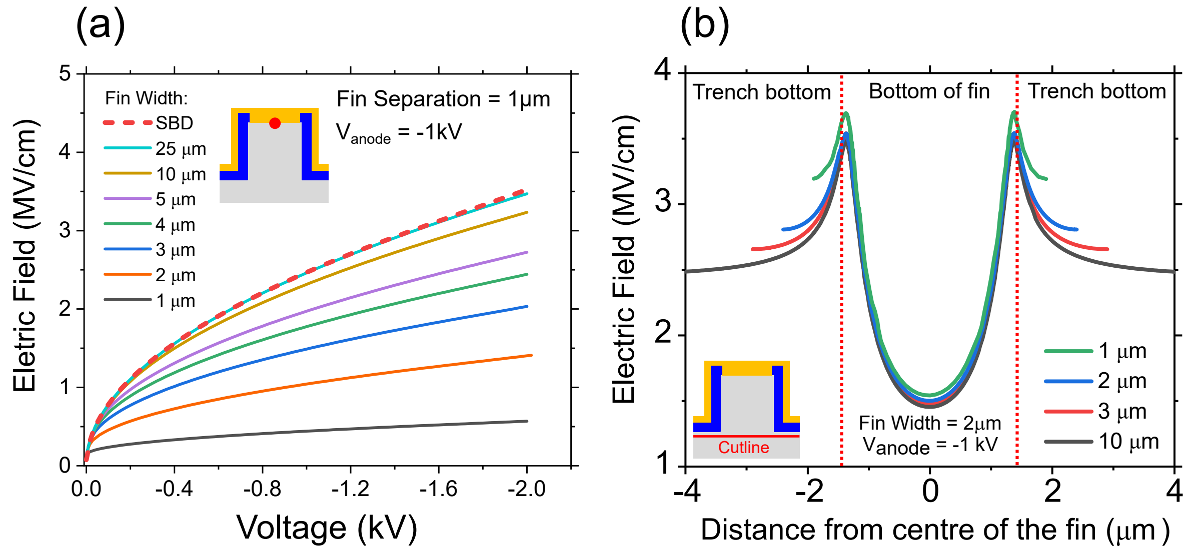


Figure 4.7: Simulated field-voltage scaling for varying fin dimensions, with an anode bias of 1 kV. (a) Constant fin separation and varying fin widths. The loss of sidewall clamping in wider fins is demonstrated, with the field at the centre of the 25 μm fin scaling like that of a planar interface. The red dot on the device schematic indicates the position at which the field was extracted. (b) Simulated field profiles for a variety of fin separations, (fin width = 2 μm), with the cutline taken at 1 nm below the trench-bottom Ga_2O_3-oxide interface, (as shown in the inset). The red dotted lines indicate the approximate boundaries between the fin and the trench bottom. Figure reproduced from [38].

field profile of a 90° terminated corner diode, along with a cut-line taken 10nm below the oxide-semiconductor interface, is shown in Fig. 4.6(a). High fields are observed in the vicinity of the 90° termination, with a peak field of 5 MV/cm. Fig. 4.6(b) shows the the same profiles for a rounded trench bottom corner, with a peak field of 3.5 MV/cm observed below the semiconductor-oxide interface. The mesh densities in the high-field regions for the two simulations are different. The mesh density for the 90° terminated corners would be expected to have a stronger impact on the field than for the rounded corners. This is as the field gradients in the vicinity of the 90° protrusion will be high when compared to the rounded corner structure, and an insufficiently dense mesh will fail to resolve this. Three simulations were performed for the 90° termination, with mesh densities x1, x2 and x4 that of the mesh density used in Fig.4.6(a). The extracted peak fields were approximately the same in each, demonstrating that the mesh density used in these simulations was sufficiently high.

Fig. 4.7(a) shows the results of a set of simulations for a fin separation of $1\mu m$, and a range of fin widths (1-$25\mu m$). The electric field is extracted from the centre of the Schottky-barrier interface, at the top of the fin, as indicated by the red dot in the inset. The highest field at this interface should be observed here, as the RESURF effect from the side-wall anode will be weakest. The red-dotted line shows the field-voltage scaling of a planar SB. In the case of a fin of infinite width,

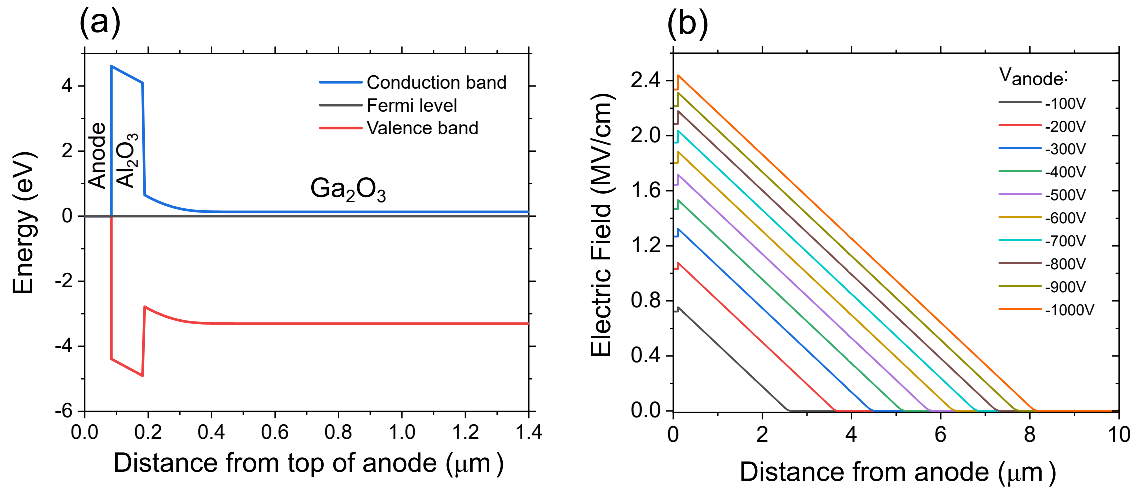


Figure 4.8: Simulated electrical properties of the planar MOS-CAP structure shown in Fig.4.1(d). (a) Band diagram of the MOS-CAP structure under zero bias. (b) Field profile across the oxide-Ga_2O_3 interface for a range of anode voltages. The anode-oxdie interface is defined as 0μm, and the oxide-Ga_2O_3 interface is situated at 0.105μm.

the RESURF effect would be completely suppressed, and the field-voltage scaling should be identical to that of a planar SB. In fins of finite width, the RESURF effect will be present to some degree over a portion of the interface. Here, the RESURF effect will be said to be suppressed when the field-voltage scaling at the centre of a fin is identical to that of the planar SB interface. As shown in Fig.4.7(a), the field scaling with voltage is weaker than that of a planar SBD for fins with widths <10μm, i.e. field clamping is observed. For devices >25μm, the RESURF effect is lost at the centre of the fin, and the field-voltage scaling is approximately that of the planar SB. All devices used in this study have fin widths <3μm, and so the RESURF effect will be present in all devices studied [33][98].

Fig.4.7(b) shows the impact of fin separation on the field profile at a constant voltage of -1kV on the anode. A constant fin width of 2μm is used, with fin separations varying between 1μm and 10μm. The field profile is extracted using a cutline taken across the bottom of the fin, offset 1nm below the trench-bottom β-Ga_2O_3–oxide interface, as indicated by the red line in the inset. Fin separation is observed to have an insignificant effect on the peak fields close to the oxide corners, while fields in the trench bottom, (either side of the fin), are observed to increase with decreasing fin separation. This suggests that fin separation should have a minimal impact on the breakdown voltage of the device, over the range of fin separations considered.

Simulations were also performed to determine the field-voltage scaling of the MOS-CAP structure. Fig.4.8(a) shows the simulated band structure of a MOS-CAP at zero bias. Fig.4.8(b) shows the field profile over the oxide-Ga_2O_3 interface for a range of anode voltages, with the interface located at 0.105μm. Both the simulated band diagram and the the field profiles exhibit the expected behaviour of a MOS-CAP [52].

4.3.2 Impact of Fin Geometry on the Breakdown of Trench-MOS SBDs

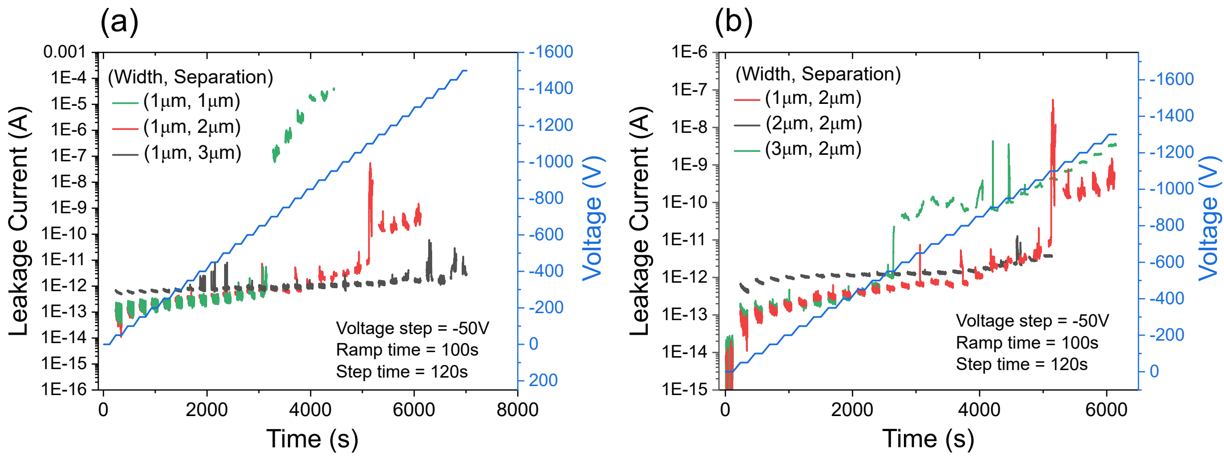


Figure 4.9: Stepped-stress breakdown of trench-MOS diodes with a number of fin widths and separations. The leakage current is monitored for 120s during each step, and the ramp time between each step is 100s. The breakdown voltage of each diode is defined at the voltage step at which the leakage current reaches 1mA, (not shown). Breakdown characteristics are shown for diodes with (a) fin widths of $1\mu m$ and varying separations and (b) fin separations of $1\mu m$ and varying widths.

The simulations in Fig.4.7 demonstrate that the breakdown voltage of the trench-MOS structure will have a strong dependence on fin width and a weak dependence on fin separation. Fig.4.9 shows the breakdown characteristics of two sets of diodes, with the variation in fin width shown in Fig.4.9(a) and fin separation shown in Fig.4.9(b). Two behaviours are observed across both sets of diodes, a jump in the leakage current without complete breakdown of the device, and a hard-breakdown event, which is characterised by a jump in the leakage current to the compliance (not shown). The expected relationship between fin width and breakdown is not observed when looking at the hard-breakdown voltages, which all have a similar value. The same is true of the relationship between breakdown voltage and fin separation, with fin separation observed to have a large impact on the device breakdown voltage, in contrast with the weak dependence predicted by the simulation data in Fig.4.7(b).

This deviation from the expected behaviour can be explained with reference to the breakdown statistics of the devices. A large variation between devices of the same dimensions was observed, as shown in Fig.4.10. Here, the leakage currents are an averaged value for each 120s voltage step, with the current behaviour over each step being comparable to Fig.4.9. Both the jump in leakage current and hard-breakdown voltages of each device vary, with the jumps in leakage current spread over a range of 150V, and the hard-breakdown spread over a range of 300V. This device-to-device variation is larger than the variation observed between different fin widths in Fig.4.9(b), and covers most of the variation observed across fin separation in Fig.4.9(a). There are two obvious reasons for this variation, and for the deviation from the expected behaviour

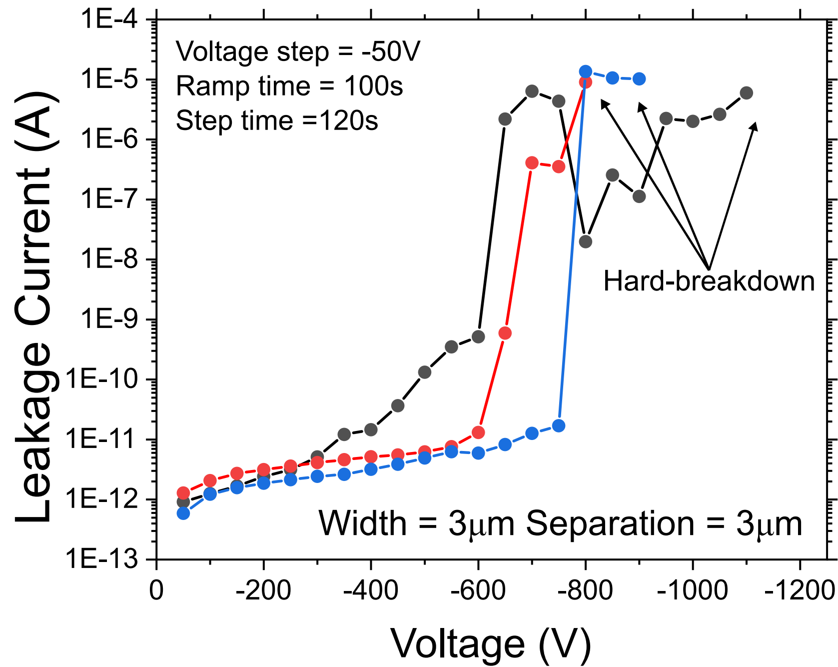


Figure 4.10: A comparison of the breakdown characteristics of three diodes with the same dimensions. The leakage current at each step is an averaged value, taken over the 120s measurement time. A large variation in both soft-breakdown voltages and hard-breakdown voltages is observed.

in breakdown scaling with device dimension, shown in Fig.4.9. The first possible explanation is that there are large variations in device processing across the wafer, e.g. changes in the oxide quality. The second is that the breakdown mechanisms, under stepped-stressed measurement conditions, is a time-dependent mechanism, and so is not solely dependent on the peak fields in the device. It is probable that a combination of these two mechanisms are responsible for the variation in device-to-device behaviour. Therefore, any dependence of the breakdown voltage on fin width would only be apparent after measuring a sufficiently large number of devices, as demonstrated in [33]. A limited number of devices were available, and so performing breakdown measurements on statistically meaningful number of devices was not possible. However, it is still possible to comment on the impact of time-dependant breakdown on the devices, if the breakdown mechanisms of the trench-MOS diodes are understood.

4.3.3 Leakage Currents and Breakdown Mechanisms in Trench-MOS SBDs

Fig.4.11 shows the leakage current of three representative trench-MOS SBDs, with different fin widths and separations. The leakage current is measured under stepped-stress conditions, and is observed to be consistent across all three devices. Below, the distinction between three distinct degradation/breakdown behaviours will be made.

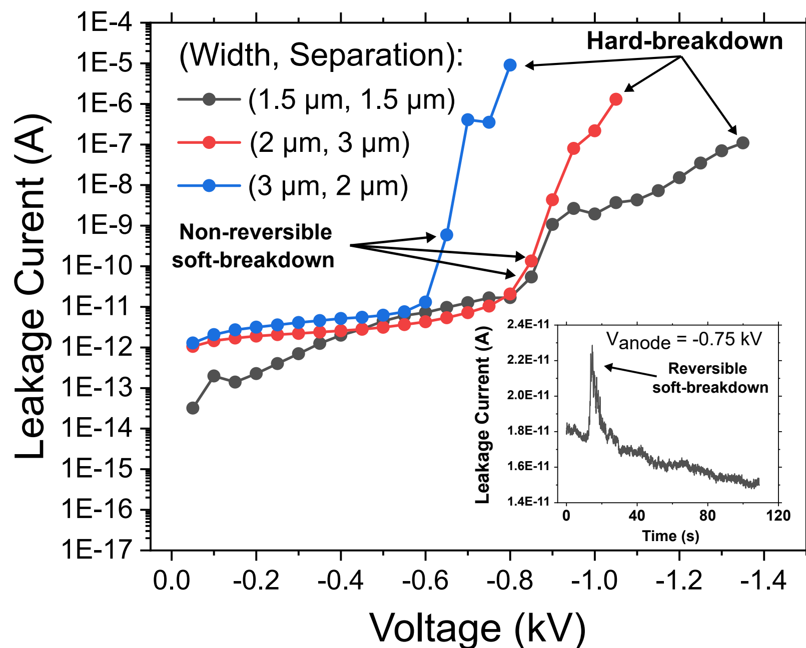


Figure 4.11: Stepped-stress leakage characteristics of a representative set of trench-MOS SBDs. Between each voltage step, the anode is ramped over the period of 100s, (leakage not shown). Non-reversible soft-breakdown voltages are taken to be the first voltage at which an elevated leakage current is observed. The final voltage step defines the breakdown voltage of each device. Inset: Leakage current of the fin width = 1.5μm diode at -0.75 kV. A reversible soft-breakdown event, characterized by the presence of current spikes, is labelled. Points below 100V are disregarded due to the current resolution of the system. Figure reproduced from [38].

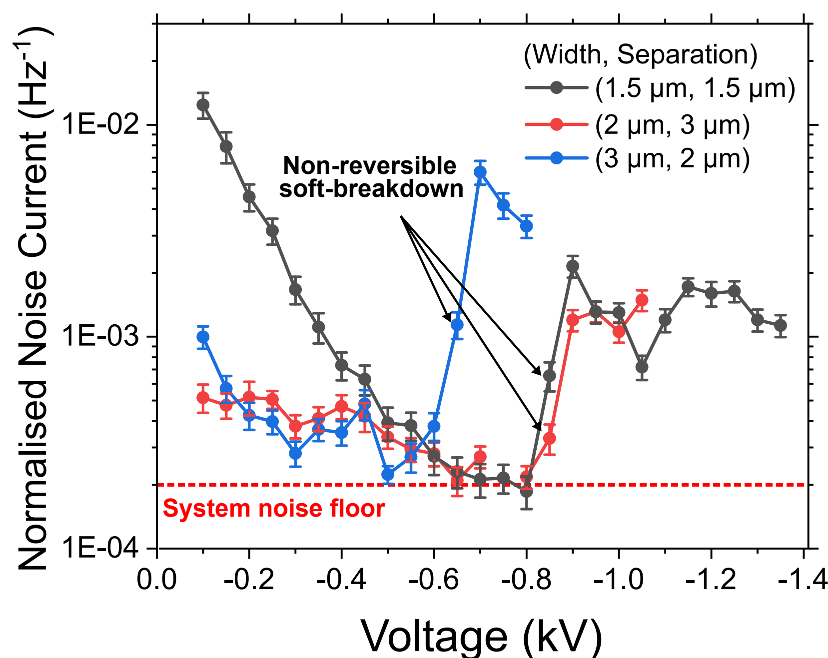


Figure 4.12: Normalised noise currents (NNC) for the three diodes in Fig.4.11. The non-reversible soft-breakdown events in each diode lead to a jump in the noise level. Points below 100V are disregarded due to the current resolution of the system. Figure reproduced from [38].

There are two distinct types of soft-breakdown event; events which likely indicate the degradation of the device, but are not related to catastrophic failure event. The first is characterized by reversible spikes in leakage current during a voltage step, with little change in the leakage baseline, as shown in the inset of Fig.4.11. The second soft-breakdown behaviour is characterized by a sharp, non-reversible increase in the leakage current between voltage steps. After the non-reversible soft-breakdown event has occurred, the reversible current spikes are no longer observed. At higher voltages than that of the non-reversible soft-breakdown, hard-breakdown of the device is observed. Hard-breakdown of the devices is characterized by sudden increase in device current to the measurement compliance of 1mA, occurring at the voltages of the final voltage steps, (Fig.4.11).

The noise analysis of the leakage currents in Fig.4.11 is shown in Fig.4.12. The non-reversible soft-breakdown events are labelled, with the onset voltage defined as the first step in which an elevated leakage current is observed. Across all measured diodes, a generic behaviour was observed: there is a decrease in the NNC before the non-reversible soft-breakdown event, albeit with some variation in magnitude. Following this soft-breakdown, the NNC increases, remaining approximately constant until hard-breakdown. The NNC magnitude after non-reversible soft-breakdown was broadly similar for all devices.

In order to perform the noise analysis in Fig.4.12, the power spectrum exponent α was extracted at each voltage step in Fig.4.11, as described in section 4.2.3. At low voltages, all diodes exhibit an noise exponent of $\alpha \approx 1$, corresponding to 1/f noise, as shown in Fig.4.13. The exponent increases to a value of $\alpha \geq 2$ before the non-reversible soft-breakdown, dropping to a value close to 1 immediately after soft-breakdown. The presence of the obvious reversible current spikes did not have a significant impact on the value of alpha at each voltage step; removing those current spikes from each step shifted α by a value within error of the original value.

4.3.4 Leakage Currents in MOS-CAPs and Planar SBDs

In order to understand the origin of the leakage current and noise current in the trench structure, it is necessary to analyse the possible leakage paths in the trench-MOS diode structure. Using both a planar MOS-CAP structure and a planar SBD structure, (Fig.4.1(c) and Fig.4.1(d)), it is possible to isolate the current leakage and the noise behaviour of the trench-MOS oxide and the fin SB interface. Step-stressed breakdown and voltage-sweep measurements of planar SBDs are shown in Fig.4.14. The step-stressed leakage current increases with each voltage step, with the leakage current at -0.75kV, shown in the inset. This step is representative of the behaviour at all voltage steps, with no current spikes characteristic of reversible soft-breakdown observed. A non-reversible soft-breakdown event is not observed over the course of the measurement, with a hard-breakdown at 1kV. The absence of soft-breakdown events suggests that there is minimal degradation of the device during the stepped-stress measurement. Degradation of the device would be apparent if the leakage current demonstrated a strong dependence on the overall

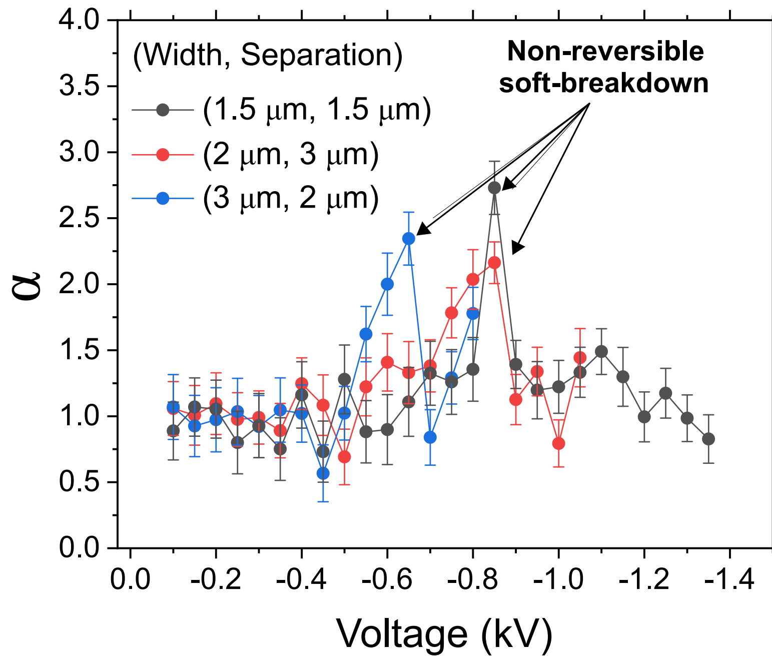


Figure 4.13: The power spectral density exponent (α) extracted at each voltage step, for the three diodes in Fig.4.11. The voltage steps at which each non-reversible soft-breakdown event occurs are labelled. Points below 100V are disregarded due to the current resolution of the system. Figure reproduced from [38].

stress time of the device. Comparing the step-stressed breakdown characteristic to the voltage sweeps of diode 2, and the diode swept-breakdown of diode 3, supports the conclusion that device degradation is not observed; no significant difference is seen between the leakage currents of the three diodes, suggesting minimal degradation before device breakdown.

Fig.4.15. shows the breakdown characteristics of a MOS-CAP structure. Unlike the SBD structure, the leakage current of this device remains approximately constant below 1kV. The MOS-CAP undergoes a non-reversible soft-breakdown event above 1kV, indicated by the sharp jump in leakage current, and a hard-breakdown event, at approximately 2kV. The current spikes, characteristic of reversible soft-breakdown, are observed for all measured MOS-CAPs (see inset). These spikes are observed for voltages >50V, with a significant increase in their frequency as the non-reversible soft-breakdown voltage is approached. They are not observed after the soft-breakdown, although they may simply be obscured by the orders of magnitude increase in the leakage current.

The NNC for both the planar SBD and the MOS-CAP structures are shown in Fig.4.16. The noise current for the planar SBD decreases as voltage increases, as shown in Fig.4.16(a). In the case of the MOS-CAP, the NNC oscillates around a level of approximately $2\text{x}10^{-3}\text{Hz}^{-1}$, both before and after soft-breakdown (Fig.4.16(b)). All measured MOS-CAP structures exhibit similar behaviour.

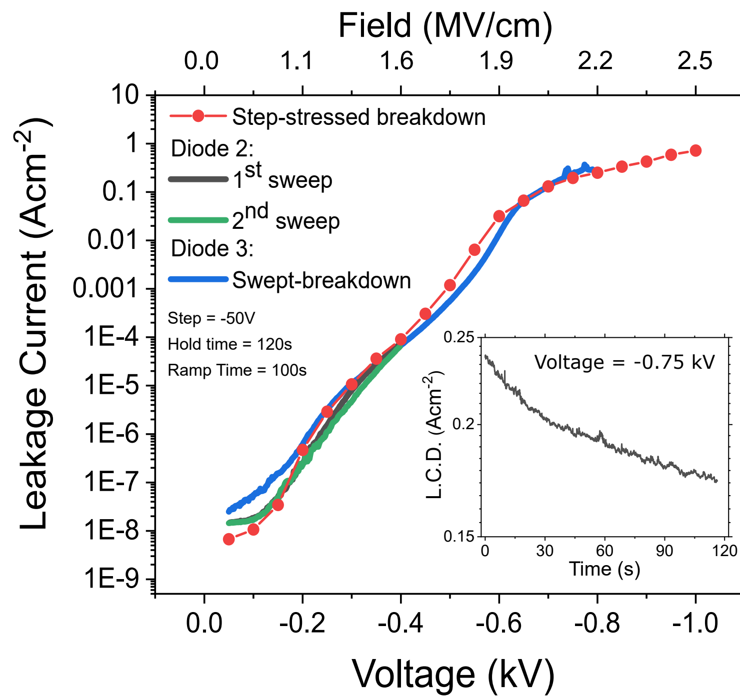


Figure 4.14: Stepped-stress breakdown and voltage-sweep measurements of planar SB diodes, diameter 90μm. Diode 2 was swept consecutively from 0V to -400V, and diode 3 was swept from 0V to breakdown. The sweep rate used for diode 2 and diode 3 was 1V/s. The diodes did not breakdown during the sweep measurements. The corresponding values of field at the SB interface are extracted from simulations. Inset: Time dependence of the step-stressed leakage current at -0.75kV. Figure reproduced from [38].

It should be noted, with reference to Fig.4.7, that the voltage range covered in Fig.4.16(a) covers all relevant fields observed in the trench diodes. Although the hard-breakdown voltage of the 3μm fin is the lowest, (Fig.4.11), the breakdown field is highest, because of the stronger scaling of field with voltage in the 3μm fin, when compared to 2μm, (see Fig.4.7). Therefore, the highest surface field, across the SB interface, reached in Fig.4.11. is 1.35MV/cm, at 0.8kV for the fin width = 3μm, which is equivalent to -300V for a planar SBD.

Fig.4.17. shows the power spectrum density exponent α as a function of voltage for the MOS-CAP structure. An increase in α is observed, from <1, to approximately 1.5 before the non-reversible soft-breakdown event. After soft-breakdown, 1/f noise is observed.

4.4 Discussion

The leakage currents in the trench-MOS structure, (Fig.4.11), can be attributed to two distinct leakage paths; leakage at the SB interface, and leakage through the trench bottom oxide corners and trench bottom oxide. Leakage through the fin side wall is unlikely as the RESURF effect

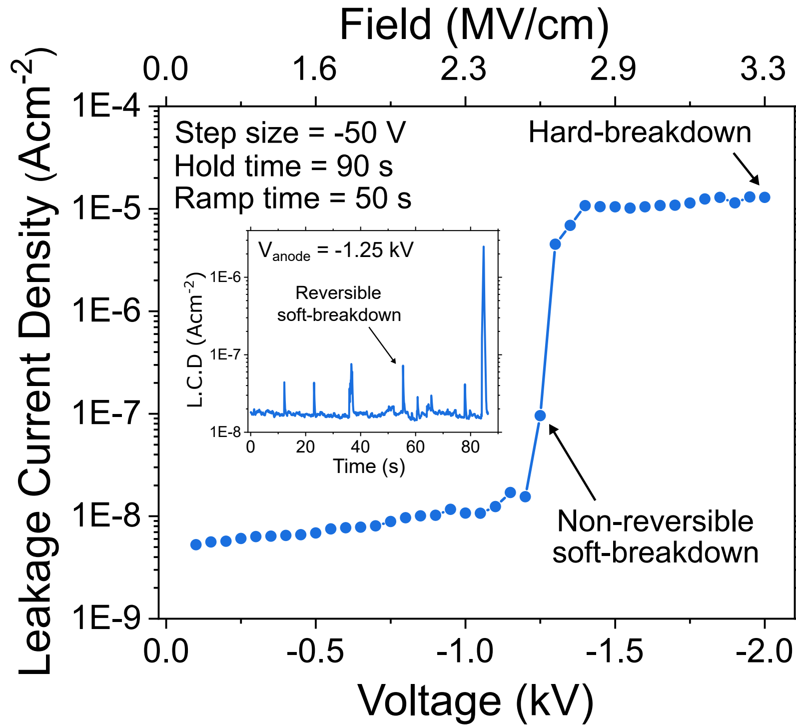


Figure 4.15: Stepped-stress leakage characteristics of a MOS-CAP structure with dimensions 160x170μm. Between each voltage step, the anode is ramped over the period of 50s, (leakage here not shown). The corresponding values of field at the oxide-semiconductor interface are extracted from simulations. Inset: Leakage current at -1.25 kV. Reversible soft-breakdown events, characterized by the presence of current spikes are visible <1kV. Figure reproduced from [38].

reduces the fields in this region, (see Fig.4.1(b)). The normalised noise current for the trench structure, (Fig.4.12), shows the presence of these two distinct noise regimes during the step-stressed measurement. The first regime, from -100V to soft-breakdown, exhibits a linear decrease in $\log_{10}$(NNC). The second regime, observed after non-reversible soft-breakdown, is characterized by a sharp increase in the noise current until hard-breakdown. Decomposing the trench-MOS SBD structure into constituent components, the normalized noise appears to be a composite of the behaviour observed in the planar SBD and the MOS-CAP structure. The low-voltage regime noise behaviour of the trench-MOS SBD can be explained with reference to the noise current of the planar SBD structure in Fig.4.16(a). The low voltage noise behaviour of the trench-MOS SBDs, and the noise behaviour of the planar SBD is qualitatively the same, with a linear decrease in $log_{10}(NNC)$ with voltage. This suggests that in the first regime the noise and leakage currents in the trench-MOS SBD is dominated by the bulk leakage current over the SB interface.

Simulations of the planar SBD suggest that the maximum field observed in Fig.4.14 over the metal-semiconductor interface, far away from the device edges, is 2.5MV/cm. The field at the first voltage step, (-50V), is 0.55MV/cm. Above 0.2MV/cm, the dominant leakage mechanism across

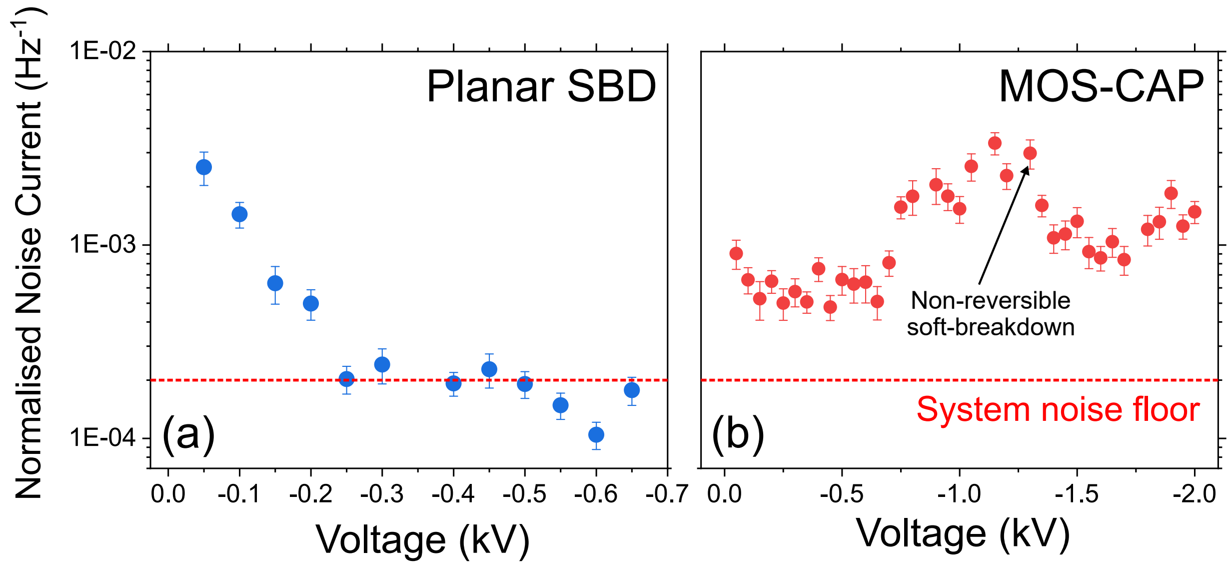


Figure 4.16: (a) The normalised noise current (NNC) of the planar SBD stepped-stress measurement shown in Fig.4.14. Above 200V the system noise floor is reached. (b) The NNC of the MOS-CAP stepped-stress measurement shown in Fig.4.15. The NNC is approximately constant over the measurement voltage range.

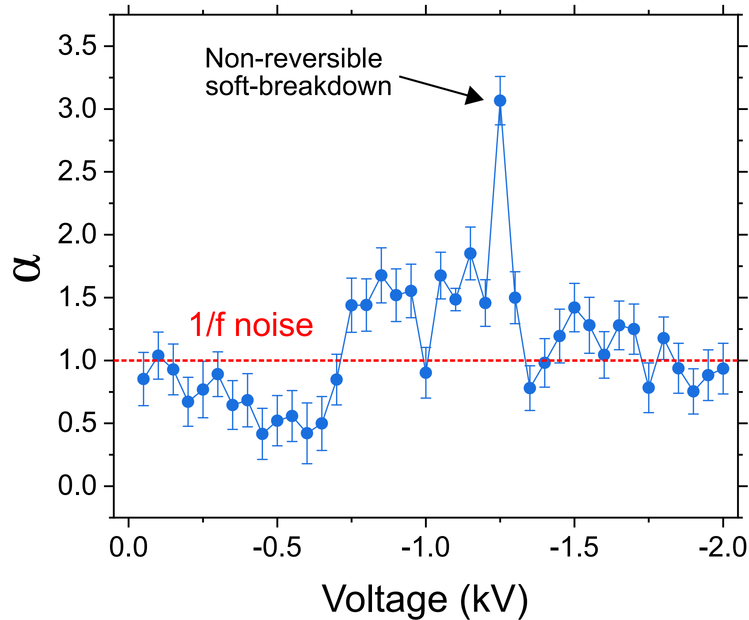


Figure 4.17: Power spectral density exponent extracted at each voltage step for the MOS-CAP stepped-stress measurement shown in Fig.4.15. Figure reproduced from [38].

the SB is barrier tunneling, as demonstrated by Li *et al.* [96]. This leakage mechanism should lead, in the absence of barrier degradation, to a reversible leakage current. Indeed, no change or degradation was observed for multiple voltage sweeps over the range 0kV to 0.4kV (Fig.4.14). The decrease in NNC as a function of voltage, observed for the planar SBD in Fig.4.16(a), can be explained by the relative scaling of the noise current i_N and the average leakage current i_{Av}. i_N was observed to increase during the measurement, but the absolute leakage current scaled more quickly. As a result, normalizing i_N to the leakage current leads to a decreasing NNC.
While the low voltage behaviour of the trench-MOS SBDs can be explained with reference to the planar SBD structure, the high voltage noise behaviour can be explained with reference to the MOS-CAP noise current in Fig.4.16(b). Both reversible and non-reversible soft-breakdown events occur for both structures. It seems reasonable that these events are related to a time-dependent breakdown mechanism over the oxide interface, as described in [212]. The leakage current observed before the non-reversible soft-breakdown is possibly mediated by pre-existing defects in the oxide layer (Fig.4.15). Both the MOS-CAP structures and the trench-MOS SBDs exhibit non-reversible soft-breakdown events, and both have an approximately constant NNC after these events. This suggests that the non-reversible soft-breakdown event in the trench structures is related to a change in the dominant leakage path, from the SB interface at lower voltages to a newly seeded leakage path in the oxide layer at higher voltages.
The approximately constant NNC of the MOS-CAP structure can be explained by considering the oxide leakage current before the non-reversible soft-breakdown event. The NNC is a measure of the localisation of the leakage current, with a more localised leakage exhibiting a higher NNC. In the case of the trench-MOS diodes, the transition from leakage across the bulk SB interface to an oxide leakage path represents a large change in the degree of localisation of the current. Despite the large increase in leakage current, the NNC jumps during the non-reversible soft-breakdown event, as the factor i_N scales more quickly. However, in the case of the MOS-CAP, the current before the non-reversible soft-breakdown event is already localised to a small area, via some density of leakage paths present at low biases. i_N does increase after soft-breakdown for the MOS-CAP, but this is offset when normalising by the jump in leakage current, and so the NNC is not changed significantly. The small, factor of 2, decrease in the NNC after non-reversible soft-breakdown is far smaller than the orders of magnitude changes in the trench-MOS diodes. It is likely that this is simply the result of the large change in leakage current, (during non-reversible soft-breakdown), dominating over any changes in the degree of current localisation.
The seeding of highly resistive soft-breakdown paths in oxide layers has been previously discussed by Degraeve *et al.* [213]. Degradation of this type is consistent with the jump in NNC after the non-reversible soft-breakdown events shown in Fig.4.11. An increase in NNC suggests that any increase in leakage current is preferentially confined to a localised leakage path, as opposed to an increase in the number of leakage paths [214]. A transition from bulk leakage at the SB interface to leakage through a leakage path in the oxide represents a transition to a more localised current

path with a correspondingly smaller number of fluctuators responsible for the noise. Hence there is an increase in the fractional change in current associated with changes in trap occupancy and an increase in the normalized noise current.

Furthermore, a degradation of the oxide layer is supported by the change in the power spectral density exponent during the breakdown measurements of trench-MOS SBD (Fig.4.13). The value of α = 1 at low voltages is indicative of 1/f noise associated with uncorrelated bulk leakage across an interface [210]. This value was then observed to increase from α = 1 to α = 2 before the non-reversible soft-breakdown event. In this region, reversible soft-breakdown current spikes are observed as seen in the insets in Fig.4.11 and Fig.4.15. It is noted that the FFT of an impulse exhibits a value of α = 2, so the increase in α is consistent with the presence of multiple current spikes. However, removing the obvious voltage spikes from the signal before applying a DFT left the value of α unchanged. This demonstrates that the determination of α for the trench-MOS diodes was robust. These spikes and soft-breakdown events are absent in the planar SBD, but present for the MOS-CAP breakdown measurements (Fig.4.15). Following the irreversible soft-breakdown, α = 1, and is consistent with the permanent degradation of the oxide layer via the formation of a percolation path, as discussed in [213][214]. A similar behaviour is observed in the MOS-CAP structure, Fig.4.17, while the value of α is approximately 1 for the planar SBD structure throughout the measurement.

The hard-breakdown of the MOS-CAP structure occurs at a voltage of approximately 2kV, which corresponds to a field of 3.3MV/cm in the bulk of the oxide (extracted from simulations and shown in Fig.4.15.). Similar breakdown voltages/fields were observed across all measured MOS-CAP structures. This is lower than the oxide breakdown field consistently observed at the device field corners described by Li *et al.* [33], during sweep-voltage breakdown measurements of trench-MOS diodes. This discrepancy can be explained by a degradation of the oxide under high bias stress. The stepped stress measurements performed in this study subject the oxide layer in each device to a prolonged bias stress, when compared to breakdown measurements in which the voltage is swept at a constant rate [33]. This prolonged bias stressing will lead to charging and defect creation in the oxide, triggering premature breakdown.

While the RESURF effect significantly enhances the breakdown voltages of these trench-MOS SBDs, the transition in leakage mechanism under prolonged bias stress ultimately leads to device failure. The design and deposition of the dielectric layers in these devices requires careful consideration to avoid a significant reduction in the operating voltages of real-world devices. This challenge is fundamental in all devices employing MOS/MIS junctions to implement RESURF effect, (i.e. field-plating and junction termination extension technologies), including both lateral devices such as high electron-mobility transistors and vertical devices such as trench SBDs [24][206][98]. As W. Li and H. G. Xing have argued, the challenge of managing high electric fields is particularly acute in (ultra)wide-bandgap semiconductors, insofar that the semiconductor can sustain an electric field higher than the practical electric field of the insulator [18]. For example,

considering the effect of time-dependent-breakdown, the practical achievable field in GaN is 3 MV/cm versus 2 MV/cm in SiO_2. One way to address this is to develop Schottky or pn junctions with sufficiently high energy barriers [100]. For instance, a barrier height of > 2.5 eV for Ga_2O_3 is necessary to reach 6 MV/cm in Ga_2O_3 (see Fig.2.21(a)). Schottky or pn diodes allow current flow through the junction without undergoing time-dependent-breakdown, and would allow for the less aggressive application of the RESURF effect, reducing fields over the critical failure points of the device [18].

4.5 Conclusions

In this work it has been demonstrated that, under bias stressing of trench-MOS β-Ga_2O_3 SBDs, the dominant leakage mechanism transitions from the Schottky barrier to a degraded Al_2O_3 dielectric layer. This has significant implications for the applications and suitable voltage range for β-Ga_2O_3 trench-MOS SBDs. The higher achievable breakdown voltage afforded by the RESURF technique introduces potentially life limiting fields in the Al_2O_3. This merits further investigation of the mean time to failure of such structures. This study highlights the importance of developing suitable MOS/MIS junctions, as well as high-barrier Schottky and pn junctions, to fully exploit the high-field handling afforded by β-Ga_2O_3.

CHAPTER 5

SELF-HEATING EFFECTS AND ORIENTATION DEPENDENCE OF ELECTRICAL AND THERMAL PROPERTIES IN β-GA_2O_3 MOSFETS

The low crystal symmetry of β-Ga_2O_3 presents two potential problems for device design. The low and anisotropic thermal conductivity and the potentially anisotropic electrical conductivity of β-Ga_2O_3 both have the potential to significantly impact device performance. In this chapter, anisotropy in both the thermal and electrical properties of β-Ga_2O_3 are investigated in thin-channel MOSFETs. The presence of intrinsic variations in device performance as a function of crystal orientation would impact design considerations over a range of devices. Conversely, an absence of anisotropy leaves the orientation as a parameter that can be optimised with respect to other considerations, e.g. material growth rates, density of trapping states, optimising device layout on substrates with respect to the density of devices. All devices used in the following studies were provided to us by our collaborators at the Air Force Research Laboratory (USA). Parts of this chapter have been previously published in IEEE Transactions on Electron Devices [42].

5.1 Introduction

Arguably, the most significant problem facing the commercialisation of β-Ga_2O_3 devices is its low thermal conductivity. Large increases in channel temperature, due to self-heating under bias, can degrade the device performance and ultimately lead to premature device breakdown. Thermal management solutions at the device design level in β-Ga_2O_3 have been widely discussed [215][216][217][218] and the impact of buffer orientation on self-heating has been alluded to [215]. However, less attention has been paid to the in-plane orientation of the device. This will have to be considered alongside any anisotropic electrical behaviour in β-Ga_2O_3 device, and the

relative importance of the two effects will have to be considered.

A thorough understanding of device self-heating can be gained by direct measurements of device channel temperature profiles as a function of power dissipation. Spectroscopic techniques have been previously exploited in the case of GaN HEMTs, such a micro-Raman measurements, IR spectroscopy and Quantum rod thermography [219][220][221]. Such measurements are not suitable for all device architectures, and are often time-consuming. Methods such as Raman nanothermography and thermoreflectance have been used in the case of β-Ga_2O_3 [222][223]. However, it not always possible to apply these methods directly to devices as they require specialised equipment and are resolution limited.

Electrical methods used to determine device temperature, which provide an averaged channel temperature, are often employed when in-situ device measurements are required [224][225][226]. Understanding how closely the values extracted using spectroscopic methods correspond with those extracted using electrical methods is key for accessing the suitability of electrical methods for identifying changes in peak channel temperature. In general, electrical methods are insensitive to the peak temperatures due to the presence of device hotspots. This is a particular problem for devices such as GaN HEMTs, as their high peak electrical fields lead to large variations in temperature along the device channel [227]. This is not necessarily the case in β-Ga_2O_3 MOSFETs; the low thermal conductivity of β-Ga_2O_3 and the difference in the field profiles between HEMTs and MOSFETs will result in large differences in channel temperature profiles.

In this chapter, a single set of β-Ga_2O_3 thin-channel MOSFETs is used to investigate device self-heating. The utility of two measurement techniques are compared: Raman nanothermography and a pulsed IV characterisation technique. Channel temperature profiles of the device at different biases are extract using Raman nanothermography. Coupled electrical and thermal simulations are then used to corroborate this data, with Joule heating profiles extracted from Silvaco ATLAS and loaded into an ANYSYS based thermal simulation. The temperature profiles are compared to channel average temperatures extracted by Blumenschein *et al.*, using a pulsed IV technique [42]. It is shown that the electrical and spectroscopic techniques provide an similar understanding of the device self-heating for the thin channel β-Ga_2O_3 MOSFETs. The potential anisotropy in self-heating, with respect to the lateral orientation of a device on the substrate, is then investigated using coupled electrical-thermal simulations. Lateral device orientation on a [010] substrate was shown to have an insignificant impact on device self-heating.

Pulsed IV measurements are then used to investigate variations in device R_{ON} across two sets of thin-channel β-Ga_2O_3 MOSFETs, with varying channel and gate orientation relative to the sample substrate. Raman spectroscopy is used to extract the gate and channel orientations with respect to the principle axes of β-Ga_2O_3. A large and consistent anisotropy in electrical behaviour is observed across two sample sets. This anisotropy was not correlated with the underlying substrate orientation, and was instead attributed to variations in the fabrication of the device gates. This highlights the necessity of optimising device fabrication before considering any intrinsic

anisotropies in the electrical properties of β-Ga$_2$O$_3$.

5.2 Self-heating Effects in β-Ga$_2$O$_3$ MOSFETs

While simulations of device self-heating provide a useful way to compare the relative merits of different device designs, it is critical to measure device self-heating directly. Both electrical methods and spectroscopic methods can be used to measure channel temperatures as a function of operating power. A spectroscopic method that has been successfully applied in the case of the β-Ga$_2$O$_3$ is the Raman nanothermography technique. This method relies on the deposition of TiO$_2$ particles on a device surface. The measurements of the particles' Raman spectra as a function of device operating bias can be used to extract spatial self-heating profiles, with the temperature extracted using shifts in the wave number of a TiO$_2$ Raman mode. Pomeroy *et al.* were able to extract channel temperature profiles in β-Ga$_2$O$_3$ MOSFETs using this technique [222]. These profiles were observed to be in good agreement with simulated profiles, as shown in Fig.5.1.
Pulsed IV based methods for measuring device self-heating have previously been reported in packaged GaN HEMTs [228], and in β-Ga$_2$O$_3$ MOSFETs [225]. Both of these measurements rely on a pulsed IV calibration of device R_{on} and I_D with respect to temperature. This calibration can then be used to relate values of R_{on} and I_D to a channel averaged temperature in DC operation. The pulsed IV techniques are beneficial as they do not require any particular device layout or geometry, and are not limited by device packaging or top-side metallisation. However, Simms *et al.* demonstrated that such electrical techniques underestimate the devices peak operating temperature in the case of GaN HEMTs, a critical parameter when determining the average lifetime of a device [229][230]. Although this will also be the case in β-Ga$_2$O$_3$, it is not clear to what degree the two methods will differ, due to the large differences in the thermal conductivities of GaN and β-Ga$_2$O$_3$. In this section, the device self-heating of a set of β-Ga$_2$O$_3$ MOSFETs is measured using Raman nanothermography, and this data is compared to channel averaged pulsed IV characterisation previously reported by our collaborators, Blumenschein *et al.* [42].

5.2.1 Devices and Experimental Details

The devices used in this study were thin-channel β-Ga$_2$O$_3$ MOSFETs, as shown in Fig.5.2. The device channel consisted of a 65nm layer of MOVPE grown Si-doped β-Ga$_2$O$_3$, on an insulating (010) Fe-doped β-Ga$_2$O$_3$ substrate. The donor concentration extracted from Hall measurements was 2x10^{18} cm^{-3}, with an electron mobility of 90 cm^2/Vs. The source and drain contacts were formed using a Ti/Al/Ni/Au (20/100/50/50 nm) stack, with a Ni/Au stack being used for the gate (L_G = 250nm). Au pads deposited on the source and drain stacks to act as heat sinks. The gate dieletric consisted of a 20nm ALD grown layer of Al$_2$O$_3$, with a 90nm plasma-enhanced chemical vapor deposition (PECVD) SiO$_2$ passivation layer. A source-to-drain spacing of 8μm was used

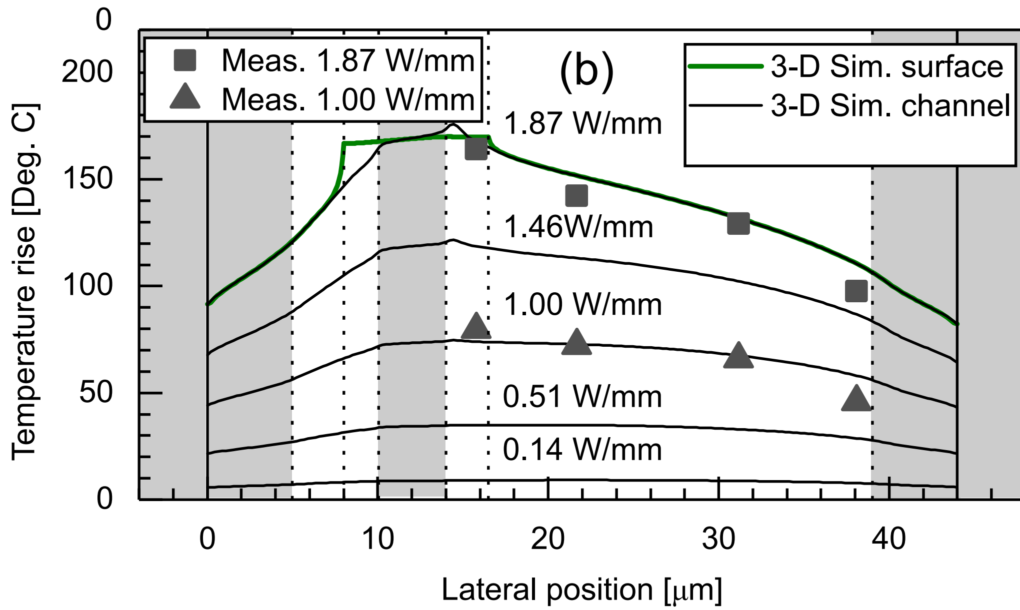


Figure 5.1: A comparison of MOSFET channel temperature profiles measured using Raman nanothermography and simulated using TCAD, (reported by Pomeroy *et al.*). Figure reproduced from [222].

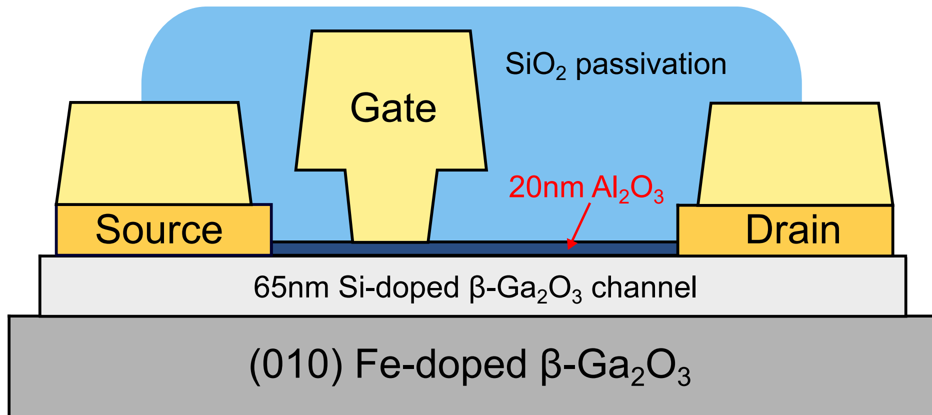


Figure 5.2: A schematic of the β-Ga$_2$O$_3$ MOSFETs used in this study.

for all measurements, with a gate length of 250nm. The fabrication of these devices has been previously described by Blumenschein *et al.* [42].

Direct Raman spectroscopy is sufficient to measure channel temperature profiles in GaN HEMTs, exploiting the temperature dependence of GaN Raman peak shifts on temperature [231]. This technique is particularly suited to extracted peak temperature values, which are situated at the drain edge of the gate in GaN HEMTs [232]. However, the wide-bandgap of β-Ga$_2$O$_3$ poses a problem with respect to the axial resolution of the measurement. The refractive index of β-Ga$_2$O$_3$

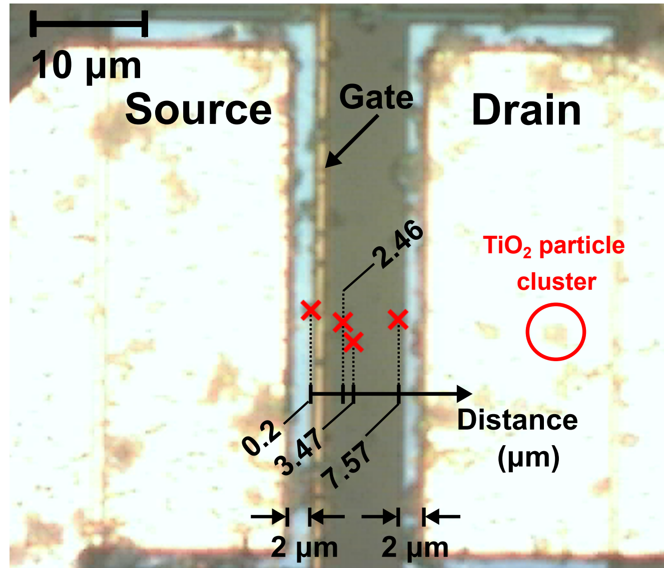


Figure 5.3: Distribution of TiO_2 particles across the MOSFET channel. Figure reproduced from [42].

is 1.95 parallel to the [010] direction [15]. This refractive yields an axial resolution of 7.2μm, for a laser wavelength of 532nm, and a microscope objective with a numerical aperture of 0.5 (see Eqn.3.3). Therefore, temperature values extracted via direct Raman spectroscopy will be averaged over a depth far larger than that of the channel, significantly reducing the sensitivity of the measurement to channel self-heating effects.

Raman nanothermography offers a practical way to circumvent the problem of axial resolution in wide-bandgap semiconductors. This technique exploits the behaviour of Titanium dioxide (IV) anatase (TiO_2) nanoparticles deposited on the device surface [233]. During device operation, TiO_2 particles reach thermal equilibrium with the device channel almost instantaneously, due to their low heat capacity. The channel temperature can then be measured indirectly, by extracting the temperature of each particle using Raman spectroscopy, with the particles acting as thermometers on the surface of the MOSFET channel. TiO_2 nanoparticles were distributed onto the device surface using a drop-cast method. A powder of 99.98% pure TiO_2 (anatase) particles, with radii <25nm, was mixed in ethanol, creating a TiO_2 suspense. Sonication of this suspense in an ultrasonic bath ensured a uniform density of particles throughout the ethanol. The particle–ethanol suspense was drop-cast onto the channel, while the device substrate was heated to 80° using a hot-plate. Rapid evaporation of the ethanol left a distribution of particles over the device surface. Four particles in the channel at four distinct locations on the channel surface were then selected for measurements. These particles were selected based on their central position in the channel, and approximately even spacing. Fig.5.3. shows the particle distribution across the length of the device channel, with the position of each particle marked. Both individual particles and clusters

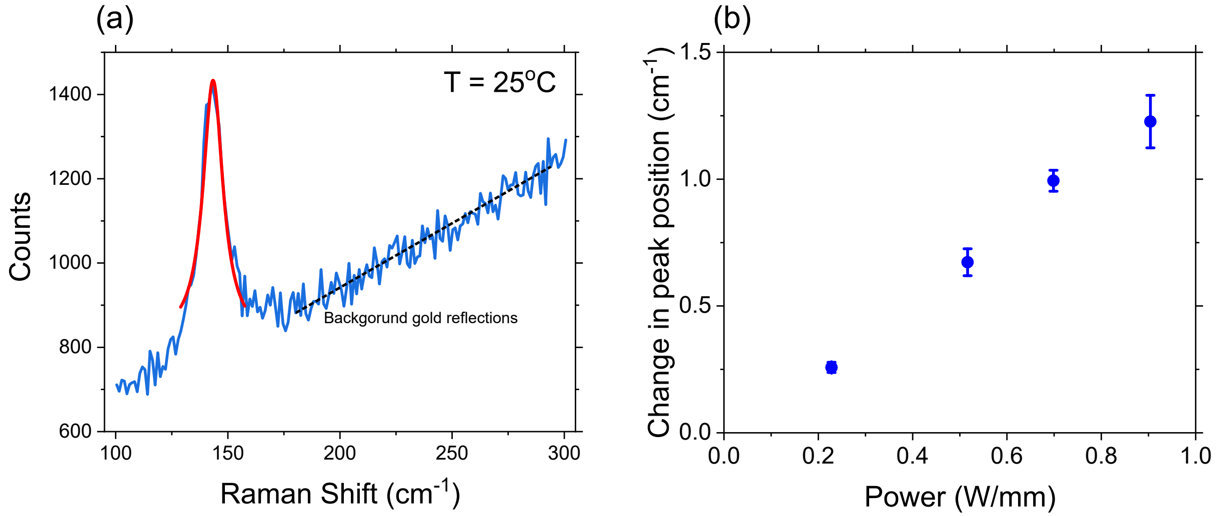


Figure 5.4: (a) A typical room temperature calibration peak of a TiO_2 particle. The zero bias peak is extracted using a Lorentzian fit, as shown by the red line. The linear increase in the background is due to reflection off the gold-plate contacts. (b) The shift in Raman peak position as a function of device operating power.

of particles were observed on the device surface. It was not possible to determine whether Raman measurements were taken using a single TiO_2 particle as opposed to a small agglomerate of particles. This will have little bearing on the measurement, provided that an agglomerate is smaller than the lateral resolution of the Raman system.

During the measurements the wafer was held at 25^oC using a thermal baseplate. A calibration was performed for each particle, with the Raman shift measured while the device was unbiased. This Raman measurement was carried out using a 532 nm Ar+ laser and 0.5 NA objective lens, (corresponding to a beam radius of 0.543 μm). An example of a Raman spectra taken for a TiO_2 is shown in Fig.5.4(a), with the previously reported Raman peak close to 150 cm^{-1} being the most distinct [234]. A linear background subtraction was preformed on this spectra, and the position of the Raman mode peak was then extracted using a Lorentzian fit for each particle, with a small variation in peak position observed between the four particles.

The channel temperature at each particle position was then measured across the channel by applying a dc bias between the source and drain. The bias conditions used were V_G = 0 V and V_{DS} = 2–8 V in steps of 2 V, which corresponded to channel power densities of 0.228, 0.517, 0.698, and 0.904 W/mm. At each bias point, the Raman shift of each particle was measured. A shift in the Raman peak, compared to the zero bias condition, was then extracted as a function of operating power, as shown in Fig.5.4(b). The temperature of each particle at each power was then determined, using a calibration of Raman shift relative to temperature. This calibration consisted of measuring the Raman peak shift of TiO_2 oxide particles held at a constant temperature by a thermal baseplate. Varying the baseplate temperature yielded the peak shift as a function

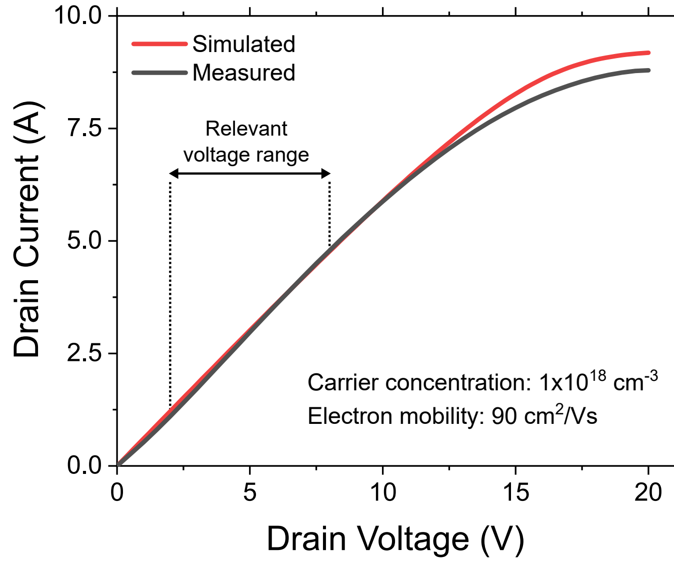


Figure 5.5: A comparison of the simulated and measured I_D-V_{DS} curves of the device, V_{GS} = 0V. The voltage range over which the Raman measurements were performed is marked.

of temperature. This relationship was linear to first order, with a small deviation at higher temperatures. Therefore, a quadratic fit was used to extract an equation relating the peak shift to temperature,

$$\Delta\omega = 0.0000135T^2 + 0.244T - 0.61, \tag{5.1}$$

where the peak shift $\Delta\omega$ is taken relative to a reference temperature of 25.3^oC. This temperature calibration method is well established in the literature [235][236][237][238].

Both electrical and thermal simulations were then performed to compare to the temperatures extracted using the Raman nanothermography technique. 2D electrical simulations were performed in Silvaco ATLAS, implementing a 2D drift diffusion model for the Joule heating distribution. The Joule heating profiles was then used in a ANSYS 3D finite element simulation, to extract a temperature profile over the device. The effective electron mobility in the channel was set to 90 cm^2/Vs, extracted from Hall measurements of the devices. The electron concentration was set to $1x10^{18}$ cm^{-3}, with full activation of the Si-donors assumed. A comparison of the measured and simulated I_D-V_{DS} is shown in Fig.5.5, with the voltage range used in the Raman nanothermography measurements marked. There is a slight disagreement in the saturation voltage of the two curves, however, there is no significant disagreement over the relevant voltage range of these measurements. This is critical for the simulation of the temperature distribution, as the field distribution across the channel has a significant impact on the self-heating profiles (see section.2.4.3). A difference in the measured and the simulated V_{th} of the device was observed, with a measured threshold voltage of V_{th} = -15V, and a simulated threshold of V_{th} = -20V. A potential reason for this disagreement is discussed later in this section.

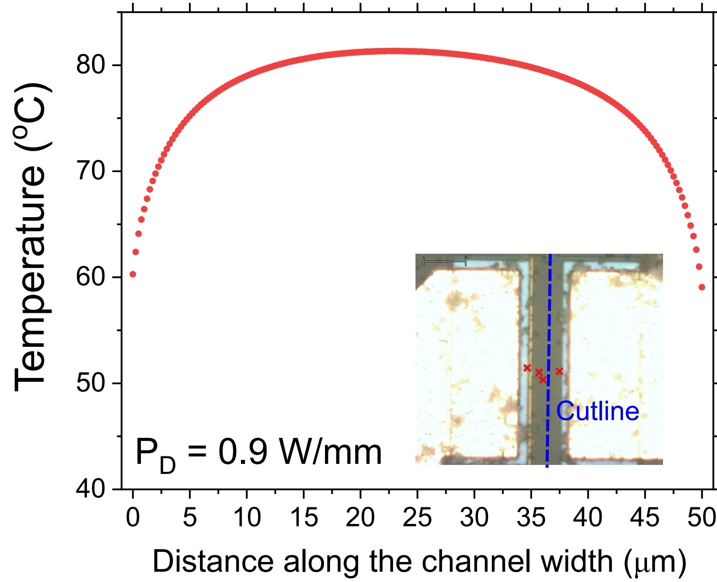


Figure 5.6: ANSYS simulation of the temperature profile of the channel, taken down the gate width (cutline shown in the inset). The temperature across the central 20μm is approximately constant.

5.2.2 Raman Nanothermography Results

The inset of Fig.5.3 shows the position the four TiO_2 particles used for the Raman nanothermography measurements. While these particles are distributed along the entire channel length, they not evenly distributed along the channel width, and are not at the centre of channel. This should not have a significant impact of the extracted temperature profiles of the device, as the temperature at is not expected to vary significantly from the channel centre. This assumption can be confirmed using simulations of the device channel temperature. Fig.5.6 shows a simulated temperature profile along the width of the channel (cutline shown in the inset), with a substrate temperature of 25^oC. It is clear that the variation in channel temperature is insignificant along the central 20μm of the channel width. The temperature drops towards the edge of the channel due to an increase in the lateral heat flux, across the channel surface and also into the metal contacts.

Fig.5.7(a) shows the extracted temperature line profiles taken along the channel, using the particles marked in Fig.5.3, for four different operating powers. The maximum variation in temperature across the channel is approximately 10°C, with the maximum channel temperature observed at the drain side of the gate. The position of the maximum temperature in the channel, and the qualitative shape of the temperature profiles, was consistent across all of the values of power considered. Furthermore, the temperature profile shape is consistent with previous

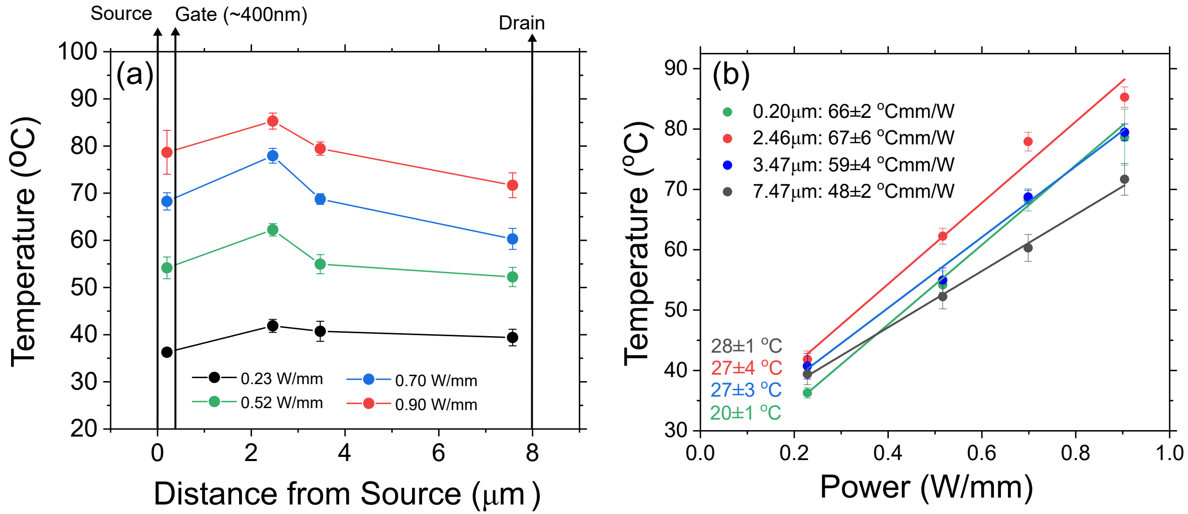


Figure 5.7: (a) The temperature profile of the device, extracted from the four particles in Fig.5.3(a), for four different power. (b) The corresponding values of thermal resistance (R$_{th}$) extracted from (a), using the scaling of temperature with power. Figure adapted from [42].

thermal characterization on β-Ga$_2$O$_3$ MOSFETs reported by Pomeroy *et al.* (see Fig.5.1). The variation in the error bars for each data point reflects the precision of the Lorentzian fit used to extract Raman shift values at each temperature. Fig.5.7(b) shows the power-temperature scaling of each of the particles. From the linear fits the thermal resistance is extracted at each location on channel surface. The intercept of each fit should correspond to the baseplate temperature (25°C).

5.2.3 Simulation Results

The 2D drift diffusion model Silvaco ATLAS simulated Joule heating power profile for V$_{GS}$ = 0V, V$_{DS}$ = 8V is shown in Fig.5.8(a). The values have been normalised to the maximum heating value observed in the device. Fig.5.8(b) shows a cutline taken across the device channel, passing through the position of the peak heating power under the gate. There is a clear peak in Joule heating at the drain-side of the gate. This can be attributed to an increased channel resistance in this region, caused by a narrowing of the channel. This narrowing is due to the presence of a depletion region at zero gate bias, resulting from the built in voltage of the MOS gate structure. This behaviour is similar to that of a partially on device, which will experience significant localised heating over the resistive depletion region at the drain edge of the gate [239]. As well as the heating in the gate region, there is also a significant degree of distributed heating along the length of the device channel, with a consistent heating power 15% that of the peak heating power observed.
The Joule heating profiles, simulated over a drain voltage range of 2-8V, were then loaded into an ANSYS 3D finite element thermal simulation. The thermal conductivities at 300K of β-Ga$_2$O$_3$ were defined as 23.4 Wm^{-1}K^{-1}, 10.7 Wm^{-1}K^{-1} and 13.7 Wm^{-1}K^{-1}, in the [010], [100] and [001]

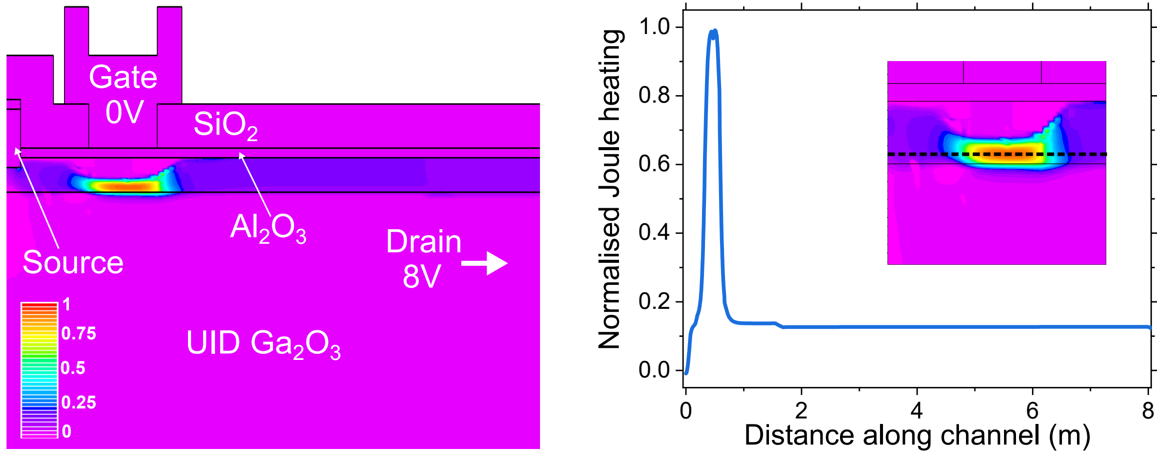


Figure 5.8: A simulation of the Joule heating power in the device channel. (a) A schematic of the device with the normalised Joule heating of the channel (V_{GS} = 0V, V_{DS} = 0V) displayed. (b) A cutline of the Joule heating, for the simulation shown in (a). The position of the cutline is shown in the inset. A heating power approximately 15% of the peak is observed along the entire profile of the channel.

crystallographic directions respectively. The temperature dependence of the thermal conductivity was taken to be the same as those reported by Guo *et al.* [34]. Slomski *et al.* have previously demonstrated that the effect of doping has a negligible effect on the thermal conductivity of β-Ga_2O_3, and so this was not considered in the model [240]. The thermal conductivities of the Al_2O_3, SiO_2 and Au were set to 3 $Wm^{-1}K^{-1}$, 1 $Wm^{-1}K^{-1}$ and 315 $Wm^{-1}K^{-1}$ respectively, with no temperature dependence defined [241][242]. The backside of the device wafer was thermally grounded to a value of 25°C, to replicate the effect of a thermal baseplate.

Fig.5.9 shows the ANSYS simulated temperature distribution for a power dissipation of 0.9 W/mm. The 3D structure of the device consists of the channel, the substrate and the contact metallisation, with a mirror boundary condition applied down the centre of the device. Fig.5.10 shows the temperature profile extracted from these simulations, down the centre of the channel width (from source to drain), compared to the corresponding Raman nanothermography results. The simulated temperature profile exhibits a small step at the position of the gate bar, due to a large heat flux into the gate metallisation, but otherwise exhibits a high degree of symmetry. There is a large drop in channel temperature close to both the source and the drain contacts, which can be attributed to a large heat flux into the contact pads. There is a disagreement between the simulated profile and the measured profile, with the simulated profile overestimating the temperature in the gate-drain access region and underestimating the temperature close to the drain edge of the gate. The high degree of symmetry in the simulated profile, with respect to the centre of the channel, is not consistent with the temperature profile reported by Pomeroy *et al.*

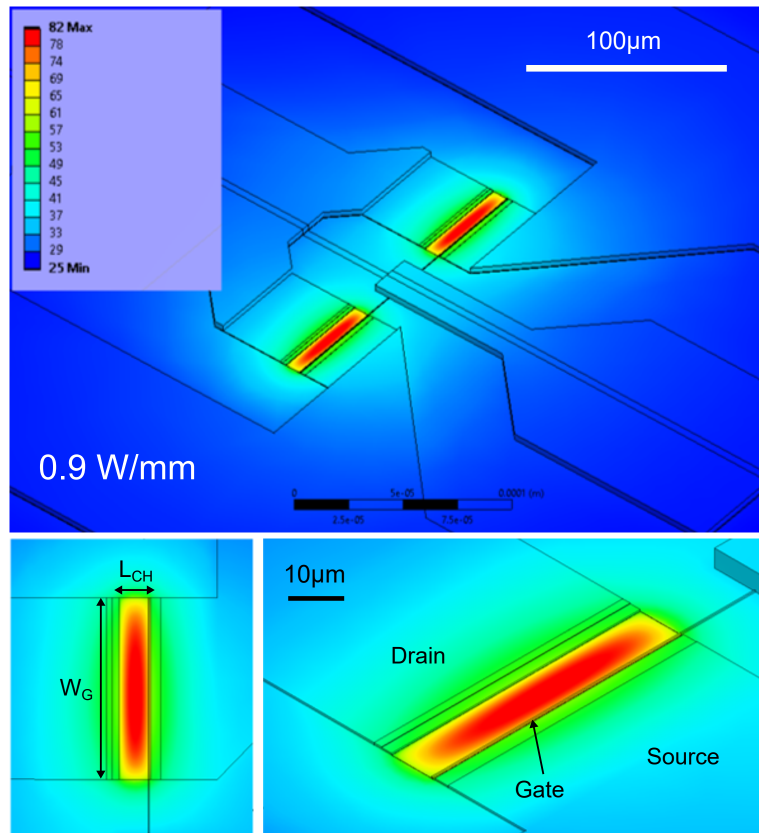


Figure 5.9: ANSYS simulations of the channel 3D temperature profiles of the MOSFET. Top: A view of the device under bias with a power dissipation of 0.9 W/mm. Bottom: Enlarged image of the channel.

(see Fig.5.1). This may be due to the thin channel in the devices considered in this study; a high channel resistivity will lead to a relative increase in the gate-drain access region heating relative to the heating under the gate region. This is especially true at low drain biases (V_{GS} = 0V, V_{DS} < V$_{sat}$), as the absence of large field spikes at the drain edge of the gate results in a more uniform heat generation profile [239].

Despite the gate bias of V$_{GS}$ = 0V, there is a small depletion region under the gate, due to the built in potential of the MOS-CAP gate structure (see Fig.5.8). This depletion region has a limited impact on device self-heating for channel thicknesses of >1μm to 100nm. However, at 65nm, the depletion region leads to a significant narrowing of the channel under the gate. Therefore, it seems reasonable that further reductions in the channel thickness would lead to a relative increase in the self-heating under the gate, as the resistivity of this region increases. A mechanism that could potentially lead to channel thinning is electron trapping in the substrate. It is well established in the literature that charging in the substrate can lead to a back gating effect; a depletion region at the bottom of the channel [184]. This leads to a modulation of the effective

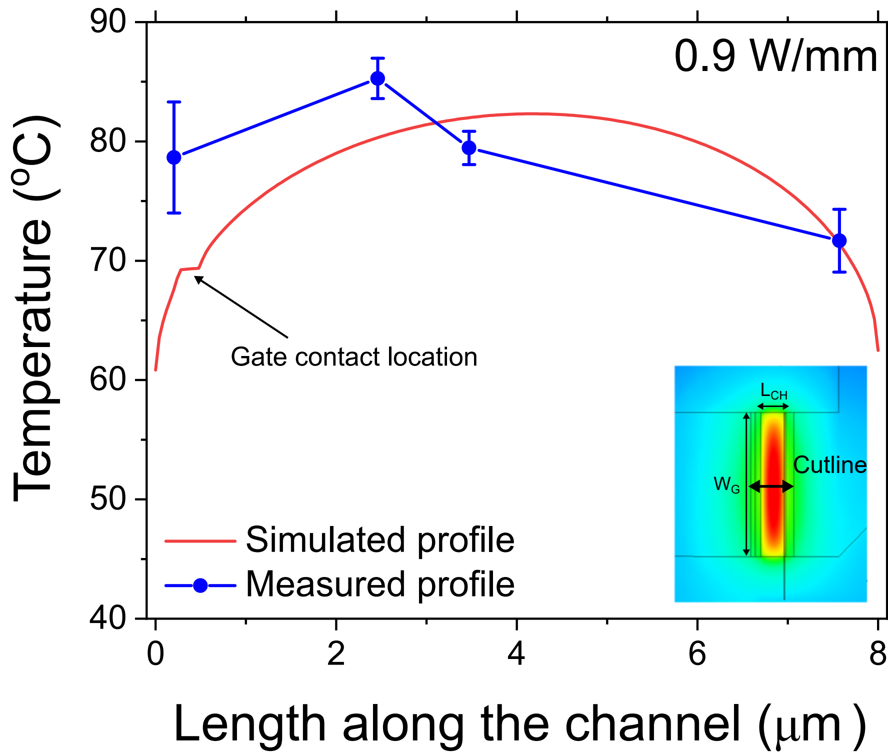


Figure 5.10: A comparison of the simulated and measured channel heat profile for a power dissipation of 0.9 W/mm. Inset: cutline used for the simulation along the length of the channel.

channel width and a corresponding reduction in the device threshold voltage. It is not trivial to measure trapping close to the channel in these devices; standard trap characterisation methods such as CV profiling and deep-level transient spectroscopy require larger area gates. However, trapping effects in Fe-doped β-Ga$_2$O$_3$ substrates are well documented [243][185][244]. This is consistent with the simulated threshold voltage of the device (V_{th} = -20V) being more negative than the experimentally value (V_{th} = -15V). Furthermore, the simulated Joule heating profile possesses a higher degree of symmetry than the experimentally measured profile, suggesting a relative underestimation of the heating under the gate region compared with the channel region. Even a small modulation of 10nm in the channel width would have a significant effect on a 65nm channel. Fig.5.11 shows the effect of channel width on the normalised Joule heating profile of the channel. For each width, the simulation parameters were adjusted to achieve an I_D-V_{DS} curve that matched with the measured curve. For decreasing channel thickness, an absolute increase in the heating across the entire channel was observed, which can be attributed to the increase in channel resistance with decreasing area. Therefore, a thinning of the device channel, is consistent with both the lower symmetry of the measured heating profile and the more negative threshold voltage, (when compared to simulations). It was found that the threshold voltage observed in a

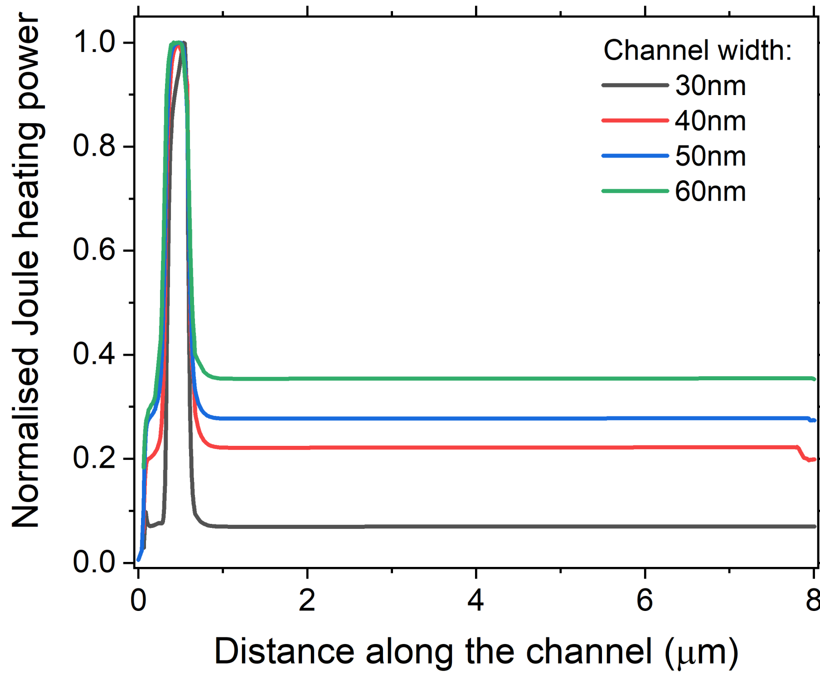


Figure 5.11: The impact of channel thickness on its normalised Joule heating profile, for a power dissipation of 0.9 W/mm.

40nm channel is consistent with the the measured threshold voltage of the device.

5.2.4 Effect of Device Orientation on Self-heating

So far, only one device orientation has been considered, with the device gates aligned to the [001] direction on a [010] substrate. However, it would be reasonable to expect the orientation of the device to have some effect, considering the significant anisotropy in β-Ga$_2$O$_3$'s thermal conductivity (varying between 10 W/mK and 27 W/mK). In order to investigate the impact of device orientation on self-heating an ANSYS simulation was performed. The device was simulated with a gate aligned with the [001] direction, for a constant power dissipation of 1 W/mm. This structure was rotated in steps of 10° relative to the [001] direction, with the [010] remaining perpendicular to the channel surface. This was repeated to cover a total rotation of 150°. For simplicity, an angle of 90° was set between the [001] and [100] directions.
Fig.5.12 shows the average and maximum channel temperatures with respect to the angle between the channel and the [001] direction. Each has been normalised to the maximum value extracted over the entire rotation. It is clear that the in-plane device orientation has no significant impact on self-heating in the channel, with a variation of <1% observed across both parameters. The insensitivity of the self-heating to orientation can be attributed to two factors. The first is that the majority of the heat flux from the channel was directed into the substrate. This

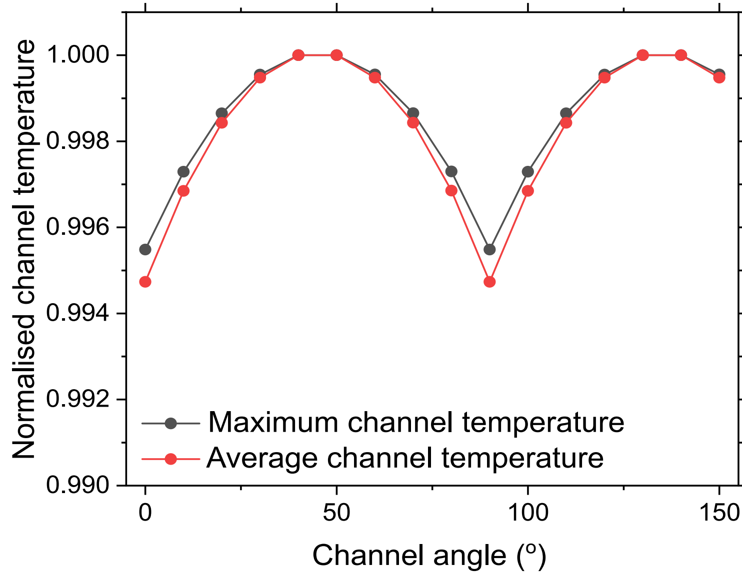


Figure 5.12: The simulated normalised maximum and average channel temperatures as a function of the in-plane channel orientation, for a power of 1 W/mm. The [010] is fixed perpendicular to the channel surface, and the device gate is rotated relative to the [001] and [100] directions. The angle between these two directions is set to 90°.

is particularly true of the centre of the channel, were the lateral temperature gradients were small; the 65nm separating the surface of the channel and the substrate was is significantly smaller than the 8μm channel length and 50μm channel length. The second factor suppressing orientation effects on the self-heating is the size of the metal contact pads. This metallisation was observed to have a significant cooling effect on the channel, with a large lateral heat flux into the pads. The effect of the contact pad thickness was observed to dominate over any changes in the device orientation. As such, the effect of orientation will not be included in the discussion for this section. It is important to note that the insensitivity of self-heating to the device orientation has only been demonstrated in the case of for [010] substrates. Devices on substrates with different growth directions would be expected to exhibit a larger anisotropy.

5.2.5 Pulsed IV Method for Measuring Channel Temperature

While the Raman thermography measurements and simulations provide spatial information about the channel temperature, pulsed IV characterisation can provide an averaged channel temperature and an averaged channel thermal resistance. This technique requires a calibration to be performed (described below), for the scaling of device R_{on} and I_D as a function of temperature. A channel averaged temperature can then be measured as a function of power dissipation in the channel, by extracting R_{on} and I_D from pulsed I_D-V_{DS} curves. The pulsed measurements outline in this section were performed by our collaborators at North Carolina State University and the

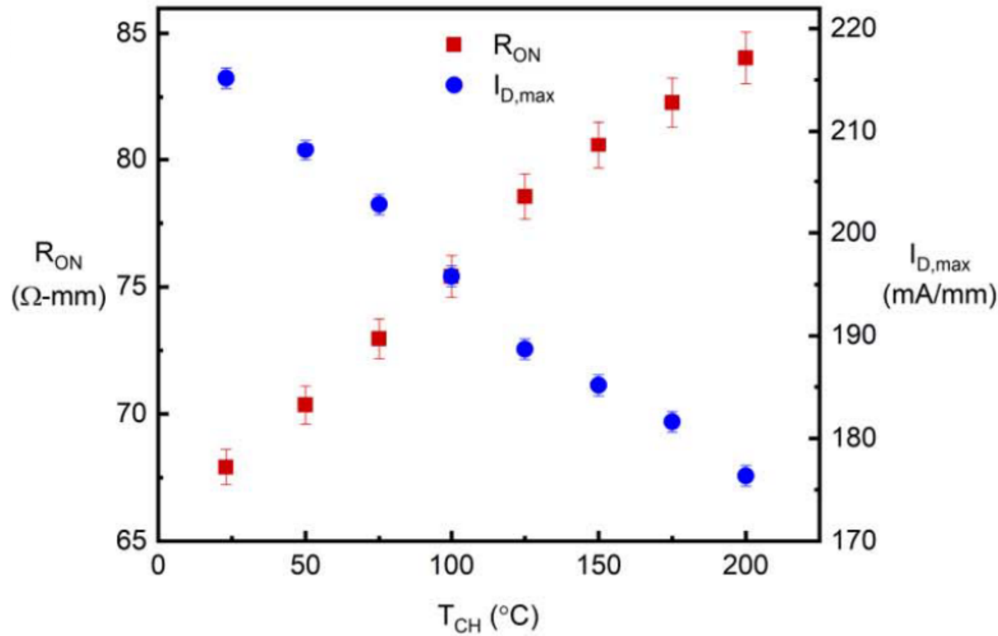


Figure 5.13: The pulsed IV method calibration data, with I$_{Dmax}$ and R$_{on}$ measured as a function of channel temperature. Figure reproduced from [42].

Air Force Research Laboratory [42].

Pulsed IV characterisation of the device was performed, with the substrate held a constant temperature throughout the measurement using a thermal baseplate. A pulsewidth of 200ns, with a duty cycle of 0.02% was used to suppress self-heating in the MOSFETs; a drop in the saturation current was observed when using larger pulse widths, suggesting a significant degree of device self-heating. To calibrate the measurement, the temperature of the baseplate was varied between 25^oC and 100^oC. At each temperature, a pulsed I$_D$-V$_{DS}$ characterisation was taken. The device R$_{on}$ was extracted using a fit to the linear region of each I$_D$-V$_{DS}$ curve (V$_G$ = 0V). The value of the maximum drain current (I$_{Dmax}$) was extracted from the V$_G$ = 0V curve at V$_{DS}$ = 15V. This information was used to equate each R$_{on}$ or I$_{Dmax}$ value with a channel averaged temperature, with the calibration data shown in Fig.5.13.

Self-heating in the device was then achieved by dissipating power in the channel using a non-zero drain voltage Q-point. The current during the Q-period was measured, and the power dissipation calculated using $P_{diss} = I_D V_{DS}$. During the NQ-period, the effect of the power dissipated during the Q-period was quantified by extracting both the device R$_{on}$ and I$_{Dmax}$ from the pulsed I$_D$-V$_{DS}$ characteristic. Fig.5.14(a) shows the change in R$_{on}$ and I$_{Dmax}$ as a function of the power dissipation. The values in Fig.5.14(a) were then plotted as a function of channel averaged temperature (Fig.5.14(b)), using the calibration data shown in Fig.5.13. The channel thermal resistances were extracted using both R$_{on}$ and I$_{Dmax}$, with a high degree of agreement

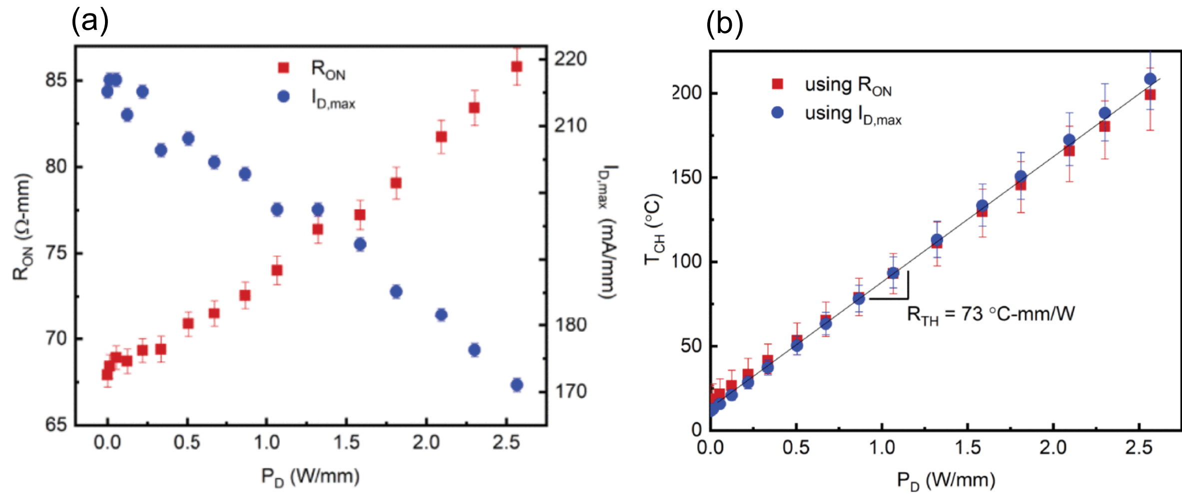


Figure 5.14: (a) R$_{on}$ and I$_{Dmax}$ extracted from I$_D$–V$_{DS}$ characteristics as a function of channel temperature (T$_{ch}$). (b) The thermal resistance of the channel extracted from both the I$_D$ and R$_{on}$ power scaling relationships. Figure adapted from [42].

observed between the two values. It is worth noting that a larger range of operating powers is used in Fig.5.14(b), when compared to the Raman nanothermography method (Fig.5.7(b)). It was not possible to match the same power dissipation in the Raman nanothermography measurements as the devices had to biased for longer periods of time, when compared to the pulsed IV measurements. At higher powers (> 1W/mm) device failure was observed during the course of the Raman nanothermography measurement.

The assumption underpinning the characterisation technique is that the 200ns pulse width is sufficiently small to suppress any self-heating effects in the device channel. To verify this, a transient heating simulation of the device channel was performed, as shown in Fig.5.15. The transient rise in channel temperature was simulated using the Deybe model for the heat capacity of β-Ga$_2$O$_3$, as shown in the inset of Fig.5.15. The Deybe temperature (θ_D), reported by Guo *et al.* [34], was used to generate the Deybe fit. The average channel temperature is report here, as this will have a more significant impact of the drain current, when compared to localised hotspots.

A 200ns pulse width will lead to an approximately 9°C rise in the average channel temperature, but this will not be reflected in the measurement of the channel temperature, as the measurement aperture would not be positioned at the end of the pulse, (see section.3.2.3.) For an aperture positioned at the centre of the pulse, (e.g. a 100ns aperture centred on 100ns), the expected self-heating is only around 6°C. This will lead to small offsets in the calculated channel temperature, and could be mitigated with a pulse widths of the order of 10s of nanoseconds. As the pulsed IV measurement technique applies heating before and after the pulse, via a Q-point drain bias, the 6°C rise will only impact the low-power measurement. This is as heating outside of the pulse will dominate over the 6^oC rise at higher powers. Overall, the self-heating expected over the course of 100ns-200ns should have a minimal impact on the extracted thermal resistance.

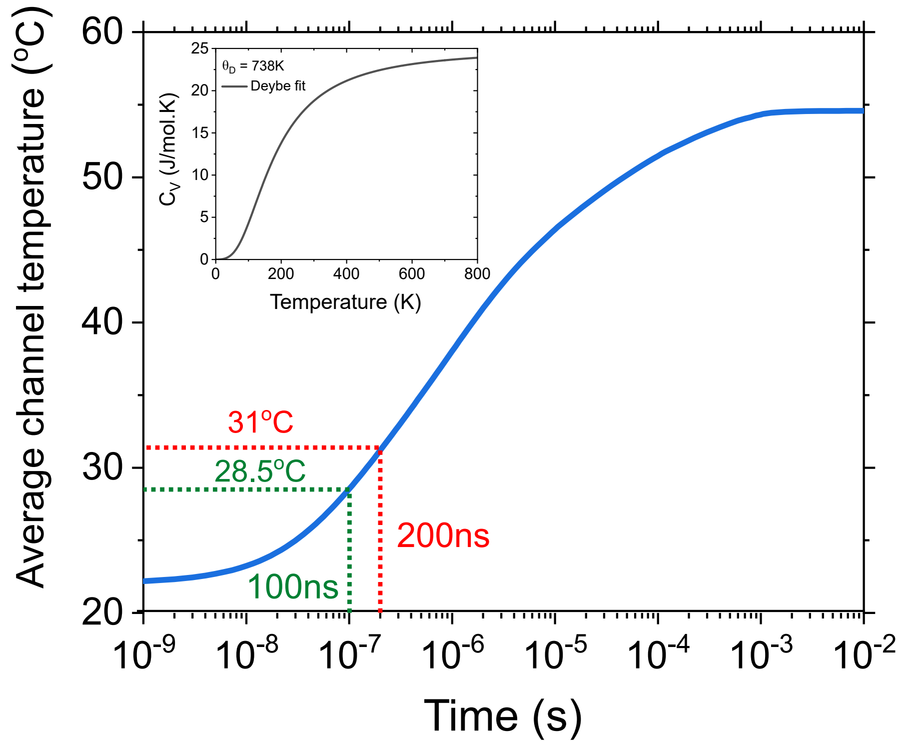


Figure 5.15: A simulation of the transient heating of the device channel. Inset: the Deybe model heat capacity of β-Ga$_2$O$_3$ used in the simulations. The Deybe temperature is taken from [34].

5.2.6 Discussion

There are differences between the Raman nanothermography method (Fig.5.7(b)) and the pulsed IV method that should be considered when extracting the thermal resistance of the device channel (Fig.5.14(b)). A temperature offset is expected between the pulsed IV method and the Raman nanothermography method. The calibration of the pulsed IV method assumes that the baseplate temperature corresponds to the surface temperature of the device. However, air-cooling of the device surface will lead to an overestimation in the surface temperature. This offset will become larger with temperature, as the cooling of the surface will depend on the difference between the local air temperature and the surface temperature. As such, there will be a larger offset at higher powers when compared to lower powers, leading to an overestimation of thermal resistance of the channel. It is also worth noting that the two methods yield temperature-power relationships with differing zero-power temperature values, despite each measurement using the same baseplate temperature. Offsets in the baseplate temperature between the two measurements will have a larger relative impact the lower power points. This will affect the value of the channel thermal resistance; the low-power points have the largest impact the channel resistance linear fits, as they have the smallest error bars. Fig.5.11 also suggests that the different bias conditions used for the two measurements may impact the agreement between the two self-heating profiles. The Raman

nanothermography measurements operate the devices in steady-state, with a constant drain bias of 8V or less applied. Meanwhile, the pulsed IV method relied on drain biases as high as 15V. This difference in applied drain bias had the potential to change the charge of trapping states in the device to differing degrees, leading to variations in the effective channel thickness between the two measurement conditions. Further investigation of this effect is required to quantify its impact on the device self-heating.

Regardless, the two methods yield broadly similar temperature-power relationships and thermal resistances for the device channel. At 0.9 W/mm, the pulsed IV method yields a channel temperature of approximately 82°C (Fig.5.14(b)), while the Raman nanothermography method yields a peak channel temperature of 85°C. This is a high degree of agreement, and is in contrast to what has been observed in a material system such as GaN. Simms *et al.* reported up to a 50% disagreement between average channel temperature values extracted from electrical techniques and the peak channel temperature extracted using Raman micro-thermography [229]. This was attributed to the presence of large hotspots in GaN, which electrical techniques obscured by averaging over the channel. In contrast to GaN HEMTs, the Raman nanothermography measurements (Fig.5.7(a)) and the corresponding simulations of the channel temperature profile (Fig.5.10) demonstrate a lack of hotspots in the β-Ga_2O_3 MOSFETs. This effect has been previously observed by Pomeroy *et al.* in MOSFETs with thicker channels, (see Fig.5.1). The lack of hotspots can be attributed to three factors, the high electrical resistivity of the channel, the high thermal resistivity of β-Ga_2O_3 and the lower biases used in this study. The high electrical resistivity leads to a distributed heating through the gate-drain access region, while the low thermal conductivity of β-Ga_2O_3 limits the heat flux out of the channel. High drain-gate biases would lead to larger field spikes, increasing the degree of self-heating at the gate-drain edge, (as discussed in section.2.4.3) [239]. Therefore, a larger variation in the channel temperature profile may be expected in devices operated at higher power.

The absence of local hotspots and the good agreement between the pulsed IV method and the Raman nanothermography method means that the channel averaged temperature extracted using the pulsed method is suitable for comparing the performance of thin-channel β-Ga_2O_3 MOSFETs. Although the peak channel temperatures will differ from the average channel temperatures, both will scale in a similar fashion for distributed heating in the channel, as can be inferred from Fig.5.7(a) and Fig.5.10. This is significant as the pulsed IV method allows for the rapid characterisation of multiple devices without the need for specialised equipment.

5.3 Investigation of Anisotropic Electrical Performance in β-Ga$_2$O$_3$ MOSFETs

It has already been demonstrated that device self-heating is expected to be effectively isotropic in thin-channel β-Ga$_2$O$_3$ MOSFETs, on a [010] orientated substrate. In this section, an investigation of anisotropic electrical performance in two sets of β-Ga$_2$O$_3$ MOSFETs is presented. Understanding the magnitude and source of any anisotropies in device performance is critical for the fabrication of high performance β-Ga$_2$O$_3$ MOSFETs. If such anisotropies exist, they must be taken into consideration when fabricating devices. If none are observed, then the orientation of sample substrates can be optimised for higher growth rates [245], higher etch rates [246] and integration of more thermally conductive substrates [247].

5.3.1 Devices and Experimental Details

Two separate MOSFET sample sets were used in this study, one fabricated on a wafer provided by the Tamura corporation (GoX) and the other by the Leibniz-Institut für Kristallzüchtung (IKZ). Both sets of MOSFETs had a similar design to those shown in Fig.5.2. The schematics of these two device sets are shown in Fig.5.16. For both samples the channel was grown using MBE and implantation doped with silicon.
A self-aligned gate technology was used for both sample sets. All three contacts were defined using optical lithography to ensure alignment, (see Fig.5.17(a)). Part of the gate was then wet-etched, removing the majority of the gate metallisation, as shown in Fig.5.17(b). This technique allows for well-aligned sub-1μm gate lengths, as shown in Fig.5.17(c) and Fig.5.17(d). These MOSFETs have a channel and a gate orientation that vary in steps of 30°, from a baseline 0° gate angle to a 150° gate angle. A schematic of two of these device orientations is shown in Fig.5.17(e). The gate angles are not defined with respect to the orientation of the substrate; the offset between the device gates and the substrate orientation will be determined later in this study. Devices measured in this section had source-to-drain spacing of 8μm, with gate lengths 200nm.

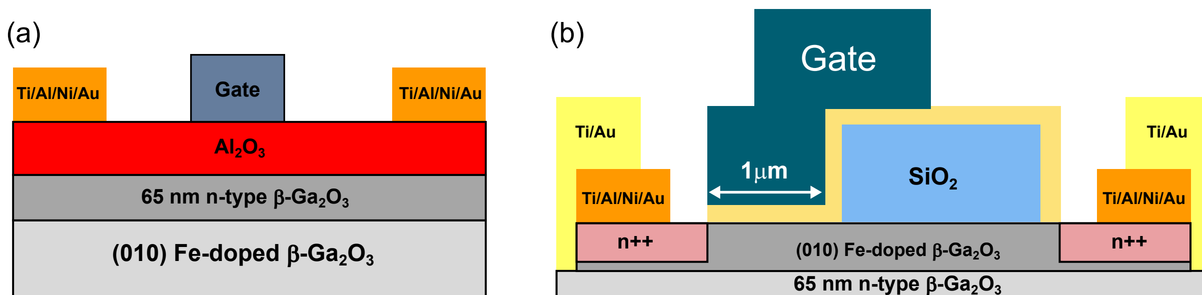


Figure 5.16: Schematics of (a) the GoX sample and (b) the IKZ sample.

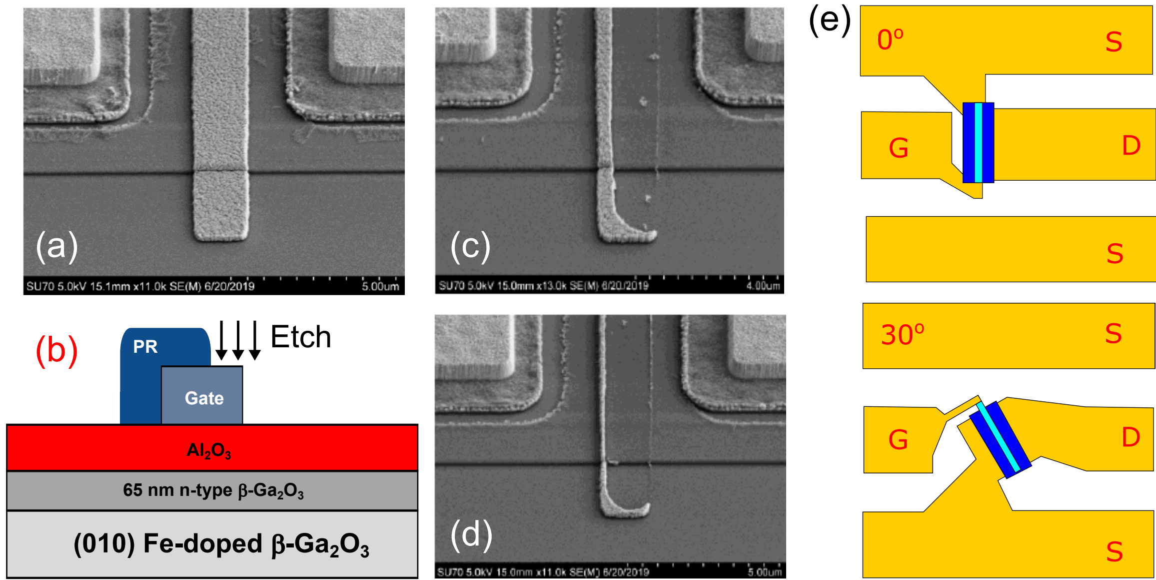


Figure 5.17: (a) A self-aligned gate, with the gate, source and drain pads defined using using optical lithography. (b) Photoresist is used to partially cover the gate and the exposed metal is wet etched. The gate after an etch is shown with dimensions of (c) 750nm and (d) 200nm. (e) Schematic of two transistors with 0° and 30° orientated gates.

5.3.2 Measurements

Three sets of measurements were performed to characterise potential anisotropy in these devices: pulsed IV characterisation; measurements of device R_{on}, extracted from pulsed I_D-V_{DS} curves; and DC IV characterisation as a function of temperature. The purpose of the pulsed IV and R_{on} measurements was to establish whether the electrical characteristics had any orientation dependence across multiple cells on the substrate, and across the two samples. Pulsed characterisation was performed, as opposed to DC characterisation, primarily to avoid trapping effects in the device, which could potentially be induced by the drain bias. Self-heating is not expected to have a strong orientation dependence in these devices, as demonstrated in section.5.3. It was not possible to investigate trapping directly using deep level transient spectroscopy or capacitance-voltage measurements, as both of these techniques require large area gates. Therefore, the presence of interface traps and long time constant trapping states could not be investigated. However, no significant dispersion was observed during stressed pulsed measurements of the devices, suggesting that pulsed IV characterisation was sufficient to suppress the role of trapping on the device behaviour.

DC IV measurements as a function of temperature were used to determine if any observed anisotropy in electrical behaviour was due to an intrinsic variation in electron scattering mechanisms. DC IV characterisation was performed as a function of temperature, opposed to pulsed IV characterisation, as the pulsed Auriga system was not integratable with the Cryogenic measure-

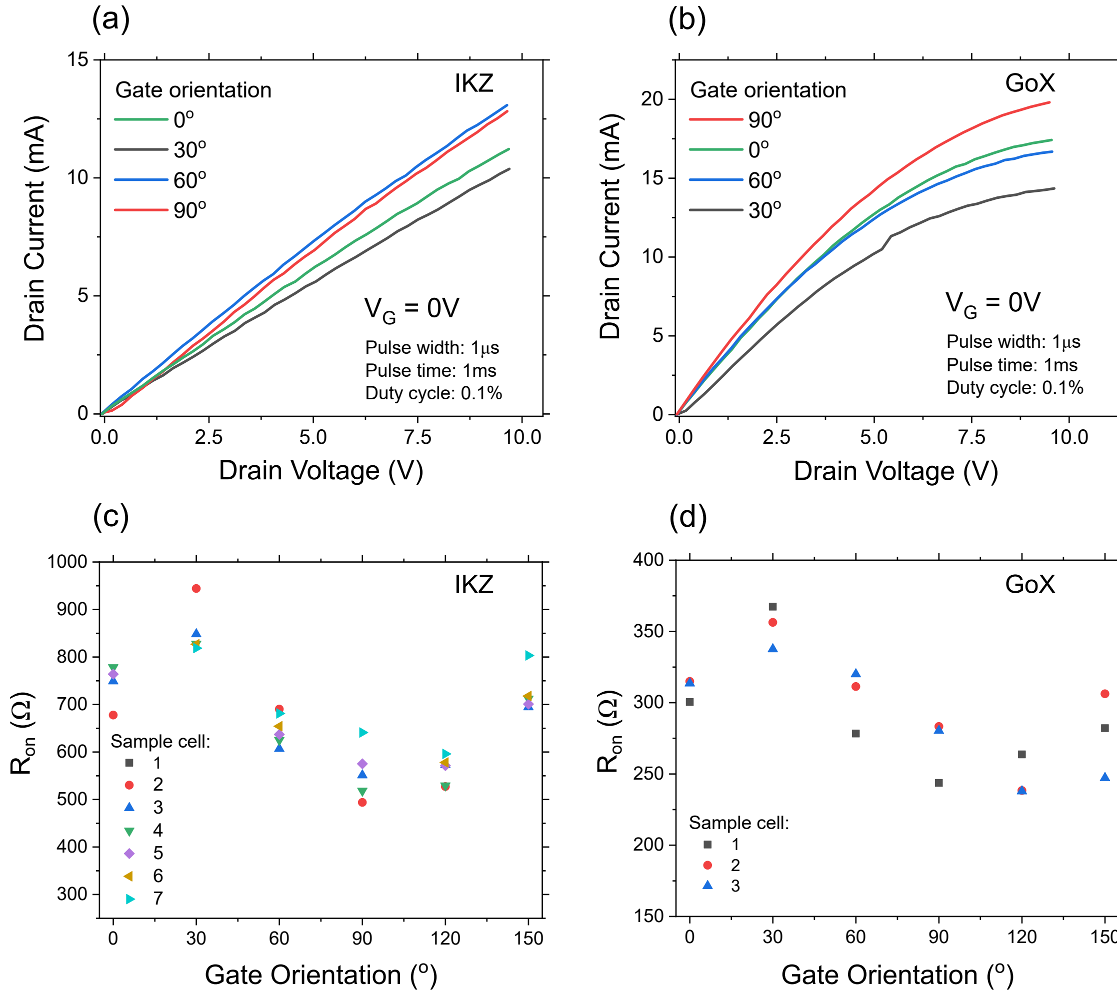


Figure 5.18: Pulsed IV curves taken using four gate orientations on (a) the IKZ sample and (b) the GoX sample. Only the V_G = 0V curves are shown. The values of R_{on} extracted from low voltage (V_D < 0.1V) DC IV sweeps (V_G = 0V). Values of R_{on} were extracted across several device cells as a function of gate orientation for (c) the IKZ sample and (d) the GoX sample.

ments system (see section.3.2.5). All values of R_{on} were extract using linear fits to low voltage DC I_D-V_{DS} curves (V_{GS} = 0V, V_{DS} < 0.5V).

5.3.3 Results of Electrical Charaterisation

Fig.5.18(a) and Fig.5.18(b) show the V_{GS} = 0V pulsed IV curves for four devices with different gate orientations, (in the same sample cell), for the IKZ and the GoX samples, respectively. While current saturation is reached at 10V for the GoX sample, the IKZ I_D-V_{DS} curves remain approximately linear over the voltage range 0-10V. This can be attributed to the difference in contact resistance (R_C) between the two samples; the weaker scaling of drain current with drain voltage for the IKZ sample implies a higher contact resistance or channel resistance. A higher

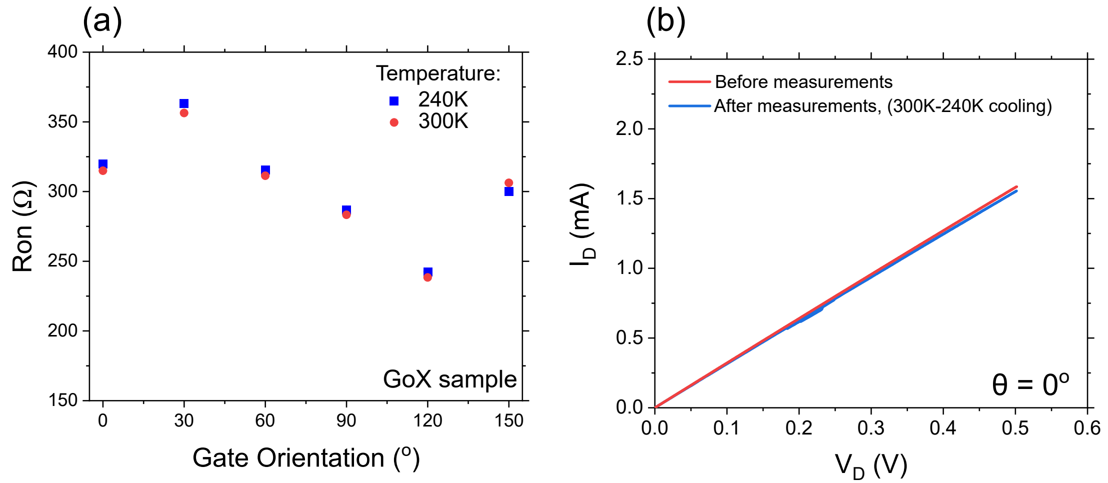


Figure 5.19: (a) Values of R_{on} extracted at two temperatures for the GoX sample. (b) The low-field I_D-V_{DS} curves (300K) used to extract device R_{on}, before and after cooling to 240K. No change is device behaviour is observed.

R_C has the effect of stretching out the IV curve with respect to voltage. It is clear that there is a variation across both samples in the I_D-V_{DS} curves as a function of device orientation.
Fig.5.18(c) and Fig.5.18(d) show the values of R_{on} measured across all available cells on the IKZ and GoX samples, respectively, extracted from low voltage (V_D < 0.1V) DC IV curves at V_G = 0V. A full set of devices (0^0 - 150^0) were not available in each cell, due to gate failure. It is clear that there is a high degree of consistency across the measured cells, with the values of R_{on} being in broad agreement for each gate orientation. An anisotropy in R_{on} is observed across all cells across both samples, with a peak value at 30° and a minimum value at 120°.
Fig.5.19(a) shows the variation in R_{on} for one of the cells the GoX sample, (corresponding to cell 2 in Fig.5.18(d)). No significant difference between the 300K and the 240K measurements is observed. This behaviour was consistent across other sample cells, and also consistent with cells on the IKZ sample. No change in device behaviour, across the relevant voltage range, was observed before and after the low temperature measurements, as shown in Fig.5.19(b). This suggests that there was no significant change in device trapping behaviour for the temperature and voltage ranges used in the measurements shown in Fig.5.19(a). Before attributing the observed anisotropy in R_{on} to an underlying anisotropy in the material, the orientation of the sample substrates must be determined. While both samples have a substrate growth direction of [010], the in-plane orientations of the [100] and [001] directions are not known.

5.3.4 Measurement of Substrate Orientation

Determining the orientation of the sample substrates in critical for investigating the orientation dependence of device behaviour. It is possible to quickly determine the orientation of the substrate

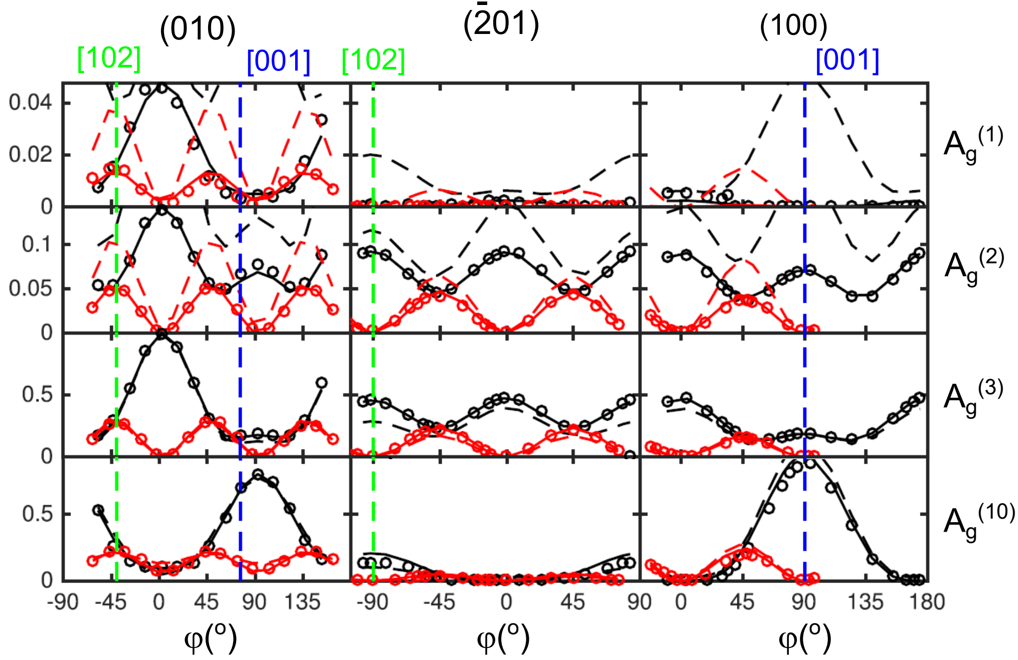


Figure 5.20: Raman scattering intensities for selected Raman modes. Experimental data (circles), fits to model (solid lines) and modelled intensities from ab-intio-calculated tensor elements (dashed lines) are all shown. The black lines represent scattering intensities in the parallel polarisation configuration and the red lines intensities in the cross polarisation configuration. All values are normalised to the peak A$_g$ ^{3} intensity. For the (010)-orientation, ϕ = 0° coincides with the [100]-direction, for the other two orientations ϕ = 0° corresponds to the [010]-direction. Figure adapted from [67].

if the sample has been cut down its cleavage planes, by measuring the relative angles of the sample edges. However, if this is not the case, the anisotropy of phonons modes can be exploited to measure the substrate orientation instead.

Kranert *et al.* previously determined the Raman scattering tensor for all 15 Raman active modes [67]. They investigated the variation in the Raman mode intensity as a function of substrate orientation relative to the polarisation angle of a laser [67]. It was shown that there is a large variation in the scattering intensity of modes as a function of polarisation angle. This behaviour can be exploited to determine the crystal orientation of β-Ga$_2$O$_3$ using Raman spectroscopy. A Raman spectrometer uses a probe laser that is lineally polarised when incident on a sample. By rotating a β-Ga$_2$O$_3$ sample relative to the laser polarisation, and recording the Raman spectrum at each step, it is possible to extract the orientation of in-plane crystal directions.

The 10 A_g Raman modes were used to determine substrate orientation, as the B_g excitations are suppressed on the (010) plane (see section.2.1.1). Fig.5.20 shows the variation in the normalised intensities (with respect to the peak value of the A$_g$ ^{3} mode) of four of the most prominent A$_g$ modes. The solid line represents the expected values extracted from modelling, while the

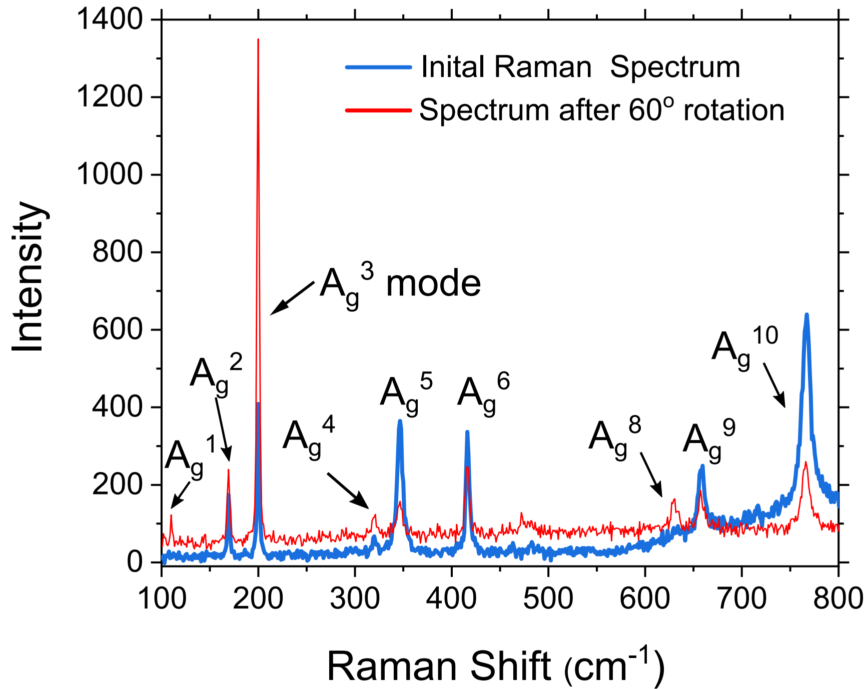


Figure 5.21: Raman spectrum of the β-Ga$_2$O$_3$ GoX sample before and after a rotation of 60°, relative to an arbitrary starting angle. The relative intensities of the majority of the the Raman modes exhibit a significant change. It was not possible to fit to the A$_g$ ^{7} mode due to its low intensity.

data points were measured experimentally, with a high degree of agreement between both data sets. Where applicable, the [001] and [102] directions are marked, with the angle with the ϕ=0° coinciding with the [100] direction for the (010) plane. Only the black lines are relevant to this study, as they represent parallel polarisation of the laser with respect to the plane, (the sample was not measured in the cross-polarisation configuration).

Fig.5.21 shows two measured Raman spectrum of the GoX sample substrate, using an incident laser with a wavelength of 488nm. The first and second spectra are taken with a relative 60° sample rotation. Of the 10 A$_g$ modes, 9 have been identified, with the A$_g$ ^{7} potentially visible at 480cm^{-1}, but not distinct enough from the background to be distinguished. It is clear that the sample rotation has lead to a relative change in most of the modes, with the A$_g$ ^{4} mode exhibiting the least change; it is expect that this mode's intensity will have the least contrast with angle [67]. On the basis of these spectra, the A$_g$ modes 2, 3, 5, 6 and 10 were chosen to determine the orientation of the sample. The samples were rotated in steps of 10°, and the Raman spectra at each was taken. For each spectra, a Lorentzian fitting function was used to extract the peak intensity of the chosen modes. The measured variation in intensity as a function of angle, for the GoX sample, is shown in Fig.5.22(a). The minima of the A$_g$ ^{2} and the A$_g$ ^{3} modes coincide with

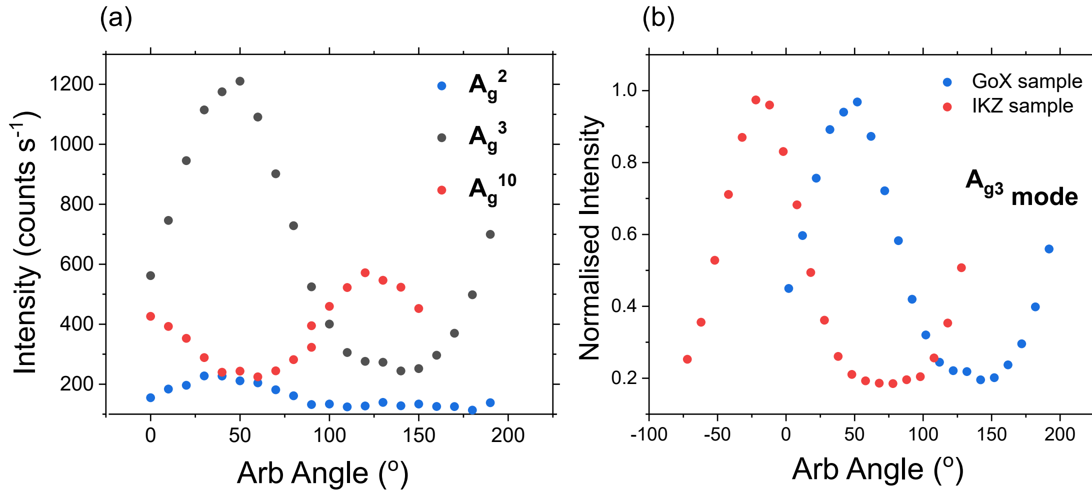


Figure 5.22: (a) Three modes measured for the GoX sample as a function an arbitrary angle between the device substrate and laser polarisation angle. A clear peak is visible for each mode. (b) The 50° offset between the two samples demonstrates that there is a difference in orientation their device gates, with respect to the substrate.

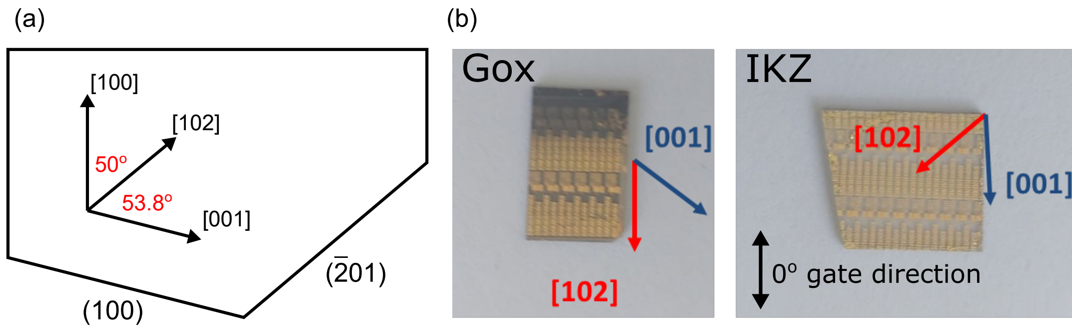


Figure 5.23: (a) The crystalline directions and cleavage plane angles of a [010] β-Ga$_2$O$_3$ substrate. (b) The Gox and IKZ sample wafers with the crystalline directions marked. The 0° gate angle is aligned with the vertical direction.

the maxima of the $A_g{}^{10}$ mode. This is expected behaviour of the modes at $\phi = 0^o$, (see Fig.5.20). Therefore, it can be determined that the [100] direction is 50° offset from the 0° gate in the GoX sample. This procedure was repeated for the IKZ sample. Fig.5.21(b) shows the $A_g{}^3$ mode peaks for the two samples, with a clear $\approx 50^o$ offset.

From the data shown in Fig.5.22, it is possible to map the crystalline axes onto the sample wafers, with reference to the coordinate system shown in Fig.5.23(a). By identifying the [100] direction, the orientation of the [102] axis can be determined for both samples. Fig.5.22(b) shows the extracted crystal axis orientations projected onto images of the samples. Both samples are orientated in the picture in such a way that the vertical direction is aligned with the 0° device's gate. For the GoX sample, the 0° gate are approximately aligned with [102] direction, while the

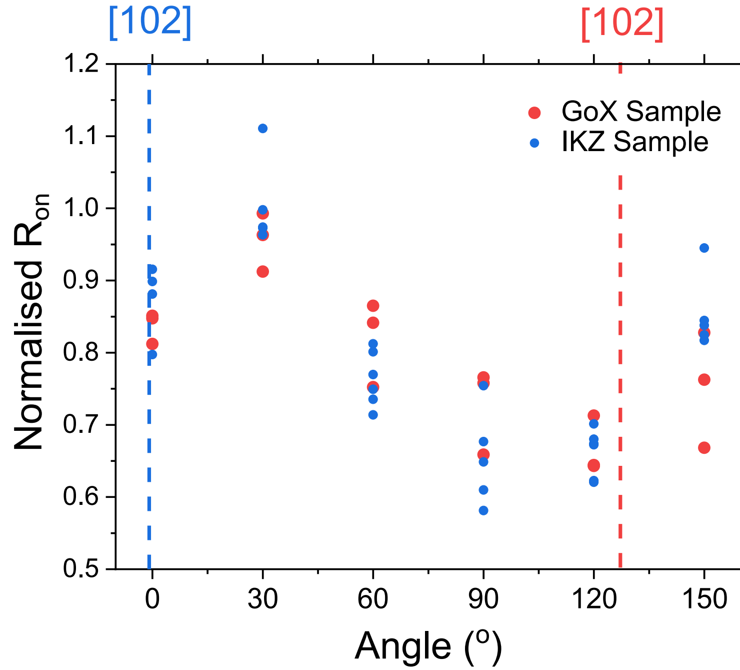


Figure 5.24: The values of R$_{on}$ for both samples, as a function of orientation, normalised against the 30° device R$_{on}$. The orientation of the [102] direction is marked for both samples.

0° gates are approximately aligned with the [100] direction for the IKZ sample.

A comparison of the R$_{on}$ values for both samples is shown in Fig.5.24. Here, the values for each sample have been normalised to one of the values extracted from a 30° orientated device. The angle of the [102] directions for each of the samples is indicated by the dotted lines. It is clear that the variation in device R$_{on}$ with gate angle is not related to the orientation of the [102] direction, (the same is also true of the [100] direction).

5.3.5 Discussion

A clear anisotropy in the pulsed IV characterisation of both sample sets has been observed, (Fig.5.18(a) and Fig.5.18(b)), with the device R$_{on}$ varying as a function of gate angle. This variation in R$_{on}$ exhibits a weak temperature dependence, as shown in Fig.5.19(a). Any effects of trapping on the device R$_{on}$ can be discounted, as there is no change in the device behaviour before and after measurements (Fig.5.19(b)), suggesting that the range of biases used did not induce any trapping effects in the devices. Furthermore, as shown in Fig.5.24, the observed anisotropy does not correspond to the orientation of the substrate. Therefore, the anisotropy cannot be attributed to intrinsic variations in the properties of β-Ga$_2$O$_3$. Instead, problems associated with the fabrication of these devices must be responsible.

The insensitivity of the observed anisotropy to orientation, and its consistency across both samples sets, suggests that it is related to either the contact geometry or the e-beam defined

gates of the devices. Variations in contact geometry (as seen in Fig.5.17) can be discounted, as the resulting changes in sheet resistance would be far smaller than the channel resistance. Instead, the anisotropy is attributed to variations in the gate geometry as a function of device orientation. This is consistent with the variation in normalised device R_{on} shown in Fig.5.24, as changes in gate geometry with angle would have a large impact on the transport in the channel. It is suggestive that the maximum and minimum normalised R_{on} are separated by an angle of 90°, indicating that the fabrication process yields inconsistent results in the x and y directions.

It is possible that anisotropies in the intrinsic properties of β-Ga$_2$O$_3$ are obscured by large variations in the processing of these devices. There are two principle explanations for potential anisotropy in β-Ga$_2$O$_3$ that have been previously discussed in the literature. The first is variations in the electron mobility due to anisotropic scattering by polar-optical phonon modes. There is some disagreement in the literature about the impact anistropic scattering on the mobility of β-Ga$_2$O$_3$. Ghosh *et al.* argued that a variation in the coupling strength of phonon modes will vary strongly in different crystal directions. In this work, they performed ab initio calculations of electron–phonon coupling in β-Ga$_2$O$_3$, finding that the room temperature low-field mobility of electrons is limited by interactions with the 21 meV phonon mode [248]. A significant variation in the coupling strength of this mode phonon was observed down different crystalline directions. This was attributed to the polarisation of different modes, as the polar-coupling strength in a given direction is determined by the projection of the net dipole strength along that direction. However, Golz *et al.* suggest that the variation in electrical conductivity down different crystal directions is no more than 6%, extracted from a 3D conductivity tensor, constructed from Van der Pauw of several β-Ga$_2$O$_3$ substrates with different growth directions [249]. Furthermore, this close to isotropic behaviour was observed over the temperature range of 175K - 380K. This seems to be inconsistent with experimentally measured anisotropies, such as a 15% variation in field-effect mobility observed by by Wong *et al.*, extracted along two perpendicular directions in a set of FatFETs [119]. The minimum mobility was observed down the [001] direction, and the maximum perpendicular to the [001] direction. Similarly, a 20% variation in the Hall mobility was observed between the (010) plane (78 cm^2/Vs) and the (001) (98 cm^2/Vs) plane by Villora *et al.* [250]. As the anisotropy in electron-phonon scattering cannot account for a variation this large, a second mechanism must be responsible.

This second mechanism, responsible for the measured anisotropy in electron mobility, is most likely variations in conductivity caused by structural defects in β-Ga$_2$O$_3$. In particular, the the formation of grain boundaries in β-Ga$_2$O$_3$ during growth is expected to be highly anisotropic. Fiedler *et al.* directly observed the presence of incoherent twin boundaries along the (001) plane using TEM [251]. These boundaries exhibited both dangling bonds and local lattice relaxations. Assuming that the dangling bonds form deep acceptor states, they were able model a minimum current flow down the [001] direction, and a maximum down perpendicular to this direction, consistent with the Hall measurements reported by Villora *et al.* and Wong *et al.* [250] [119].

The anisotropy in conductivity and mobility arises form the formation of space charge regions along these boundaries, due to the trapping of negative charge in the deep acceptor states. Electrons travelling perpendicular to such boundaries would have their mobility suppressed by an additional barrier term ($\mu_{barrier}$). This barrier has an associated activation energy of E_a, with the barrier mobility term taking the form [249],

$$\mu_{barrier} = \mu_0 e^{\frac{E_a}{kT}}, \tag{5.2}$$

where μ_0 is a constant.

The degree of anisotropy in electron mobility should have a strong temperature dependence, whether it is due to variations in electron-phonon scattering rates or due to the presence of grain boundaries. In the case of electron-phonon scattering, the temperature dependence is due to the transition between optical-polar phonon scattering limited mobility and ionised impurity scattering limited mobility. Impurity scattering is an isotropic process, as opposed to optical-phonon electron scattering [80]. As such, a change in temperature should effect the relative anisotropies observed in different crystalline directions. Fig.2.6(b) shows that, over the temperature range of 300K-240K the optical-polar phonon limited mobility will approximately increase by a factor of three, and the ionised-impurity limited mobility should decrease by a factor of two. The cross-over transition temperature for the two processes is approximately 250K. Meanwhile, in the case of grain boundaries, a strong temperature dependence will also be observed. The exponential relationship in Eqn.5.2 demonstrates that a reduction in temperature will lead to a rapid decrease in electron mobility. Fig.5.19(a) shows that no significant variation in the anisotropy is observed over the temperature range 240K-300K. The observed lack of temperature dependence over the range 240K-300K suggests that the impact of any intrinsic variations in β-Ga_2O_3's properties are insignificant in these devices.

An observed anisotropy in device R_{on} has been shown to be insensitive to substrate orientation, and has been attributed to variations in gate fabrication. Intrinsic variation in mobility may also be be present, however, variations in device processing dominate over any potential intrinsic effects. This highlights the fact that, as a relatively novel semiconductor, the processing of β-Ga_2O_3 devices is far from optimised. As long as significant processing variations are present in the fabrication process, the layout of devices should not be determined by a potential anisotropy in the electrical properties of β-Ga_2O_3. Instead, device layout should be optimised to satisfy considerations such as maximising device density, device yield and ensuring desirable properties such as lower contact resistance.

5.4 Conclusions

Raman nanothermography measurements and coupled electrical and thermal simulations were used to investigate self-heating in a set of thin-channel β-Ga_2O_3 MOSFETs. An absence of hotspots was observed in the Raman nanothermography measurements and the simulations, with

difference in the heat profiles extract from both techniques attributed to a possible modulation in the channel thickness. Differences in the thermal resistances extracted using the Raman nanothermography technique and a pulsed IV technique, previously reported on by Blumenschein *et al.* [42], can be attributed to differences in the temperature offsets in both measurements, and the larger range of powers covered in the pulsed IV technique. Regardless, there was a high degree of agreement between the two methods. This, and the absence of hotspots in the device, leads to the conclusion that the pulsed IV characterisation is suitable for accessing device lifetime due to self-heating in thin-channel β-Ga_2O_3 MOSFETs, with the extracted average channel temperatures scaling with the peak channel temperatures. This is significant as the pulsed IV technique is more widely applicable and less time-consuming than the Raman nanothermography technique. Simulations confirm this will be the case for all lateral device orientations on a [010] substrate, with the anisotropic thermal conductivity of β-Ga_2O_3 having no significant impact on the device self-heating.

Having established that there is no significant anisotropy expected in device self-heating, the electrical anisotropy in two sets of thin-channel β-Ga_2O_3 MOSFETs was investigated. Pulsed IV characterisation of MOSFETs with varying gate orientations revealed a variation in the I_D-V_{DS}. Measurements of device R_{on} as a function of device orientation demonstrated a large anisotropy across all measured cells, and across both sample sets. The lateral orientation of the device gates were then determined with respect to the substrates using Raman spectroscopy. It was found that the anisotropy in device R_{on} did not correlated with any underlying crystalline direction in the substrate, and that the absolute values of R_{on} were insensitive to the temperature, over the range of 300K-240K. As such, the observed anisotropy could not be attributed to any intrinsic properties of β-Ga_2O_3. Instead, this anisotropy was attributed to variations in the fabrication of the device gates. This highlights the need to optimise the fabrication of devices in an emerging semiconductor such as β-Ga_2O_3, as problems associated with processing dominate over any variations in the intrinsic material properties.

Chapter 6

The Location and Impact of Trapping States on β-Ga$_2$O$_3$ Devices

The commercialisation of β-Ga$_2$O$_3$ for power applications hinges on the ability to fabricate devices with stable behaviour when subjected to high-bias stresses. Memory effects in such devices have the potential to limit the application space of β-Ga$_2$O$_3$, particularly in the case of high-bias switching. The charging of trap states can lead to large and semi-permanent changes in device behaviour. Understanding the impact of such states on β-Ga$_2$O$_3$ device behaviour is critical to mitigating their effects. In this chapter, two studies are presented, both of which are concerned with extracting trap state locations and trap state energies in both lateral and vertical devices. Each study attempts to quantify the impact of these trap states on device performance. The first study uses a set of β-Ga$_2$O$_3$ MOS-CAP test structures, provided by our collaborators at Cornell University, USA. The second study used a set of field-plated β-Ga$_2$O$_3$ MOSFETs, provided to us by our collaborators at the National Institute of Information and Communications Technology, Japan.

6.1 Introduction

The (ultra)wide-bandgap of 4.9eV in β-Ga$_2$O$_3$ allows for a wide range of conduction and valence band trap energy offsets. Deep-level states can possess detrapping time constants that far exceed the lifetime of a typical device, inducing semi-permanent changes in device behaviour. The problem of electron trapping manifests itself in many features of a devices characteristics; current collapse and knee-walkout in a device's I_D-V_{DS} output-characteristics have the potential to severely limit high voltage performance. Both bulk and interface/surface traps in power devices can lead to a large device dynamic on-resistance (R_{on}), resulting in significantly increased power

losses. This presents a problem for the touted high-voltage applications of β-Ga_2O_3, the primary motivation behind much of the current research into the material. Addressing the nature and origin of these traps is necessary precursor to the commercialisation of this new technology. To do this, it is critical to understand the impact of traps states on device behaviour and reliability, and as such it is necessary to understand the location of traps within a device's structure.

Previous work into trapping in β-Ga_2O_3 has mostly focused on theoretical calculations and measurements of bulk samples. Less has been done to quantify how the trapping states affect device performance. McGlone *et al.* previously reported on the existence of a deep-level trap, with activation energy (E_a) of 0.77eV, in delta-doped MESFETs [179]. This trapping state was observed to induce threshold voltage instabilities in the device. It is probable that the same trapping state was also responsible for the problem of drain current lag in a set of MOSFETs, reported by Polyakov *et al.* [252]. Trapping states have also been shown to degrade the performance of charge blocking layers in lateral β-Ga_2O_3 MOSFETs. Mishra *et al.* observed enhanced leakage currents and threshold voltage instabilities in set of vertical MOSFETs, after UV illumination. This was attributed to a deep-level trapping state in an Mg-implantation doped charge blocking layer [184]. Recovery of the initial device behaviour required current injection into the charge blocking layer, which was electrically isolated from channel and substrate in the zero bias condition. Neal *et al.* reported enhanced device R_{on} and reduced breakdown voltages in Si-doped β-Ga_2O_3 Schottky Barrier Diodes. This behaviour was the result of changes in the occupancy of partially ionized shallow-level bulk traps, with a conduction band offset of 0.11 eV [253]. All of these studies have highlighted the significance of trap state location within the device structure. Although all studies observed similar changes in device behaviour, such as threshold voltage instabilities, the recovery times of each set of devices were strongly dependent on both activation energy and trap location dependent. Adding to such work is the focus of this chapter.

6.2 Trapping at Al_2O_3/β-Ga_2O_3 Interfaces

In this section, trapping at an Al_2O_3/β-Ga_2O_3 interface is investigated by means of capacitance-voltage characterisation. A kink in the CV characteristics in a MOS-CAP structure indicates the presence of trapping states. High bias stressing leads to the emergence of a distinct trapping ledge in the CV characteristics. This ledge is consistent with a trapping state at the Al_2O_3/β-Ga_2O_3 interface, demonstrated with simulations of the CV characteristics. Observed hysteresis in the CV characteristic is shown to be consistent with a deep-level interface trapping state, with the presence of the hysteresis dependent on both the trap state conduction band offset and the sweep rate of the measurement. A comparison of the theoretical CV characteristics with the measured characteristics of the device revealed the presence of fixed oxide charge and background interface trap charge that is independent of the trapping ledge. Charge density values were extracted from simulations, and used to determine the upper bound surface potential observed over the ledge.

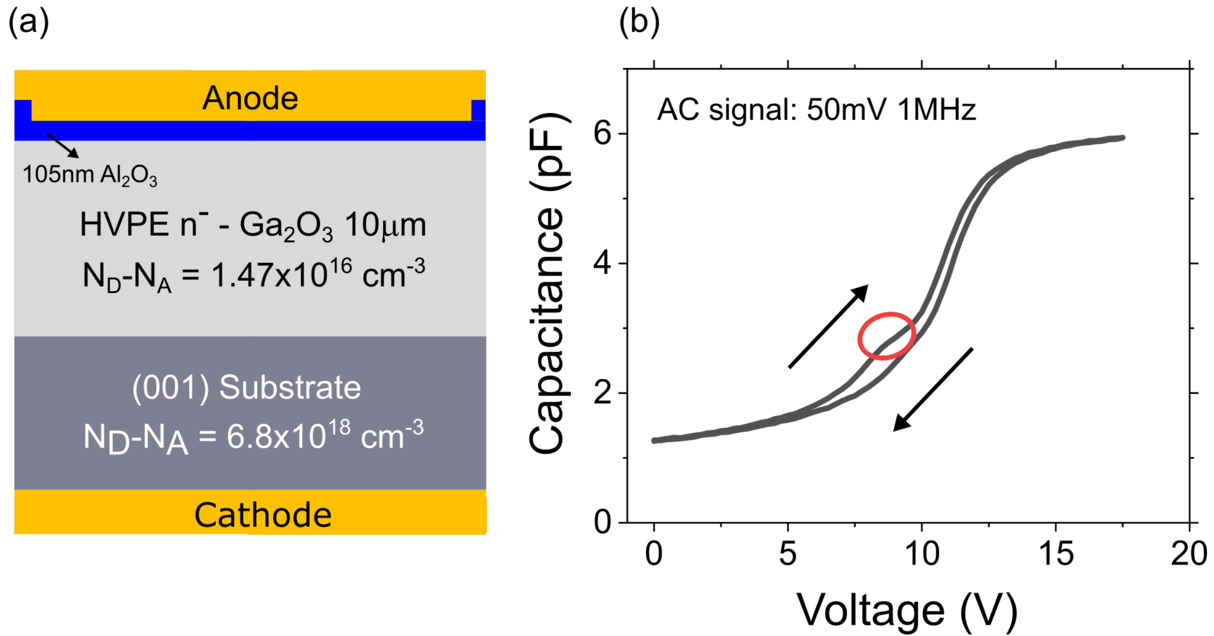


Figure 6.1: (a) A schematic of the MOS-CAP device structure used in this study. (b) The CV characteristic of the MOS-CAP structure, with both an up and a down sweep. The circle marks a kink in the up sweep of the CV curve, and represents a deviation from the expected device behaviour.

This provided an upper bound interface trap state energy of 2.3 eV. The MOS-CAP structure used in this study is shown in Fig.6.1(a). This device belongs to the same device set presented in chapter.4. The anode of the MOS-CAP is isolated from the doped, HVPE grown β-Ga_2O_3 by a 105nm ALD grown Al_2O_3 layer. A Ti/Au layer at the bottom of the substrate forms a cathode, while the anode is formed by depositing Ni on top of the oxide layer. Each MOS-CAP is circular, with a radius of 45μm. A detailed description of the device fabrication can be found in Li *et al.* [33].

6.2.1 High-voltage CV Characterisation

Fig.6.1(b) shows the CV characteristic of the MOS-CAP structure, using a 1MHz AC signal with a peak-to-peak voltage of 50mV. The accumulation capacitance of 6pF is consistent with an oxide thickness of 95nm, close to the reported 105nm ALD grown layer. A deviation from the typical CV curve profile is observed on the up sweep, at approximately 7.5V, in the form of a kink in the capacitance (as indicated by the red circle in Fig.6.1(b)). No kink is observed on the down sweep. The hysteresis and the kink suggest some charging mechanism in the MOS-CAP; the difference between the integral of the up and down sweeps yields the total charge stored by the capacitor over the course of the measurement. The fact that this value is non-zero implies that non-capacitive charging has occurred.

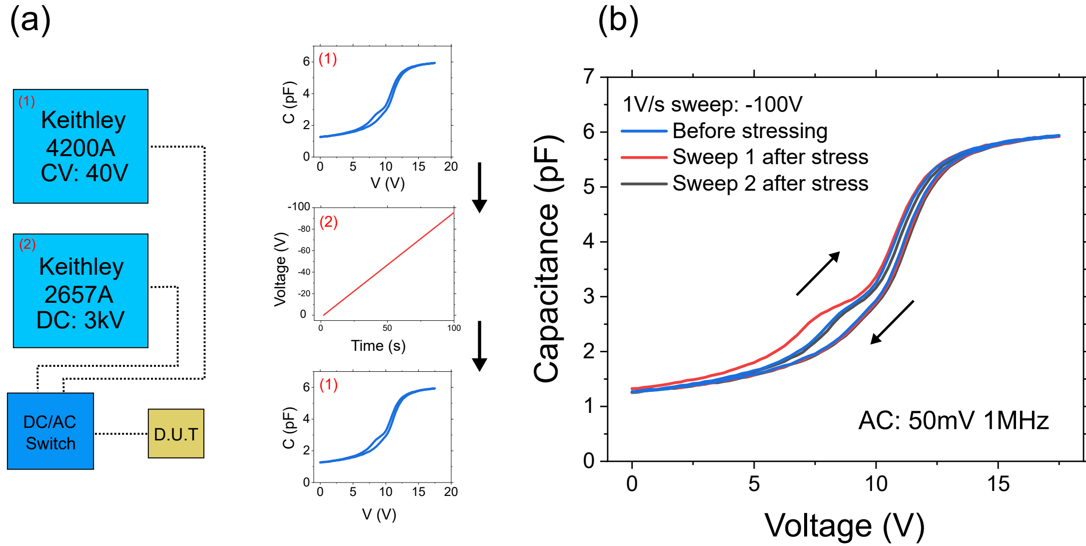


Figure 6.2: (a) A schematic illustrating the measurement configuration used to investigate the CV kink. A Keithley high-voltage 2657A 3kV source and a Keithley 4200 CV SMU are connect to the same device under test (DUT) using a CV/DC switching interlock box (Keithley 8020). A CV sweep is taken before and after stressing the device. The stressing consists of a 1V/s sweep of the MOS-CAP anode to some negative bias. (b) The change in CV characteristics due to a -100V stress sweep. The kink becomes more prominent after stressing, with complete recovery observed in a subsequent sweep.

The kink in the CV up sweep merits further investigation, as this feature is possibly related to an electron trapping mechanism. To this end, negative bias stressing of the device was used to investigate this feature. Fig.6.2(a). shows the measurement configuration used to stress the device. A high-voltage Keithley 2657A 3kV system was integrated with a Keithley 4200 CV SMU via a Keithley 8020 interlock system. The interlock system allows for switching between the high-voltage system SMU and the CV SMU, without the need to change the cabling of the system or the need to reprobe the device. This is critical as any movement in the cabling or probes would necessitate a recalibration of the CV SMU. With this setup, it was possible to bias stress the device, and then to immediately measure the CV characteristics, as shown in Fig.6.2(a). An initial CV sweep was taken, followed by a bias stress of the device that consisted of a 1V/s ramp to a negative anode bias. Several CV sweeps were then taken immediately after stressing to monitor changes in the device behaviour and device recovery. Fig.6.2(b) shows the CV sweeps taken before and after a -100V stress ramp of the anode. The CV sweep taken before the stress exhibits the kink in the up sweep seen in Fig.6.1(b). Immediately after stressing the device, the kink is observed to become more prominent, covering a wider voltage range. A second CV sweep demonstrated that the MOS-CAP quickly recovers to its prestress state.
Fig.6.3(a) shows CV sweeps taken immediately after five stress sweeps (covering a voltage range of -100V to -500V), compared against the initial behaviour of the device. The stress conditions were

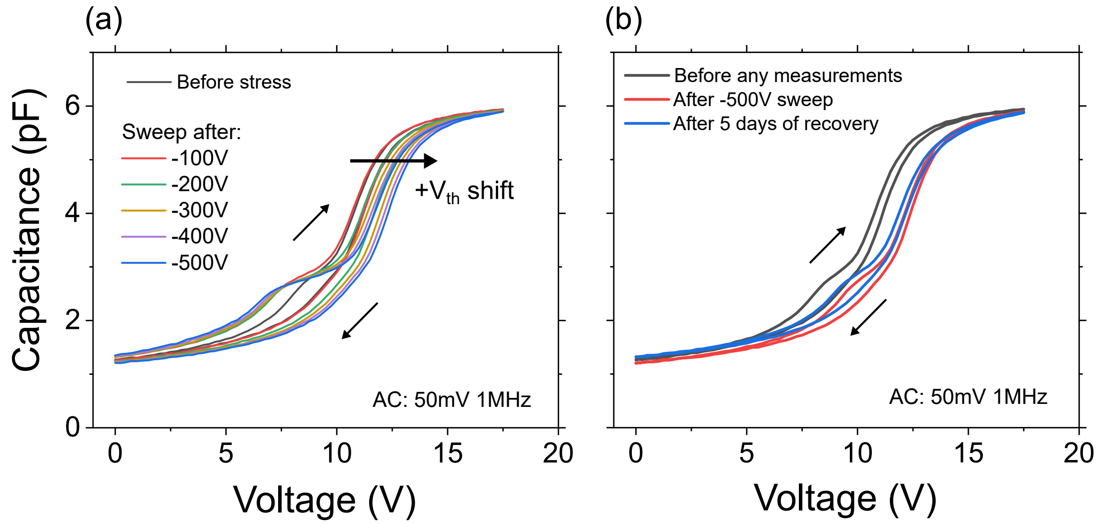


Figure 6.3: (a) CV characteristics taken after five bias stress conditions. The stresses are applied in order of increasing bias, and the up-sweep kink/ledge is allowed to fully recover between each stress measurement. After stressing, a prominent ledge is observed in each CV sweep. (b) Recovery of the CV characteristic taken after the -500V stress measurement. The ledge recovers quickly, but a large shift in threshold voltage persists, along with a stretch-out of the curve. There is only partial recovery of the device after 5 days.

applied in order of increasing voltage, with the device allowed to recover after each measurement. For each of the stress conditions, the prestress behaviour of the device was recovered in <30s. Two key changes in device behaviour are observed with increasing stress voltage: there is an increase in the prominence of the kink, which evolves into a ledge in the up-sweep characteristic at higher voltages; and there is a positive threshold voltage between each of the measurements. A large increase in magnitude of the hysteresis is also observed immediately after stressing. While the kink is recovered between each stress measurement, the positive shift in threshold voltage was observed to be semi-permanent. Fig.6.3(b) compares the CV characteristics taken: before stressing the device, approximately 60s after the -500V stress measurement, and 5 days after the -500V stress measurement. It is clear that the only a small recovery of the threshold voltage is observed over the course of 5 days. It was not possible achieve device recovery using optical methods, due to the presence of the anode and cathode metallisation. Some stretch-out of the curve is also observed, even accounting for the offset in threshold voltage; the black and red curves do not overlap.

6.2.2 Modelling and Simulations

In order to explain the origin of the ledge in Fig.6.3(a) it is necessary to propose a physical model, and test this model with device simulations. It is useful to consider the ledge in terms of the depletion region present in the MOS-CAP. The ledge represents an approximately constant value

of capacitance over a voltage range of approximately 4V. A fixed capacitance implies a depletion region of fixed width, (section.2.2.2). A fixed depletion width implies that the depletion region is screened from changes in anode voltage. An accumulation of charge close to the anode-depletion region interface would have the effect of screening changes in voltage. This accumulated charge must then persist at the interface, as the ledge is not observed on the down sweep of the CV characteristic. Both of these observations are consistent with a trapping mechanism. There are three types of traps that could account for this behaviour: oxide traps, interface traps and bulk traps in the semiconductor.
Simulations were performed in silvaco ATLAS in order to investigate the effect of trapping on the CV characteristic of the MOS-CAP. These simulations were performed using the AC small signal solution functionality in silvaco ATLAS, with the anode to cathode capacitance extracted. Initially, a constant density of bulk acceptor like traps were implemented. A trap state density of 1x10^{16} cm^{-3} was used, for a range of trap state energies (0.3eV - 1eV in steps of 0.1eV). This doping density was chosen as it is comparable to the reported doping density of 1.5x10^{16} cm^{-3} in the trench-MOS diode drift region; significantly higher acceptor trap densities would suppress the conductivity of this drift region. No ledge was observed for simulations including only bulk traps, indicating that such traps could not be responsible for the observed ledge behaviour.
Having discounted bulk trapping states as the cause of the trapping ledge, simulations investigating the impact of interface traps were performed. These simulations required both an interface trap energy (E_t) and trap state density. An approximate trap state density was extracted using Fig.6.4. The capacitive charge stored in the up and down sweep is extracted by integrating over the voltage range 0-12.5V (outside of this range the curves overlap, implying no net storage of charge). The difference in the charge is taken to be the charge stored during the up and down sweeps. Using the MOS-CAP diameter of 90μm, and assuming one unit of charge (e) is trapped by each interface trap, an interface trap density of 2.5x10^{12} cm^{-2} was extracted. Fig.6.5(a) shows a simulation of the CV curve, assuming a trap state density of 2.5x10^{12} cm^{-2} for a range of interface trap state conduction band offsets (E_C - E_t). The traps are assumed to be acceptor like, as the traps are assumed to be unoccupied at zero bias (as implied by the net loss of charge inferred from the integrated values in Fig.6.4). These simulations are performed in the steady-state, with the device reaching equilibrium between each voltage step (+0.25V). A clear trapping ledge is visible for each of the energies considered, with the width of the ledge approximately fixed. The onset capacitance of the ledge differs with each energy, with an increase observed with a decrease in the conduction band offset of the trap. The width of the ledge was dependent on the doping density, as can be seen in Fig.6.5(b).
The corresponding band diagrams for Fig.6.5(a) are shown in Fig.6.6. The voltages displayed for both the 0.6eV and the 1eV trap correspond to the voltage range covered by the ledge. There are two key observations here: the band bending at the oxide-semiconductor interface does not change over the width of the ledge; and the Fermi-level offset from the conduction band at the

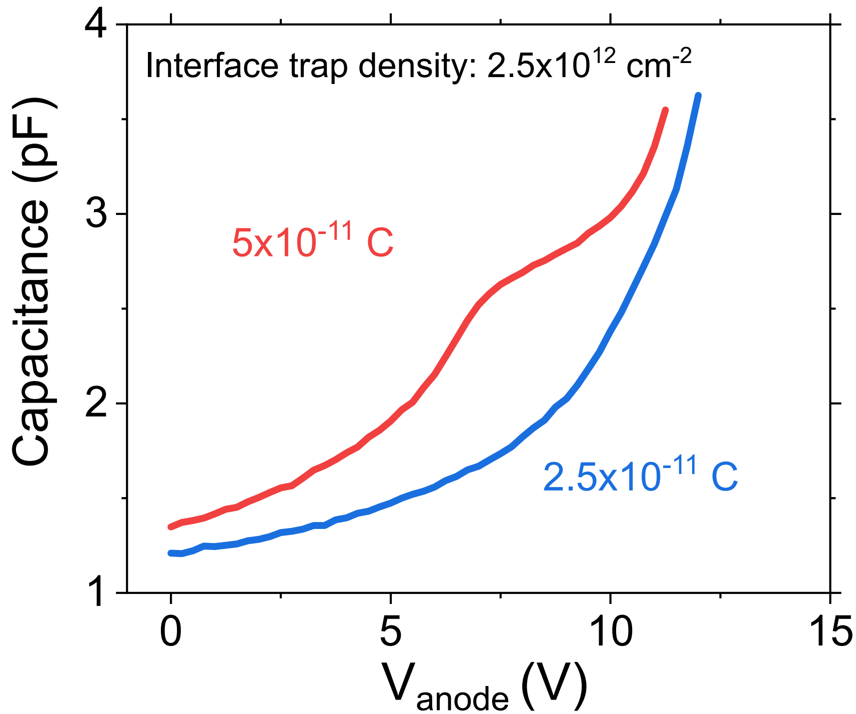


Figure 6.4: The integrated values of the up and down CV sweeps, with the difference in charge used to extract a trap density at the interface.

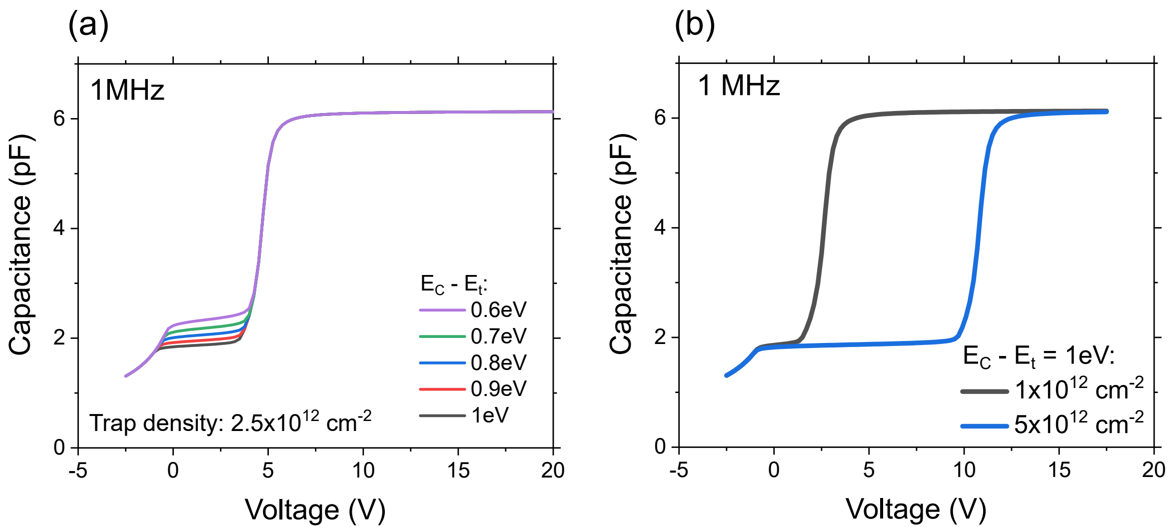


Figure 6.5: (a) Simulated steady-state CV curves for a fixed trap density and a range of conduction band offsets. (b) The impact on trap state density on the ledge width, for a conduction band offset of 1eV.

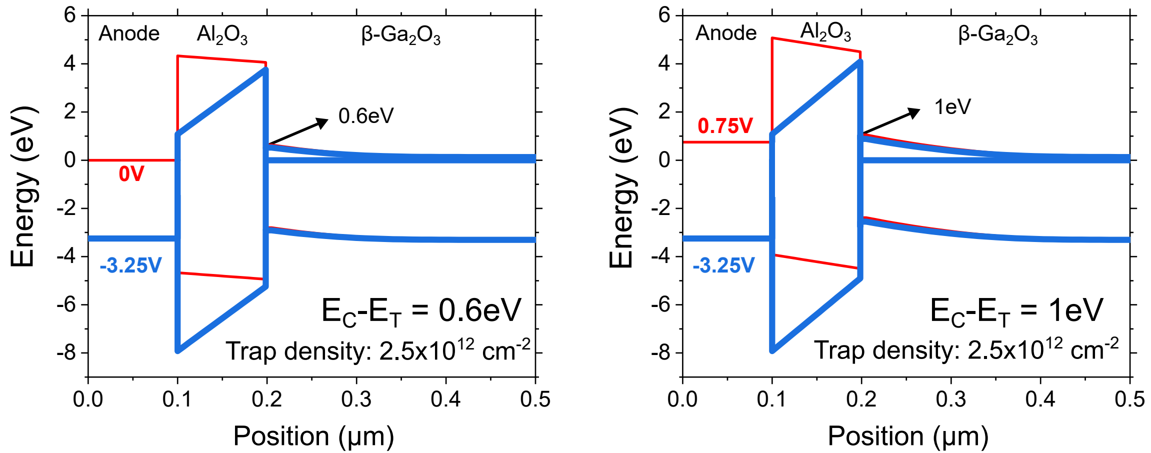


Figure 6.6: Band diagrams simulated for two interface trap energies. The voltages correspond to the anode voltage range over with the simulated ledge was observed (see Fig.6.5). No change in the surface potential or the depletion width is observed over the width of the ledge.

interface equals the trap state energy across the entire ledge. This suggests that, as the interface traps cross the Fermi level, some mechanism leads to a pinning of the surface potential. As the trap states begin the measurement situated above the Fermi level, crossing the Fermi level will lead to a charging of the trap states. This charging of the trap states would screen changes in the anode voltage from the bulk of the semiconductor, fixing the surface potential. This fixing of the surface potential leads to a fixing of the depletion width, consistent with the fixed capacitance over the ledge. While these simulations suggest that the trapping ledge in the up sweep can be attributed to interface trap states, the hysteresis observed in Fig.6.3 still requires an explanation. A model for an interface trap based mechanism for the hysteresis in the CV characteristic is shown in Fig.6.7. Here, a MOS-CAP structure's band diagram is shown, with some continuous density of interface traps over a small energy range in the bandgap. Initially, the device is at zero bias, and the interface traps above the Fermi energy will be unoccupied. As the anode voltage is swept up, band bending is observed, with the bands bending down at the interface. This has the effect of reducing the offset between the interface trap energy levels and the Fermi level, as the energy difference between the conduction band edge and interface trap levels will remain constant. As the lowest energy interface trap states cross the Fermi energy ($C=C_1$), they will experience a change in occupancy, trapping electrons. This correspond the onset of the ledge; as the voltage is swept up further, more charge will be trapped at the interface, screening changes in the anode voltage. The ledge ends once all of the interface traps are occupied, and no further charging can occur. The absence of a ledge on the down sweep can be explained with reference to the conduction band offset of interface traps. If this is sufficiently large, the interface traps will not detrap on the time scale of the measurement, even as they pass above the Fermi level. As there is no changes in the charge state, the ledge will not be observed on the down sweep. The

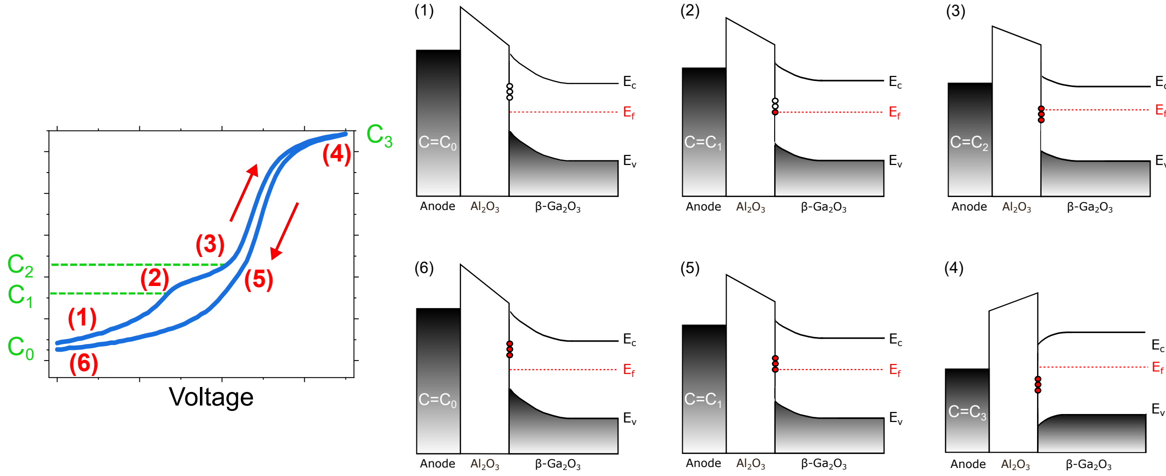


Figure 6.7: A model for the CV hysteresis. (1) At zero bias, interface traps above the Fermi level are unoccupied. (2) Electrons are trapped as interface states cross the Fermi level. The depletion width is fixed while the trap states fill. (3) Trap states continue to fill, acting to screen changes in the anode voltage, reducing the capacitance-voltage scaling of the device. (4) The device is swept into the accumulation regime. (5) Deep-level states remain occupied as the pass above the bandgap due to slow response times at room temperature. (6) Deep-level states remain occupied over the measurement time of the down sweep, leading to a hysteresis in the CV curve.

fact that the ledge is recovered between measurements suggests that the interface traps detrap on a time scale of <30s.

To confirm the model proposed model in Fig.6.7, simulations of the hysteresis are performed. To do this, it is necessary to implement the Heiman model for the silvaco ATLAS CV simulations. In this model, traps are not assumed to be confined just to the interface, but also some depth into the oxide. The spatial distribution of traps is assumed to be even with respect to distance (d) into the oxide. The electron capture cross-section as a function of oxide depth (σ_n(d) in this model is given by the expression,

$$\sigma_n(d) = \sigma_n e^{-\kappa d}, \tag{6.1}$$

where σ_d is the capture cross-section of the trap state in the bulk of the semiconductor and κ is given by the expression,

$$\kappa = \frac{2m_e^*(E_C - E_t)}{\hbar^2}. \tag{6.2}$$

The Heiman model assumes that transport between the oxide traps and semiconductor is via electron tunneling, as represented by the exponential term in Eqn.6.1. Fig.6.8 shows simulated CV hysteresis for three trap state energies. Traps are situated at the interface and up to 1nm in the oxide, with the even spatial distribution specified by the Heiman model. As the value of σ_n is not known for the interface trapping state, it was set to the standard value in silvaco ATLAS of 1x10^{-13} cm^2. The sweep rate was set to 1.25 V/s, the same sweep rate used in Fig.6.1(b) and Fig.6.3. A small degree of hysteresis is observed for the 0.5eV trap state, but the ledge is present

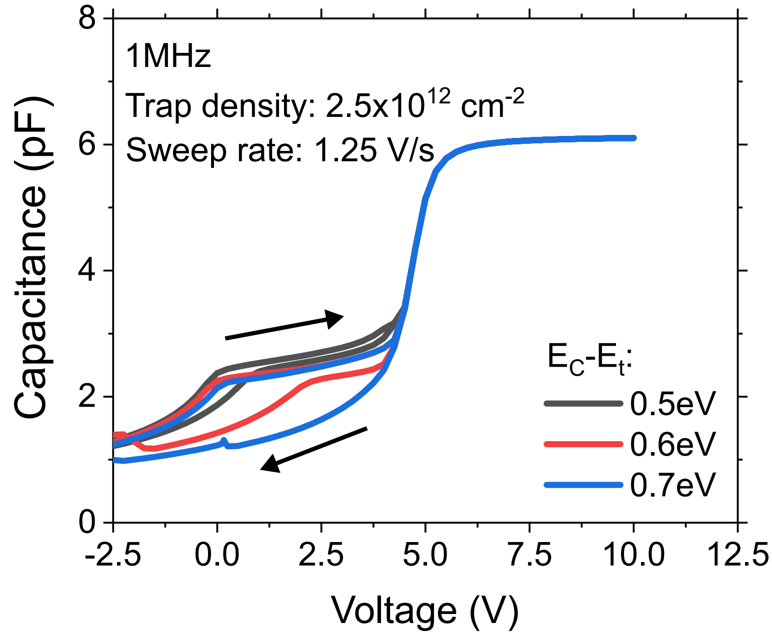


Figure 6.8: Simulation of hysteresis in CV characteristics using interface traps and the Heiman model. Traps are uniformly distributed 1nm into the oxide. An electron capture cross-section of 1x10^{-13} cm^2 is assumed at the interface. Only partial suppression of the ledge is observed for the 0.5eV down-sweep. Full suppression is observed for energies > 0.7eV.

in both the up and down sweep. In contrast, the ledge is only partially present in the 0.6eV down sweep, and completely absent from the 0.7eV down sweep. This suggests that the smaller conduction band offset, in the case of the 0.5eV trap, allows for almost complete detrapping on the down sweep. The 0.7eV state is far enough from the conduction band edge that recovery is not achieved on the down sweep, leading to the suppression of the trapping ledge. This was true of all simulations with energies >0.7eV. These simulations confirm that the model proposed in Fig.6.7 is consistent with the behaviour observed in Fig.6.3.

It has been established that the trapping ledge and the hysteresis observed after high-bias stressing can be explained by the presence of an interface trapping state. In theory, it is possible to extract the conduction band offset of this state directly from simulations. However, as shown in Fig.6.9(a), there is a large disagreement between the simulated and measured CV curves, with the measured curve corresponding to the down-sweep of a prestressed measurement. The measured curve has a large positive shift in voltage compared to the simulated curve, and is noticeably stretched out. The large voltage offset is consistent with negative charge storage in the oxide, which would deplete the MOS-CAP at zero bias. The stretch-out can be attributed to the filling of background interface traps, distributed continuously in the bandgap [254].

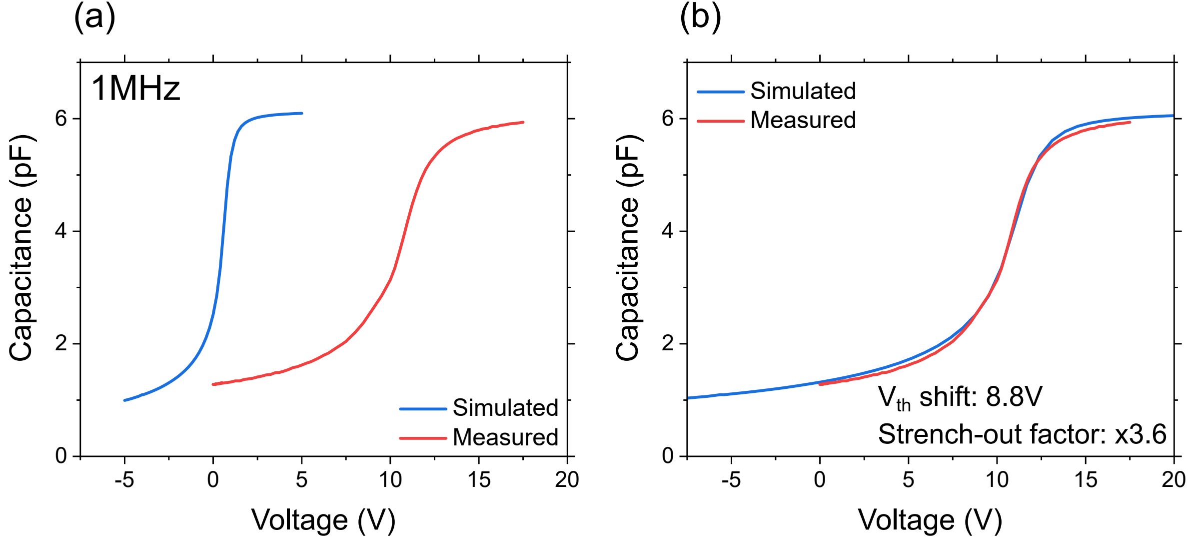


Figure 6.9: (a) Simulated CV curve compared to the measured prestressed down sweep CV curve. (b) Agreement between the simulated and measured curves is achieved by stretching the simulated curve by a factor of x3.6 and shifting by a voltage of +8.8V.

In order to calculate the conduction band offset of the ledge interface trap state, the surface potential at the ledge must be found. In order to calculate this, the amount of charge trapped at the interface and in the oxide must be determined. In the case of excess interface charge (interface trapping states not associated with the ledge), a consistent stretch out factor of x3.6 suggests an approximately constant interface trap density background over the voltage range 0-17.5V (as shown in Fig.6.9(b)). It is therefore possible to calculate the density of excess charge at the interface for any voltage. Integrating the measured CV curve from 0V a voltage ΔV gives the total stored charge in the MOS-CAP (ΔQ). The charging will be described by the following expressions,

$$Q_C = \frac{1}{3.6}\Delta Q, \quad Q_{it} = \frac{2.6}{3.6}\Delta Q, \tag{6.3}$$

where Q_C is the stored capacitive charge and Q_{it} is total charge trapped by the background interface traps. The onset voltage of the ledge in Fig.6.3 is approximately 7.5V. Using Eqn.6.3, a charged background interface charge density of 7.8x10^{11} cm^{-2} is extracted at the onset of the ledge.

In the case of the threshold voltage shift, it is not possible to determine definitively the amount of trapped charge. This is as the distribution of fixed charge in the oxide layer is not known, and cannot be determined with the measurements presented in this section. However, it is possible to calculate an upper bound for the surface potential by assuming all the fixed charge sits at the $Al_2O_3/\beta-Ga_2O_3$ interface. Assuming the fixed charge lies at the interface means that its density (Q_{ox}) can be expressed in terms of the threshold voltage shift (ΔV_{th}) shown in Fig.6.9(b) [255],

$$Q_{ox} = C_{ox}\Delta V_{th}. \tag{6.4}$$

For a threshold voltage shift of 8.8V, Eqn.6.4 gives a value of Q_{ox} = 4.2x10^{12} cm^{-2}. Summing over the contributions of Q_{it} and Q_{ox} gives a total charge density of 5x10^{12} cm^{-2}, at the onset voltage of the ledge (7.5V). This interface charge density yields a surface potential of 2.3V at the ledge, corresponding to a interface trap conduction band offset of 2.3eV.

6.2.3 Discussion

Trapping states in a β-Ga_2O_3 MOS-CAP (Fig.6.1(a)) have been observed, indicated by a kink in the MOS-CAP's CV characteristic (Fig.6.1(b)). A distinct trapping ledge was observed after the application of a high bias stress, as shown in Fig.6.3(a). A large degree of hysteresis was also observed, with the ledge completely suppressed on the down sweep of the CV characteristics. Complete recovery of the ledge/kink observed after a single CV sweep. This ledge has been attributed to the presence of traps at the Al_2O_3/β-Ga_2O_3 interface. Bulk trapping can be discounted, as simulations of the MOS-CAP, in the steady state, do not exhibit the trapping ledge feature. In contrast, steady state simulations of interface traps exhibit a distinct trapping ledge, with the width of ledge determined by the trap density and the capacitance of the ledge determined by the conduction band offset of the trap, as shown in Fig.6.5. This behaviour is consistent with a previously reported ledge in MOS-CAPs with the same structure, which was also attributed to interface trapping [39].
The transition from the kink to the ledge after high bias stressing, (Fig.6.3(a)), can be explained in terms of the ledge width. For stress voltages <400V the ledge behaviour has not saturated; an increase in the ledge width is observed with increasing stress bias. The onset voltage position of the ledge is unchanged, with the position of the higher voltage edge of the ledge increasing with voltage. The increase in the ledge width is associated with an increased density of unfilled traps, as shown in Fig.6.5(b). This suggests that, initially, there are some traps at the interface that are already charged. The high voltage bias before the CV sweep in (Fig.6.3(a)) would act to detrap electrons in these states before the CV sweep, increasing the effective trap state density. The fact that these traps are charged in equilibrium suggest either that they are interface traps that sit close to the Fermi energy, or that they are border traps with a detrapping rate limited by tunneling through the oxide layer. This is supported by the simulations of device hysteresis in Fig.6.8. The hysteresis is suppressed for traps with energies <0.5eV suggesting that, either the measured traps have conduction band offsets larger than this value, or they are distributed further than 1nm into the oxide, and so will have a longer response time to a change in bias.
The trapping states responsible for the ledge have to be distributed over a small range of energies in the bandgap; a trapping ledge is only apparent for a discrete energy level, or a high density of trapping states distributed over a small range of energies (Fig.6.7). In principle, this energy range can be extracted by comparing the measured CV characteristics of the device to simulations. The onset capacitance of the ledge can be related to the conduction band offset of the trap state energy furthest from the conduction band edge, while the highest capacitance on the ledge can

be related to the energy closest to the conduction band. However, this would require a complete understanding of the distribution of fixed oxide charge present in the Al_2O_3 layer.
The presence of fixed charge in the Al_2O_3 is apparent from the inconsistency between the simulated CV profiles of the MOS-CAP and the measured profiles (Fig.6.9(a)). The measured curves are noticeably stretched out when compared to the simulated curve. Furthermore, the onset of accumulation in measured characteristics occurs at a high positive bias in the measured CV, even in the absence of the trapping ledge (Fig.6.1(b)). The stretch-out the curve suggests a background density of background interface trap states distributed throughout the bandgap [254]. The large shift in the accumulation onset voltage is consistent with fixed charge in the oxide, as it would introduce an offset in the anode voltage. The impact of fixed oxide charge can also be observed in Fig.6.3(b). The observed positive shift in threshold voltage across the five measurements suggests that a net negative charging of the oxide, consistent with the injection of electrons from the anode into the oxide at bias. This trapped charge must be sufficiently far from the interface, or sufficiently deep in the bandgap, to explain the fact that initial device behaviour is not recovered over the course of 5 days.
In order to extract the interface trap energy using the model presented in Fig.6.7, the surface potential at the onset voltage of the ledge must be calculated accurately. However, it is not possible to extract the distribution of fixed charge in the Al_2O_3 layer, which is necessary to determine the charge density for a given threshold voltage shift [256]. An upper bound in trap state energy can be extracted with the assumption that all fixed oxide charge is located at the Al_2O_3/β-Ga_2O_3 interface, using the parameters in Fig.6.9(b). Using this assumption, an interface trap density of 5×10^{12} cm^{-2} is extracted. This is consistent with the values previously reported by Li *et al.*, extracted from the shift in flat-band voltage after bias stressing [39]. The surface potential at the ledge onset voltage of 7.5V with the assumed ledge interface trap density yields a trap state energy of 2.3 eV. It would appear that a lower bound for the interface trap energy could be provided by the simulations in Fig.6.8, with the sweep rate determining providing the lower bound in trap state energy that will yield full hysteresis of the curve. However, the electron capture cross-section of the interface trapping state is not known, (with an assumed value of 1×10^{-13} cm^2), and so these simulations cannot be relied on for a quantitative analysis of the hysteresis.
The presence of a deep-bandgap interface trapping state highlights an unresolved problem in the fabrication of β-Ga_2O_3 devices. Interface and oxide traps states have the potential to introduce both short-lived shifts in device behaviour and persistent changes in parameters such as threshold voltage, respectively. This problem is compounded by the high fields that oxide layers in β-Ga_2O_3 devices are expected to routinely handle, e.g. in the case of RESURF effect [98][39]. Commercialisation of devices will require high-quality interfaces to ensure stable device operation.

6.3 Long-lifetime Trapping and Memory Effects in β-Ga$_2$O$_3$ MOSFETs

In this section, the impact of trapping states on β-Ga$_2$O$_3$ field-plated MOSFETs are investigated. Initially, pulsed and long-duration bias stressing is used to demonstrate the presence of trapping in the devices, and to infer potential trap locations. Deep-level current transient spectroscopy measurements are then used to extract a trap state activation energy for the observed bulk trapping state. A significant change in trapping behaviour is observed after low-temperature thermal cycling of the devices, with a transition from the initial activation energy to new activation energy observed. All distinct trapping bulk trapping states were suppressed after the application of a 350K thermal stress. The transitions between different trapping behaviours, and their implications for β-Ga$_2$O$_3$ is discussed.

6.3.1 Devices

The devices studied were a set of β-Ga$_2$O$_3$ field-plated MOSFETs, grown on an insulating (010) Fe-doped substrate, as shown in Fig.6.10 [22]. Ozone-assisted MBE was used to grow a 1.2μm layer of unintentionally doped (UID) β-Ga$_2$O$_3$. A channel doping of 3x10^{17} cm^{-3} was achieved via Si$^+$ ion implantation of a box profile with a depth of 300nm. Capless implantation doping activation annealing (in N$_2$) was then carried out at 950°C for 30 minutes. Implantation doping was also used to dope the regions under the source and drain contacts (5×10^{19} cm^{-3}) [137]. A 20nm layer of Al$_2$O$_3$ gate dielectric was then deposited using ALD, and 400nm of SiO$_2$ passivation using CVD. A metal stack of Ti (20 nm)/Au (230 nm) was used to form the Ohmic contacts. CF$_4$ RIE gate recess through the SiO$_2$ was followed by deposition of the gate electrode, Ti (3 nm)/Pt (12 nm)/Au (280 nm), and a Ti/Au gate-connected field plate. Devices with several field-plate lengths (L$_{FP}$) and source-drain spacings were available, along with gate-lengths (L$_G$) of 2µm and 4µm, with all devices having a gate width of 500µm. Room temperature TLM measurements of the contacts gave a contact resistance of 1.5Ωmm (see section.3.2.1). Pulsed electrical I$_D$-V$_{DS}$ and I$_D$-V$_{GS}$ measurements were performed, with a duty cycle of 0.1%, to characterize device performance across the sample wafer. Off-state gate leakage currents (I$_G$) leakages of 10^{-9} A/mm or less were observed for devices over the entire area of the wafer. Qualitative electronic behaviour was consistent for all measured devices, varying as expected with source-drain spacing, field-plate length and gate length.

6.3.2 The Impact of Bias Stress on the Device Output Characteristics

In this section, trapping in field plated β-Ga$_2$O$_3$ MOSFETs is investigated using both short-duration, pulsed stress biases and long-duration constant stress biases. The purpose of these two distinct stress conditions is to infer the presence of electron trapping in the device, and to differentiate between long and short time constant traps. Although the terms 'long' and 'short'

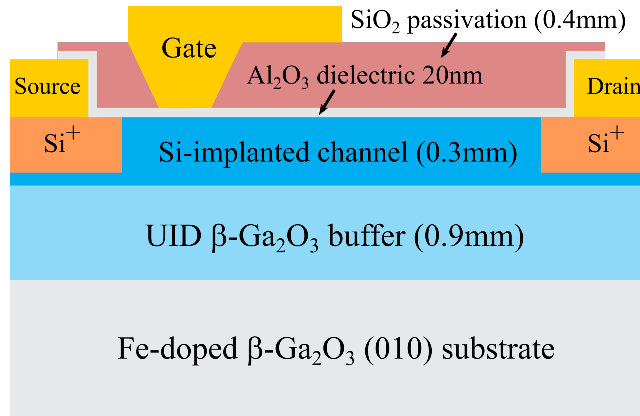


Figure 6.10: A schematic of the field-plated MOSFET structure used in this section.

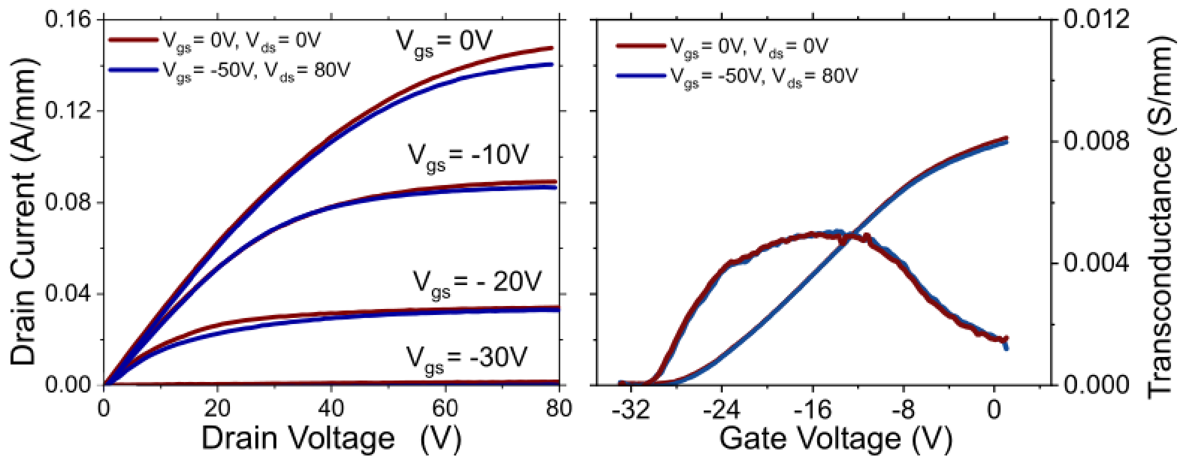


Figure 6.11: Pulsed (a) I$_D$-V$_{DS}$ (b) I$_D$-V$_{GS}$ output characteristics, measured using a 1µs pulse width and a 1ms quiescent bias of: V$_{DS}$ = 0V, V$_{GS}$ = 0V (red) and V$_{DS}$ = 80V, V$_{GS}$ = -50V (blue).

are not well defined, the short duration measurements will detect traps with time-constants approximately <1ms and long-duration traps with time-constants approximately >1ms. These measurements are necessary as characterising such traps will require different measurement systems, determined by the required time resolution.

The MOSFET devices used in this section had a gate length, gate width, gate-source spacing, gate-drain spacing of 2μm, 500μm, 5μm, and 15μm respectively, with a field-plate of 1μm. The DC output characteristics were observed to exhibit severe droop at high drain biases [35]. This is attributed to large rises in channel temperature, due to self-heating. Greatly improved IV characteristics, with reduced thermal droop, can be obtained with low duty cycle pulsed measurements, as shown in Fig.6.11. A pulse width of 1μs was used, with a Q-point of V$_{DS}$ = 0V and V$_{GS}$ = 0V (red lines).

In order to investigate the impact of short-duration stress on the device behaviour, both the

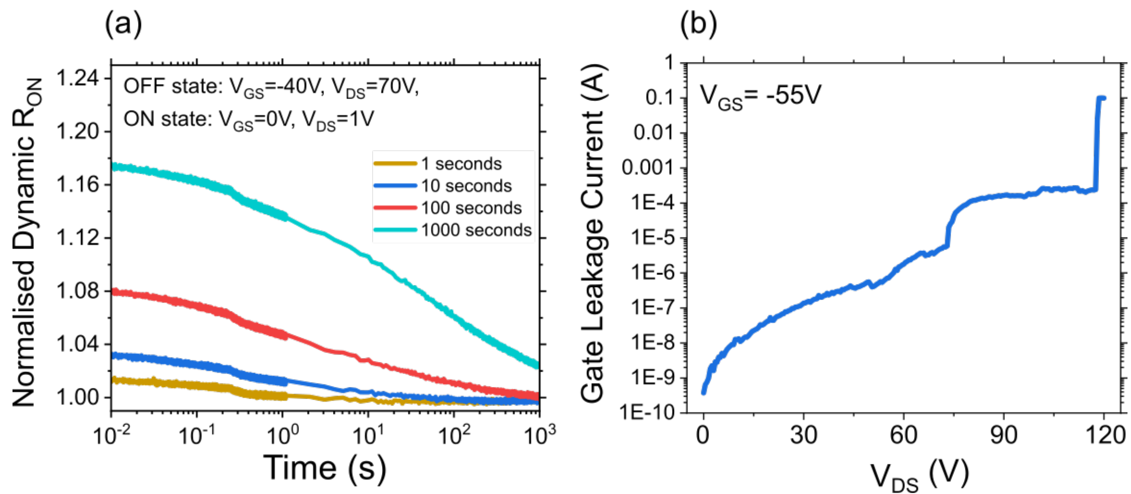


Figure 6.12: (a) Dynamic R$_{on}$ measured after applying a stress bias of V$_{GS}$ = -40V, V$_{DS}$ = 70V. (b) The leakage current of a device gate as a function of drain bias, in the off-state. A soft-breakdown of the gate oxide is observed at V$_{DS}$ = 70V, and hard breakdown at V$_{DS}$ = 120V.

gate and drain were biased during the Q-point of the pulsed measurement. Fig.6.11 shows this measurements, with a Q-point stress bias of V$_{DS}$ = 80V and V$_{GS}$ = -50V (blue lines). A pulse width of 1μm was used, with a pulse separation of 1ms. Neither current collapse or knee-walkout is observed with this quiescent stress bias. The pulsed I$_D$-V$_{GS}$ measurements show no V$_{th}$ shift or transconductance collapse between the stressed and unstressed measurements. This indicates that there has been no significant change in electron trapping charge states during the measurements. If traps are present in the device, a filling time on the order of milliseconds is insufficient to significantly impact their occupation.

The impact of long-duration stress conditions was then investigated. A gate-drain stress, V$_{GS}$ = -40V, V$_{DS}$ = 70V, was applied for various times and the device recovery was monitored for 1000s, as shown in Fig.6.12(a). A lower gate-drain access region bias was used, when compared to the pulsed measurement in Fig.6.11, as higher biases were found to trigger device breakdown during the course of the measurement. The breakdown characteristic of a device is shown in Fig.6.12(b). In the off-state, a drain bias of 70V triggers a large increase in the gate leakage current, attributed to degradation of the gate oxide. As such, drain bases >70V were not considered for long-duration stressing of the devices. The current transients shown in Fig.6.12(a) exhibit up to an 18% increase in device R$_{on}$, with the recovery time increasing with stress time. This increase in device R$_{on}$ can be attributed to the change in electron trap charge states during the application of the stress bias.

It is not possible, from the measurements presented so far, to differentiate between gate region trapping and gate-drain region trapping. In order to gain information about the location of the trapping region, the drain stress bias point was varied with a constant gate stress of V$_{GS}$ = -40V, Fig.6.13(a). Ideally, a zero-bias gate-stress would be applied along with the drain stress,

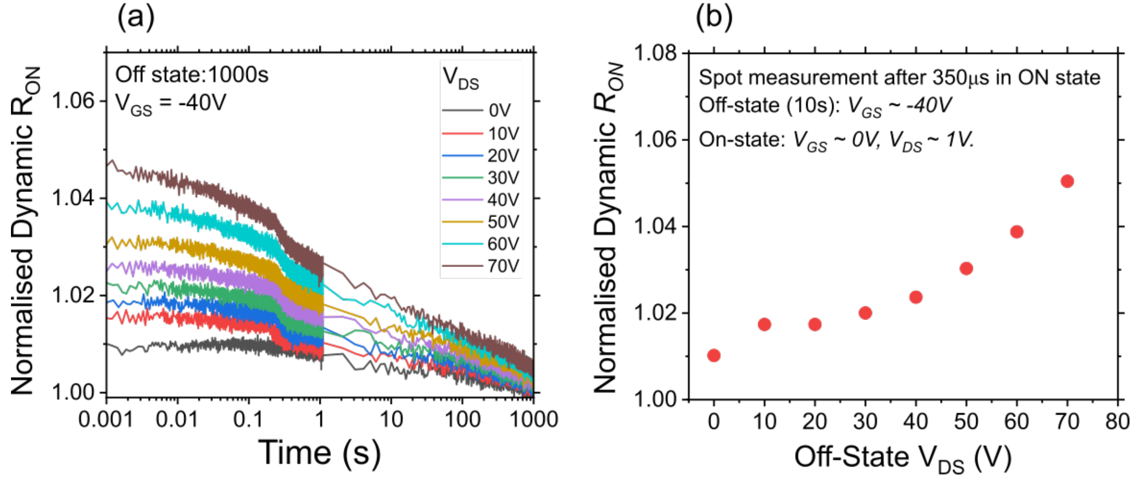


Figure 6.13: (a) The effect of drain-bias stress on the device recovery. An increase in the device R_{on}, after stressing, with increasing drain bias stress. (b) Dynamic R_{on} extracted 5ms after the stressing of the device, for each of the stress conditions in (a).

however, holding the device in the off-state allows for a meaningful compassion with the data in Fig.6.12, as induced changes in the trapping charge states of the device will depend on the field -profile across the channel. The field-profiles in the on and the off states will differ significantly, with the voltage drop over the depletion region in the off-state (approximately the length of the gate) and over the whole channel in the on-state (10μm). An increase in device R_{on} is observed with increasing drain bias, consistent with electron trapping in the gate-drain access region. The values of device R_{on} extracted immediately after trapping are shown in Fig.6.13(b). The increase in R_{on} and recovery time for the low drain bias condition, V_{GS} = -40V, V_{DS} = 10V, is also indicative of gate region trapping, as the drain stress bias in this instance is low in comparison to the gate bias. However, an increase in R_{on} is characteristic of trapping in the channel, and so the probable trap state location in this device is the the gate-drain access region.

The presence of electron trapping states have been inferred from the long-duration bias stressing measurements, with changes in device behaviour being attributed to changes in the charge state of these traps. The precise change in charge state, e.g. positive or negative charging, can be inferred from changes in the device's transfer characteristics, after bias stressing. A bias-stress condition in off-state of V_{GS} = -70V, V_{DS} = 70V was applied for 1000 seconds. Then an I_D-V_{GS} sweep was taken, (V_{DS} = 1V), 0.01 and 100 seconds after stressing. Each of these measurements lasted for approximately 0.5 seconds. A 10% drop in the peak transconductance (g_m) is observed after the gate-to-drain stress, as shown in Fig.6.14. A negative V_{th} shift of approximately 1V was observed immediately after stressing (Fig.6.14 inset), with only partial device recovery observed after 100 seconds. Both the drop in g_m and increase in device R_{on} seen after bias stressing, (Fig.6.13 and Fig.6.14), can be attributed to negative charge trapping in the bulk gate-drain region, while the negative V_{th} shift can be attributed to a net positive charging under the gate region. Given the

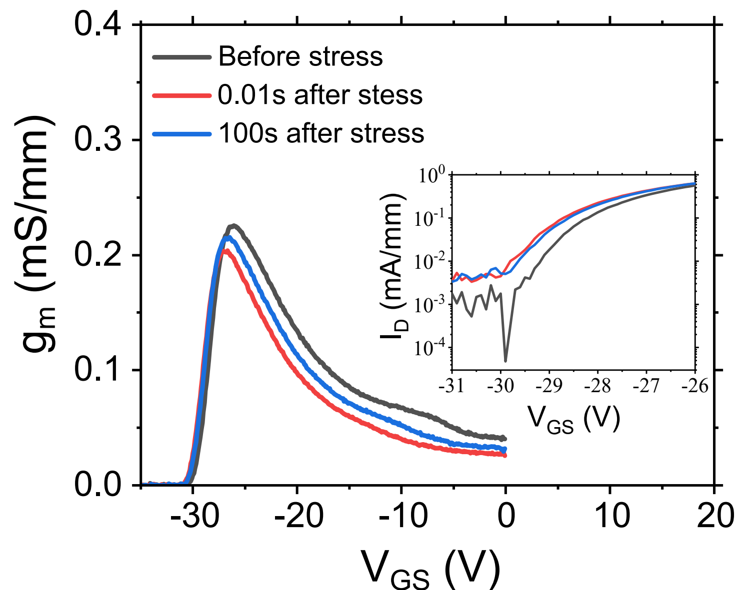


Figure 6.14: Transconductance as function of V_{GS}, before and after 1000s of device stress, (V_{GS} = -70V, V_{DS} = 70V). After the device stress an on-state bias of V_{GS} = 0V, V_{DS} = 1V is applied, a 10% suppression in g_m is observed. Inset: I_D-V_{GS} characteristics, with a threshold voltage shift of -1V observed.

large negative gate stress, this would be consistent with the depopulation of electron traps under the gate. It is not yet clear if the current transient signatures are caused by a single trapping state, or the superimposed behaviour of several states. To this end, it is necessary to extract the trapping state energy or energies, using the deep-level current spectroscopy technique.

6.3.3 Deep-level Current Transient Spectroscopy

Deep-level spectroscopy is a group of standard measurement techniques for the extraction of trapping state activation energies in bulk semiconductor layers. Principally, there are three techniques used: capacitance-mode deep-level transient spectroscopy [257], deep-level optical spectroscopy [258] and deep-level current transient spectroscopy. In the context of lateral MOSFETs, the first two techniques can be difficult to implement. Capacitance mode spectroscopy relies on measuring the CV frequency dispersion of a device, or the temperature dependence of a single frequency CV curve. Both of these approaches then model the CV characteristics in terms of a trap-level's capacitive response to the input signal. However, the magnitude of capacitance signals are limited by the gate length of the MOSFETs. Optical spectroscopy relies on observing the device's response to an optical signal of varying wavelengths to extract a conduction band/valence band offset of a trapping state. In the case of field-plated MOSFETs, this technique is not sensitive to the regions in which the strongest trapping signal would be expected. Off-state stressing of devices leads to peak fields at the drain side edge of the gate; the high fields in

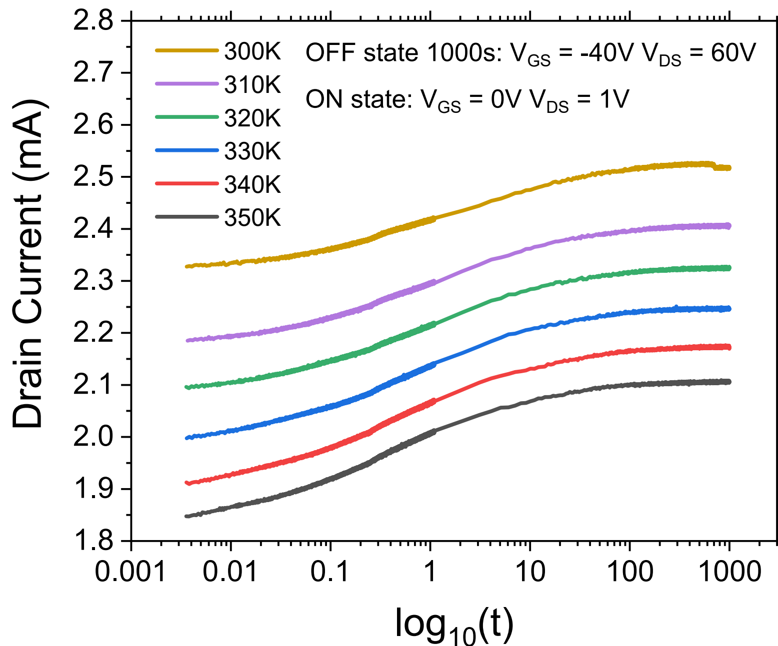


Figure 6.15: Transient current recovery curves over the temperature range 300K-350K, with an on-state condition of of V_{GS} = 0V, V_{DS} = 1V. The stress condition of V_{GS} = -40V, V_{DS} = 60V was applied for 1000s.

this region are expected to lead to the largest changes in trap occupancy. However, the gate and the field-plate metallisation hinders the direct illumination of this region. Deep-level current transient spectroscopy, however, only requires a measurement of the drain current as a function of time. Sensitivity to a particular trapping state is only limited by the offset of the trap state energy to the conduction band/valence band offset, and by the time resolution of the measurement system.

Deep-level current transient spectroscopy consists of bias stressing the device and then measuring its recovery. A stress condition was applied to the device in the off-state, (V_{GS} = -40V, V_{DS} = 60V), for 1000s, with the aim of modifying the charge state of the traps present in the device. The device was then switched into the on-state, (V_{GS} = 0V, V_{DS} = 1V), and the recovery of the current was monitored for 1000s. This current transient measurement was performed over a range of temperatures, with the device baseplate temperature being controlled using a liquid nitrogen cooled low-vacuum cryogenic probe system, coupled with an electrically heated thermal baseplate (as discussed in section 3.2.5). Drain current recovery curves were measured after stress using non-field plated devices. Both field-plated devices and non-field plated devices showed qualitatively the same behaviour; non-field plated devices were used as they exhibited the largest increase in R_{on} with device stress. At temperatures above room temperature, gate-drain stress biases were limited to 140V to avoid device breakdown in the off-state. A family of recovery

curves for a non-field plated device are shown in Fig.6.15. The drop in the on-state current at 1000s with device temperature is consistent with the expected increase in channel resistance at higher temperatures. Self-heating is expected to be <1^oC for the chosen on-state bias and corresponding drain current (the maximum power density used was 0.005 W/mm), and so is discounted in the analysis going forward. A clear drop in drain current is observed immediately after bias stressing the device. Each curve then recovers over the course of 1000s. with the most rapid period of recovery occurring over the range 0.1-10s. The drop in drain current after stressing indicates charge trapping in the device.

In order to extract the recovery time constants of traps in the device, each of the recovery curves were fitted using a series of stretched exponential functions [259],

$$I_D(t) = I_\infty - \sum_{n=1}^{N} \alpha_n exp[(t/\tau_n)^{\beta_n})] \tag{6.5}$$

where I_∞ is the drain current after device recovery, α_n is a weighting factor, τ_n the characteristic time constant of the recovery process and β_n is a constant. The fitting was performed using a MATLAB script, with a non-linear least squares methods and a Levenberg-Marquardt algorithm. An initial value of each parameter in Eqn.6.5 was used to implement the fitting algorithm. Both α_n and β_n were initially set to 1, while the initial value of τ_n was varied based on the curve being fitted. Sensitivity testing of the initial parameter vales was performed by varying the input parameters and observing the changes in the fitting function. Trap state time constants are extracted by taking the derivative of the fitted I_D curves. A single trapping state will yield a single peak in the derivative and multiple trap states will yield multiple peaks. The position of this peak is interpreted to be the trapping/detrapping time constant. This fitting procedure was repeated for all measured temperatures, and an Arrhenius plot of the resulting τ_n values was used to extract the activation energy/energies. This procedure has previously been described by Pavelka *et al.* [260].

Fig.6.16. shows the I_D recovery curve of the device at 300K, after a stress condition of V_{GS} = -40V, V_{DS} = 60V was applied for 1000s, taken from Fig.6.15. A single stretched exponential term was sufficient to fit the I_D recovery curve, suggesting that only a single trapping state is significantly contributing to changes in the device behaviour and the device recovery. The derivative of the fitting curve is shown in red, with a peak sitting at approximately $\log_{10}$(t) = 0. At temperatures above 300K, the peak was observed to shift to lower values of $\log_{10}$(t) (as shown in Fig.6.17(a)), which is consistent with a higher rate of electron emission from states due to thermal agitation. Fig.6.17(b) shows the corresponding Arrhenius plot, with each value of τ corresponding to the position of a peak in the fit curve derivative. A linear fit to this data yields an activation energy of 120$\pm$10 meV. The error is determined through sensitivity testing of the fits; multiple fits of the curves in Fig.6.15, with different input fit parameters for the fit procedure, yield a maximum variation in the extracted activation energy of 10meV.

Interestingly, a large shift in the device's trapping behaviour was observed after thermally cycling

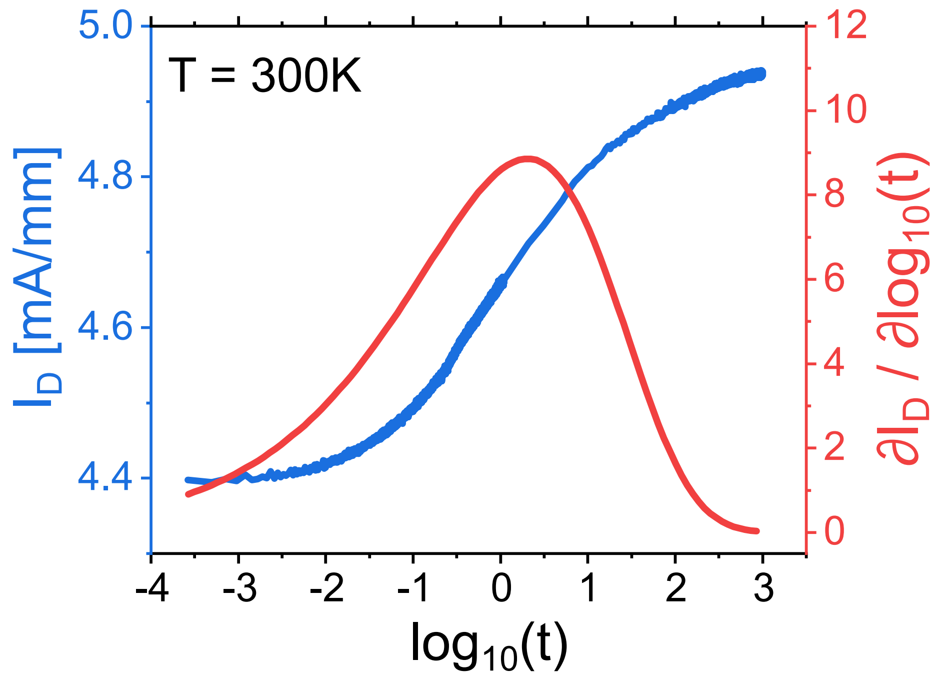


Figure 6.16: Recovery in I_D after stressing the device for 1000s (1000s), at 300K. A derivative of stretched exponential fit to the I_D recovery curve is used to extract a detrapping time constant (red).

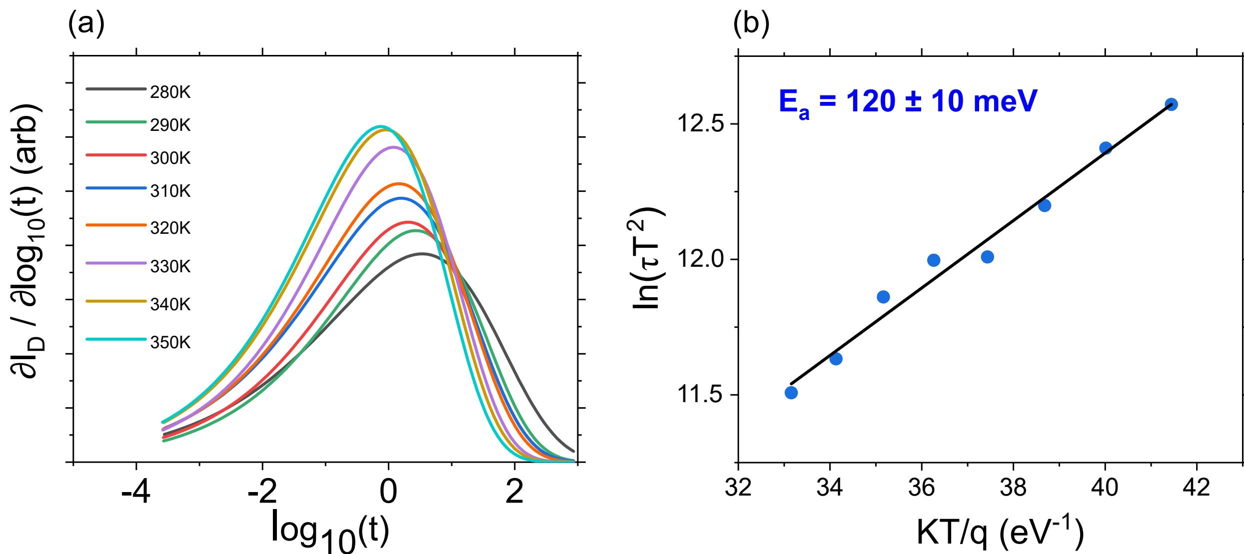


Figure 6.17: (a) The derivatives of the fitting functions for the recovery curves in Fig.6.15, over the temperature range of 270K-350K. The peak of each curve is used to extract a characteristic time constant of the recovery process (τ). (b) An Arrhenius plot of the τ values in (a), with an extracted activation energy of 120meV.

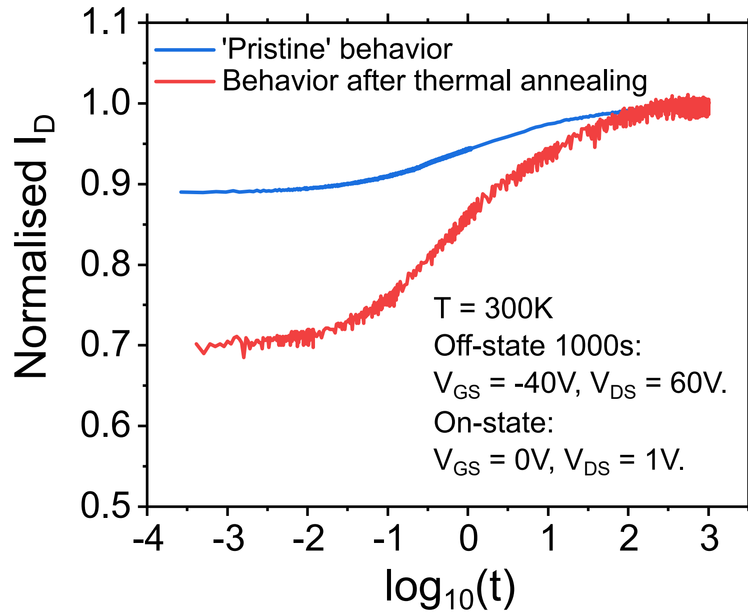


Figure 6.18: Recovery in I_D at 300K), after thermal cycling the sample between 100K-300K, compared to the pristine device behaviour.

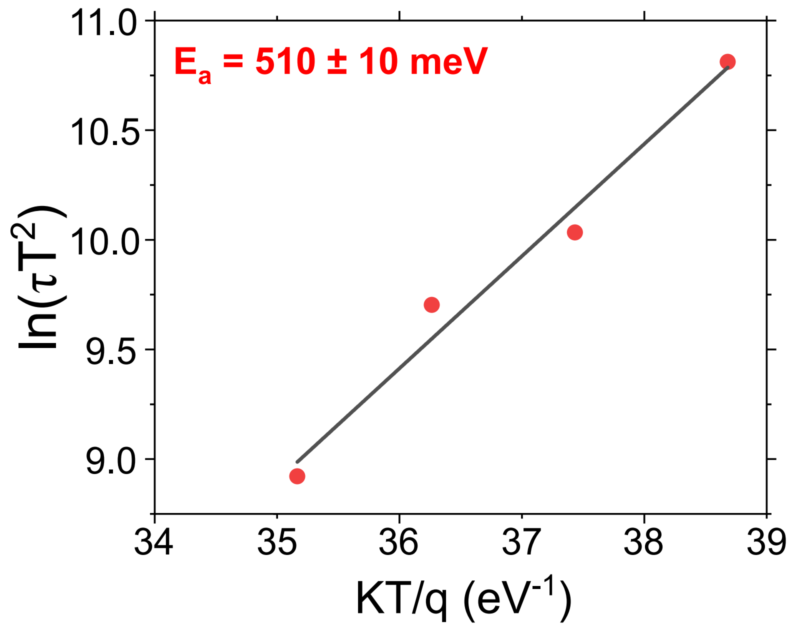


Figure 6.19: An Arrhenius plot for the trapping behaviour after thermal cycling, over the temperature range 300-330K, yielding an activation energy of 510meV.

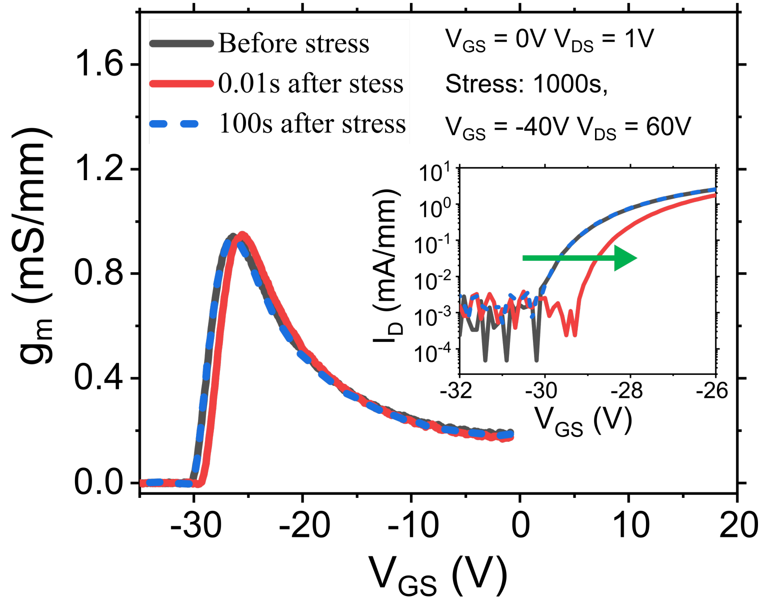


Figure 6.20: Transconductance before and after 1000s of device stress, (V_{GS} = -40V, V_{DS} = 60V). After bias-stressing the device, an on-state bias of V_{GS} = 0V, V_{DS} = 1V is applied. A marginal, 3%, increase in g_m is observed immediately after stress. Inset: The corresponding I_D-V_{GS} characteristics, with a threshold voltage shift of approximately +0.9V observed.

the devices to cryogenic temperatures. The sample underwent a temperature ramp from 300K to 100K and back to 300K. The wafer temperature was lowered to 100K at a rate of 2 K/minute and raised back at a rate of 5 K/minute. Fig.6.18. shows the device behaviour after this thermal cycling, at 300K, compared to the 'pristine' behaviour shown in Fig.6.15. A clear change in device behaviour was observed, with a larger decrease in I_D observed after the same stress conditions. This was observed consistently across the sample wafer, and consistently across different measurement temperatures. Fig.6.19 shows Arrhenius plots for the new trapping behaviour. An activation energy of 510$\pm$10 meV was extracted after the 300K-100K-300K temperature ramp. A single stretched exponential term was sufficient to fit the I_D curves.

Fig.6.20. shows the result of long-duration bias stress on a device, in the presence of this new trapping state, with the same measurement conditions as in Fig.6.14. Suppression of g_m after stressing the device for 1000s is insignificant, while the observed shift in V_{th} is approximately +0.9V. Full device recovery is observed after 100s. Only a small increase in device R_{on} is observed during this measurement, when compared to Fig.6.18. This is explained by the latency time of the measurement, with each measurement taking 0.5-1s; this allowed for partial device recovery before the transfer characteristics were measured. A further change in device properties was observed after thermally stressing the device. The sample substrate was held at 350K for 2 hours, after which a suppression of the 510 meV trapping state was observed, along with a permanent

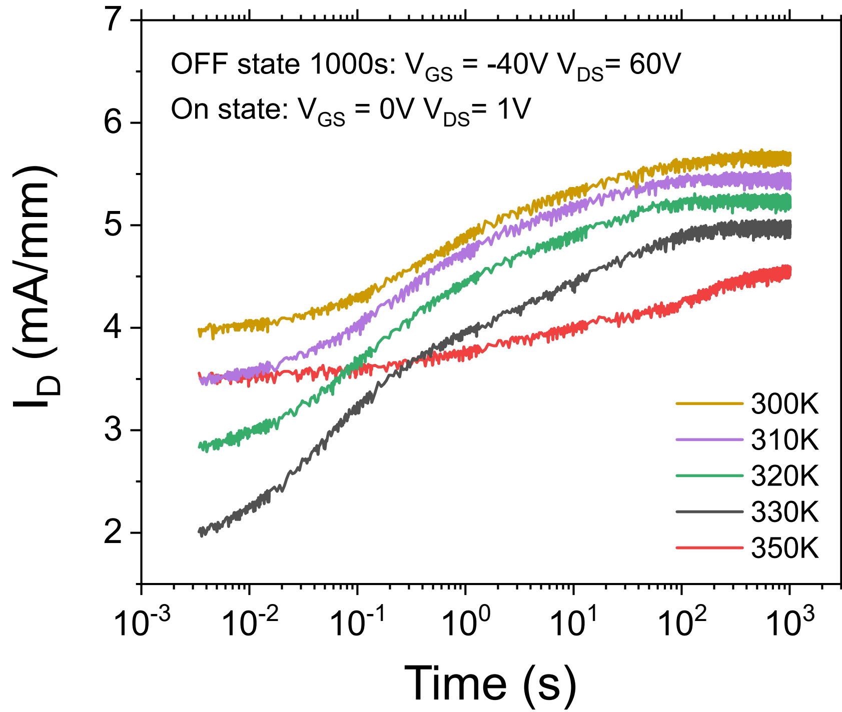


Figure 6.21: I_D recovery curves demonstrating the effect of a 350K thermal stress. Measurements were taken from the lowest temperature to the highest. Consistent trapping behaviour is observed over the range of 300K-330K. A significant change is behaviour is observed at 350K. No distinct trapping states are observed, and device recovery is not achieved after 1000s.

V_{th} shift of +1V. The 120 meV trapping state signature was also not observed after this thermal stressing. Bias stressing the devices for 1000s, (V_{GS} = -40V, V_{DS} = 60V), led to a 9-10%increase in device R_{on}, with device recovery not observed after 1000s. No distinct time constants could be extracted using the deep-level transient spectroscopy technique. This behaviour is shown in Fig.6.21, with a clear change in behaviour observed for the 350K recovery curve, when compared to the lower temperature curves.

6.3.4 Discussion

Initially, a trapping state of 120 meV was observed in the field-plated β-Ga$_2$O$_3$ MOSEFTs. Two dramatic and discontinuous changes in device behaviour were then observed. The first change, observed after low temperature thermal cycling of the MOSFETs, was a transition from the 120 meV trapping state to a 510 meV trapping state. The second change was the the suppression of the 510 meV trapping state after thermally stressing the substrate at 350K. Between each of these changes, the observed trapping behaviour was self-consistent and consistent across multiple devices. It is not possible to conclusively explain these changes with the available data.

In this discussion, a description of what information can be inferred for each stage of device behaviour will be presented. Possible reasons for the discontinuities will also be discussed.
The first trapping state observed in pristine devices, (E_a = 120 meV), can be attributed to negative charge trapping in the bulk gate-drain region. This is consistent with the observed drop in g_m and the increase in device R_{on} after bias stressing, (Fig.6.14). The positive charging under the gate region, (as indicated by the negative threshold voltage shift), is consistent with the depopulation of electron traps under the gate. The extracted activation energy of this trapping state corresponds to a previously observed trapping state in Si-doped β-Ga$_2$O$_3$ films, with an activation energy of 120 meV [127]. It has been speculated that this trap is related to the location of Si donors on the Ga(II) site, or the presence of interstitials resulting from implantation damage. Therefore, this trapping state can be attributed to the processing techniques used in the fabrication of these devices, as the channel was implantation doped using Si^+ ions to achieve n-type conductivity. The position of these traps would also be consistent with the measurements presented in Fig.6.12 and Fig.6.13, as the sensitivity to the applied drain bias stress suggested a trapping state located in the gate-drain access region.
After thermal cycling the sample between 300K and 100K, a second trapping state dominated, with an activation energy of E_a = 510 meV. This state had a significant effect on device behaviour, with a 30% increase in device R_{on} observed after bias stressing, as shown in Fig.6.18. The initial 120 meV trapping state was no longer observed. It is likely that the 120 meV is still present in the device, but that its signature is obscured by the new trapping state. Fig.6.20 shows an approximately +0.9V V_{th} shift after stressing the device, as opposed to the observed negative shift for the 120meV trapping state (Fig.6.14.). This +0.9V shift in V_{th} is consistent with negative charge trapping under or close to the gate. The large increase in R_{on} after stress suggests that negative charging is not just occurring under the gate but is also distributed into the gate-drain access region. Due to the sudden change in device behaviour, after heating to 350K (Fig.6.18), it was not possible to isolate the origin of this second trapping state. Structural changes in the device are unlikely, but it is possible that the cooling-heating cycle has modified the charge state of some existing state in the bulk of the device. However, at this time, it is not possible to conclusively provide a model for this behaviour.
The device behaviour after heating to 350K, where the 510meV trap level is suppressed, cannot straightforwardly be explained. It is likely that the stretched out 350K curve in Fig.6.18 is due to a superposition of recovery process, with a recovery time >1000s (the pre-stress device behaviour was not recovered after 5000s). This would explain why it was not possible to extract peaks in the derivatives for the fitting curves after this change in behaviour. It is likely that the 'anneal' has caused some semi-permanent changes in the device behaviour, and, due to the wide-bandgap of β-Ga$_2$O$_3$, could be arbitrarily long-lived. It is also possible that thermal and bias stressing of the devices has lead to change in charge states of traps that are electrically isolated from the channel. Such behaviour was observed in GaN HEMTs with C-doped buffers, in the form of

current collapse. Uren *et al.* demonstrated that this behaviour resulted from capacitive coupling between an electrically isolated buffer and a biased drain contact [112]. A persistent change in the potential distribution across the device was shown to persist for time scales >10^5 s. Likewise, in β-Ga_2O_3, changes in such electrically isolated region's charge states could lead to persistent changes in device behaviour, that would not be well modelled using the stretch-exponential fitting deployed in the DLTS method. A direct investigation of buffer effects in these devices was not possible, as methods such as device back-biasing require a conductive substrate [40].
The distinct and discontinuous changes in device behaviour observed with thermal stressing can not be straightforwardly explained. The emergence of the 510meV trapping state is likely due to the change in charge state of a pre-existing bulk trapping state. The annealing of the 510meV, and the subsequent absence of device recovery over reasonable time periods (>5000s), suggests the charging of an electrically isolated region in the device structure. Both charging of the substrate and the surface passivation would lead to persistent changes in device behaviour. However, it is not possible to attribute this behaviour to any specific mechanism with the existing data. The presence of these two distinct trapping regimes, and their relative change with time, highlights an important challenge potentially facing β-Ga_2O_3 devices. Understanding the origin of this trapping behaviour, and whether it is specific to a particular device architecture/design, is paramount for mitigating its effects.

6.4 Conclusions

Trapping effects have been investigated in both β-Ga_2O_3 MOS-CAP structures and field-plated MOSEFTs. Interface trapping has been observed in the MOS-CAP structure, demonstrated by the presence of a trapping ledge in the device's CV characteristics. This ledge became apparent after high-bias stressing of the MOS-CAP anode, and was only observed in the up sweep of the CV characteristic, with a significant degree of hysteresis observed. The ledge was characterised by an approximately fixed capacitance over a voltage range of approximately 4V. The fixed capacitance consistent with a fixed depletion region width over this voltage range, indicating charging mechanism that fixed the effective anode bias at the semiconductor-oxide interface. Electrical simulations of the CV characteristic in the steady state demonstrated that this ledge behaviour is consistent with the filling of interface traps at the interface, with the onset of the ledge occurring when the the trap level crossed the Fermi energy. Time dependent simulations demonstrated that the observed hysteresis in the CV characteristic is consistent with deep-level interface traps, whose response time is longer than that of the measurement sweep rate. Analysis of the theoretical and measured CV curves of the device allowed for the extraction of the trapping ledge surface potential, giving an upper bound interface trap state energy of 2.3 eV.
The presence of bulk electron trapping states in β-Ga_2O_3 MOSFETs were then investigated. Initially, trapping effects were probed using pulsed stress measurements and long-duration

stress measurements. Trapping effects were observed during long-duration stress measurements, but not pulsed measurements, suggesting a longer-time constant trapping state or states. The sensitivity of the device behaviour to drain bias was consistent with a trapping state or states in the gate-drain access region. Deep-level transient spectroscopy measurements were used to probe the trapping behaviour of the device, and a single trapping state was found to have an activation energy of 120±10 meV. A second trap state was detected after ramping the sample temperatures over a range of 100-300K with an activation energy of 510±10 meV. Finally, this second state was suppressed after thermally stressing the device at 350K. The 510 meV and was replaced by a broad continuum of states responsible for a slow recovery, representing a semi-permanent change in the device behaviour. It is probable that this suppression of the 510 meV trapping state was related to charging of an electrically isolated region in the device. However, it was not possible to confirm the origin of this new trapping state, or the reason behind this change in device behaviour.

Both the interface trapping states observed in the MOS-CAP, and the bulk trapping states observed in the MOSFETs, demonstrate the unresolved problem of trapping states and memory effects in β-Ga_2O_3. The suppression of interface and bulk trapping states is critical for the stable operation of β-Ga_2O_3 devices. High-fields over oxide layers and electrically isolated regions in the semiconductor are intrinsic to the operation of such devices. Semi-permanent shifts in device behaviour, such as oxide charging or increases in device R_{on}, will lead to unpredictable device operation. Furthermore, the presence of interface charge leads to the screening of electrode voltage from the semiconductor bulk, reducing control over the device characteristics. Further work is require to reduce the impact of trapping on β-Ga_2O_3 device operation.

Chapter 7

Conclusions

The realisation of commercial β-Ga_2O_3 power device has to potential to open up new high-voltage application spaces that other wide-bandgap semiconductors will struggle to exploit, such as high-voltage direct current (HVDC) converters for flexible grid operation. Investigating the reliability and performance issues of β-Ga_2O_3 devices has been the focus of this thesis, with particular attention paid to electrical and thermal issues that will need to be overcome to achieve commercialisation. The three studies presented in this thesis have covered a range of devices, with both lateral MOSFETs and vertical SBDs considered. Electrical characterisation, Raman spectroscopy and device simulations have all been used to investigate breakdown mechanisms in devices, device self-heating, potential electrical anisotropies in β-Ga_2O_3, and electron trapping. In the case of each, solutions have been proposed that may help towards the commercialisation of β-Ga_2O_3 devices.

Firstly, the leakage and breakdown mechanisms in β-Ga_2O_3 trench-MOS Schottky-barrier diodes were investigated by means of bias step-stressed measurements. Breakdown of these devices occurs over the oxide layer when they are subjected to a constant bias sweep [33]. However, it is necessary to understand leakage and breakdown mechanism under prolonged bias stress, as this more accurately reflects real-world operation. The leakage current of these devices was measured by step-stressing the anode in reverse bias, with the current attributed to two principle leakage paths in the trench-MOS SBD structure: the oxide layers and the Schottky-barrier interface. The measured leakage currents of several trench-MOS SBDs were analysed using a novel noise technique developed by Dancanale *et al.* [41]. Fourier transforms of the leakage current noise reveals two distinct leakage regimes in the trench-MOS diode. The low voltage regime is characterised by a linear decrease in the leakage current noise on a log scale, whereas the high voltage regime is characterised by an approximately constant leakage current noise. A

sharp jump in the leakage current noise separates the two regimes. Comparing this behaviour to that of the MOS-CAP and planar SBD, it was clear that leakage over the SB interface dominates at low voltages and leakage over the oxide layers dominates at high voltages. The jump in leakage current noise between the two regimes can be attributed to a non-reversible degradation of the oxide layer. This behaviour is observed across devices of different geometries, and is consistent with device breakdown occurring over a degraded oxide layer. This result is significant as high oxide fields in reverse bias are intrinsic to trench-MOS diodes employing the RESURF effect [98]. As such, the problem of oxide degradation is one that cannot be avoided entirely. A less aggressive application of the RESURF effect, through the engineering of higher SBs in β-Ga_2O_3, would help to mitigate the problem of breakdown over the oxide layers.

Continuing to explore the concept of power device device failure, the impact of device self-heating was investigated in a set of thin-channel β-Ga_2O_3 MOSFETs. Alongside the high operating voltages, device self-heating is a significant barrier for commercialisation, due to the low thermal conductivity of β-Ga_2O_3. The high channel temperatures in β-Ga_2O_3 devices are expected to severely limit their mean-time-to-failure. An absence of localised self-heating hot-spots has been demonstrated in these devices using the Raman nanothermography technique. 3D finite element simulations of the channel temperature profile were performed, utilising electrical simulations of the channel Joule heating profile. These simulations corroborated the absence of hot spots, with no sharp peaks in the temperature observed across the length of the channel. A comparison of the Raman nanothermography measurements to previously reported channel averaged temperatures, extracted using a pulsed IV method [42], demonstrates a high degree of agreement between the two methods. This is significant as the electrical methods are less time consuming, allowing for the rapid comparison of device self-heating across a large number of devices. This is not possible for many semiconductors and material systems, as the presence of hot-spots mean that channel averaged measurements do not provide a meaningful estimation of device lifetime.

The exploration of device self-heating using Raman nanothermography only considered one channel and gate orientation, with respect to the underlying substrate. Self-heating may be expected to be dependant on the orientation of the device channel, due to the highly anisotropic thermal conductivity of β-Ga_2O_3 (27 W/mK in the [010] direction to 10.9 W/mK in the [100] direction). To this end, the self-heating in thin-channel β-Ga_2O_3 MOSFETs on [010] grown substrates were simulated as a function of device orientation. The heating of the channel was shown to be largely insensitive to device orientation, with minimal variation in the average and peak channel temperatures observed. This was attributed to large heat fluxes into the substrate and the contact pad metallisation at either end of the channel. These heat fluxes dominated over the variation in the lateral thermal conductivity of the channel, masking the impact of β-Ga_2O_3's anisotropic thermal conductivity. This demonstrates that, over the range of powers considered, the lateral orientation of devices on [010] substrates is not a major design consideration.

While the impact of the anisotropic thermal conductivity was determined to have an insignificant

impact on device self-heating, it was unclear as the whether anistropic electrical behaviour would play a significant role in β-Ga_2O_3 device performance. To this end, the electrical anisotropy of thin-channel β-Ga_2O_3 MOSFETs was investigated by means of pulsed IV measurements. A large anisotropy in the device R_{on} was observed as a function of channel and gate orientation. This anisotropy was consistent across multiple cells on two separate sample substrates. In order to be able to attribute this anisotropy to either intrinsic variations in the electrical properties of β-Ga_2O_3, or to variations in device fabrication, the orientation of the sample substrates had to be determined. Raman spectroscopy was used to measured the in-plane orientation of the [001] and [100] directions for two sample substrates. It was found that the variation in device R_{on} did not correlate with any underlying crystalline direction, but only with the layout of the device on the substrate. Therefore, the observed anisotropy could not be attributed to any intrinsic properties of β-Ga_2O_3, but to artifacts associated with the fabrication and processing of the devices. By comparing the processing of the two sample sets, artifacts with the fabrication of the device gate were proposed as the origin of the variation in device R_{on}. This highlights the problem of discerning physical effects from processing variations in a novel material such as β-Ga_2O_3.
The presence of a distinct interface trapping state at a Al_2O_3/β-Ga_2O_3 interface was then investigated using a set of β-Ga_2O_3 MOS-CAPs. The capacitance-voltage characteristics of these devices exhibited a kink when sweeping the anode up from 0V to 17.5V, and no kink when sweeping it back down to 0V. High negative bias stressing of the device anode caused the kink to transition to a distinct ledge, with a fixed capacitance observed over a voltage range of 4V. Furthermore, after stressing, semi-permanent shifts in threshold voltage were also observed. The presence of the ledge implied that, over a range of anode voltages, the depletion width of the device was fixed. This requires a screening mechanism that shields the device from changes in the anode voltage. The charging of trapping states close to the semiconductor-oxide interface, or in the bulk of the oxide, would both lead to a screening of the anode voltage. Electrical simulations demonstrated that the ledge behaviour is consistent with interface trap states at the semiconductor-oxide interface. Furthermore, time dependent simulations implementing the Heiman model for interface and border traps successfully reproduced the hysteresis in the CV characteristics, with the ledge only observed when sweeping the anode voltage up. Using extracted values of the interface and oxide trap density, and by considering the behaviour of the surface potential over the ledge, an upper bound for the conduction band offset of the trap was determined to be 2.3 eV. The semi-permanent shifts in threshold voltage were attributed to traps deep in the oxide, whose charge state is modified by high-bias charge injection from the anode. The presence of this deep-level interface trapping state presents an issue for the high-voltage operation of β-Ga_2O_3 devices; the high fields that oxide layers in β-Ga_2O_3 devices are expected to routinely handle will lead to changes in device behaviour, such as shifts in threshold voltage and increased R_{on}. Commercialisation of devices will require high-quality interfaces to ensure stable device operation.
Bulk trapping in β-Ga_2O_3 was then investigated in MOSFETs using deep-level transient spec-

troscopy. The presence of trapping in the MOSFETs was inferred from pulsed bias-stress measurements and long-duration bias-stress measurements. The positive threshold voltage shift and the increase in device R_{on} indicated the presence of trapping states in the gate-drain access region. Deep-level transient spectroscopy revealed the presence of a single trapping states, with an activation energy of 120 meV. A transition in device behaviour was then observed, after thermally cycling the device over the temperature range of 100-300K, with the emergence of a 510 meV state. Thermally stressing the device at 350K lead to a suppression of this 510 meV state. After the suppression of the 510 meV state, deep-level transient spectroscopy revealed a broad contiumm of states, with device recovery not observed 5000s after bias stressing. This behaviour was observed consistently over the sample wafer, however, it was not possible to model the origin of this change of this device behaviour. However, it is probable that it is related to the charging of an electrically isolated region in the device, with similar behaviour having previously been observed for carbon buffer traps in GaN HEMTs [40].

7.1 Future Work

The performance and reliability of β-Ga_2O_3 devices has been the focus of this thesis. The investigation of trench-MOS SBD breakdown in chapter 4 lays the foundation for future work into such device structures. The reliability of these devices at elevated voltages should be investigated via mean-time to failure measurements of a statistically significant number of devices, over a range of possible operating voltages. Stepped-stress MTTF lifetime measurements have previously been demonstrated in the case of GaN pn diodes, and could provide accurate estimations of device lifetime in the case of β-Ga_2O_3 trench-MOS diodes [261]. Such measurements would also allow for a more meaningful comparison of different device designs, e.g. different fin geometries and diodes area/edge ratios. Additionally, an investigation into the breakdown of devices with differing radii of curvature at the trench-bottoms is merited, as simulations demonstrated this to be a critical parameter in determining the peak electric fields observed in the oxide. Along with modifying the Schottky barrier height of the anode, optimising the shape of the trench-bottom corners appears to be the most promising route to increasing the breakdown voltage and lifetimes of the trench-MOS diode structure.

The results of chapter 5 provide compelling evidence that small changes in the depth of a thin-channel in β-Ga_2O_3 MOSEFTs has a significant impact on the self-heating of the device. The fabrication of a sample set with varying channel depths, implemented via different implantation doping profiles, would allow for a rigorous investigation of this effect. It is important to understand whether the effect of channel temperature is significant when compared to other parameters, such as the thickness of the metal contacts (and their heat-sinking effects). The variation in threshold voltage of such devices would also allow for a modeling of a potential back gating effect in these devices.

The results of the high-voltage CV study chapter 6 revealed the presence of a deep-level interface trapping state at the Al_2O_3/β-Ga_2O_3 interface. Only an upper bound for the trap energy could be determined as the distribution of bulk charge in the Al_2O_3 was not known. To build on this work, the same measurements could be performed across a number of MOS-CAP structures with differing oxide thickness. This would allow for a determination of the bulk oxide charge distribution, and an accurate determination of the interface trap conduction band offset. This conduction band offset would aid in the determination of the physical origin of this trapping state. Finally, the instability observed in the MOSEFT trapping behaviour, present in chapter 6, should be explained. It was not possible to determine in the trapping behaviour was the result of bulk trapping state in the channel, or if the trapping state was situated in electrically isolated region within the device structure. The fabrication of the devices on a conductive substrate would allow for the investigation of buffer traps using back biasing techniques. This technique has been successfully applied in GaN [262], and can be used to confirm or to rule out the role of buffer trapping on current collapse in the channel.

APPENDIX A

A.1 List of Publications

- T. Moule, S. Dalcanale, A. S. Kumar, M. J. Uren, W. Li, K. Nomoto, D. Jena, H. G. Xing and M. Kuball, *"Breakdown Mechanisms in β-Ga_2O_3 Trench-MOS Schottky-Barrier Diodes"*, IEEE Transactions on Electron Devices, vol. 69, no. 1, pp. 75-81, 2022.

- N. A. Blumenschein, N. A. Moser, E. R. Heller, N. C. Miller, A. J. Green, A. Popp, A, Crespo, K. Leedy, M. Lindquist, T. Moule, S. Dalcanale, E. Mercado, M. Singh, J. W. Pomeroy, M. Kuball, G. Wagner, T. Paskova, J. F. Muth, K. D. Chabak and G. H. Jessen, *"Self-Heating Characterization of β-Ga_2O_3 Thin-Channel MOSFETs by Pulsed I–V and Raman Nanothermography"*, IEEE Transactions on Electron Devices, vol. 67, no. 1, pp. 204-211, 2020.

- A. Mishra, T. Moule, M. J. Uren, M. H. Wong, K. Goto, H. Murakami, Y. Kumagai, M. Higashiwaki, and M. Kuball, *"Characterization of trap states in buried nitrogen-implanted β-Ga_2O_3"*, Applied Physics Letters, vol. 117, no. 24, p. 243505, 2020.

- X. Zheng, T. Moule, J. W. Pomeroy, M. Higashiwaki, and M. Kuball, *"A trapping tolerant drain current based temperature measurement of β-Ga_2O_3 MOSFETs"* Trench-MOS Schottky-Barrier Diodes, Applied Physics Letters, vol. 120, no. 7, p. 073502, 2022.

- T. Moule, M. Singh, J. W. Pomeroy, S. Karboyan, M. J. Uren, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, and M. Kuball, *"Dynamic R_{ON} in β-Ga_2O_3 MOSFET Power Devices"*, 2019 Compound Semiconductor Week (CSW), pp. 1-1, 2019.

- T. Moule, M. Singh, S. Karboyan, E. Mercado, S. Dalcanale, M. J. Uren, Y. Zhang, Z. Xia, S. Rajan, and M. Kuball, *"Electrical and Thermal Characterisation of β-(Al_xGa_{1-x})$_2O_2$ / Ga_2O_3 HEMTs"*, 2019 International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH), 2019.

- T. Moule, M. Singh, J. W. Pomeroy, A. Green, V. Vasilyev, D. E. Walker Jr., N. Moser, M. J. Uren, K. Chabak, G. Jessen, M. Kuball *"Orientation-Dependent Electrical Performance of β-Ga_2O_3 MOSFETs"*, 3rd International Workshop on Gallium Oxide and Other Related Material (IWGO), 2019.

A.2 List of Presentations

- T. Moule, S. Dalcanale, A. S. Kumar, M. J. Uren, W. Li, K. Nomoto, D. Jena, H. G. Xing and M. Kuball, *"Breakdown Mechanisms in β-Ga_2O_3 Trench-MOS Schottky-Barrier Diodes"*, UK Nitride Consortium Winter Meeting, 2022, Oral Presentation.

- T. Moule, M. Singh, J. W. Pomeroy, S. Karboyan, M. J. Uren, M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi, M. Higashiwaki, and M. Kuball, *"Dynamic R_{ON} in β-Ga_2O_3 MOSFET Power Devices"*, 2019 Compound Semiconductor Week (CSW), pp. 1-1, 2019, Oral Presentation.

- T. Moule, M. Singh, J. W. Pomeroy, A. Green, V. Vasilyev, D. E. Walker Jr., N. Moser, M. J. Uren, K. Chabak, G. Jessen, M. Kuball *"Orientation-Dependent Electrical Performance of β-Ga_2O_3 MOSFETs"*, 3rd International Workshop on Gallium Oxide and Other Related Material (IWGO), 2019, Oral Presentation.

- T. Moule, M. Singh, M. J. Uren, and M. Kuball *"Deep-level trapping states in β-Ga_2O_3 MOSFETs"*, CDT-CMP Annual Conference 2019, 2019, Poster Presentation.

- T. Moule, M. Singh, M. J. Uren, and M. Kuball *"Capacitance-voltage characterisation of β-(Al_xGa_{1-x})$_2O_3$ / Ga_2O_3 HEMTs"*, Centre for Doctoral Training in Condensed Matter Physics Annual Conference 2018, 2018, Oral Presentation.

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