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Electrical and Thermal Characterisation of GaN-based Devices for RF and Power Electronics

By

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A dissertation submitted to the University of Bristol in accordance with the requirements of the degree of DOCTOR OF PHILOSOPHY in the School of Physics.

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Abstract

The rapid increase in global energy demand in the period of significant environmental concern requires us to look beyond standard Si based electronics and towards the wide bandgap semiconductors. AlGaN/GaN based heterostructures are capable of fast switching, larger breakdown voltages and higher power densities, offering a viable alternative to conventional Si solutions. GaN-based devices are predicted to dominate key automotive, consumer and industrial markets in the next decade however, to achieve widespread commercial application a number challenges relating to electrical and thermal reliability have to be overcome.

In this thesis, the relationship between vertical charge transport processes in GaN buffers is explored. By combining electrical characterisation of GaN-on-Si power HEMTs with TCAD simulations the dominant vertical charge transport processes are identifies as 3D variable range hopping most likely in the defect band in the carbon-doped GaN buffer and 1D hopping along the dislocation in the unintentionally doped GaN channel. The effect of these charge transport process on dynamic On-resistance (R_{ON}) is studied by examining the temperature and field dependence of dynamic R_{ON} in the transfer length method (TLM) structures and in lateral Schottky barrier diodes grown on the identical epitaxy. The results indicate that the variation in dynamic R_{ON} is dominated by charge transport processes in GaN layers and not by trapping.

In addition, comprehensive electrical and thermal characterisation of early generation "buffer-free" GaN-on-SiC RF HEMTs (where thin GaN channel is grown directly on AlN nucleation layer) is combined with computational simulations to determine device design for optimised electrical and thermal performance. Removal of thick doped buffer eliminates the issue of trapping in this layer and brings the high thermal conductivity substrate closer to the source of Joule heating during device operation. However, reduction in GaN thickness results in significant decrease in thermal conductivity of this layer offsetting some of the benefits of "buffer-free" design. The effects of GaN thickness and thermal interface between the GaN channel and SiC substrate are discussed in detail. Moreover, the position of Fermi level in the AlN nucleation layer becomes a critical parameter for carrier confinement, with thicker GaN layers showing increase in short channel effects.

Finally, electrical and thermal characterisation of proof-of-concept GaN HEMTs bonded onto SiC substrate using novel low-temperature technique is demonstrated. The bonding process utilises thin water layers trapped between the AlGaN/GaN heterostructure and the bond substrate to create a covalent bond. The devices are characterised before and after bonding showing no evidence of compromised electrical performance, while exhibiting all the major benefits associated with new high thermal conductivity substrate. This bonding technique could provide a promising solution to hetero-integration of III-V micro-electronic devices.

Dedication and acknowledgements

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Overall, there are too many people to acknowledge here by name, but I wholeheartedly hope I made my gratitude clear to all.

Author's declaration

I declare that the work in this dissertation was carried out in accordance with the requirements of the University's Regulations and Code of Practice for Research Degree Programmes and that it has not been submitted for any other academic award. Except where indicated by specific reference in the text, the work is the candidate's own work. Work done in collaboration with, or with the assistance of, others, is indicated as such. Any views expressed in the dissertation are those of the author.

SIGNED: .... DATE: ....

Table of Contents

Page

List of Tables xi

List of Figures xiii

1 Introduction 1

1.1 Thesis outline . . . 6

2 Theoretical Background 9

2.1 Material Properties . . . 9

2.1.1 Crystal Structure . . . 9

2.1.2 Polarization Effects . . . 12

2.1.3 Phonon Dispersion . . . 15

2.1.4 Heat Transport in Semiconductors . . . 17

2.1.5 Thermal Conductivity of GaN . . . 19

2.2 AlGaN/GaN HEMT Structure . . . 21

2.2.1 Substrate . . . 22

2.2.2 Nucleation and Strain Relief Layer . . . 23

2.2.3 Buffer Layer and Carbon Doping . . . 24

2.2.4 AlGaN Barrier and Capping . . . 27

2.2.5 Ohmic and Schottky Contacts . . . 29

2.2.6 Passivation . . . 32

2.3 GaN HEMTs and Diodes Operation . . . 33

2.3.1 DC Performance . . . 33

2.3.2 GaN HEMT as Power Switch . . . 35

2.3.3 GaN HEMT as RF Switch . . . 38

2.3.4 Schottky Barrier Diode Operation . . . 38

2.4 GaN Device Reliability . . . 40

2.4.1 Trapping in GaN . . . 41

2.4.2 Dislocations in GaN Buffer . . . 43

2.4.3 Short Channel Effects . . . 43

2.4.4 Surface Trapping . . . 44
2.4.5 Buffer Trapping . . . 46
2.4.6 Device Breakdown . . . 47
2.4.7 Self-Heating and Reliability Implications . . . 49

3 Experimental Techniques and Methods **53**
3.1 Experimental Equipment and Capabilities . . . 53
3.1.1 Measurement Environment . . . 53
3.1.2 Electrical Connections and Cabeling . . . 54
3.1.3 Probe Stations for Electrical Measurements . . . 55
3.1.4 Probe Station for Thermal Measurements . . . 57
3.1.5 Measurement Instrumentation . . . 58
3.2 Electrical Characterisation Techniques . . . 62
3.2.1 DC & Pulsed Current-Voltage Measurements . . . 62
3.2.2 Substrate Ramp Sweeps . . . 65
3.2.3 Current Transient Measurements . . . 66
3.3 Raman Spectroscopy for Temperature Measurements . . . 71
3.3.1 Raman Scattering . . . 71
3.3.2 Raman Thermography . . . 73
3.3.3 Mechanical Strain Correction . . . 76
3.4 Computational Simulations . . . 79
3.4.1 Electrical 2D TCAD Simulations . . . 79
3.4.2 Thermal 3D FEA Simulations . . . 81

4 Low-Field Vertical Charge Transport Processes in GaN Channel and Buffer Layers **83**
4.1 Introduction . . . 84
4.2 Experimental Details . . . 85
4.2.1 Sample Description . . . 85
4.2.2 Experimental Method . . . 86
4.3 Results . . . 87
4.4 Discussion . . . 89
4.5 Simulations . . . 97
4.6 Conclusions . . . 99

5 The Effects of Charge Transport Processes on Dynamic On-Resistance in GaN-on-Si Schottky Barrier Diodes **103**
5.1 Introduction . . . 104
5.2 Experimental Method . . . 104

5.2.1 Sample Description . . . 104
5.2.2 Experimental Method . . . 106
5.3 Results . . . 108
5.3.1 TLM Structures . . . 108
5.3.2 Schottky Barrier Diodes . . . 112
5.4 Discussion . . . 116
5.4.1 TLM Structures and Vertical Transport Mechanisms . . . 116
5.4.2 Schottky Barrier Diodes - Computational Simulations . . . 117
5.4.3 Schottky Barrier Diodes - Trapping Phase . . . 118
5.4.4 Schottky Barrier Diodes - Recovery Phase . . . 120
5.5 Conclusions . . . 124

6 Electrical and Thermal Characterisation of "Buffer-Free" GaN-on-SiC HEMTs 125
6.1 Introduction . . . 126
6.2 Experimental Details . . . 127
6.3 Results . . . 130
6.3.1 Electrical Characterisation . . . 130
6.3.2 Thermal Characterisation . . . 136
6.4 Discussion . . . 138
6.4.1 Electrical Measurements . . . 138
6.4.2 Electrical Simulations . . . 140
6.4.3 Thermal Analysis of Conventional GaN-on-SiC HEMTs . . . 145
6.4.4 Thermal Analysis of "Buffer-Free" GaN HEMTs . . . 146
6.5 Conclusions . . . 152

7 Electrical and Thermal Characterisation of GaN-on-SiC HEMTs Covanlently Bonded by Adaptive Low-temperature Method 155
7.1 Introduction . . . 156
7.2 Experimental Details . . . 157
7.2.1 Sample Description . . . 157
7.2.2 Bonding Technique . . . 158
7.2.3 Experimental Details . . . 160
7.3 Results . . . 162
7.4 Discussion . . . 169
7.5 Conclusions . . . 175

8 Summary and Conclusions 177

A Appendix A 183
A.1 Publications . . . 183

A.2 Presentations 183

Bibliography **185**

LIST OF TABLES

TABLE **Page**

1.1 Figure of Merit Relative to Si 3

2.1 Substrate Material For GaN Growth 22

4.1 Hopping Conductivity Models 95

6.1 Thermal Conductivity Values for Ansys Simulations I 146

6.2 Thermal Conductivity Values for Ansys Simulations II 148

7.1 GaN Phonon Temperature Dependence Coefficients 168

7.2 Thermal Conductivity Values for Ansys Simulations 173

List of Figures

Figure		Page
1.1	Spider diagram Si, SiC and GaN.	2
2.1	Wurtzite GaN structure and first Brillouin zone.	10
2.2	GaN electronic band diagram in the first Brillouin zone.	11
2.3	Spontaneous and piezoelectric polarization in AlN/GaN heterostructures.	13
2.4	Lattice constant and band gap relationship for GaN, AlN and InN material systems.	14
2.5	Polarization and band diagram for an AlGaN/GaN heterostructure.	15
2.6	1D atomic balls and springs diagram.	15
2.7	Phonon dispersion for a diatomic 1D chain of atoms and full dispersion diagram for wurtzite GaN.	16
2.8	Normal and Umklapp phohon scattering processes.	18
2.9	GaN thermal conductivity dependence of temperature, dislocation density and layer thickness.	20
2.10	Typical AlGaN/GaN-on-Si HEMT epitaxial stack.	21
2.11	Three main types of strain relief layers.	23
2.12	Schematic representation of edge and screw dislocations.	24
2.13	Position of some of the common extrinsic dopants in the GaN bandgap.	25
2.14	Formation energies for C incorporation into GaN.	26
2.15	Free hole concentration and resistivity relation.	28
2.16	The effects of AlGaN and GaN cap thickness on 2DEG concentration.	29
2.17	Formation of Ohmic and Schottky contacts.	30
2.18	Typical Ohmic contact stack.	31
2.19	HEMT geometry and IV characteristics.	34
2.20	Hard and soft switching in power GaN HEMT.	36
2.21	Specific On-resistance of Si, SiC and GaN.	37
2.22	GaN RF HEMT operation.	39
2.23	Lateral GaN Schottky diode structure and IV characteristics.	39
2.24	Main degradation mechanisms in GaN HEMTs.	40
2.25	The effects of trapping on HEMT IV characteristics.	42

2.26 Short channel effects in GaN HEMTs. 44
2.27 Effects of surface trapping in GaN HEMT. 45
2.28 Charge distribution during GaN HEMT operation. 46
2.29 Major leakage paths in GaN HEMTs. 48
2.30 Effects of gate-drain spacing on HEMT breakdown. 49
2.31 Typical plot for calculation of the mean time to failure. 50
2.32 Joule heating profile simulations for GaN HEMT. 51

3.1 Coaxial and triaxial cables. 54
3.2 Probe station for electrical measurements. 55
3.3 Cryogenic probe station for electrical measurements. 56
3.4 Probe station for thermal measurements. 57
3.5 Main instruments used for electrical characterisation. 58
3.6 Major components of the Raman spectrometer and the corresponding optical path. . . 60
3.7 Probe station and instruments for device biasing during thermal measurements. . . . 61
3.8 GaN HEMT typical IV characteristics. 62
3.9 Pulsed IV measurement timeline and bias conditions. 63
3.10 THe effects of self heating on GaN HEMT IV characteristics. 64
3.11 Bidirectional substrate ramp sweep biasing conditions and interpretation. 65
3.12 Timeline and schematic representation of a typical current transient measurement. . 67
3.13 Comparison of current transient measurements performed in the linear and saturation region. 68
3.14 General overview of current transient measurement and data analysis process. 69
3.15 Different types of Raman scattering. 71
3.16 Optical phonon modes in wurtzite GaN. 73
3.17 Temperature calibration of GaN E_2 phonon mode and TiO_2 E_g mode. 74
3.18 Raman spectrum of TiO_2 nanoparticles. 76
3.19 Thermomechanical stress correction based on shift in GaN E_2 and A_1 Raman modes. 78
3.20 Meshing of a lateral GaN Schottky Diode in Silvaco Atlas TCAD software. 79
3.21 Meshing of a GaN HEMT in Ansys FEA software. 81

4.1 Device epitaxial stack and test structures. 85
4.2 Substrate stress transients: measurement timeline. 87
4.3 Bidirectional substrate ramp sweep with relevant charging regions marked. 88
4.4 Temperature substrate stress transient measurement. 89
4.5 Forward stepped substrate stress transient measurements of the potential difference of 10 V. 90
4.6 Bidirectional substrate ramp transients of the potential difference of 10 V. 91
4.7 Temperature and field dependence of the process τ_1. 92

4.8 Temperature and field dependence of the process τ_2. 93
4.9 Updated 1D lumped element diagram of the expitaxy. 94
4.10 Band diagrams showing charge transport in the epitaxy during and after applying stress. 97
4.11 Activation energy of the band-to-band leakage across the UID GaN channel. 98
4.12 Simulated TLM structure in Silvaco Atlas TCAD Software. 98
4.13 Simulated substrate ramps and substrate stress transients. 100

5.1 Schematic diagram of experimental structure and the epitaxy. 105
5.2 Substrate stress transient measurement timeline. 107
5.3 Bidirectional substrate ramp sweeps for temperatures between 300 - 450 K. 108
5.4 Temperature dependence of substrate stress transient measurements of TLM structures and corresponding recovery curves. 110
5.5 On-resistance measurements of TLM structures with no stress applied. 111
5.6 Temperature and field dependence of dynamic R_{ON} of TLM structures. 112
5.7 IV characteristics and On-resistance of Schottky diodes in the absence of applied stress.113
5.8 Schottky diode recovery transients from reverse bias stress. 114
5.9 Temperature and field dependence of dynamic R_{ON} measured for Schottky diodes. . . 115
5.10 Diagram of Schottky diode simulated in Silvaco Atlas TCAD software. 118
5.11 Time dependence of the total net sheet charge density at the top and bottom of GaN:C buffer during trapping. 119
5.12 Simulated recovery transient for a Schottky barrier diode. 120
5.13 Time dependence of the total net sheet charge density at the top and bottom of GaN:C buffer during recovery from reverse bias stress. 121
5.14 Total net charge distribution immediately after stress in the Schottky diode. 122
5.15 Simulated maximum total net sheet charge concentration at the top and bottom of GaN:C buffer as a function of applied stress and temperature. 123

6.1 QuanFINE ("buffer-free") technology compared to conventional GaN-on-SiC HEMT. . 127
6.2 Pulsed IV measurement timeline. 128
6.3 Schematic diagram of micro-Raman thermography measurement on "buffer-free" HEMT.129
6.4 DC IV characteristics of "buffer-free" GaN-on-SiC HEMTs. 130
6.5 DC IV characteristics of conventional GaN-on-SiC HEMTs. 132
6.6 Vertical leakage current for "buffer-free" and conventional GaN-on-SiC HEMTs. . . . 133
6.7 DIBL measurements of "buffer-free" and conventional GaN-on-SiC HEMTs. 133
6.8 Pulsed IV measurements of "buffer-free" GaN-on-SiC HEMTs. 134
6.9 Pulsed IV measurements of conventional GaN-on-SiC HEMTs. 135
6.10 Pulsed IdVg dependence on quiescent bias point duration for "buffer-free" GaN-on-SiC HEMTs. 136

6.11 Raman spectrum of "buffer-free" GaN-on-SiC HEMTs. 137
6.12 Operating temperatures of "buffer-free" HEMTs as a function of power dissipation. . 138
6.13 Operating temperatures of conventional GaN-on-SiC HEMTs as a function of power dissipation. 139
6.14 Simulated "buffer-free" GaN-on-SiC structures and corresponding band diagrams. . . 141
6.15 Simulated IdVg measurements corresponding to Case 1 and Case 2 band diagrams. . 142
6.16 DIBL measurement and simulations for "buffer-free" GaN-on-SiC HEMTs. 142
6.17 Simulated Off-state density for "buffer-free" GaN-on-SiC HEMTs. 143
6.18 Cross-sectional TEM images of AlN nucleation layer and interfaces for conventional devices and QuanFINE technology. 144
6.19 DIBL as a function of gate length and GaN thickness. 144
6.20 Comparison between micro-Raman measurement and Ansys simulations for conventional GaN-on-SiC HEMTs. 147
6.21 "Buffer-free" GaN-on-SiC HEMT structure simulated in Ansys. 147
6.22 Comparison between micro-Raman measurement and Ansys simulations for "buffer-free" GaN-on-SiC HEMTs. 149
6.23 Lateral temperature profiles and peak channel temperature as a function of GaN thickness. 150
6.24 Percentage temperature drop across each epitaxial layer as a function of total GaN thickness. 151
6.25 Peak chennel temperature as a function of total GaN thickness and TBR_{eff} for power dissipation of 8 W/mm. 152

7.1 Original device structure and epitaxy. 157
7.2 Schematic representation of key steps involved in the bonding technique investigated in this study. 159
7.3 TEM image of bonded interface between AlN (bottom of AlGaN/GaN heterostructure thin film) and the bond substrate. 160
7.4 Schematic diagram showing micro-Raman thermography measurement of GaN HEMTs before and after bonding. 162
7.5 DC IV characterisation before and after bonding. 163
7.6 Pulsed IV characterisation before and after bonding. 164
7.7 Dynamic R_{ON} measurement performed on the devices before and after bonding. . . . 165
7.8 Bidirectional substrate ramp sweep performed on a single finger GaN HEMT before and after bonding. 166
7.9 Bidirectional substrate ramp sweep dependence on device active area. 167
7.10 Vertical leakage measurements before and after bonding. 168
7.11 Raman spectra of GaN HEMTs before and after bonding. 169
7.12 GaN temperatures as a function of power dissipation before and after bonding. 170

7.13 Comparison between surface temperature (based on TiO_2 nanoparticles) and GaN measurements for devices before and after bonding. 171
7.14 GaN HEMT structure simulated using Ansys FEA Software. 173
7.15 Teperature measurements and Ansys simulations for devices before and after bonding.174

List of Acronyms and Initialisms

- 2DEG - Two Dimensional Electron Gas
- 2DHG - Two Dimensional Hole Gas
- AFM - Atomic Force Microscopy
- BFOM - Baliga Figure of Merit
- BHFFOM - Baliga High Frequency Figure of Merit
- CB - conduction band
- CCD - Charge Coupled Device
- CFOM - Combined Figure of Merit
- CTE - Coefficient of Thermal Expansions
- CVD - Chemical Vapour Deposition
- CVU - Capacitance-Voltage Unit
- DB - Defect Band
- DIBL - Drain Induced Barrier Lowering
- DOS - Density Of States
- DUT - Device Under Test
- EFL - Electron Fermi Level
- FEA - Finite Element Analysis
- FET - Field Effect Transistor
- FOM - Figure of Merit
- FP - Field Plate

- GET - Gated Edge Termination
- GSG - Ground-Signal-Ground
- HEMT - High Electron Mobility Transistor
- HVPE - Halide Vapour Phase Epitaxy
- JFOM - Johnson Figure of Merit
- KFOM - Keyes Figure of Merit
- LED - Light Emitting Diode
- LO - Longitudinal Optical
- LPCVD - Low Pressure Chemical Vapour Deposition
- MBE - Molecular Beam Epitaxy
- MOCVD - Metal Organic Chemical Vapour Deposition
- MOSFET - Metal Oxide Semiconductor Field Effect Transistor
- MTTF - Mean Time To Failure
- NA - Numerical Aperture
- NL - Nucleation Layer
- NNH - Nearest-Neighbour Hopping
- PECVD - Plasma Enhanced Chemical Vapour Deposition
- PL - Photoluminescence
- PMU - Pulse Measurement Unit
- RF - Radio Frequency
- SEM - Scanning Electron Microscopy
- SIMS - Secondary Ion Mass Spectroscopy
- SBD - Schottky Barrier Diode
- SMU - Source Measurement Unit
- SRL - Strain Relief Layers

- STEM - Scanning Transmission Electron Microscopy
- TBR - Thermal Boundary Resistance
- TBR_{eff} - Effective Thermal Boundary Resistance
- TCAD - Technology Computer-Aided Design
- TEM - Transmission Electron Microscopy
- TLM - Transfer Length Method
- UID - Unintentionally Doped
- UHV - Ultra High Vacuum
- VB - Valence Band
- VRH- Variable Range Hopping

Chapter 1

Introduction

Global energy demand grows rapidly each year and is predicted to increase by almost 50% from 2020 to 2050 [1], which in combination with current concerns about the direction of climate change and its impact on human life worldwide calls for more efficient energy solutions across all the sectors. Si-based power electronics has dominated the market for over 60 years thanks to continuous optimization of device processing and development of new structures such as insulated gate bipolar transistors (IGBTs) and thyristors [2]. However, despite Si devices nearing their theoretical limits, over 90% of power electronics is still made up of Si [3] [4]. The demand for higher blocking voltages, faster switching speeds as well as more compact and efficient modules creates a unique opportunity for novel wide bandgap semiconductors to exploit.

Figure 1.1 shows a comparison of some critical material parameters between Si, SiC and GaN. The parameteres shown in the figure represent typical values quoted in the literature, however they do not fully reflect the anisotropic nature of some material properties. Out of the three, GaN shows the highest critical electric field, exceeding that of Si by an order of magnitude, indicating GaN transistors are capable of withstanding 10 time the voltage of equivalent Si device of the same size, making it a good candidate for high power electronics. In addition, GaN exhibits high electron mobilities on the order of 1250 $cm^2/V{\cdot}s$ for bulk (see red star in Fig. 1.1) and 2000 $cm^2/V{\cdot}s$ for 2DEG, which in combination with high saturation velocity of the carriers offer higher switching speeds and wider bandwidth that can be effectively utilised in 5G power amplifiers. It has to be noted that carrier mobilities for each of the considered materials will exhibit anisotropic behaviour, due to anisotropy in effective masses of the carrier and is describe in more detail in the following chapter.

Although thermal conductivity (κ) of GaN as measured in most heteroepitaxially grown devices is ~half of silicon carbide's, GaN single crystals have been measured with κ as high as

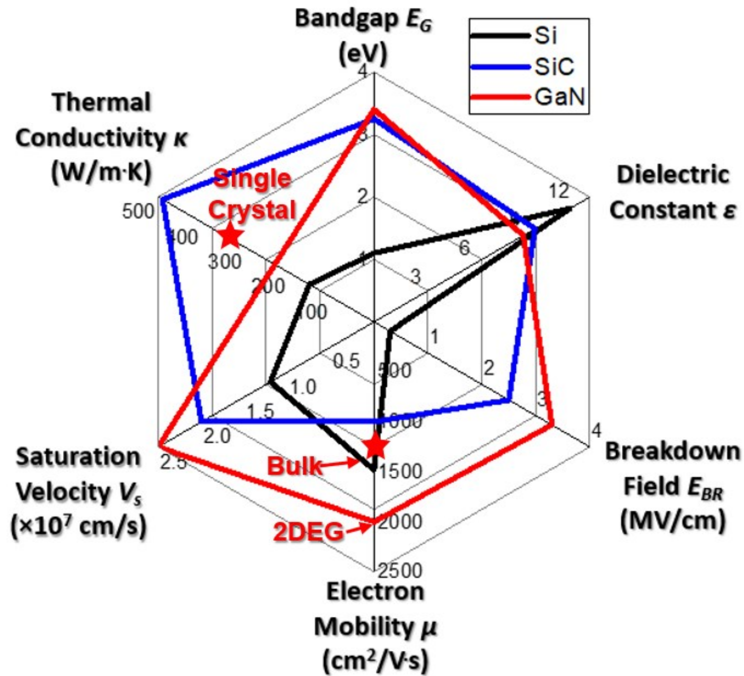

Figure 1.1: **a)** Spider diagram comparing key material properties of Si, SiC and GaN. Reported values found in [5].

269 W m^{-1} K^{-1} [6], with theoretical predictions in excess of 400 W m^{-1} K^{-1} at room temperature [7] [8] [9]. However, thermal conductivities of SiC and GaN are anisotropic in nature, resulting in reduced κ in certain crystallogrpahic directions. For GaN the anisotropy results in up to 14% difference in κ at 300 K [10], while for SiC, the difference can be as high as ~30% [11].

GaN-on-SiC RF HEMTs offer the advantages of GaN-based heterostructure with added thermal benefits of SiC substrate. Even though existing technologies based on GaAs and InP HEMTs allow for higher achievable operating frequencies, small bandgaps of these materials limit their power handling capabilities. For RF application GaN enables significant improvements in power capacity of the devices compared to aforementioned materials.

In addition to GaN and SiC other prominent materials have emerged over the past few decades competing for a share of a market previously occupied by Si. Some notable examples include gallium arsenide, indium phosphite (both mentioned above), and very recently gallium oxide in its beta phase (β-Ga_2O_3) as well as diamond. GaAs and InP show outstanding electron mobilities up to 5400 and 8400 cm^2/V·s respectively, however their bandgap exceed that of Si only by a small margin, limiting their application to relatively low voltages. Due to its ultra wide bandgap, β-Ga_2O_3 can achieve breakdown fields three times larger than GaN. However, low electron mobility (and lack of available p-type conduction due to flat valence bands) in combination with very low thermal conductivity limit the application of this material to a high-voltage, low frequency region [12]. Lastly, despite its excellent breakdown fields, high electron mobilities and outstanding thermal conductivity, diamond poses a variety of challenges on a more

Table 1.1: Figure of Merit Relative to Si

Figure of Merit	Si	SiC	GaN
Baliga ($\epsilon\mu E_G^3$)	1	223	190 (330)
Keyes ($\kappa\sqrt{cv_s/4\pi\epsilon}$)	1	3.6	1.8
Baliga High Frequency (μE_C^2)	1	45	36 (63)
Johnson ($E_C^2 v_s^2/4\pi^2$)	1	215	400

Data taken from [15], and [5]. Some FOMs for GaN quoted using bulk mobility values with added values based on 2DEG mobility in the brackets.

practical level. Deep p-dopant in the form of boron and lack of n-doping, high costs of growth, difficult processing as well as issues in diamond integration with other materials are only some of the problems facing this technology [13] [14]. Although these materials can possibly play an important role in future electronic devices for power and RF applications, currently SiC and GaN show most promise in replacing Si in the existing applications.

To assess the suitability of a chosen technology for a chosen application, some key performance parameters need to be considered. For power electronics, qualities such as breakdown field and voltage, area specific On-resistance, peak saturation current and peak power output are particularly important [15]. For this reason wide bandgap semiconductors such as SiC and GaN are more suitable, offering reliable performance while being able to handle large power densities. For RF electronics, the suitability of a device high frequency switching applications can be assessed by examining quantities such as carrier mobility, On / Off drain current ratio, peak drain current, transconductance, f_T and f_{max}. In RF electronics, capacity to handle is less important, while minimising switching losses is of crucial importance. Therefore, semiconductors with large electron mobilities such as GaAs and InP are more suitable for RF applications.

In addition to examining key device parameters and material properties, figures of merit (FOMs) have been developed to quantify combined material parameters in the chosen area of interest. Table 1.1 shows a comparison between SiC and GaN relative to Si across five major FOMs.Performance of a power device switching at low frequencies can be assessed based on Baliga figure of merit (BFOM), which attempts to quantify conduction losses that are dominant in this application mode. Here, despite comparable bandgap and dielectric constant of GaN and SiC, HEMTs based on GaN heterostructures have an edge over the latter material mainly due to high electron mobility of the 2DEG. However, bulk mobility of GaN is significantly lower then that of the 2DEG (see Fig. 1.1), which would reduce the BFOM of GaN by around 40%. To quantify suitability of a given material for high frequency applications, Johnson's figure of merit (JFOM) and Baliga's High Frequency figure of merit (BHFFOM). The first one has been derived to define the switching losses for a low voltage transistor from a power-frequency product, while the latter attempts to describe the efficiency of a FET in high power applications [16] [17]. In both

metrics GaN devices utilising high electron mobility of the 2DEG outperform both Si and SiC indicating suitability of this technology for high frequency applications. The conduction losses of a power FET can be quantified based on Baliga figure of merit (BFOM), which is defined as the product of carrier mobility, dielectric constant and the bandgap of the device. In this metric GaN heterostructures show significant improvement on SiC transistors predominantly due to high electron mobility of the carriers in the 2DEG.

In addition, Keyes figure of merit (KFOM) describes the thermal limits for switching applications and is defined by thermal conductivity of the material and saturation velocity of the carriers [18]. Due to its excellent thermal conductivity SiC significantly outperforms GaN, which due to the compromised quality of heteroepitaxially grown films falls short of theoretically predicted thermal conductivities and experimentally measured values for single crystals. Although GaN HEMTs show improved performance in this metric, SiC devices outperform bulk GaN due to significantly higher thermal conductivity and comparable bulk carrier mobilities. Overall, despite improved switching and conduction losses in GaN, SiC is a more suitable material for high power applications as it offers improved thermal management and reliability at more extreme operating conditions.

Despite very promising performance of AlGaN/GaN HEMTs in comparison to competing technologies, commercialisation of GaN based micro-electronic devices took decades starting in the late 1960s with the first report of single crystal GaN film grown on 2 cm^2 sapphire substrate by Maruska and Tietjen [19]. Early GaN films were very defective and contained large quantities of impurities, defects and unintentional dopants, but throughout 1970s and 80s major improvement in growth quality and doping control have been made [20], culminating in development of first GaN-based blue LEDs by Nakamura *et al.* [21] that has been awarded with Noble Prize in Physics in 2014.

The first demonstration of a 2DEG in an AlGaN/GaN heterostructure was carrier out by Khan *et al.* in 1992 by growing a high electron mobility transistor on sapphire using a low-pressure MOCVD method [22], however soon after GaN HEMTs started being grown on SiC and eventually Si [23] [24]. Despite significant lattice and themal expansion coefficient mismatch, the cheap cost of production was the main driving force for developing modern GaN-on-Si HEMTs. Over the years, growth and fabrication techniques have improved significantly in combination with the introduction of field plates and reliable passivation leading to more robust transistors compared to the early devices. In addition, various techniques have been developed (such as p-GaN, recessed and tri-gates) to allow for commercial production of E-mode HEMTs, which are defined by positive threshold voltage [25] [26] [27].

Modern GaN based devices are gradually becoming more commercially available for power and RF applications, however there are still some major issues relating to device reliability preventing GaN technology from dominating the semiconductor markets. Despite best efforts to optimise growth conditions, GaN devices still contain significant concentrations of impurities,

unintentional dopants and crystalline defects that provide avenues for device degradation especially at high voltage operation. Nowadays surface effects are well controlled using carefully designed field plates and passivation layers, however there are still unresolved issues relating to the impact of buffer layers on device performance. Since modern GaN transistors are grown on foreign substrates, effects of lattice and thermal expansion coefficient mismatch result in significant strain and dislocation inside the epitaxy especially near the heterointerfaces. This situation makes it necessary to include thick buffer layers in order to reduce the quantities of defects and to separate electrically active regions from the highly defective areas. The buffer layer is therefore of critical importance for GaN HEMT operation, and is the main focus of the work presented in this thesis.

To ensure device operation at high voltages, GaN buffers have to be insulated by the introduction of extrinsic dopants, mainly iron (Fe) and carbon (C). Fe is the dopant of choice for RF applications, with typical doping concentrations in excess of $\sim 10^{18}$ cm^{-3} and its main purpose is to suppress vertical leakage currents and to ensure appropriate carrier confinement in the channel. In addition, Fe-doped buffers in combination with well designed field plates have delivered record power outputs [28] [29]. However, Fe is insufficient to provide adequate insulation for power applications, therefore carbon doping is commonly used in power transistors with the doping concentrations on the order of 10^{19} cm^{-3}. C doping results in lower Off-state leakage and higher breakdown voltages in comparison to Fe. Although introduction of these dopants performs its intended function of insulating GaN buffers, some aspects of their electrical behaviour are not well understood. Recent work on C-doping in GaN indicates the variation in doping concentration can have a significant impact of charging and discharging properties of the buffer [30]. Moreover, despite providing excellent insulation, C-doped buffers are susceptible to phenomena such as dynamic R_{ON}, where the device On-resistance increases temporarily (in some cases for 1000s of second) following a period of Off-state stress. A solution to the issue of dynamic R_{ON} has been proposed by Panasonic with their gate-injection transistor (GIT) [31], however introduction of p-GaN region for hole injection carries its own significant reliability challenges [32]. In any case, it is impossible to completely avoid incorporation of C during device growth by MOCVD method and even relatively small concentrations of this dopant can have significant impact on electrical performance of the devices.

In addition to electrical considerations, the push towards higher achievable power densities and faster switching speeds poses significant challenges for thermal performance of GaN based devices. As the device power output increases, so does the peak channel temperature. Since the device lifetime is directly related to operating temperatures by the Arrhenius equation, effective heat conduction away from the hot spot is of paramount importance. The heat diffusion inside the device can be affected by a variety of factors such as thermal conductivities of the epitaxial layers, quality of the interfaces and even the device design and geometry. Modern solutions for thermal management of commercially available devices involve combination of GaN with high-thermal

conductivity substrates such as SiC and diamond (if possible), as well as careful engineered packaging including microfluidic cooling.

The main theme of this thesis revolves around understanding of the electrical and thermal performance GaN - based RF and power device by performing experimental measurements on novel GaN structures and combining these results with computational simulations to build a deeper understanding of physical mechanisms limiting their performance. From the electrical perspective, the effects of C doping on the dynamic electrical behaviour of the buffer are studied in detail, followed by the analysis of new ideas involving complete buffer removal and its benefits for RF electronics. From the thermal perspective, the impact of individual epitaxial layers and interfaces on heat dissipation in an operating devices is studied.

1.1 Thesis outline

The main theme of this thesis is the electrical and thermal characterisation of GaN - based power and RF devices. For this reason, Chapter 2 includes some fundamental concepts relating to electrical and thermal properties of GaN. In this chapter, device operation as well as key reliability issues will be discussed to provide an appropriate context and motivation for the work presented here. In addition, Chapter 3 gives an outline of experimental techniques for electrical and thermal characterisation used in this thesis, giving a comprehensive description of experimental environment, hardware and software used throughout this work. This part of the thesis concludes the introductory segment of this work and is followed by the chapters outlining key research outputs of the thesis.

Chapter 4 describes a study carried out on GaN-on-Si transfer length method (TLM) structures, aimed at investigating the charge transport processes in the C - doped GaN buffer and channel layers. This study involves substrate ramp sweep measurements and current transient measurements aimed at separating and identifying key charge transport mechanisms taking place in the GaN layers in the voltage range up to 200 V. Chapter 5 constitutes a continuation and extension to the previous chapter. Here, the ideas developed on simple TLM structures are applied to lateral GaN-on-Si Schottky barrier diodes. The relationship between dynamic On-resistance and charge transport processes in the buffer is explored using a combination of electrical measurements and computational simulations.

In chapter 6, novel "buffer-free" GaN-on-SiC HEMTs are characterised from the electrical and thermal perspective and their performance is compared to conventional GaN-on-SiC HEMTs with thick Fe - doped buffer. The experimental measurements are combined with computational simulations to obtain a comprehensive image of the device performance in each of the investigate areas. Further computational parametric analysis is carried out and a device design for optimised electrical and thermal performance is proposed.

Chapter 7 focuses on electrical and thermal characterisation of proof-of-concept GaN HEMT

devices transferred and bonded onto SiC substrates using novel adaptive low-temperature resulting in covalent bonding between the transferred heteroepitaxial film and the bond substrate. Using a combination of experimental measurements and computational simulations, this work serves as a demonstration of the benefits of this technique, as can be applied to a wide range of III-nitride devices and substrates. The main findings of this thesis are concluded in Chapter 8.

Chapter 2

Theoretical Background

This chapter describes key theoretical concepts relating to GaN-based RF and power micro-devices including electrical and thermal properties of the material. Epitaxial structure of typical GaN-based transistors and diodes is discussed with particular focus on device operation, reliability and challenges involved in growth and fabrication of GaN on foreign substrates.

2.1 Material Properties

This section introduces key theoretical concepts relating to fundamental material properties that allow for creation of GaN-based electronic devices, starting on a molecular level with crystal structure and polarization effects, and moving on to band diagrams, phonons and heat transfer in semiconductor materials.

2.1.1 Crystal Structure

Gallium nitride is a group III-V binary, direct band gap semiconducting material that exists in three possible structures: rocksalt - represented by face-centered cubic lattice of Ga and N atoms, zinc-blende - consisting of face-centred tetrahedral lattice with only half of the available sites occupied by atoms, and wurtzite. GaN rocksalt phase is meta-stable and therefore currently unsuitable for device fabrication. However GaN-based devices can be manufactured from zinc-blend and wurtzite structures, with the latter being far more common and well established, therefore it will be the main focus of this thesis. Wurtzite GaN cell structure shown in Fig. 2.1a consists of intermittent layers of hexagonal close packed gallium (Ga) and nitrogen (N) atoms, misaligned in relation to one another by 5/8 of the c lattice constant. The c lattice constant lies in

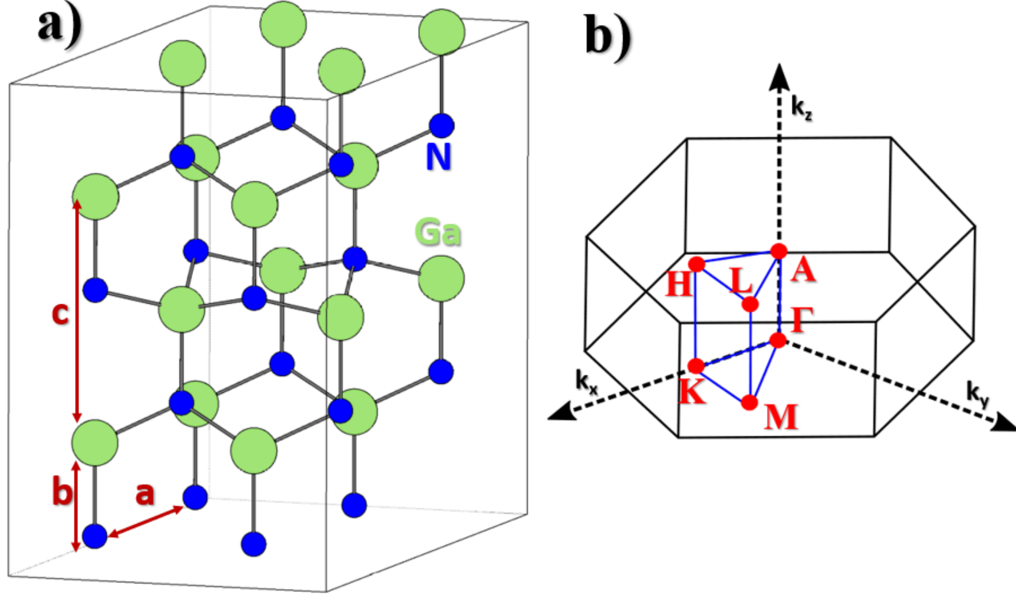

Figure 2.1: **a)** Schematic representation of GaN wurtzite structure in real space. The ratio of c/a is an important parameter affecting spontaneous polarization of the crystal. **b)** First Brillouin zone of a hexagonal structure in momentum space with key symmetry points indicated.

the [0001] direction (axial direction of the hexagonal column) and describes the closest distance between two equivalent atoms in the unit cell. Most GaN-based devices have Ga-face (grown in the [0001] direction) at the top face, however successful device fabrication based on N-faced GaN (grown in the [000$\bar{1}$] direction) has also been reported [33] [34]. The conventional N-rich conditions and high temperatures present during MOCVD growth favour formation of Ga-polar GaN, hence the devices grown in [0001] direction are more prevalent than the N-polar alternative, which is more challenging to realise. The polar nature of Ga-N bond results from the difference in electronegativity, which is defined as atom's ability to attract electrons. Nitrogen is ~70% more electronegative than gallium, resulting in a dipole moment along the bond. Due to lack of inversion symmetry in the GaN structure, the choice of face termination will affect the direction of polarization in the crystal and will have a significant impact on thermal stability, chemical behaviour and adatom mobility [35].

Transformation of crystal Wigner-Seitz unit cell (primitive unit cell in real space) of GaN wurtzite structure into reciprocal space gives the first Brillouin zone, which is shown in Figure 2.1b. The first Brillouin zone is constructed from perpendicular bisectors of the reciprocal lattice vectors starting at the origin. The centre of Brillouin zone is denoted by the point Γ, which corresponds to reciprocal lattice wavevector $k = 0$. Wavevectos k_x, k_y and k_z correspond to transformation of Cartesian coordinates into the reciprocal lattice space. According to Bloch theorem, if the energy in the real lattice space is periodic, then the wavefunction that satisfies the Schrödinger equation can be expressed as a function that is periodic in the reciprocal lattice

space. Consequently, Bloch theorem also predicts periodicity of energy in the reciprocal space. Thus, when considering electronic band diagrams of a material, it is sufficient to investigate it only within the first Brillouin zone.

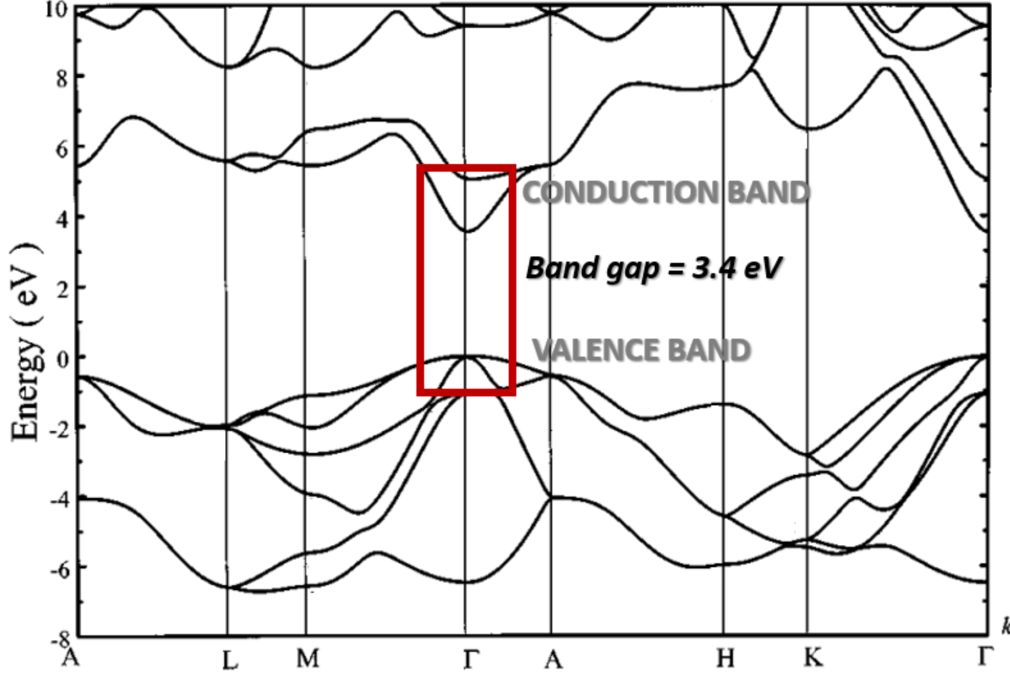

Figure 2.2: Electronic band diagram of wurtzite GaN with direct band gap of 3.4 eV at room temperature (highlighted by a red box). The other forms of GaN structures include rocksalt and zinc-blende, which differ in electronic band diagrams. Figure adapted from [36] with the permission of AIP Publishing.

Figure 2.2 shows the electronic band diagram of GaN across the first Brillouin zone. At temperatures exceeding 0 K only the bands closest to the Fermi level (within thermal energy $k_B T$) will be partially filled and therefore they will determine the electrical properties of the material. For GaN, the minimum band gap is located at the point Γ, with the energy of 3.4 eV at 300 K. The curvature of the band determines the effective mass of the carriers. Due to high curvature of the conduction band (see the red box in Fig. 2.2) effective mass of electrons in GaN is low resulting in high mobility of the carriers. However, the curvature of the valence bands at Γ point for wurtzite GaN is not isotropic, consequently leading to anisotropy in effective mass of the carriers. In the direction parallel to c axis, the electrons are heavier than in the perpendicular direction, with effective masses of $m^*_{e,par}$ = 0.2 m_0 and $m^*_{e,perp}$ = 0.18 m_0, where m_0 denotes the mass of a free electron. For comparison effective mass of electrons in Si m^* = 1.06 m_0, while in SiC $m^*_{e,par}$ = 0.29 m_0 and $m^*_{e,perp}$ = 0.42 m_0 [37] [38]. In addition, at the Γ point valence band of GaN is made up doubly degenerate band, corresponding to effective hole masses of $m^*_{h,par}$ = 1.10 m_0 and $m^*_{h,perp}$ = 1.65 m_0 and a split-off band with hole masses $m^*_{h,par}$ = 0.15 m_0 and $m^*_{h,perp}$ = 1.10 m_0 [39].

As the minimum of the conduction band and maximum of the valence band coincide at Γ point, wurtzite GaN is a direct band gap semiconductor. Based on experimental data collected for a wide range of semiconducting materials, breakdown electric field E_B for direct band gap semiconductors can be described according to an empirical formula as:

$$E_B \propto E_G^{2.5} \tag{2.1}$$

where E_G is the band gap [40] [41]. Thus, wide band gap semiconductors such as GaN are less susceptible to breakdown due to impact ionization, resulting in critical field of GaN of 3.3 MV/cm.

2.1.2 Polarization Effects

Nitrogen, unlike gallium and other group III elements, is a highly electronegative element, which in combination with lack of inversion symmetry leads to formation of dipole in the unit cell of GaN. Thus, group III-V semiconductors possess strong polarization fields, which can be divided into two components: spontaneous and piezoelectric polarization. Spontaneous polarization (P_{SP}) is a direct result of difference in electronegativity between Ga and N, where the effective Coulomb attraction of the N nucleus is greater than that of the metal leading to polarization along the [0001] direction in an unstrained crystal. Spontaneous polarization strongly depends on the molecular symmetry, with AlN exhibiting higher P_{SP} than GaN, due to increase in bond length and reduction in the c/a ratio (see Fig. 2.1a) [42]. III-V nitrides show positive correlation between deviation of lattice parameter ratios from the ideal closed packed hexagonal structure and the magnitude of spontaneous polarization [43].

Moreover, if the material is strained such that the ideal lattice parameters change, an additional component of polarization - piezoelectric polarization (P_{SP}) will be induced in the lattice. Piezoelectric polarization can be described according to Hooke's law as:

$$P_{PZ,i} = \sum_j e_{ij}\epsilon_{ij} \tag{2.2}$$

where e_{ij} denotes the piezoelectric constant and ϵ_{ij} is the deformation potential. The total polarisation of a crystal P_{TOT} is simply defined as the sum of these two components:

$$P_{TOT} = P_{SP} + P_{PZ}. \tag{2.3}$$

Piezoelectric polarization is very sensitive to stress and plays an important role during pseudomorphic growth of III-V nitrides with different lattice constants, as the lattice mismatch will induce strain in the top layer. Thus, the total polarization can be affected by application of stress that results in change in dipole moment along the [0001] axis. Figure 2.3 shows variation in polarization of a heterostructure consisting of AlN and GaN (both materials have wurtzite lattice structure, but differ in lattice constant) with applied stress compared to unstrained free-standing GaN layer (Fig. 2.3a). If tensile stress is applied to AlN, then the total polarization increases due

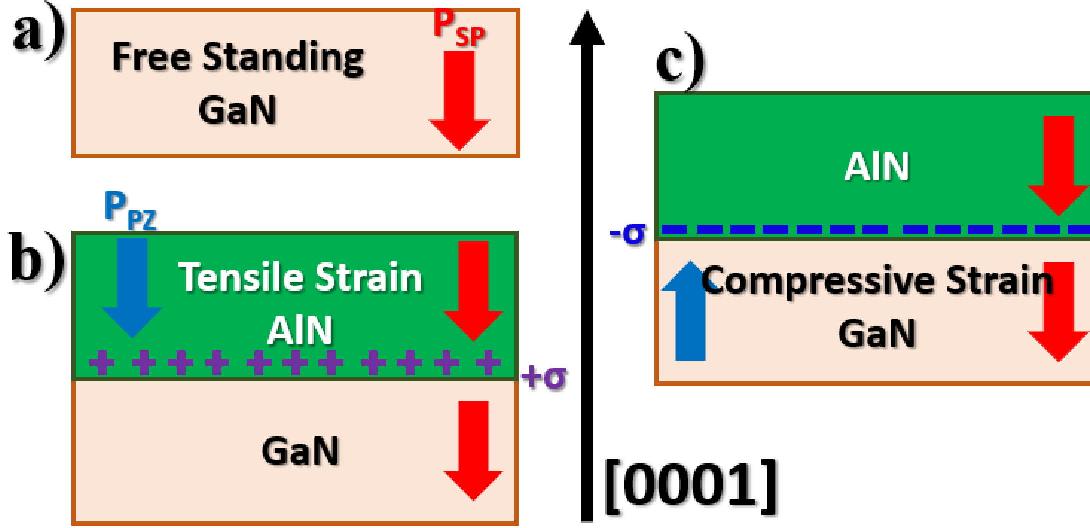

Figure 2.3: Direction of spontaneous (red) and piezoelectric (blue) polarization vectors and polarization charges σ for **a)** free standing GaN, **b)** tensile-strained AlN on GaN and **c)** compressive-strained GaN on AlN.

to both P_{SP} and P_{PZ} acting along the same direction (Fig. 2.3b). On the other hand, if GaN is grown on top of AlN resulting in biaxial compressive strain, the negative polarization charge will accumulate at the heterointerface as the piezoelectric polarization acts in the opposite direction to spontaneous polarization vectors of AlN and GaN (Fig. 2.3c).

The example shown in Figure 2.3 demonstrates the importance of stress on the formation of polarization charges in heterostructures. Heterostructure is defined as a system consisting of two materials grown one on top of the other with different energy bandgap, which leads to formation of band offset at the interface due to discontinuity in valence and conduction bands. All the work presented in this thesis revolves around AlGaN/GaN heterostructure. AlGaN is an alloy created by addition of Al atoms to GaN. At first approximation, many physical properties of ternary compounds such as AlGaN can be determined using Vegard's law, which involves linear interpolation of property in question [44]. Vegard's law has been established empirically, and can be successfully applied to estimate parameters such as band gaps and lattice constant of various compound semiconductors [45] [46]. Thus, the bandgap of $Al_xGa_{1\text{-}x}N$ would be expressed as:

$$E_G(x) = xE_G^{AlN} + (1-x)E_G^{GaN} \tag{2.4}$$

where x denotes the molar fraction of Al in $Al_xGa_{1\text{-}x}N$, with E_G^{AlN} = 6.2 eV and E_G^{GaN} = 3.4 eV. Unfortunately, Vegard's law is an approximation and on closer inspection for a number of different materials Vegard's law shows significant discrepancy with the experimental results, thus other non-linear models have been proposed [47] [48]. Therefore, bandgap of a ternary compound such as AlGaN can be expressed more accurately by the equation:

$$E_G(x) = xE_G^{AlN} + (1-x)E_G^{GaN} + bx(1-x) \tag{2.5}$$

where the term $bx(1-x)$ accounts for the curvature of the bandgap as a function of molar fraction x, with b denoting the bowing parameter [15].

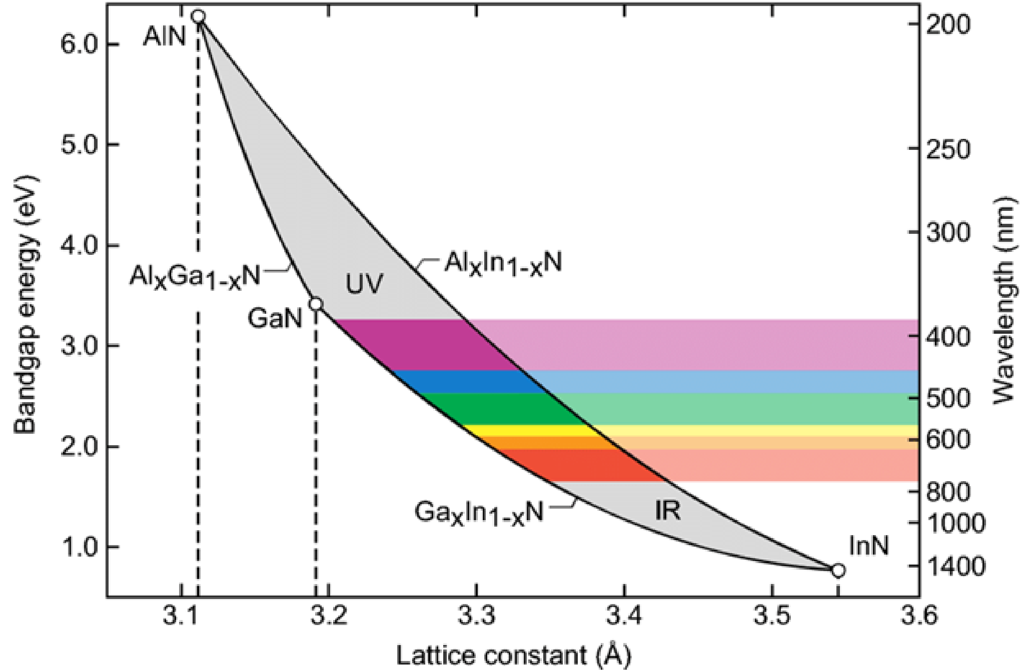

Figure 2.4: Lattice constant and band gap relationship for GaN, AlN and InN material systems. Figure adapted from [49].

As suggested by Eq. 2.5 and shown in Figure 2.4, incorporation of Al into GaN leads to increase in bandgap of the alloy. The growth of AlGaN on GaN will therefore result in an abrupt interface between the two materials. In addition, increase in Al molar fraction causes the increase in lattice constant of AlGaN. Thus, AlGaN layer grown on top of Ga-face GaN will be under biaxial tensile strain, which means the directions of spontaneous and piezoelectric polarization will align creating a region of positive polarisation charge at the heterointerface σ, which can be expressed as [42]:

$$|\sigma| = |P_{PE,AlGaN} + P_{SP,AlGaN} - P_{SP,GaN}|. \tag{2.6}$$

Figure 2.5a shows the direction of different polarization components and distribution of polarization charges. The induced positive polarization charge at the interface between GaN and AlGaN attracts the electrons, which will concentrate at the top of GaN layer right at the very heterointerface, but will not enter the AlGaN layer as the difference in its bandgap relative to GaN will act as a barrier to these charges. This high concentration of negative charge carriers within a very small space is know as the 2D electron gas (2DEG). The source of these electrons is attributed to the donor like surface states at the top of the AlGaN layer. By releasing the electrons to form 2DEG, the Fermi level is pinned at the energy level of the surface donors, creating surface potential and internal electric field in AlGaN [50]. This process is schematically shown in Figure 2.5b.

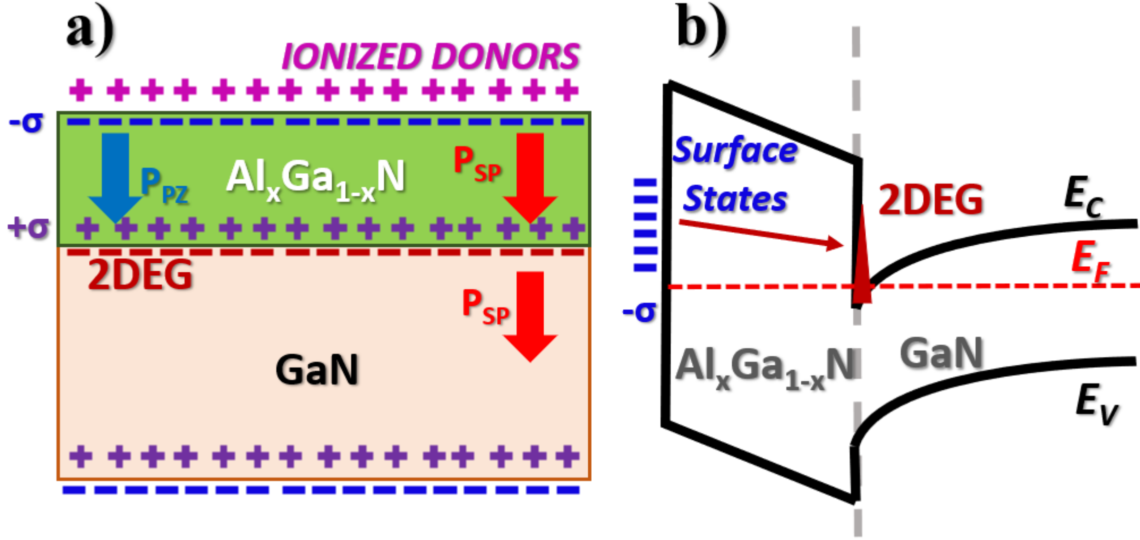

Figure 2.5: **a)** Total polarization and resulting charges in a typical $Al_xGa_{1-x}N/GaN$ heterostructure. **b)** Corresponding band diagram indicating the movement of electrons away from surface states towards heterointerface to form the 2DEG.

2.1.3 Phonon Dispersion

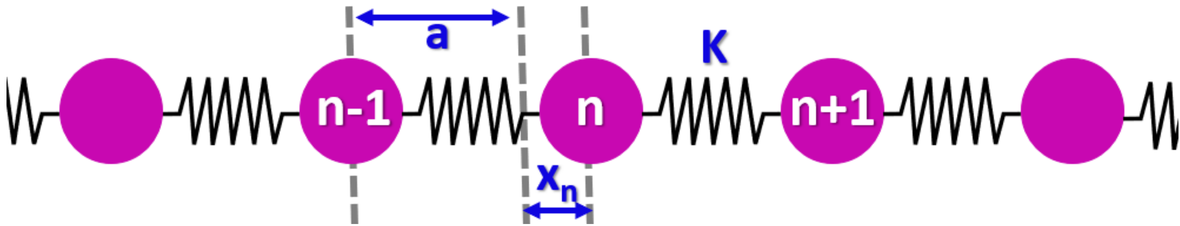

Figure 2.6: Schematic representation of a 1D lattice of atoms as balls on sprigs with spring constant K, with interatomic spacing of a and possible displacement of x_n.

Phonons represent vibrations in the crystal lattice resulting in displacement of atoms around their equilibrium position and are extremely helpful in understanding heat flow in solid materials. Figure 2.6 shows an infinite 1D monoatomic chain, with atoms represented as point masses and bonds as springs with the spring constant K. The displacement of the nth atom in the chain can be described in relation to its neighbouring atoms by combining Newton's 2nd law and Hook's law according to the expression:

$$m\frac{d^2t}{dx^2} = K(x_{n+1} + x_{n-1} - 2x_n) \tag{2.7}$$

where x_i denotes the displacement of an atom at the position n_i and m denotes its mass. By solving the above differential equation, we obtain the dispersion relation for the vibrational frequency of the atoms ω:

$$\omega = \sqrt{\frac{2K}{m}}\left|sin\left(\frac{ka}{2}\right)\right| \tag{2.8}$$

where k stands for wavevector in the inverse space.

The solution to diatomic lattice of masses m_1 and m_2 can be obtained by solving simultaneous equations based on Eq. 2.7. Thus, the dispersion relation for this system becomes:

$$\omega^2 = K\left(m_1^{-1} + m_2^{-1}\right) \pm K\sqrt{\left(m_1^{-1} + m_2^{-1}\right)^2 - \frac{4sin^2(ka)}{m_1 m_2}}. \tag{2.9}$$

At Γ point of the Brillouin zone k=0, which simplifies the above equation to:

$$\omega_\Gamma = \sqrt{K\left(m_1^{-1} + m_2^{-1}\right) \pm K\left(m_1^{-1} + m_2^{-1}\right)}. \tag{2.10}$$

Equation 2.9 implies there are two possible frequencies at Γ: one with $\omega = 0$ and one with $\omega = \sqrt{2K\left(m_1^{-1} + m_2^{-1}\right)}$. The phonon branch with zero energy is call the acoustic branch – this mode represents coherent movement of atoms in the lattice, while the branch with non-zero energy is call optical branch – these modes represent out-of-phase motion of adjacent atoms in the lattice. Figure 2.7 shows a wavevector-frequency dispersion relation for a diatomic chain of atoms. Although optical phonons display higher frequency oscillations, the group velocity of acoustic branch is much higher, meaning they are significantly more efficient in heat conduction in a semiconductor material.

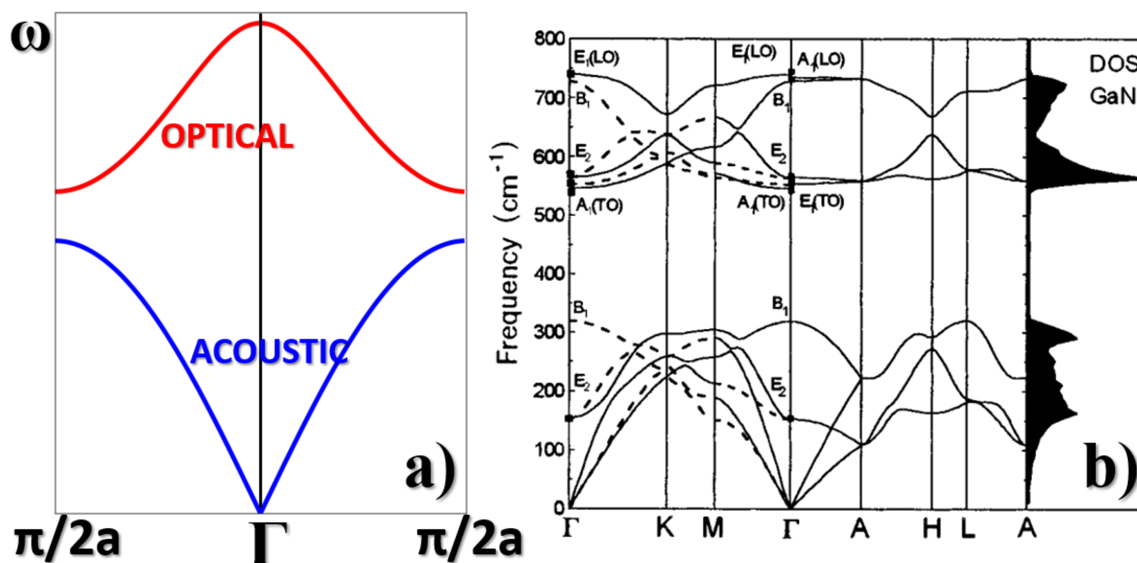

Figure 2.7: **a)** Calculated wavevector-frequency curve for a diatomic 1D chain of atoms with two separate phonon branches: acoustic (blue) and optical (red). **b)** Full wavevector-frequency phonon dispersion for wurtzite GaN. Figure reprinted from [51] with the permission of APS.

In general, for a unit cell with N atoms there will be $3N$ phonon branches with 3 acoustic and $3N$-3 optical branches. Phonon dispersion can either be obtained using computational methods (e.g. dynamic lattice calculations and density-functional perturbation theory) [51] [52] or measured using inelastic neutron scattering (suitable for large crystals), X-ray or Raman scattering [53]. Figure 2.7b shows a phonon dispersion for GaN with acoustic and optical modes

separated by a gap, which in general case of III-V semiconductor will widen as the mass difference between the atoms increases.

In a crystal structure phonon motions are characterised by their displacement vectors which are determined by the symmetry operation of the crystal. The symmetry operations of the crystal can be described using group theory. By assessing the symmetry of an infinite crystal in equilibrium it is possible to assign a space group, which for wurtzite structures is C_{6v} – indicating cyclic symmetry with 6-fold rotational axis. The phonon modes included in this point group include two A_1 modes, two B_1 modes, two E_1 and further two E_2, all of which are marked in Fig. 2.7b. Further discussion of the phonon modes in GaN and their application for temperature measurements are presented in the next chapter.

Due to lack of spin, phonons are classified as bosons and as such they follow Bose-Einstein statistics. The population of phonons with an energy E at the temperature T can therefore be described according to the equation:

$$n(E,T) = \frac{1}{e^{\frac{E}{k_B T}} + 1}. \tag{2.11}$$

In addition, phonons do not follow Pauli exclusion principle and thus, as temperature tends to 0 K, phonons accumulate in their ground state resulting in no available heat carriers. As the temperature increases, when the thermal energy $k_B T >> E$ the equation 2.11 tends to Rayleigh-Jeans limit:

$$n = \frac{k_B T}{E} \tag{2.12}$$

suggesting linear increase in thermal conductivity of the material with temperature. This idea was further developed in Debye model where by applying equipartition theorem to lattice vibrations in 3D, the variation of specific heat with temperature was derived. At temperatures above the Debye temperature T_D the specific heat tends to $3k_B$ in agreement with Dulong-Petit law, as all the phonon modes are occupied and active. However, below T_D specific heat increases approximately as T^3 due to increasing number of active phonons in the lattice. The Debye temperature can be describe according to:

$$T_D = \frac{hv}{2k_B}\sqrt{\frac{6N}{\pi V}} \tag{2.13}$$

where h, v, N and V are the Planck's constant, speed of sound, number of particle and volume respectively. T_D represents the temperature at which the highest vibrational mode of the lattice becomes active.

2.1.4 Heat Transport in Semiconductors

The process of heat diffusion in 1D can be described according to the equation:

$$J_x = -\kappa \frac{dT}{dx} \tag{2.14}$$

where J_x is the heat flux, κ_x is the thermal conductivity and $\frac{dT}{dx}$ is the temperature gradient. By considering the kinetic theory of gases it can be demonstrated that the flux of particles in 1D can be described by $0.5 n_p < v_x >$, where n_p is the concentration of particles and $< v_x >$ is the mean velocity of particles. When a particle moves through a temperature gradient, the energy it released in the process is equal to $c\Delta T$, where c is the heat capacity of the particle and ΔT is the difference between the starting and final temperature.

For particles travelling over a distance l under a thermal gradient, the flux J can be expressed as:

$$J = -\frac{1}{3} n_p < v^2 > lc \frac{dT}{dx} = -\kappa \frac{dT}{dx}. \tag{2.15}$$

Therefore, thermal conductivity can be described according to the expression:

$$\kappa = \frac{1}{3} cvl. \tag{2.16}$$

In semiconductors and insulators heat transport is mainly facilitated by phonons, with the thermal conductivity described by the equation 2.16, which implies its strong dependence on specific heat capacity of the phonons and their mean free path. At low temperatures, specific heat capacity increases as T^3 according to Debye theorem as the phonons only scatter with the crystal boundaries and impurities in the lattice. Since collisions with the lattice and impurities do not change the momentum of individual phonons, they cannot bring about the thermal equilibrium. However, increase in temperature leads to anharmonicity in the lattice motion resulting in scattering of phonons with each other.

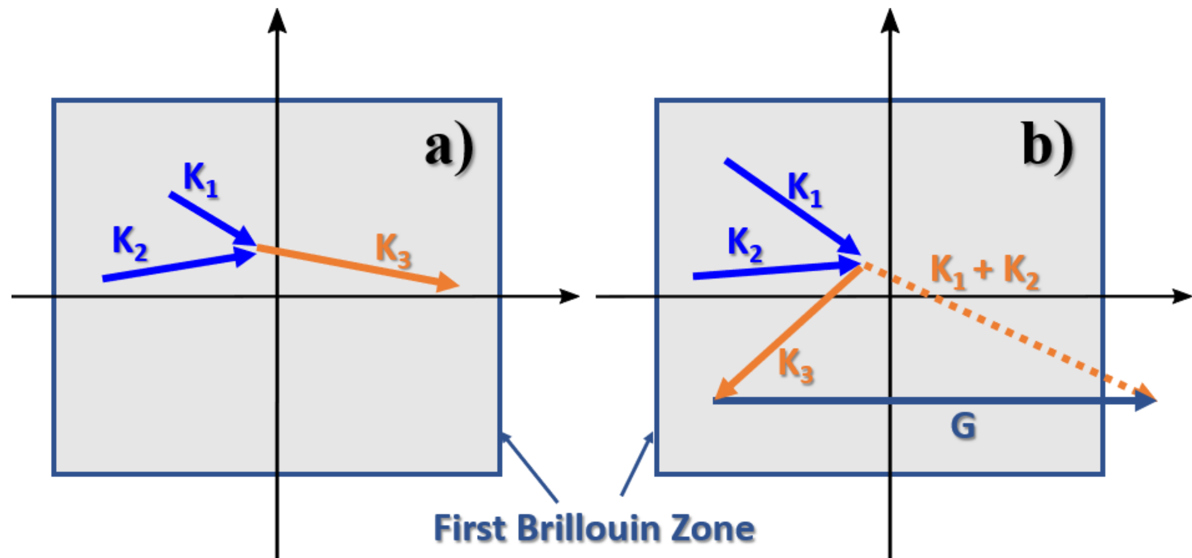

Figure 2.8: Two incoming phonons $\vec{K}_1$ and $\vec{K}_2$ scattering with one another. **a)** Normal scattering process - the resultant phonon $\vec{K}_3$ is still within the first Brillouin zone. **b)** Umklapp scattering, where the resultant phonon ends up outside of the first Brillouin zone.

The two possible modes of phonon interactions with one another are called normal and Umklapp scattering. Normal scattering process can be described as a three-phonon collision

according to:

$$\vec{K}_1 + \vec{K}_2 = \vec{K}_3 + \vec{G} \tag{2.17}$$

where $\vec{K}_1$, $\vec{K}_2$ and $\vec{K}_3$ indicate the two interacting phonons and the resultant wavevector respectively, while $\vec{G}$ represents the reciprocal lattice vector, which for a normal process is equal to 0 (see Figure 2.8a). For a perfect crystal normal scattering process does not lead to thermal equilibrium as the total phonon momentum remains the same. If, on the other hand, the resultant wavevector $\vec{K}_3$ exists outside of the first Brillouin zone, it has to be mapped back with the reciprocal lattice vector $\vec{G}$ as seen in Fig. 2.8b (see eq. 2.14 with $\vec{G} \neq 0$). Umklapp processes lead to change in phonon momentum and therefore facilitate establishing of thermal equilibrium in the material. Umklapp scattering results in the thermal resistance of a material and as the lattice temperature approaches the Debye temperature, it leads to 1/T temperature dependence of thermal conductivity [54] [55]. Figure 2.9a shows as an example of measured variation in thermal conductivity of GaN with temperature.

2.1.5 Thermal Conductivity of GaN

It has been proposed that the thermal conductivity κ of a thick GaN film at room temperature is 170 W/m·K or 250 W/m·K for single crystal GaN [58] [59]. However, theoretical calculations suggest it could be as high as 410 W/m·K, with the discrepancy attributed to scattering with lattice defects [57] [9].

Modern calculations of thermal conductivity of semiconducting materials involve solving the Boltzmann Transport Equation (BTE) using phonon dispersion curves in conjunction with phonon relaxation approximation. Callaway proposed the most famous lattice relaxation expression for thermal conductivity of a thick semiconductor film in 1959, which can be expressed as:

$$K_C = \frac{\hbar^2 q_D^5}{6\pi^2 k_B T}\left[\sum_s c_s^4 \int_1^0 x^4 \tau \bar{n}(\bar{n}+1)dx + \frac{\left(\sum_s c_s^2 \int_1^0 x^4 \tau \tau_N^{-1} \bar{n}(\bar{n}+1)dx\right)^2}{\sum_s \int_1^0 x^4 \tau_N^{-1} \bar{n}(\bar{n}+1)\left(1-\tau\tau_N^{-1}\right)dx}\right] = K_D + K_{ND} \tag{2.18}$$

where c_s is the phonon speed for s branch, q_D is the Debye radius, $\bar{n}$ is the Bose-Einstein distribution function, x is the reduced wavevector τ_N is the phonon relaxation time due to normal processes and t is the phonon relaxation time due to scattering [60]. Equation 2.15 can therefore be described in terms of the Debye term (K_D) and the term due to normal processes (K_{ND}).

The expression for thermal conductivity in Eq. 2.18 can be solved by assuming different scattering processes are independent of each other. Thus, phonon relaxation time τ can be expressed according to Matthiessen's rule as:

$$\tau^{-1} = \sum_i \tau_i^{-1} \tag{2.19}$$

where τ_i indicates relaxation time for each individual scattering mechanisms. In addition to Umklapp processes, the other main reasons for reduction in thermal conductivity of GaN film can be ascribed to scattering due to:

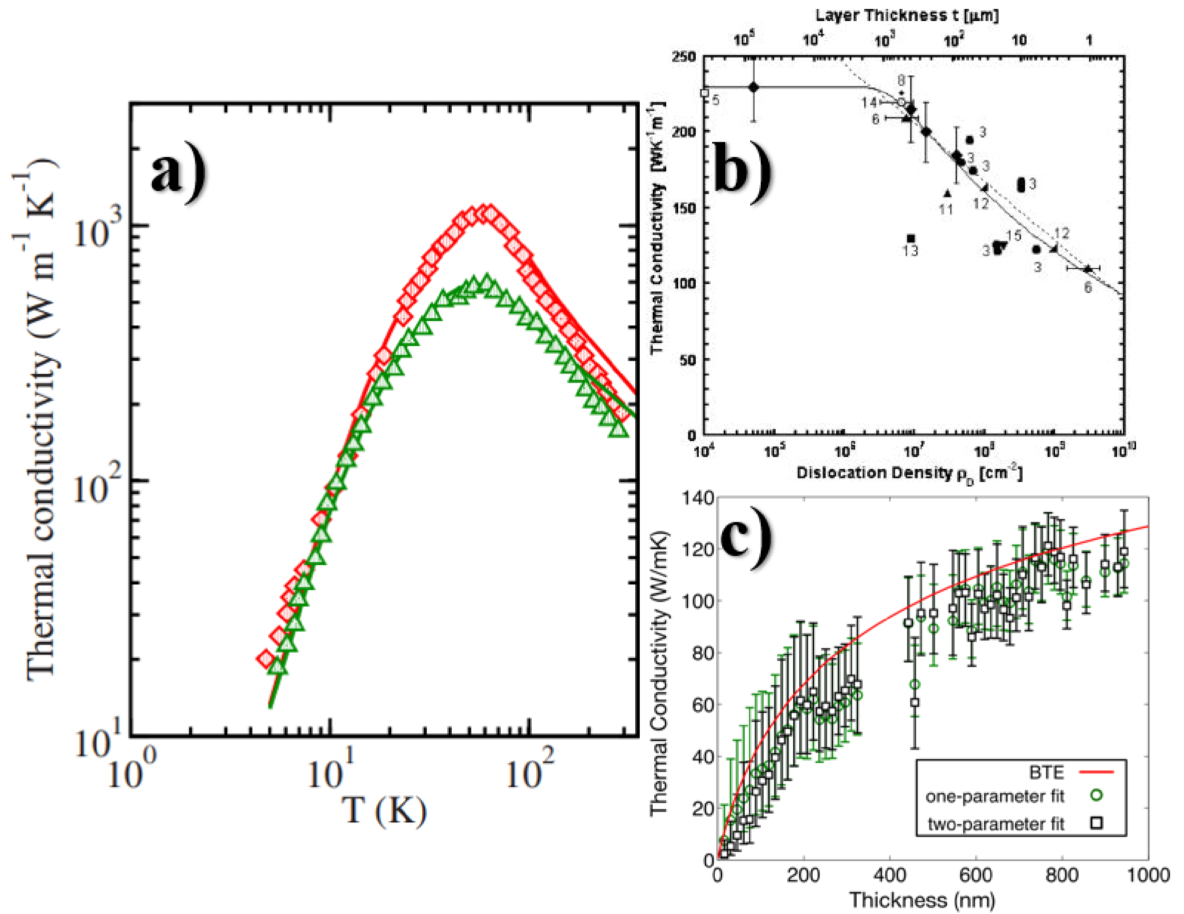

Figure 2.9: **a)** Thermal conductivity of two GaN samples as a function of temperature. Figure adapted from [9] with the permission from APS. **b)** GaN thermal conductivity as a function of dislocation density. Figure reprinted from [56] with the permission of AIP. **c)** Thermal conductivity of GaN as a function of layer thickness. Figure reprinted from [57] with the permission of the AIP.

- **dislocations** – it has been demonstrated that thermal conductivity of GaN films reduces for dislocation densities (N_{DT}) > 10^6 cm^{-2}, beyond which point the it decreases as $\kappa \propto log(N_{DT})$ [56] (see Fig. 2.9b);

- **interfaces** - as the thickness of the semiconductor d is reduced, the relaxation time for this process also falls according to $\tau^{-1} \propto d^{-1}$ [57] (see Fig. 2.9c);

- **impurities** - this includes point defects, grain boundaries and scattering due to isotopes present in the lattice, with the relaxation time $\tau^{-1} = A\omega^4$, where ω is the phonon frequency and A denotes and experimentally determined constant [9];

- **doping** - for most common dopants such as Mg, Si and C the thermal conductivity of GaN films remains unaffected until the dopant concentrations reach values in excess of 10^{19} cm^{-3}, after which thermal conductivity of GaN decreases drastically [61] [62].

In addition, GaN wurtzite crystals exhibit anisotropic thermal properties, resulting in difference in thermal conductivity κ along the c-axis as compared to in plane directions. Experimental measurements and computational simulations of GaN films indicate the thermal conductivity along the c-axis is up to 14% greater at 300 K in relation to in-plane directions, and decreases at higher temperatures [63] [64] [10]. The anisotropy in κ and its temperature dependence result from variation in phonon group velocity and phonon-phonon interaction along different lattice directions [10].

2.2 AlGaN/GaN HEMT Structure

This section describes a typical AlGaN/GaN HEMT epitaxy, contacts and passivation, highlighting some major challenges involved in growth and fabrication of the structures discussed. Figure 2.10 shows a generic epitaxial stack for an AlGaN/GaN high electron mobility transistor, which consists of the substrate, nucleation layer (NL), strain relief layer (SRL), GaN buffer, AlGaN barrier with a GaN cap (often included) and SiN_x passivation on top. In case of RF transistors often grown on SiC substrates strain relief layer is not included and most of its functions are assumed by the nucleation layer. This section describes the role of each individual layer in the epitaxial stack and highlights the challenges associated with realising their optimal functionality.

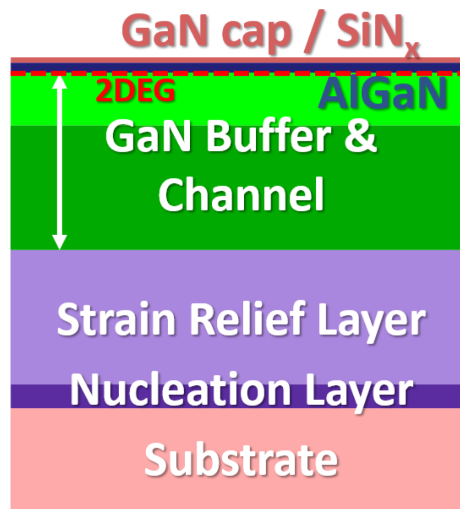

Figure 2.10: Typical AlGaN/GaN HEMT epitaxial stack consisting of a substrate, followed by a nucleation and strain relief layer. GaN buffer and channel are grown on top, with AlGaN barrier deposited next to form the 2DEG. The stack is covered with a GaN cap or passivated, usually with SiN_x.

2.2.1 Substrate

Table 2.1: Substrate Material For GaN Growth

Property	GaN	Silicon	SiC	Sapphire	Diamond
Bandgap (eV)	3.39	1.11	3.26	9.9	5.45
Thermal Conductivity (W/m·K)	230	160	490	25	1800
Lattice Mismatch (w.r.t. GaN) %	0	17	3.1	16	11
Thermal Expansion Coefficient ($\times 10^{-6}$ K^{-1})	5.5	2.6	4.46	7.5	1
Dislocation Density of GaN film (cm^{-1})	10^4 - 10^6	Low 10^8	Low 10^8	Low 10^8	10^8
Substrate Cost	Very High	Very Low	High	Medium	Extremely High
Substrate Size (mm)	30	300	150	150	10

Data taken from [15], [65] and [66].

The choice of appropriate substrate for GaN-based devices depends on several factors such as lattice mismatch between GaN and the substrate, coefficient of thermal expansion, thermal conductivity and cost. The importance of each of these factors will vary depending on intended application of the final device. Table 2.1 gives a comparison between the most common substrates used for growth of GaN.

First GaN – based power switching HEMTs have been developed on c-plane sapphire and silicon carbide (4H-SiC and 6C-SiC) due to absence of large area native GaN substrates [67]. Indeed, this is still an issue nowadays, which combined with high cost of production still constitute the main reasons for choosing other non-GaN materials as substrates for growth of GaN - based devices. For power electronics, Si is the substrate of choice as its low cost and availability of the existing Si 6- and 8-inch fabrication facilities make this material particularly attractive [68]. Due to its trigonal symmetry (111) Si plane enables growth of (0001) GaN, however the lattice mismatch of 16.9% between the two materials results in large dislocation densities in GaN films [69]. Sapphire offers only slightly smaller lattice mismatch, which in combination with low thermal conductivity, constitutes a less appealing choice especially for high power devices.

The coefficient of thermal expansion is one of the most important parameters due to growth taking place at elevated temperatures. When the epitaxy starts to cool down the residual stress in GaN can lead to bowing and even cracking, which is a significant challenge for device fabrication [70]. Due to thermal expansion coefficient of sapphire exceeding that of GaN, the layers grown on this substrate result in residual compressive stress. Conversely, for substrates with smaller coefficients GaN layers will show tensile stress (e.g. Si and SiC) [71].

Most of low RF loss power amplifiers utilise silicon carbide as a substrate of choice. SiC offers high thermal conductivity, relatively small lattice mismatch and its coefficient of thermal expansion is similar to that of GaN, resulting in reduced tensile strain as compared to Si. The main disadvantages of silicon carbide are associated with the costs of production. The dislocation

density in GaN grown on SiC is on the order of 10^8 cm^{-2}, which is comparable with Si and sapphire [67]. In recent years, a lot of attention has been devoted to integration of GaN with diamond to achieve higher power dissipations and higher operating frequencies. Despite its excellent thermal conductivity, the lattice mismatch, low coefficient of thermal expansion and high costs of production pose significant obstacles to fully utilise the thermal benefits of diamond substrates [72][73].

Often, substrate used for GaN growth include high doping concentrations, which will result in reduction in thermal conductivities shown in Table 2.1, as the added impurities lead to increased rates of phonon scattering in the material. The reduction in thermal conductivity with doping has been observed in all common substrates for GaN growth, and will strongly depend on doping concentration and the choice of dopant [74] [11].

2.2.2 Nucleation and Strain Relief Layer

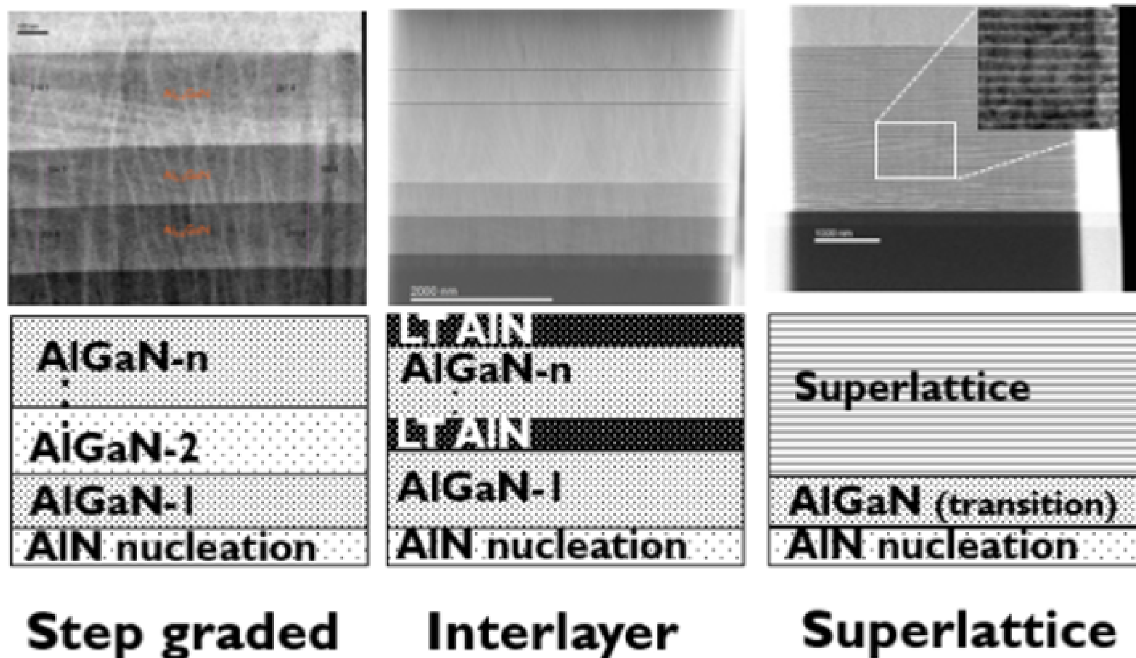

Figure 2.11: Schematic diagrams and corresponding TEM images of three most popular choices for strain relief layer architecture for GaN-on-Si devices: step graded, interlayer and supperlattice SRL. Figure adapted from [75] © IEEE (2015). In GaN GaN-on-SiC epitaxy only AlN nucleation layer is present between the substrate and the buffer.

Direct growth of GaN on foreign substrate results in large numbers of dislocations which directly adversely affect the electrical performance of the device by providing vertical leakage paths and trapping sites. It has been demonstrated by Ishikawa *et al.* that in addition to large dislocation densities, direct growth of GaN on Si substrate results in high surface roughness and formation of hollows due to melt-back etching, which is an adverse chemical process where

large areas of the substrate are etched away due to a reaction between Si and Ga during MOCVD growth [76] [77]. To improve quality of GaN growth a suitable thin nucleation layer must be deposited on top of the substrate. For GaN grown on Si aluminium nitride is the material of choice for nucleation layer, which is followed by strain relief layer (SRL) – sometimes referred to as deep buffer. SRL serves to manage the stress resulting from lattice mismatch between GaN and Si and is composed of combination of AlGaN and AlN. The three main types of SRL include: step graded, interlayer and superlattice SRL. Figure 2.11 highlights main differences between each of these three SRL designs.

Another function of the strain relief layer involves reduction in dislocation densities: introduction of layers with differing strain increases the chances of two dislocations with opposite orientation annihilating. The main types of dislocations are screw, edge and mixed dislocations (see Fig. 2.12), which differ in Burgers vector – a vector describing magnitude and direction of a crystal distortion. Due to relatively small lattice mismatch between GaN and SiC, the thick and complex strain relief layer is replaced by thin AlN nucleation layer followed directly by GaN buffer layers. Omission of SRL in GaN-on-SiC epitaxy enables full utilisation of high thermal conductivity of the substrate.

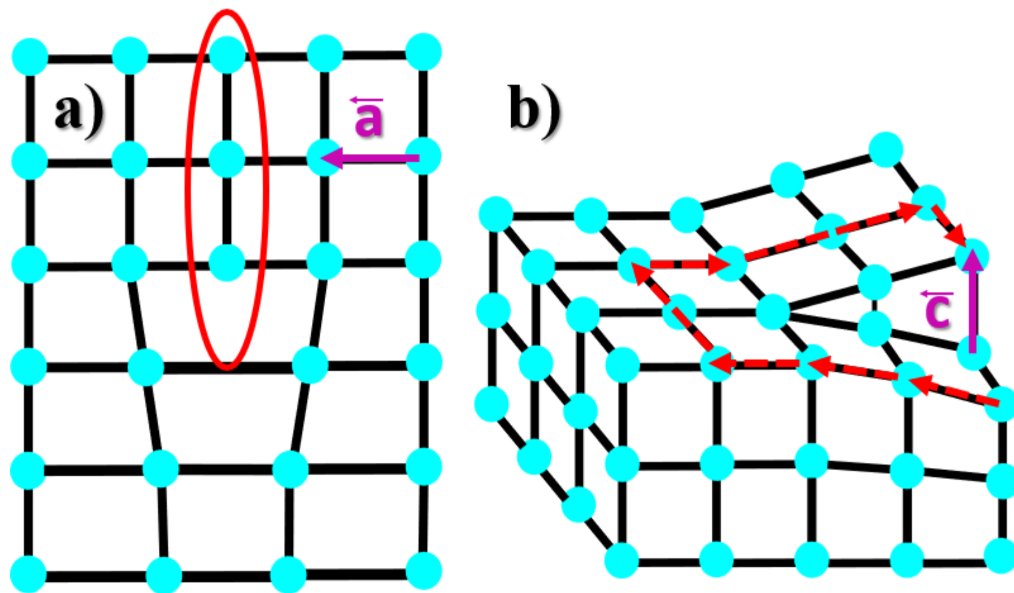

Figure 2.12: Schematic representation of a lattice with **a)** edge and **b)** screw dislocations. Purple arrows indicate the Burgers vectors with the dislocation regions highlighted in red.

2.2.3 Buffer Layer and Carbon Doping

GaN buffer is grown on top of appropriate strain relief layer and its primary functions involves vertical insulation, suppression of off-state leakage, increasing the breakdown voltage of the device and improving carrier confinement in the channel. Insulating buffer also helps prevent

short channel effects such as drain induced barrier lowering (DIBL) – a lowering in threshold voltage of the device with the applied drain bias resulting from the reduction in the size of the depletion region under the gate, and punch-through – current flow in the off state due to formation of a parallel conduction path under the gate through the buffer [78].

In the absence of intentional dopants, GaN grown by MOCVD shows slight n-type characteristics due to incorporation of donor impurities such as hydrogen, oxygen and silicon [79] [80] [81] [82]. To achieve good buffer insulation extrinsic dopants are incorporated into the buffer, pinning the Fermi level according to their position in the bad gap. The most common dopants used for buffer insulation are carbon and iron, however their positions in the bandgap are very different. Figure 2.13 gives an outline of the position of different dopants and impurities in the bandgap. Fe is incorporated substitutionally for N atom during growth resulting in formation of an acceptor state 0.5 – 0.7 eV below the conduction band leading to an n-type buffer [83][84]. Fe is a popular choice for GaN-on-SiC HEMTs for RF applications due to its relatively minor contribution to current dispersion under RF operation as compared to C [85].

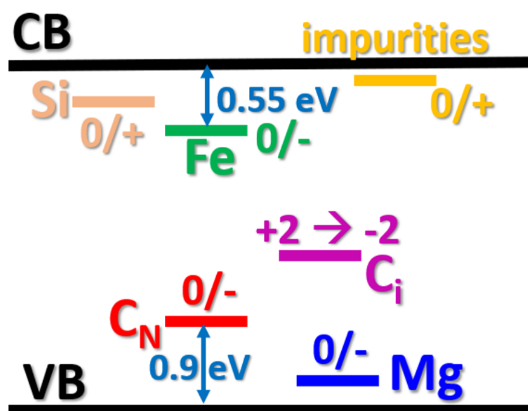

Figure 2.13: The position of some of the most common extrinsic dopants incorporated into GaN layers in relation to conduction and valence band (including their possible charge states).

In contrast, C can be incorporated either as an acceptor, if substituted for a N atom (C_N) sitting at ~0.9 eV above the valence band, or as a very shallow donor when it replaces a Ga atom (C_{Ga}) [86] [87]. In addition, C can be Incorporated as an interstitial (C_i) 1.35 eV above the valence band and can assume charge states from +2 to -2. However, the formation of C_i is only favourable under extreme Ga-rich conditions when Fermi level lies very close to the valence band, and therefore in most cases it does not form during GaN growth in large concentrations. Lyons *et al.* have performed hybrid functional calculations to investigate the relationship between donor and acceptor incorporation during GaN growth.

Figure 2.14 shows the dependence of formation energy for incorporation of C as a function of the Fermi level position, and the effects of GaN growth conditions on incorporation of C into the GaN buffer [86]. The magnitude of formation energy will determine the likelihood of formation of a given species, with lower formation energies being thermodynamically more favourable. Most

as-grown GaN films are initially n-type due to incorporation of impurities such as H, O and even Si [88]. Thus, regardless of Ga- or N-rich growth conditions, incorporation of C acceptor is energetically more favourable than formation of donors or interstitials, resulting in Fermi level pinning in the lower half of the bandgap.

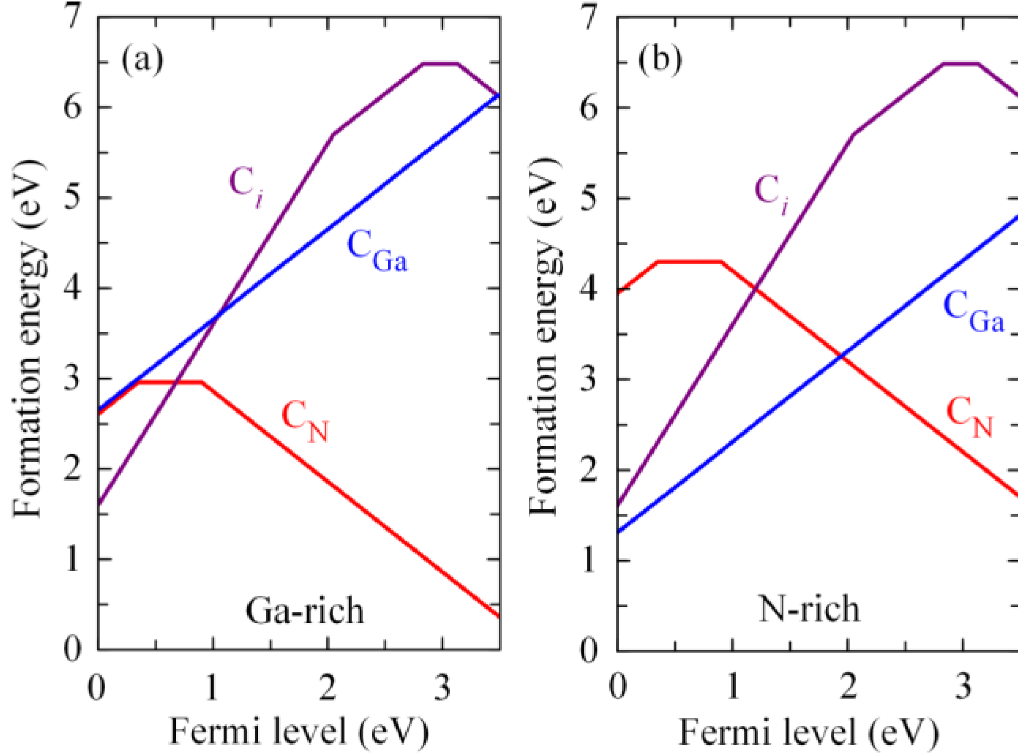

Figure 2.14: Formation energies of C donors (C_{Ga}), accpetors (C_N) and interstitials as a function of Fermi level in **a)** Ga-rich and **b)** N-rich growth conditions. Figure reprinted from [89] with the permission of APS.

For Ga-rich conditions corresponding to MOCVD growth, C is initially incorporated on the nitrogen site due to more favourable formation energy. Only after the buffer shows p-type character, C is incorporated on the Ga site leading to compensation of the acceptors (see Fig 2.14a). The N-rich conditions (shown in Fig. 2.14b) are more common for MBE growth initial C acceptor incorporation is results in Fermi level E_F dropping to 1.9 eV, which is the point where formation energies of C_{Ga} and C_N are equal. At this point carbon self-compensation is taking place. Both Ga-rich and N-rich growth lead to formation of resistive buffer, however the position of Fermi level is different: in the first case, the E_F lies below the C_N level resulting only in a partial ionization of the acceptors; for the latter case the E_F lies around 1.9 eV resulting in full ionization of C_N and equivalent concentration of ionized C_{Ga}.

Compensation ratio is defined as a ratio of concentrations of C incorporated as donors (N_D) to acceptors (N_A) and is an important parameter defining resistivity of the buffer and thus, its electrical characteristics. Assuming C doping concentration of 2×10^{18} cm^{-3} incorporated purely

on the nitrogen site in a GaN buffer, free hole concentration of ~ 10^{11} cm^{-3} should be expected, with corresponding resistivity of this layer on the order of 10^{6} Ω·cm. However, experimental measurements of C-doped buffers with comparable doping concentrations indicate resistivities on the order of 10^{13} Ω ·cm, suggesting much lower concentrations of free holes [90][91][92]. This discrepancy can be explained by incorporation of C_{Ga}, with the compensation ratio of ionized C donors to acceptors playing a cruicial role in defining electrical properties of the buffer.

By considering the concentrations of each species in the buffer, the concentration of free holes can be defined as:

$$p = \frac{N_V' + N_D}{2} + \frac{\sqrt{\left(N_V' + N_D\right)^2 + 4N_V'\left(N_A - N_D\right)}}{2} \tag{2.20}$$

where N_V' denotes adjusted effective density of states in the valence band due to only partial ionization of the acceptors [93]. N_V' is approximately related to density of states in the valence band N_V by the Boltzmann factor $exp\left(\frac{-E_A}{k_B T}\right)$. By considering Taylor expansion of the Eq. 2.20, free hole density can be defined derived as:

$$p \simeq N_V' \left(\frac{N_A}{N_D} - 1\right) \tag{2.21}$$

using first order approximation, since $N_V' << N_A$ and N_D. Moreover, the resistivity of the buffer depends on the free hole density according to:

$$\rho = \left(q p \mu_p\right)^{-1} \tag{2.22}$$

where q is the electron charge and μ_p is the hole mobility.

Figure 2.15 shows free hole concentration in the GaN buffer and its corresponding resistivity as a function of compensation ratio N_D/N_A assuming hole mobility μ_p = 10 cm^2 V^{-1} s^{-1}. From the Figure, it is clear that compensation ratio is a critical parameter defining electrical performance of the C-doped buffer. As the compensation ratio increases the concentration of free holes in the buffer falls, resulting in much more resistive buffer and better voltage blocking performance.

2.2.4 AlGaN Barrier and Capping

As outlined in previous section, band offset between AlGaN and GaN results in a formation of strong positive charge at the heterointerface, which is populated by the electrons from the surface donor-like states to form the 2DEG. The carrier density of the 2DEG will strongly depend on the total polarization present in the heterostructure. However, since the polarization depends on the stress present in AlGaN and GaN layers, barrier thickness will play an important role in 2DEG formation. In general, the 2DEG density can be described as:

$$n_s = \frac{\sigma}{q} - \frac{\epsilon_0 \epsilon_{AlGaN}}{t_{AlGaN} q^2} \left(\phi_b + E_F - \Delta E_C\right) \tag{2.23}$$

where σ, ϵ_{AlGaN}, t_{AlGaN}, ϕ_b, E_F and ΔE_C denote polarization charge, dielectric constant of AlGaN, AlGaN barrier thickness, surface potential, Fermi level and conduction band offset between

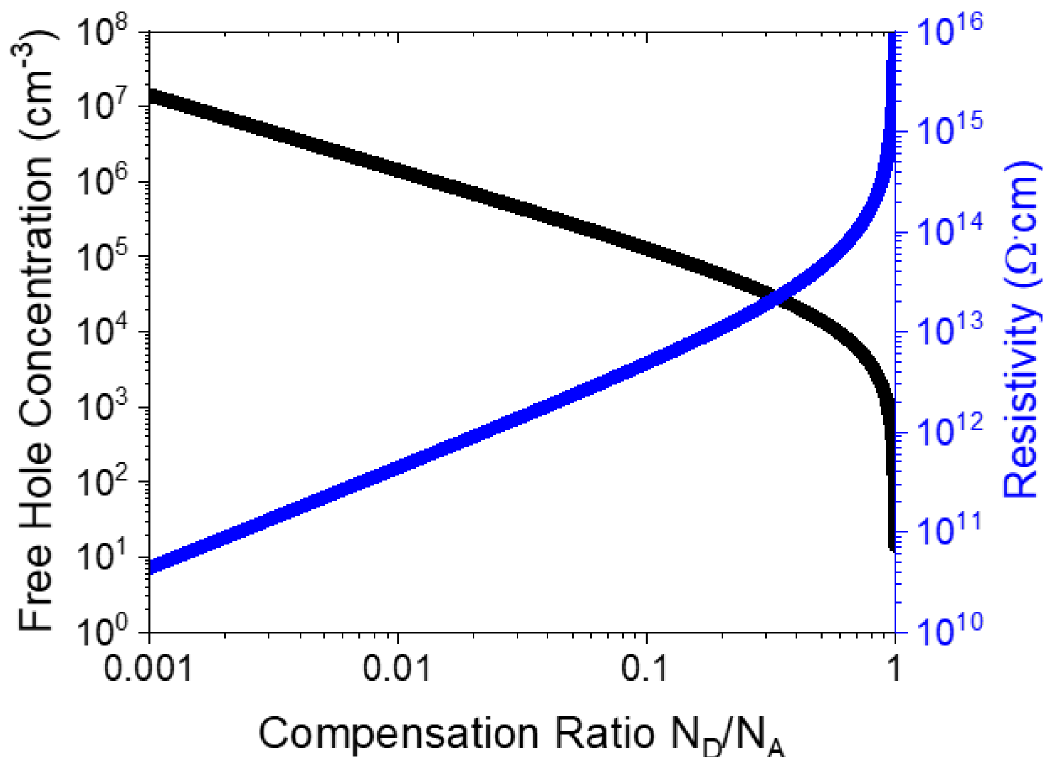

Figure 2.15: Free hole concentration in the C-doped GaN buffer and its resistivity as a function of compensation ratio of C donor to acceptors (N_D/N_A).

AlGaN and GaN [43] [95]. Figure 2.16a shows computational simulations and experimental measurements of the effects of AlGaN barrier thickness on the 2DEG density. The simulations indicate that there is a minimum barrier thickness below which there is no 2DEG present in the structure, after which there is a sudden increase in the carrier concentrations followed by a plateau. Further increase in barrier thickness results in relaxation in the barrier, thus leading to decrease in piezoelectric polarization and hence a reduction in 2DEG concentration [96].

Often, a GaN cap layer is deposited on top of AlGaN barrier to protect the surface donors, prevent surface oxidation and increase the smoothness, resulting in reduced current dispersion [94] [97]. Usually, cap thickness is on the order of 1-2nm. Figure 2.16b shows the dependence of GaN cap thickness on the 2DEG concentration and Hall mobility. The decrease in 2DEG concentration can be explained by additional negative polarization charge at the GaN cap/AlGaN interface and thus increased electric field across the barrier.

Despite the introduction of additional polarization charge GaN capping has been linked to reduction in leakage currents, increased critical voltage of the devices and even reduction in contact resistance as compared to uncapped transistors [98] [99]. Moreover, incorporation of thicker GaN cap layers in E-mode devices has been demonstrated to increase the reliability and robustness of HEMTs and diodes alike [100] [101].

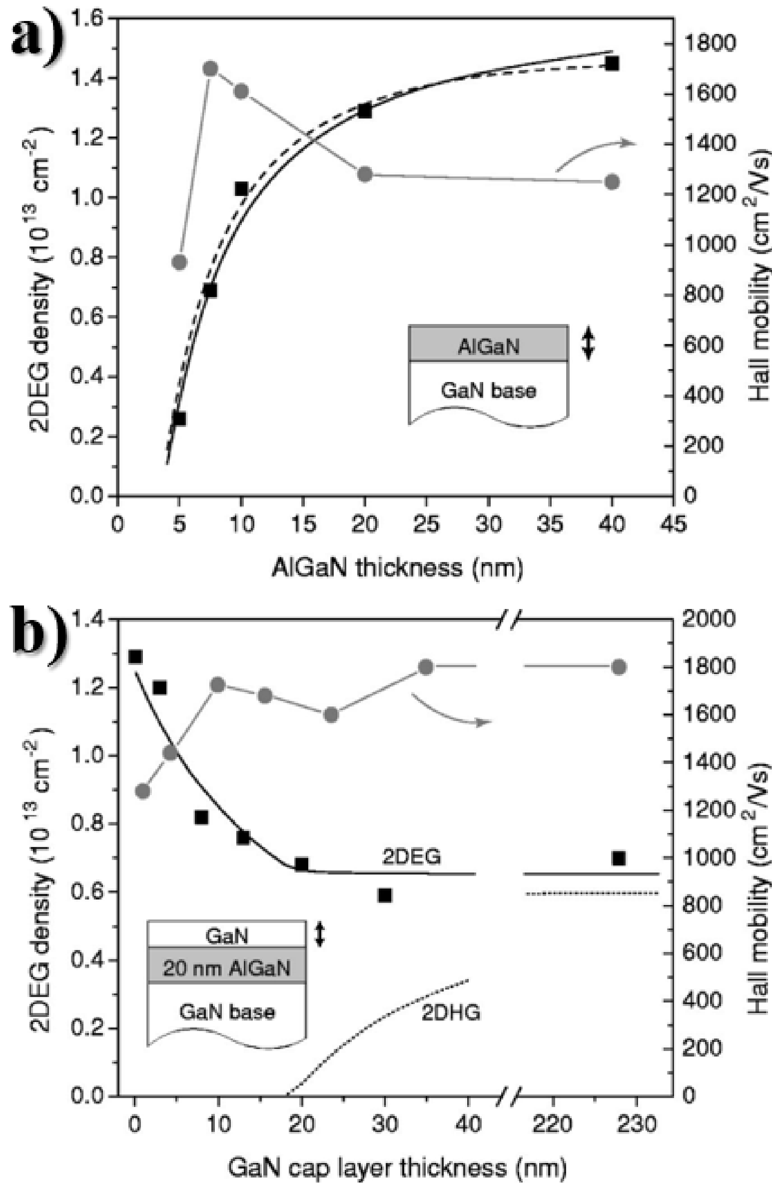

Figure 2.16: **a)** 2DEG density and Hall mobility of electrons as a function of $Al_{0.32}Ga_{0.68}N$ barrier thickness (lines show simulated data, points represent measurement). **b)** 2DEG density and mobility as a function of GaN cap thickness (lines show simulated data, points represent measurement). Figure reprinted from [94] with the permission of AIP.

2.2.5 Ohmic and Schottky Contacts

In order to create a fully functional GaN-based device with high level of control over the electron channel, appropriate contacts to the 2DEG must be created. The properties of metal – semiconductor junction can be adjusted based on electron affinity of the semiconductor (χ_e), which is defined as the separation between the conduction band minimum and the vacuum level, and the work function (Φ) of the metal, which describes the position of vacuum level in relation of Fermi

level. Figure 2.17 shows how relative magnitudes of χ_e and Φ can result in two different types of contacts and their corresponding IV characteristics.

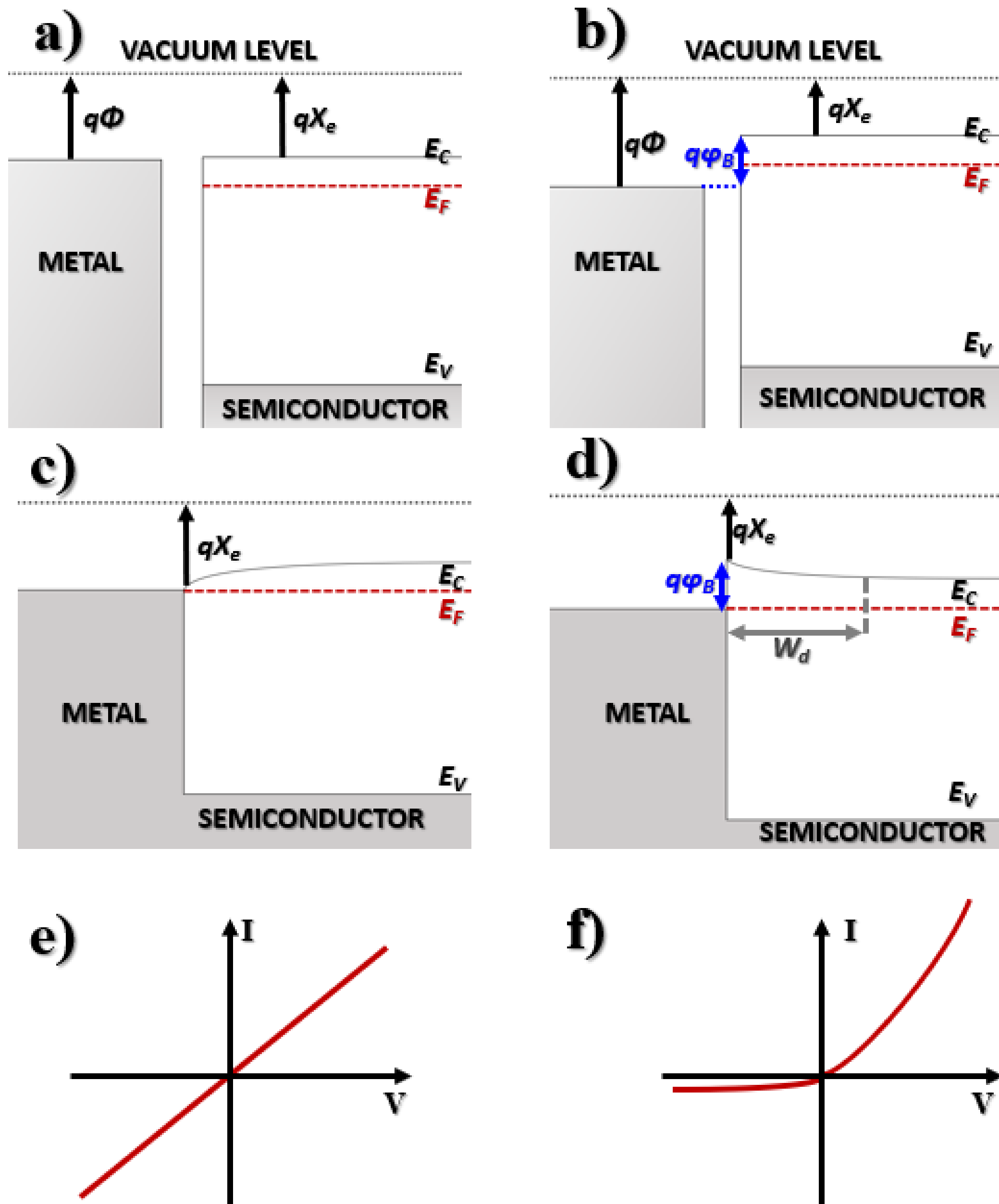

Figure 2.17: Band diagrams of metal-semiconductor junctions. Ohmic and Schottky contacts before contacting are shown in **a)** and **b)**. Ohmic and Schottky contacts after contacting are shown in **c)** and **d)**. IV characteristics of Ohmic and Schottky contacts are shown in **e)** and **f)**.

Ohmic contact is formed when work function of the metal is lower than electron affinity of the semiconductor (see Fig. 2.17a), resulting in lack of potential barrier between the two materials after the contact is formed (Fig. 2.17c). The IV characteristics of Ohmic contact follow a

simple linear relationship $I = \frac{V}{R}$, where R denotes the contact resistance (Fig. 2.17e). Low contact resistance of the Ohmic contact is of paramount importance as it affects numerous parameters vital for device operation. Low contact resistance leads to lower drain-gate access resistance, higher transconductance and higher current densities, while in case of RF devices it allows for higher cut off (f_T) and max frequency (f_{Max}).

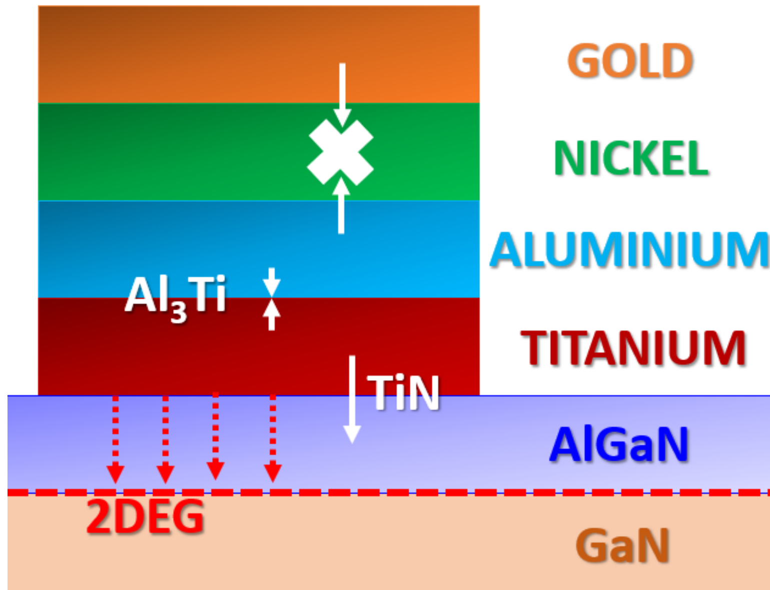

Figure 2.18: Typical Ohmic contact stack consisting of gold, nickel, aluminium and titanium. Each metal layer will be involved in a formation of different alloys, lowering the contact resistance and enabling better contact to the 2DEG.

Due to large bandgap of GaN it is difficult to find a metal with a suitably low work function to create Ohmic contacts with low enough barrier. Therefore, modern HEMTs rely on stack made up of four metals Ti/Al/Ni/Au (see Fig. 2.18) [102]. Optimization of metal thickness in the stack is important for reduction of contact resistance and to achieve smooth interfaces between individual components of the Ohmic contact. However, it is the Ti/Al thickness ratio that is of critical importance to achieve the low resistance, with the ratio of 1/6 having been reported to show the best performance for annealing at 900°C in nitrogen rich conditions [103]. When contacted to the heterostructure, Ti reacts with N in AlGaN to form an alloy with lower work function then the metal and allowing for contact formation as highlighted by red dashed arrows in Fig. 2.18. Ti can also attract N from GaN leaving behind high concentration of N vacancies, which create junctions between 2DEG and the contact stack [104]. The reaction between Ti and Al will result in the formation of $TiAl_3$ compound, which prevents further reactions between GaN and Ti. Excess Ti concentration will result in formation an insulating $Ti_{1-x}Ga_xN$ compound with metal-insulator transition occurring at $x = 0.5$ [105].

Gold is deposited at the top of the contact to improve its conductivity and protect the stack from oxidation during annealing, with Ni deposited between Au and Al to prevent interdiffusion

of these metals. However, Au based Ohmic contacts have been demonstrated to fail when exposed to temperatures of 340°C for at least 100 hours, indicating alternatives need to be sought out for high power applications [106]. One of the alternative metal stacks is Ti/Al/W, which has been demonstrated to have contact resistance below 0.5 Ω·mm with surface morphology smoother than conventional Ti/Al/Ni/Au and annealing temperatures as low as 500°C [107] [108]. In general, in recent years a wide variety of Au-free contacts with low resistance have been developed, most of which involve use of Ta, TiN and W in combination with conventional Ti and Al [109].

In contrast to Ohmic contacts, Schottky contacts are formed when the work function of the metal is greater than electron affinity of the semiconductor (Fig. 2.17b). This results in formation of an activation barrier $q\phi_b$ = $q\Phi$ - $q\chi_e$ (Fig. 2.17d), which only allows for unidirectional flow of current as shown in Fig. 2.17f. Ideal Schottky contact is characterised by low resistance and large breakdown field whilst having low reverse leakage current. In case of Schottky contact to a moderately doped semiconductor, the forward current density (J) can be described by:

$$J = A^{**}T^2 exp\left(-\frac{q\phi_b}{k_B T}\right) exp\left(\frac{q(\Delta\phi + V)}{k_B T}\right) \tag{2.24}$$

where A^{**} and $\Delta\phi$ stand for Richardson constant and image force barrier lowering respectively, with V denoting the applied potential. Since these two parameters show very weak voltage dependence, Eq. 2.24 can be further simplified to give:

$$J = J_0 exp\left(\frac{qV}{\nu k_B T}\right) \tag{2.25}$$

where ν denotes the ideality factor (ν = 1 for ideal case) [93]. Ni and gold are the most common metals used for formation of Schottky contacts to AlGaN/GaN heterostructures [110].

2.2.6 Passivation

Effective passivation is a crucial element of an efficient GaN HEMT, as this layer encapsulates surface donor-like states to prevent 2DEG depletion, reduces the off-state leakage and prevents contamination of device surface [111][112][113]][114]. The presence of surface states arising from dangling bonds, plasma damage during growth and other defects can lead to current collapse and formation of virtual gate [115], therefore it of great importance for efficient device operation to secure the surface and prevent (or at least mitigate) the effects of charge trapping in this region. The most common choice for passivation materials include SiN_x and SiO_2, however a number of other materials have also been demonstrated to provide effective surface passivation, most notably AlN , which has demonstrated an improved DC performance and reduction in current dispersion in comparison to conventional passivations [116] [117] [118].

The properties of the passivation layer will vary depending on the technique used for its deposition, with the layers deposited by low pressure chemical vapour deposition (LPCVD) showing better film quality, improved protection from trapping and less plasma damage as compared to plasma enhanced vapour deposition (PECVD) and in situ growth [119][[120]. In

addition to the above techniques, atomic layer deposition (ALD) can be utilised for passivation growth, however this technique is much more time consuming than the other techniques.

PECVD growth results in incorporation of large quantities of hydrogen, which compromises the physical properties of passivation and allows for diffusion of hydroxyl (OH^-) particles from ambient moisture. Deposition of these species leads to structural degradation of the device during Off-state stress as demonstrated in [121]. The in situ MOCVD growth has the advantage of passivation deposition directly in the MOCVD reactor, preventing any contamination during processing. Although this method shows improved performance in comparison to PECVD grown layers, LPCVD films demonstrate still improved current dispersion and higher film quality, while incorporating only a fraction of hydrogen atoms in comparison to other techniques [122]. However, a further improvement in film quality, density and step coverage can be achieved with passivation growth by ALD, which allows for deposition of thinner, high-performance layers with less surface damage to the underlying layers [116]. Often, this process is coupled with application of low energy plasma to pre-treat the surface, creating a clean and well defined interface for passivation deposition [123].

2.3 GaN HEMTs and Diodes Operation

In this section the theoretical concepts relating to operations of some of the most common GaN-based devices for power and RF electronic are explored and related to practical applications.

2.3.1 DC Performance

Figure 2.19 shows a schematic diagram of a HEMT device with the most important dimensions indicated together with typical output characteristics. Under normal operating conditions the AlGaN barrier is depleted with the electrons being confined to the heterointerface. Based on the assumption that voltage applied across the channel varies gradually from 0 V at the source to V_D at the drain (gradual channel approximation), the 2DEG charge density can be expressed as n_s:

$$n_s(x) = \frac{\epsilon(V_G - V(x) - V_{TH})}{t + \Delta t} \tag{2.26}$$

where V_G and V_{TH} are gate and threshold voltage, $V(x)$ represents potential in the channel and $t + \Delta t$ indicates the effective barrier thickness comprising of the barrier thickness t and the distance of the carrier away from the heterointerface (Δt).

The IdVd curves shown in Fig. 2.19c display two distinct regions: linear region (green), where the electric field across the channel E is less than the critical field E_C and saturation regions (blue), where $E > E_C$. In the linear region, electron velocity v_e can be described in terms of mobility μ, such that $v_e = \mu E = \mu \frac{dV(x)}{dx}$, while in the saturation region carrier velocity is equal to saturation velocity v_s.

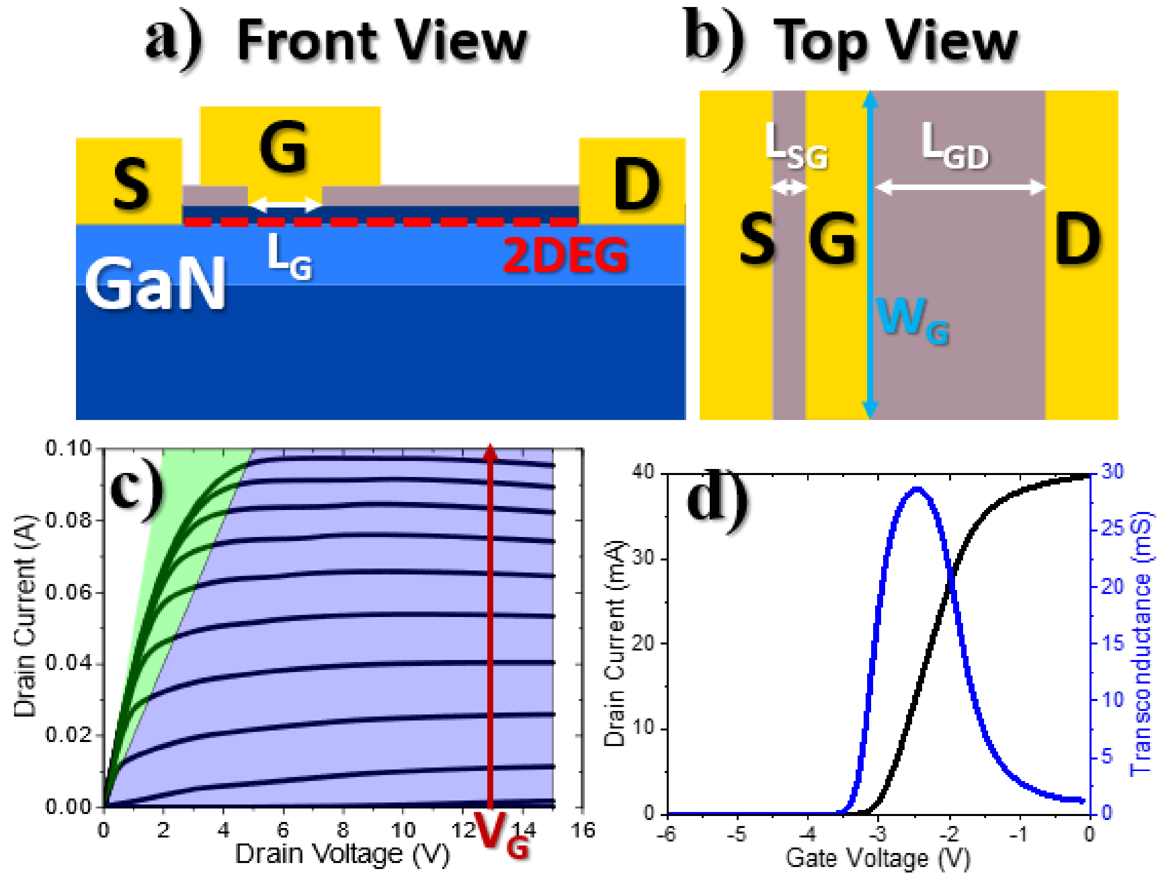

Figure 2.19: **a)** Front and **b)** top view of a typical GaN HEMT with some crucial device dimensions indicated on the diagram, such as SG-spacing L_{SG}, GD-spacing L_{GD}, gate length L_G and gate width W_G. **c)** Typical DC IdVd characteristics of a D-mode GaN HEMT with linear region highlighted in green and saturation region in blue. **d)** Typical DC IdVg characteristics (and corresponding transconductance) of a D-mode GaN HEMT.

The IV characteristics of a HEMT device can be described using standard semiconductor physics equations and expressed in a two-piece model, which relates to current flow in the linear and saturation regions separately. In general, the current flowing through the channel I_D can be describe in terms of carrier concentration n_s, carrier velocity v_e and gate width W_G according to the expression:

$$I_D = n_s(x)v_e W_G = W_G \mu \frac{dV(x)}{dx} \frac{\epsilon(V_G - V(x) - V_{TH})}{t + \Delta t}. \tag{2.27}$$

In the linear region, the drain current can be derived from the integral of the Eq. 2.27 over the channel length L. Thus, drain current of the transistor in this region can be expressed as:

$$I_D = \frac{\epsilon \mu W_G}{(t + \Delta t)L} \left((V_G - V_{TH})V_D - \frac{V_D^2}{2} \right) \tag{2.28}$$

In case of non-negligible series resistance in the transistor (long channel devices), the current can also be derived from Eq. 2.27 by including the boundary conditions such that at the source

edge $V(x=0) = I_D R_s$ and at the drain edge (for the device with channel length L) $V(x=L) = V_D – I_D(R_s + R_d)$, where R_s and R_d denote source and drain resistance.

As the electric field is increased across the device, the critical field will be reached at the drain end of the channel ($x = L$) first. The saturation current can be described as:

$$I_S = \frac{\beta V_{SI}^2}{(1-\beta R_s V_G')^2}\left[\sqrt{\left[1+2\beta R_s V_G' + \left(\frac{V_G'}{V_{SI}}\right)^2\right]} - 1 + 2\beta R_s V_G'\right] \tag{2.29}$$

where $V_G' = V_G – V_{TH}$, $V_{SI} = E_C L$ and $\beta = \frac{\mu\epsilon W_G}{(t+\Delta_t)L}$. For short channel devices V_{SI} can be much smaller than V_G', therefore equation 2.29 can be simplified to give:

$$I_D = \frac{\epsilon v_s W_G V_G'}{t+\Delta t}. \tag{2.30}$$

The control of the channel is achieved by the gate, with the gain defined by its transconductance g_m. In the saturation region, the transconductance can be expressed as:

$$g_m = \frac{dI_D}{dV_G} = \frac{\epsilon v_s W_G}{t+\Delta t}. \tag{2.31}$$

For long channel devices the transconductance can be derived from Eq. 2.29, giving:

$$g_m = \frac{\beta V_G'}{\sqrt{1+\left(\frac{V_G'}{V_{SI}}\right)}}. \tag{2.32}$$

2.3.2 GaN HEMT as Power Switch

GaN possesses a wide range of advantages over competing technologies for power switching including high breakdown field, high electron mobility and electron density. These properties allow for commercial fabrication of HEMTs with low On-resistance and capable of withstanding voltages up to 650 V.

The operation of GaN HEMT in power switching involves rapid transitions from high voltage Off-state characterised by high electric field and low current, to On-state defined by low electric field and high current. Figure 2.20 shows a schematic diagram for switching operation of a GaN HEMT as well as two possible ways for transitioning between On and Off state: hard and soft switching.

Hard switching involves increase in gate voltage followed by reduction in drain voltage, resulting in high current flow during switching and thus high power dissipation. The presence of large electric fields and high currents can lead to compromised device performance in the On state resulting from self-heating and increase in dynamic On-resistance [124]. In contrast, during soft switching the reduction in drain voltage precedes the increase in gate voltage, thus mitigating stress experienced by the device. In this mode of operation most of the stress is experienced in the Off state resulting in improved On-resistance as compared to hard switching [125].

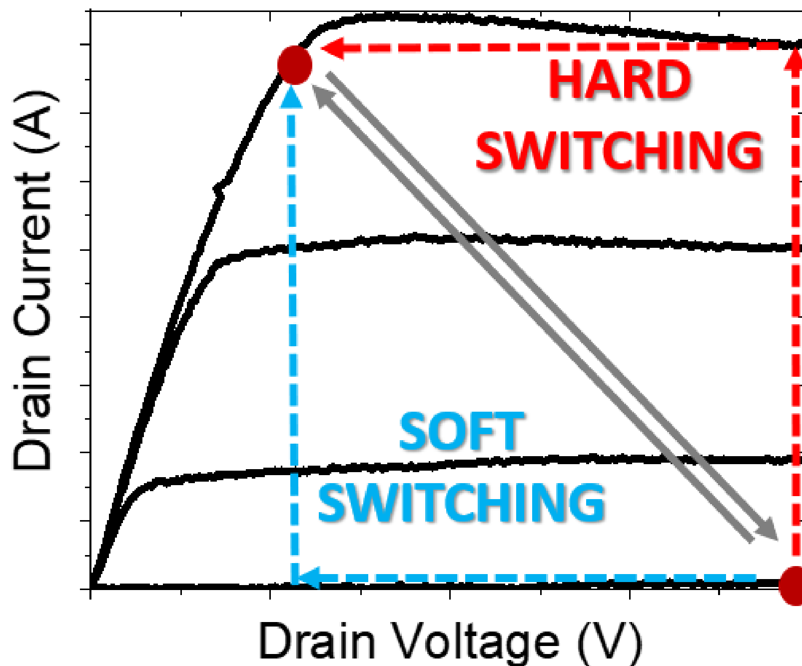

Figure 2.20: IdVd characteristics of a power HEMT showing schematic comparison between hard and soft switching from Off state to On state.

To compare a suitability of a material for power switching applications, Baliga proposed a figure of merit (FOM), which applies to power devices operating at low frequencies and relates to resistive losses of the device [126]. Lateral power GaN HEMTs undergoes breakdown when electric field distribute across the drift region is equal to critical breakdown field E_C. Thus, the theoretical maximum length of drift region before breakdown is defined as:

$$L_D = \frac{V_{BR}}{E_C} \tag{2.33}$$

where V_{BR} denotes breakdown voltage. The On-resistance of the drift region in a HEMT structure can be expressed as:

$$R_{ON} = \frac{L_D}{e\mu n_s W_G} \tag{2.34}$$

where μ denotes carrier mobility. The specific On-resistance of a lateral GaN HEMT is defined as the product of R_{ON} and device area $L_D \times W_G$. Thus, for a power switching HEMT, the specific On-resistance can be expressed according to the formula:

$$R_{ON}A = \frac{V_{BR}^2}{en_s\mu E_C^2} \tag{2.35}$$

where $R_{ON}{\cdot}A$ denotes area specific resistance [127][17]. By considering the impact ionization integral for lateral HEMT devices, the critical electric field can be expressed as $E_C \propto V_{BR}^{-1/6}$. Therefore, by combining the dependence of critical field E_C on the breakdown voltage with eq.

2.33 (assuming constant mobility in the considered field regime), we find out that the area-specific on resistance of GaN HEMT $R_{ON}A \propto V_{BR}^{7/3}$.

Figure 2.21 shows the relationship between area specific On-resistance and breakdown voltage for GaN HEMTs, highlighting the advantages of this technology over competing materials and technologies. The low On-resistance due to the presence of the 2DEG combined with large breakdown voltages make GaN based power devices an attractive choice for efficient power switching applications. The denominator of equation 2.35 defines the Baliga figure of merit (BFOM) specific for GaN HEMT. In more general cases, BFOM is defined according to:

$$BFOM = \epsilon \mu E_G^3 \tag{2.36}$$

where ϵ and E_G denote permittivity and bandgap of the investigated material [17].

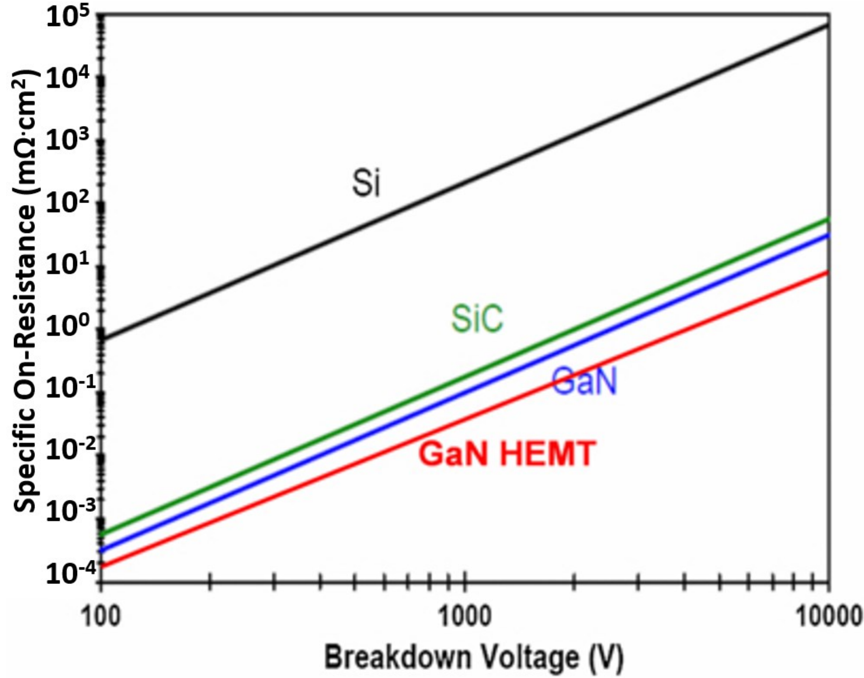

Figure 2.21: Comparison of specific On-resistance of GaN to Si and SiC, according to the equation 2.35. Figure adapted from [127] with the permission of the IOP Publishing.

The dependence of specific R_{ON} on breakdown voltage V_{BR} is not identical for vertical and lateral devices, as evident in the difference in gradient for GaN HEMT and the lines corresponding to Si, SiC and vertical GaN devices lines in Fig. 2.11. In case of Si and SiC, the critical electric field E_C shown in the denominator of eq. 2.35 can be derived by fitting Fulops power law to impact ionization data [128] [129]. Assuming constant mobility in the drift region due to sufficiently low doping concentration, the ideal specific On-resistance $R_{ON}A \propto V_{BR}^{2.5}$. A similar approach can be used for GaN as described by Ozbek-Baliga law [130], resulting in specific R_{ON} for vertical GaN devices $R_{ON}A \propto V_{BR}^{2.5}$ [127].

2.3.3 GaN HEMT as RF Switch

GaN RF switch operates along the load line as shown in Figure 2.22 stretching between points V_K and $V_{BREAKDOWN}$ to offer the largest possible voltage swing (V_{SWING}) usually in the range between 10 to 30 V whilst maximizing the current delivered. Point I_{MAX} is determined based on the maximum current flow through the transistor when it is fully On and is located at or near the knee voltage (V_K), which in turn is defined as the point dividing the linear and saturation region. Point $V_{BREAKDOWN}$ (or cut-off voltage) lies in the Off-state and is determined by the supply voltage for the circuit.

The choice of operating point (or Q – point) depends on the class of the RF amplifier. For class A, the operating point lies half way between points V_K and $V_{BREAKDOWN}$ to give a linear response, while the operating point for class B will lie closer to the cut-off voltage $V_{BREAKDOWN}$ and the amplifier circuit will rely on two transistors in the push-pull configuration.

In contrast to power devices, high breakdown voltage is less important for GaN RF switching transistors, but instead reduction of V_K and thus maximization of the possible voltage swing are primary consideration for RF HEMTs. The resistance in source and drain access regions can be reduced by increasing the carrier concentration n_s in the channel and electron mobility of the carriers. GaN HEMT technology offers both high carrier density and mobility of the 2DEG, which in combination with carrier saturation velocity of 2.5×10^7 cm/s offer high frequency operation and increased power outputs as compared to other competing technologies [15]. Johnson figure of merit (JFOM) is used to characterise the high frequency performance of the device. By considering the cut-off frequency of the device and the velocity of carriers under applied electric field, JFOM can be described according to the equation:

$$JFOM = \frac{v_s E_C}{2\pi} \tag{2.37}$$

where v_s and E_C denote saturation velocity and critical electric field [16].

2.3.4 Schottky Barrier Diode Operation

Due to large breakdown field and high carrier mobility GaN - based Schottky barrier diodes (SBDs) are perfect candidates for high-voltage, fast-switching applications such as power converters and inverters [131] [132]. Figure 2.23 shows typical IV characteristics of a Schottky barrier diode, which can be expressed according to the equation 2.25. Depending on the exact application and voltage rating of the diode, two most common device architectures involve vertical and lateral diodes, with the vertical devices being preferred for high-voltage, lower frequency applications [110] [133]. In this work, we will focus on lateral SBDs.

The epitaxial structure of a GaN-on-Si Schottky barrier diode is very similar to a HEMT structure as shown in the inset to Fig. 2.23, with some minor differences: the current flows predominantly to the Schottky and not the Ohmic contacts. Device operation involves rapid switching between Off-state and linear region in the On-state, therefore to minimise switching losses during

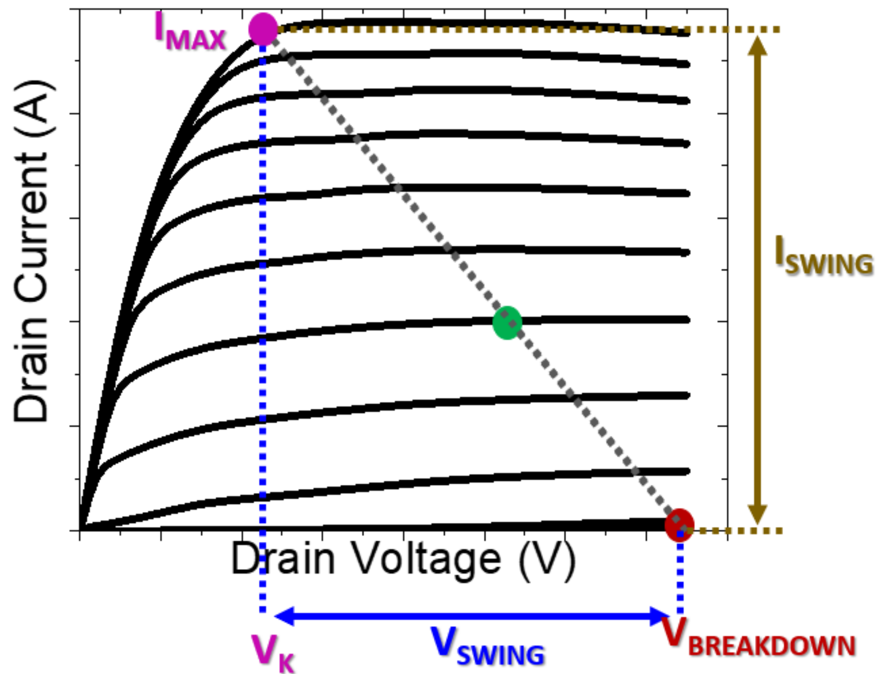

Figure 2.22: IdVd characteristics of an RF GaN HEMT with RF load line and important operating points indicated on the plot.

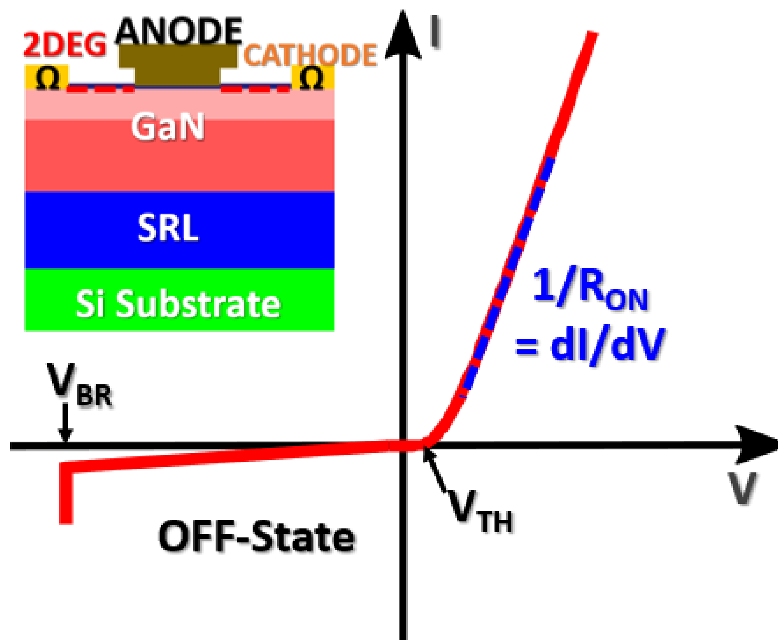

Figure 2.23: Schematic representation Schottky barrier diode IV characteristics showing threshold voltage V_{TH}, breakdown voltage V_{BR} and On-resistance R_{ON} (inverse of the gradient in the linear region). Inset: diagram of a GaN-on-Si lateral Schottky barrier diode.

operations parameters such as Off-state current, threshold voltage and On-resistance have to be

optimised.

To achieve low Off-state leakage in lateral SBDs, most optimisation schemes rely on carefully designed field plates, which serve to reduce and create more uniform electric field distribution along the cathode-anode access region, as well as passivation design in order to prevent parasitic current flows [134] [135] [136]. The most common method to achieve low V_{TH} involves recessed anode, where AlGaN barrier is locally partially or completely etched away before the Schottky contact deposition [137] [138], however recess-free structures have also been proposed recently [139]. Coincidentally, in addition to redution of threshold voltage, it has been reported that anode recessing can also reduce the On-resistance of the diode [132] [140]. Typical GaN-on-Si SBD can be biased in two possible configurations: the bias can be applied to anode while cathodes are grounded and vice versa.

2.4 GaN Device Reliability

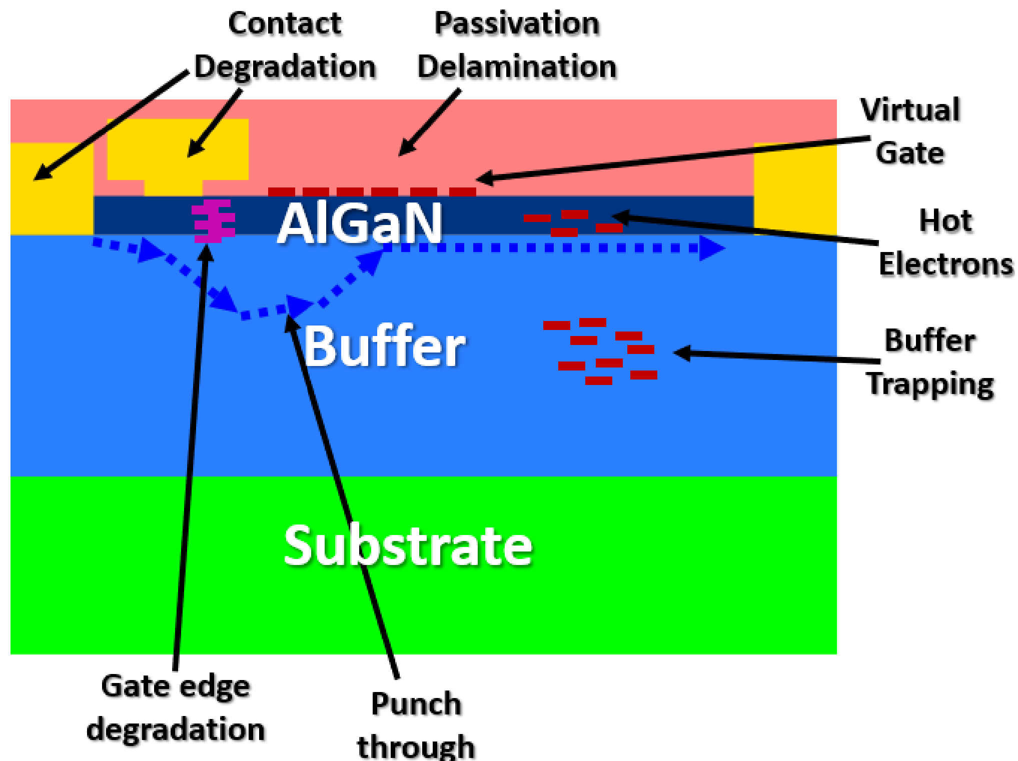

Figure 2.24: Schematic representation of main degradation mechanisms that can have a significant impact on GaN HEMT reliability.

Despite years of optimisation of growth and fabrication processes GaN HEMTs still face reliability issues due to large electric fields and high currents present during the device operation. From electrical perspective charge trapping in the buffer and at the surface can lead to deteriora-

tion of output characteristics, while inadequate thermal management can result in premature device failure. In this section some of the key reliability issues are discussed.

2.4.1 Trapping in GaN

GaN growth process often results in incorporation of significant quantities of impurities such as C, H and O with concentrations as high as 10^{16} cm^{-3} [141]. In addition, growth of GaN on lattice-mismatched substrate combined with differences in thermal expansion coefficients can lead to formation of extended defects and vacancies. All of the above can act as trap states located in the bandgap which are not in electrical equilibrium with the carriers present in the valence and conduction bands (an overview of common trap states in GaN is given in section 2.2.3). Shallow trap states are located very close to the band edges with the activation energies of the order of 10s of mV and can be activated easily under standard temperature conditions. Deep traps, however, lie much further from the band edges and their response times exceed the timescales of signals applied to transistors in switching applications. Thus, electrons captured by the deep traps will remain captured for extended periods of time and will therefore affect the operation of the device.

The trap dynamics can be described in terms of capture and emission both of which will have a corresponding time constant. For electron capture in the absence of external electric fields, the time constant of the process (τ_{cap}) can be described by:

$$\tau_{cap}^{-1} = \sigma_n v_{th} n \tag{2.38}$$

where σ_n denotes the capture cross section, $v_t h$ is the thermal velocity of the carriers and n is the free electron concentration. In most calculations these parameters are treated as constant, however in some cases application of electric field can result in alteration of capture cross-section of a trap state [142]. In case of GaN and other wide bandgap semiconductors, the number of free carriers is low resulting in longer capture time constants. The emission of the captured electrons (τ_{em}) can be described by the equation:

$$\tau_{em}^{-1} = \sigma_n v_{th} N_c exp\left(-\frac{\Delta E}{k_B T}\right) \tag{2.39}$$

where N_C denotes density of states in the conduction band and $\Delta E = E_C - E_T$ is the difference between the trap energy level (E_T) and conduction band (E_C).

In the presence of high electric fields during device operation in particular at the drain-side gate edge and under the drain, the travelling carriers can be accelerated and injected into the barrier or trapped at the device surface causing local depletion of the 2DEG. Alternatively, it is also possible, that some of the buffer traps become populated as described by the capture dynamics above with a similar effect to surface trapping. Figure 2.25 shows the effects trapping can have on IV characteristics of the device. Trapped electrons can affect the 2DEG either directly by electrostatically repelling the carriers or indirectly by changing the charge distribution at relevant interfaces. Presence of trapped charges can result in increased On-resistance (temporary

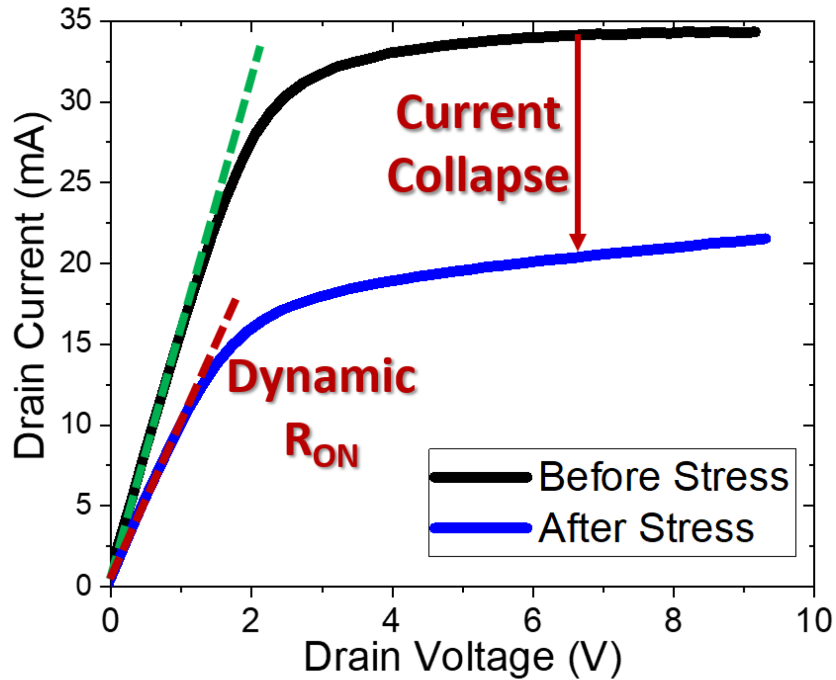

Figure 2.25: Example of IdVd measurement at V_G = 0 V before and after 100 s of Off-state stress. Device after stress shows significant increase in On-resistance and severe current collapse due to trapping.

reduction in the gradient of the linear region, also know as dynamic R_{ON}), “knee walkout” – shift in the position on the V_K towards a higher voltage or current collapse – reversible decrease in saturation current. The recovery time depends on the sources of trapping but can be as long as 1000s of seconds [143][144]. Thus, trapping will have a significant impact on device power output and is still an important issue for GaN HEMTs.

Identification of the main sources of trapping in a device is of utmost importance for the development of reliable GaN-based device for RF and power electronics. Although charge trapping has been observed in Si[145], the phenomenon of current collapse was first recognised in AlGaAs/GaAs HEMTs [146] [147]. Over the years, the issue of current collapse has been reduced to managable level by carful adjustment of surface passivation, field plate design, adjustment of epitaxial structure and doping profiles in the device [148]. However, the issue of current collapse is particularly relevant to GaN-based devices as the heteroepitaxial growth on mismatched substrates results in significant quantities of deep trap states forming in the band gap, capable of trapping charges for significant time periods [87]. The most common way for trap identification involves extraction of trap activation energy and capture cross-section from an Arrhenius plot. This technique involves plotting change in trap time constant as a function of temperature and is described in more detail in section 3.2.3. Bisi *et al.* performed a comprehensive literature review to compile a "library" of trap states which is shown in [143]. However, often extraction of apparent activation energy and capture cross-section is inconclusive for identification of sources of

dispersion and in some cases other processes and phenomena can easily be mistaken for trapping [149].

2.4.2 Dislocations in GaN Buffer

Although growth of GaN-based devices on foreign substrates is the preferred method mainly due to high price of native GaN substrates and their limited size, GaN buffers grown in this way result in dislocation densities on the order of 10^8 cm^{-2} - 10^{10} cm^{-2} as shown in Table 2.1. Point defects and extended defects such as threading dislocations have been reported to enable charge trapping, reduce 2DEG mobility and contribute to leakage currents, all of which pose major issues for reliability of GaN-based devices [150] [151] [152]. The concentration of electrically active defects is estimated for $\sim 3 \times 10^7$ cm^{-2} [152], with dislocations densities being experimentally correlated to device breakdown behaviour [153] [154].

The studies of GaN-based diodes have demonstrated screw and mixed dislocations acting as leakage paths directly affecting reverse leakage current of the investigated devices, with some notable examples given in [155] [154] [156] [157]. In addition, Knetzger *et al.* have demonstrated that dislocations are capable of locally eliminating carbon in C-doped buffers resulting in areas of carbon depletion, which can have an impact on breakdown voltage of the device [158]. It is clear that in order to ensure reliable operation of GaN-based diodes and transistors, dislocation densities must be carefully controlled and managed well as they can severely compromise the device performance.

2.4.3 Short Channel Effects

Short channel effects relate to phenomena affecting the carrier confinement and 2DEG control observed when the gate length and channel depletion width are of the similar order of magnitude. Drain-induced barrier lowering describes lowering in the threshold voltage of the device with applied drain potential due to reduction in the depletion region under the gate (Fig. 2.26a).

Punch-through (shown in Fig. 2.26b) describes Off state drain-induced current flow under the gate resulting from insufficient carrier confinement in the channel. To prevent the punch-punch through modern devices use doping in the buffer [78], however other methods of carrier confinement can also be effective [159]. Short channel effects can significantly affect device performance and reliability causing increased Off-state leakage, threshold voltage shift and generally reducing the ability to control the channel via the gate. In extreme cases, they can result in premature device failure and breakdown [160]. Short channel effects are particularly common in high frequency RF devices owing to their short gate lengths and can be mitigate by providing appropriate carrier confinement via buffer insulation [78] and by maintaining appropriately high aspect ratio (gate length to channel width L_G/t_{ch} ratio) of the device [161]. In addition, Bahat-Treidle *et al.* have demonstrated succesful mitigation of short channel effects by introduction of graded AlGaN buffer to the HEMT structure [162].

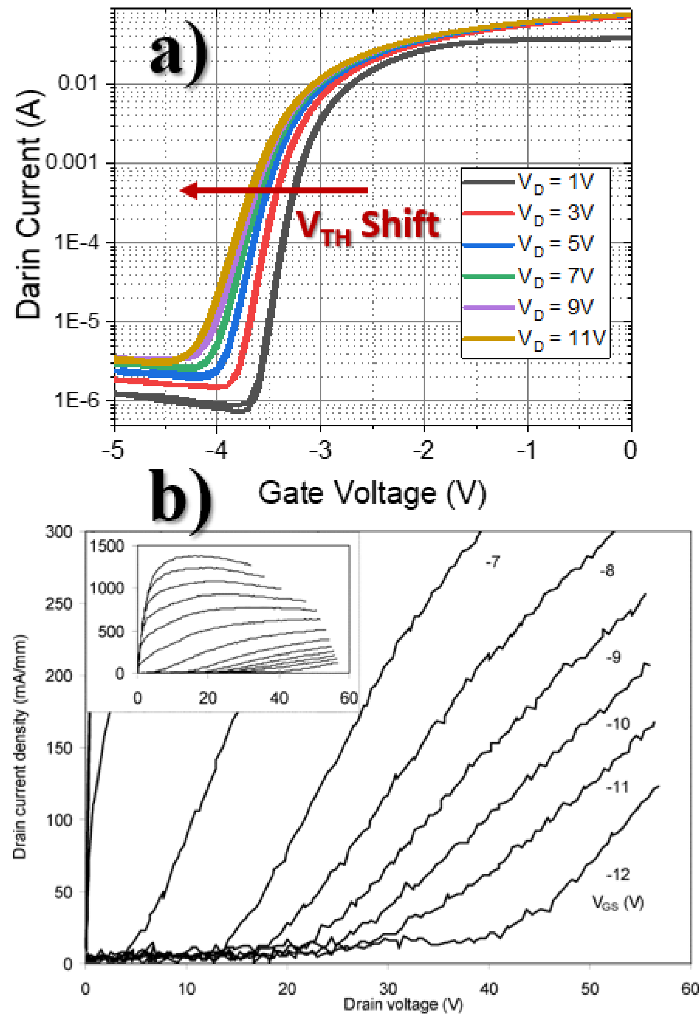

Figure 2.26: **a)** Drain-induced barrier lowering effect observed in GaN-on-SiC HEMTs with gate length L_G = 150 nm. **b)** An example of punch-through in a GaN-on-SiC HEMT with undoped GaN buffer. Inset: full IdVd characteristics of measured device. Reprinted from [78] © IEEE (2006).

2.4.4 Surface Trapping

During Off and semi-On state operation GaN HEMTs experience particularly large electric fields at the drain-side edge of the gate which can lead to compromised electrical performance of the device. The carriers travelling through high-field region of the device can obtain sufficient energy to cause impact ionization. The resultant “hot electrons” can get trapped in the layers above the 2DEG causing depletion in the channel and alter the threshold voltage, as well as lead to defect formation and degradation of the device [144][163][164]. The effects of impact ionization and thus the rates of hot electron generation can be monitored using electroluminescence (EL) measurements, where the photons generated during impact ionization can be directly observed by the light emitted in the process, or by measuring gate currents which will depend on the rate of hole generation [165] [164].

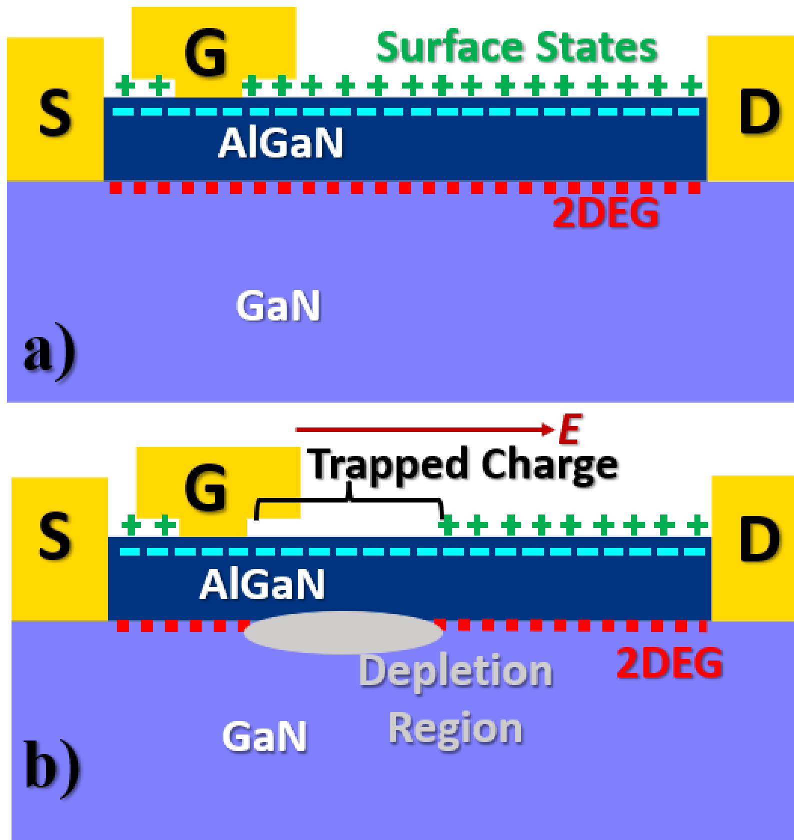

Figure 2.27: Schematic diagram to show the effects of applied external field on the surface states: **a)** device before application of electric field E and **b)** after electric field E is applied surface states are populated resulting in depletion of 2DEG in that region.

In addition, application of large negative bias to the gate can result in injection of the electrons from the gate into the surface states at the top of the AlGaN barrier, acting as a “virtual gate” and depleting the 2DEG [166]. In case of unpassivated devices these electrons can spread as far as 1 micron away from the gate causing sever 2DEG depletion across the channel [167]. A similar effect to virtual gate involves injection of the electrons into the trap states in AlGaN barrier at the gate edge via Poole – Frenkel mechanism [168]. In each case trapped charges significantly affect the output characteristics of the device altering the threshold voltage and reducing the drain current particularly during RF operation. An example of the effects of surface trapping on 2DEG is shown in Figure 2.27.

The suppression of surface trapping can be achieved by implementing carefully designed field plates and appropriate choice of passivation. Field plates serve to spread the potential across the gate-drain access region more uniformly, reducing the peak electric field at the gate edge and leading to increased breakdown voltage of the device [169]. Xing *et al.* has demonstrated that introduction of field plates to GaN power HEMT can result in breakdown voltage increase of over 500 V [170]. Moreover, the addition of field plates has also been related with reduction in the

dynamic R_{ON} [171]. At low voltages, the electric field is predominantly concentrated under the edge of the field plate, however as the applied potential increases the high field regions begin to spread across the entire length of the field plate [172]. The passivation layer serves to protect the device from the formation of the virtual gate and improves channel control of the gate terminal, resulting in increased output power density and breakdown voltage of the devices [173].

2.4.5 Buffer Trapping

Due to significant progress made in field plate and passivation design surface trapping can now be effectively managed. However, buffer trapping still poses challenges for realisation of reliable and efficient GaN HEMTs for power and RF electronics as outlined in section 2.4.2. GaN based devices are manufactured on foreign substrates due to low costs and unavailability of large are native GaN substrates. Therefore, buffer is of paramount importance to achieve defect free GaN layers with as few dislocations as possible. In an effort to suppress short channel effects and to improve carrier confinement GaN buffers contain high concentrations of intentional dopants, mainly carbon and iron. Iron is the dopant of choice for RF devices and results in relatively minor current dispersion following Off-state stress in comparison to C [85]. However, GaN buffers doped with C show higher breakdown voltages and lower Off-state leakage currents, making it a more suitable dopant for power applications [174] [175] [176]. Fe doping leads to formation of semi-insulating buffer with a Fermi level located in the upper half of the bandgap, while incorporation of carbon results in a p-type buffer, which creates a pn – junction between the UID channel and the buffer. This results in the latter layer electrically floating and acting as a reservoir for trapped charges.

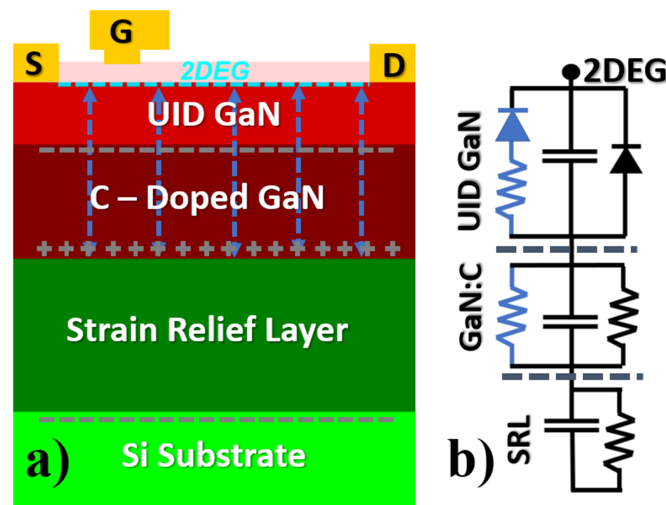

Figure 2.28: **a)** Schematic diagram of GaN power HEMT showing locations of relevant charge accumulation regions during device operation. Vertical dislocations relevant to charge transport processes in GaN layers are shown as dashed blue arrows. **b)** Equivalent lumped element representation of the GaN HEMT with dislocations highlighted in blue.

For GaN power devices, typical C concentration can vary from 10^{17} cm^{-3} to 10^{19} cm^{-3}, with the modern devices favouring higher dopant concentrations. It has been demonstrated that the compensation ratio of C donors to acceptors in a doped buffer is at least 0.4 [177], which would result in the free hole concentration on the order of 10^4 – 10^5 cm^{-3} and equivalent buffer resistivity as high as 10^{14} Ω·cm. Under the high drain bias conditions, the pn – junction is under reverse bias and forms a barrier to vertical charge flow, with the C - doped buffer layer acting as a back gate to the 2DEG. Therefore, changes to the potential in this layer will have a significant effect on the 2DEG current.

It has been demonstrated that the effects of buffer back gating can vary between different commercially available devices despite similar epitaxial structure and doping profiles [178]. Fig. 2.28 shows a schematic diagram of charge distribution in an operating GaN power HEMT together with corresponding equivalent 1D lump element representation of the device. In reality, GaN buffer is not completely isolated from the 2DEG and there exist vertical leakage paths connecting C - doped GaN buffer to the 2DEG (denoted as resistors in the diagram). Uren *et al.* proposed the "leaky dielectric" model to explain the link between the dynamic R_{ON} in power devices and vertical leakage pathways across the buffer [92]. The application on large voltage to the drain results in charge accumulation across the interfaces as shown in Fig. 2.28a. The negative charge at the top of C - doped GaN layer will interact with the 2DEG leading to increase in the R_{ON}. This negative charge accumulation can be mitigated by the presence of the dislocations providing vertical leakage paths between the 2DEG and the C - doped GaN buffer, and therefore it is essential for these leakage paths to be present across the entire length of the device. Surprisingly, the magnitude of dynamic R_{ON} depends mainly on the presence of the vertical leakage paths and not on the concentration of trap states in the buffer.

Some of the new GaN-based transistors attempt to replicate the effects of dislocations by including p-GaN "injection" regions, which provide a source of holes to counteract the negative charge trapping in the buffer during device operation [31] [179]. Although these devices are not yet prevalent in commercial power electronics, alternative methods to dislocation conduction for positive charge injections into the buffer are actively sought out and the improvements in growth techniques aim at further reduction of dislocation densities in the buffer.

2.4.6 Device Breakdown

Due to its wide bandgap GaN offers theoretical breakdown fields of the order of 3.3 MV/cm with GaN HEMTs demonstrating breakdown voltages as high as 1.6 kV [180] (see section 2.1.1). The ability to withstand large Off state voltages is of utmost importance for power applications. However, prolonged exposure to high electric fields can lead to deterioration of output characteristics of the device and its eventual breakdown, resulting from phenomena such as Schottky gate degradation [181], hot electron damage [182], defect formation and trapping [183] as well as other similar processes, with the largest electric fields being experienced at the

drain side of the gate and in the buffer. Thus, these locations are particularly prone to breakdown.

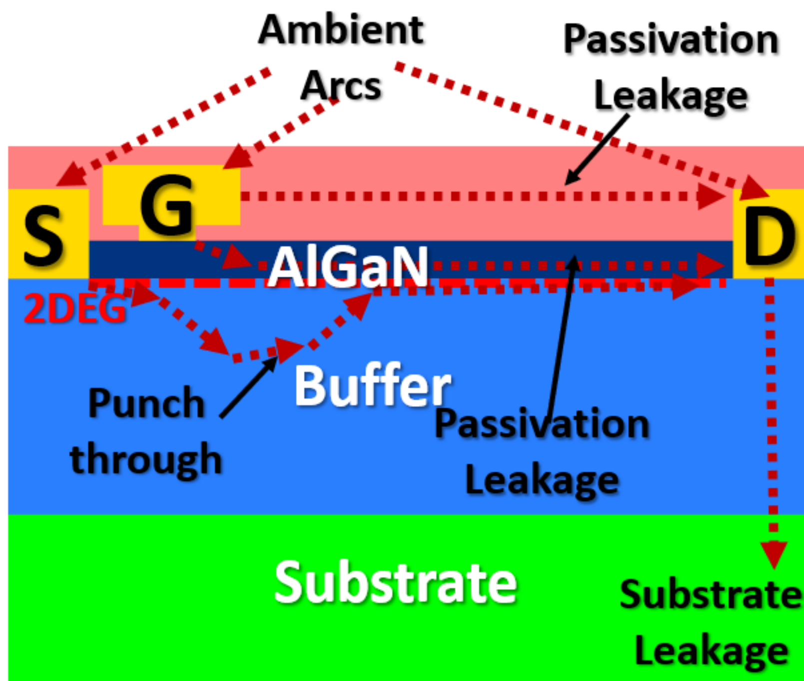

Figure 2.29: Schematic representation of major leakage path in a GaN HEMT device that can contribute towards premature device breakdown.

Generally, breakdown is defined as the voltage at which the drain current flow exceeds 1 A per mm of device width. Fig. 2.29 shows a schematic representation of the major leakage path that contribute towards device breakdown, with the most prominent examples including:

- **source – drain breakdown due to short channel effects** - drain breakdown due to short channel effects – this breakdown mechanism is closely related to the quality of the depletion region and can be prevented by improved carrier confinement or introduction of a double heterojunction [78] [162];

- **gate breakdown** - various mechanisms can be responsible for this breakdown mode; surface leakage caused by hopping conduction between drain and gate along the surface which increases with the applied drain potential is one of the main causes for gate breakdown [184] [[185] and can be prevented by appropriate passivation and surface optimization; leakage across AlGaN barrier can take place via defects, trap – assisted tunneling, Pool – Frenkel or thermionic emission, and can lead to gate breakdown [186] [187];

- **vertical (buffer) breakdown** - this breakdown mode becomes particularly significant when large potential (~ 500+ V) is applied to the drain and the vertical leakage across the buffer becomes significant; the main methods to prevent vertical breakdown include introduction of thicker GaN buffers [188], buffer doping with C and ensuring appropriate device

geometry [189]; Fig. 2.30 shows the variation in vertical breakdown voltage for AlGaN and GaN buffers as a function of source-to-drain spacing, demonstrating the possibility of increasing the critical field in the device by adjusting the distance between the electrodes. At low electrode separations the breakdown is dominated by leakage current between the gate and the drain, however as the spacing is increase, buffer plays more important role as it facilitates the leakage from the source to the drain via the substrate, with the omission of gate region [189].

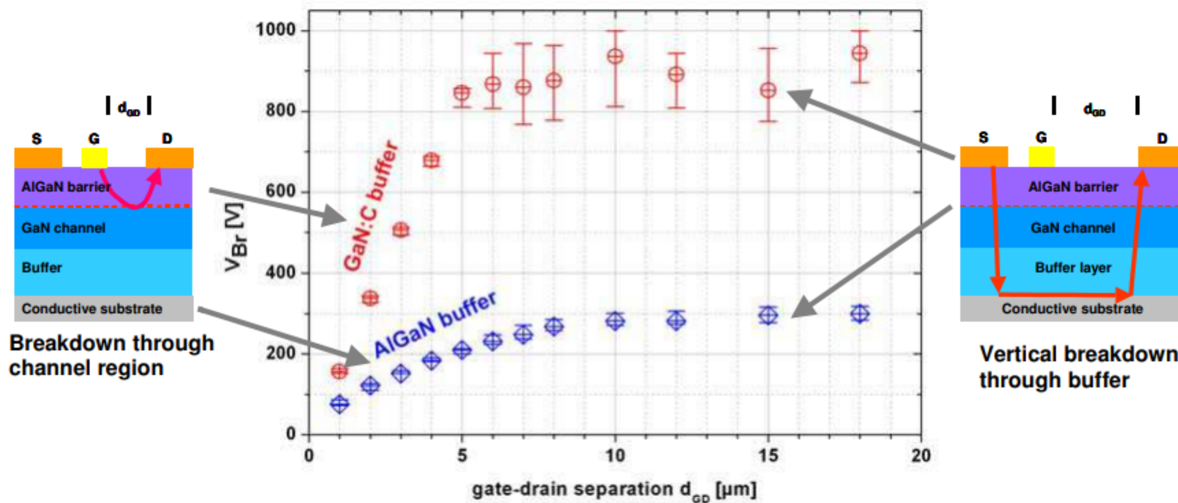

Figure 2.30: Breakdown voltage dependence on gate-drain separation for devices with two different buffer architectures: C-doped GaN buffer and AlGaN buffer. In each case, the breakdown between gate and drain gives way to breakdown through the buffer at larger electrode separations. Figure reprinted from [189] with the permission from IOP Publishing.

2.4.7 Self-Heating and Reliability Implications

In addition to the electrical failure modes describe in this section, thermal management is of vital importance as operating GaN RF HEMTs can reach power dissipations as high as 10 W/mm, leading to peak channel temperatures on the order of 200 °C [190]. Prolonged exposure to elevated device temperatures can cause contact degradation [191] as well as delamination of passivation [192], significantly reducing the expected device lifetime. The most common techniques for predicting the device wearout involve accelerated Arrhenius lifetime testing, where the transistor lifetime is measure at three temperatures and the results are extrapolated over the desired temperature range [193] (an example is shown in Fig. 2.31). High temperature operating life (HTOL) testing is another popular technique for reliability testing of GaN-based devices. This method can be performed under DC or RF operating conditions and involves monitoring of desired output characteristics at elevated temperatures as a function of time. Mean time to failure can be extracted by extrapolating the change in investigated output characteristics over time [194].

Although these techniques can be instructive for estimates of mean time to failure, they often predict excessive device lifetime as they do not take into account field-driven modes of failure [195]

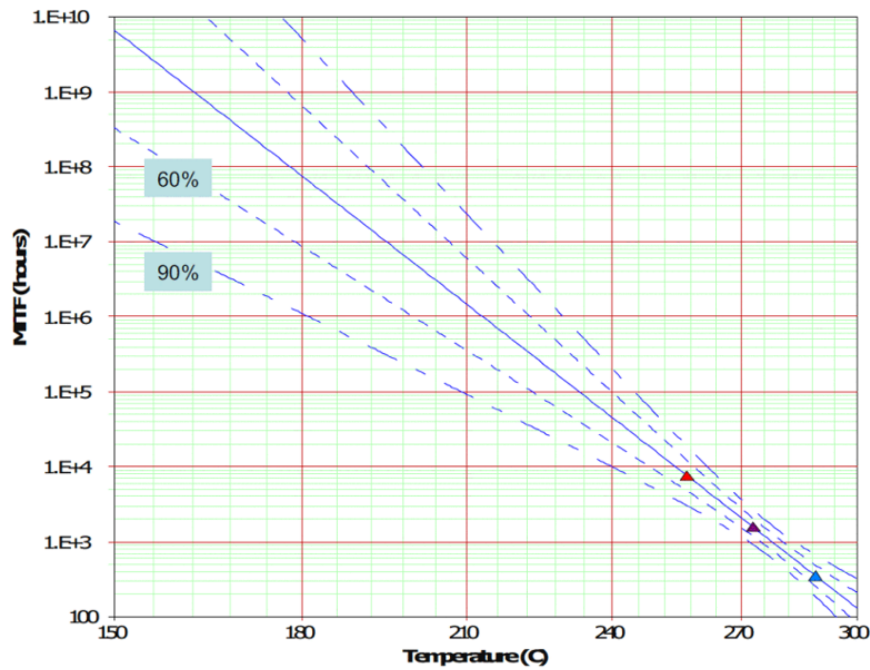

Figure 2.31: Typical MTTF plot for prediction of device lifetime based on measurements performed at 3 temperatures. Reprinted from [193] © IEEE (2008).

For conventional GaN HEMT operation the peak of the electric field exists at the drain-side of the gate edge in the vicinity of the AlGaN/GaN interface [172]. Hot electrons travelling through that region interact with the lattice and release their energy via Fröhlich interactions, which involve electrostatic coupling of an electron with a longitudinal (LO) phonon [196]. With the group velocity of optical LO phonons close to zero, these phonons remain in the high field region until they decay into transverse optical and acoustic modes or until the energy is passed on to charge carriers. Since the lifetime of the optical LO phonons (~ 350 fs) exceeds the rate of their generation (~ 10s fs) [197], there is an accumulation of non-equilibrium hot phonons in this region of high electric field at the gate edge [198]. The Joule heat is transported away from the hotspot by acoustic phonons created from the decay of the hot LO phonons.

The location of the hot spot region is strongly dependent on operating conditions (e.g. DC operation or RF operation), power dissipation and device design (i.e. presence, location and shape of field plates) [199] [200] [190]. Figure 2.32 shows an example of a simulated Joule heating for a GaN HEMT with a single field plate for voltages between 30 V and 100 V. The presence of the field plate acts to spread the electric field at the gate edge, resulting in heating region extended over a distance of ~ 0.5 μm. As the voltage is increased above 50 V, the second hot spot appears at the drain-side edge of the field plate due to its field spreading ability.

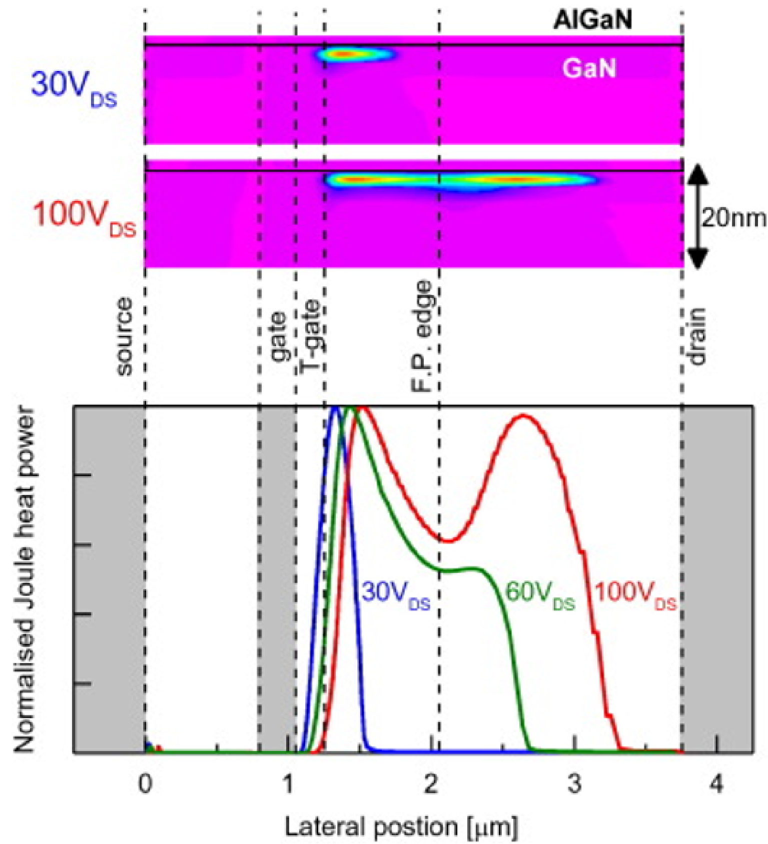

Figure 2.32: Simulated Joule heating profiles along the AlGaN/GaN interface for a device with a single source field plate. Reprinted from [190] with the permission of the Elsevire.

The heat is effectively transported away from the hot spot by the transverse phonons and therefore it is of crucial importance to create pathways for efficient heat extraction, especially in GaN-based devices for high power and RF application. The most important areas of device design to optimise thermal performance of GaN transistors and diodes involve:

- **substrate** - despite the added cost relating to GaN growth on substrates different to Si or sapphire, integration of high thermal conductivity substrates such as SiC or diamond can have significant effects on overall device performance, such as increased power outputs and longer device lifetime at higher temperatures [201] [202] [203];

- **thermal boundary resistance** - thermal boundary resistance describes a phenomenon responsible for temperature discontinuity between the GaN buffer and the substrate resulting from phonon mismatch between the two material; this effect in combination with thermal resistance due to the presence of nucleation layer can be lumped into so-called effective thermal boundary resistance (TBR_{eff}) [204]; generally, for commercially available devices the magnitude of $TBR_{eff} \geq 20$ m^2 K GW^{-1} (at 298 K) [205] but can be reduced by optimization of the nucleation layer as demonstrated in [206];

- **packaging and microfluidics** - despite integration of high thermal conductivity substrate and optimized internal thermal interfaces within the epitaxy, the packing can offset the benefits by ineffective heat conduction away from the device [207]; in recent years efforts have been made to develop new packaging techniques and materials for interfacing and heat sinking solutions to actively work towards reducing operating device temperatures [208] [209] [210].

To achieve robust and reliable devices capable of operating at high frequencies and delivering high power outputs, it is vitally important to carefully consider each of the areas listed above. Compromised thermal performance relating to one aspect of device design can have a significant impact on overall device reliability, offsetting any advantages achieved in all other design areas.

Chapter 3

Experimental Techniques and Methods

To develop an in-depth understanding of the device performance and to create accurate and reliable physical models, a wide range of experimental techniques as well as computational tools are applied during device testing and characterisation. This chapter focuses on electrical and thermal characterisation methods, as well as describes key measuring instruments, hardware and software employed to collect experimental data and create physical models for this thesis.

3.1 Experimental Equipment and Capabilities

3.1.1 Measurement Environment

All the results demonstrated in this work come from on-wafer measurements of unpackaged devices. There are many advantages to this approach, firstly it saves costs associated with manufacturing and optimization of packing as the primary focus is on the actual device. In addition, the ease of access to individual devices allows for relatively quick collection of significant amounts of data, as well as for assessment of growth and fabrication process by measuring individual devices at various locations across the wafer. Moreover, from practical prospective it is comparatively easy to control ambient conditions for unpackaged devices such as temperature or light, and to perform custom optical and electric measurements. Finally, in case of failure or breakdown, unpackaged devices can be easily inspected using a variety of optical methods.

Considering ambient sources of light can have an effect on device performance (mostly increasing the current due to photo-excitation of carriers), most measurements are performed in the dark, enclosed in metallic probe stations. These probe stations also act as Faraday cages, preventing noise and interference from ambient electromagnetic radiation. For comparison,

thermal measurements rely on optical methods and therefore are performed in a dark room without any external sources of light. The devices are probed with a class 3B laser, therefore any optical paths are carefully covered so as not to allow exposed laser beams.

3.1.2 Electrical Connections and Cabeling

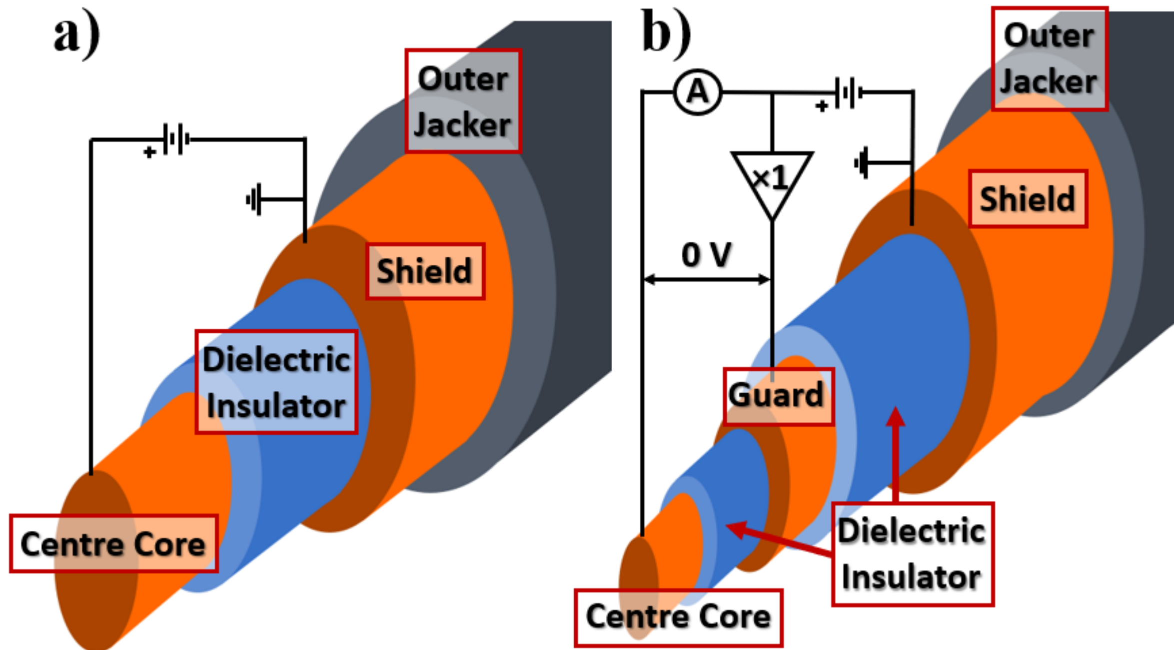

Figure 3.1: **a)** Schematic diagram showing cross-section of a coaxial cable and its biasing circuit. **b)** Schematic diagram showing cross-section of a triaxial cable and its biasing circuit. The current measured at the core cannot be attributed to internal leakage as both core and guard are maintained at the same potential.

Two main types of cabling used for electrical connections between the measuring instruments and the device under test (DUT) include coaxial and triaxial cables, which are shown in Figure 3.1. The coaxial cable (Fig. 3.1a) consists of a conductive core where the potential is applied, surrounded by an insulating layer followed by metallic shield kept at 0 V. The entire ensemble is enclosed in an insulating outer jacket to protect the cable and isolate it from the surrounding. The presence of grounded shield protects the centre core from electromagnetic radiation, allowing for accurate low current measurements.

However, coaxial cables are unsuitable for very low current measurements as the electric field present during the measurement between the centre core and the shield will result in a leakage current through the insulator in some cases sufficiently large to exceed the measured currents. To counteract this issue, traixial cables (Fig. 3.1b) include another conductive layer, guard, which is positioned in between the centre core and the shield. By biasing the guard at the same potential as the centre core (guard is biased by the current buffer), there exists no electric

field between these two layers and thus there is no leakage current between centre core and the guard. The existing leakage in the insulator between guard and shield does not affect the measurement as it flows into the current buffer.

3.1.3 Probe Stations for Electrical Measurements

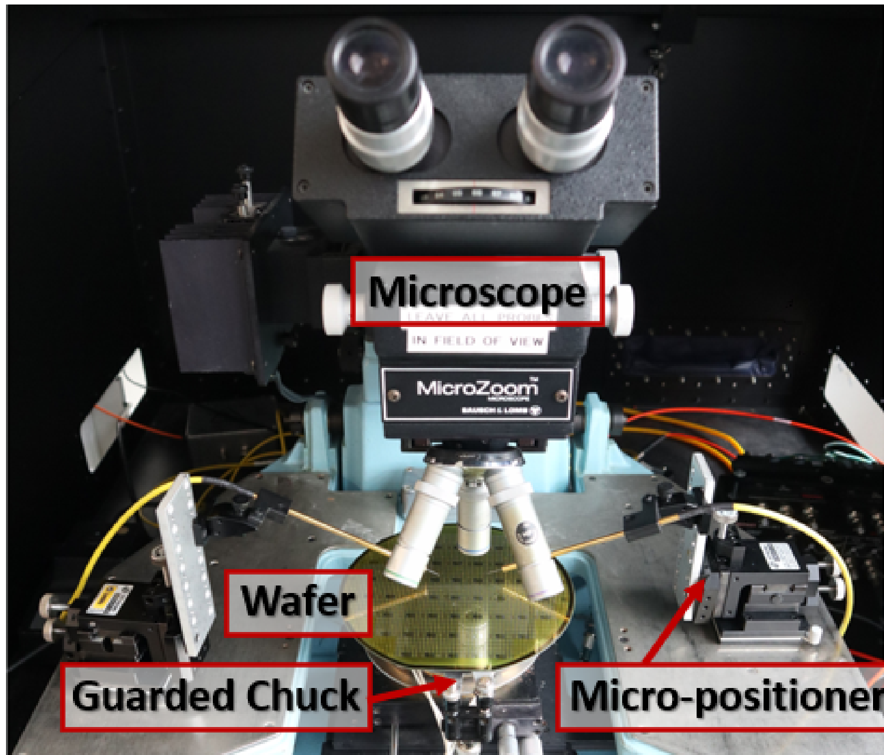

Figure 3.2: Probe station designed for electrical measurements equipped with optical microscope, micro-positioners and a 6-in wafer on top of a guarded chuck.

Figure 3.2 shows a typical measurement enclosure equipped a probe station manufactured by Wentworth Labs, which includes optical microscope, a chuck for mounting of samples and provides a metallic surface to attach magnetically held micro-positioners as shown in the figure. The micro-positioners are equipped with tungsten probes with the tip diameter in the range 5 μm to 50 μm. The micro-positioners allow for position adjustment in three separate directions with the spacial precision of 3 μm. In addition, the angle between the the probe tip and the wafer can be adjusted with the accuracy of ~2°. The measurements of RF devices were performed with the Picoprobe's Model 40A tungsten GSG probe tips with appropriate pitch, most often in the range between 100 μm to 200 μm, and with insertion losses below 0.8 dB.

The wafer is rested on a guarded chuck made up of two plates separated by an insulator, both biased at the same potential. This arrangement results in elimination of displacement current between the plates of the chuck, resulting in the top plate being guarded. In this way, the current

measurements originate solely from the device under test, as there is no electric field present within the chuck. The principle behind this set up is similar to triaxial cable described above and allows for more accurate measurements of substrate currents.

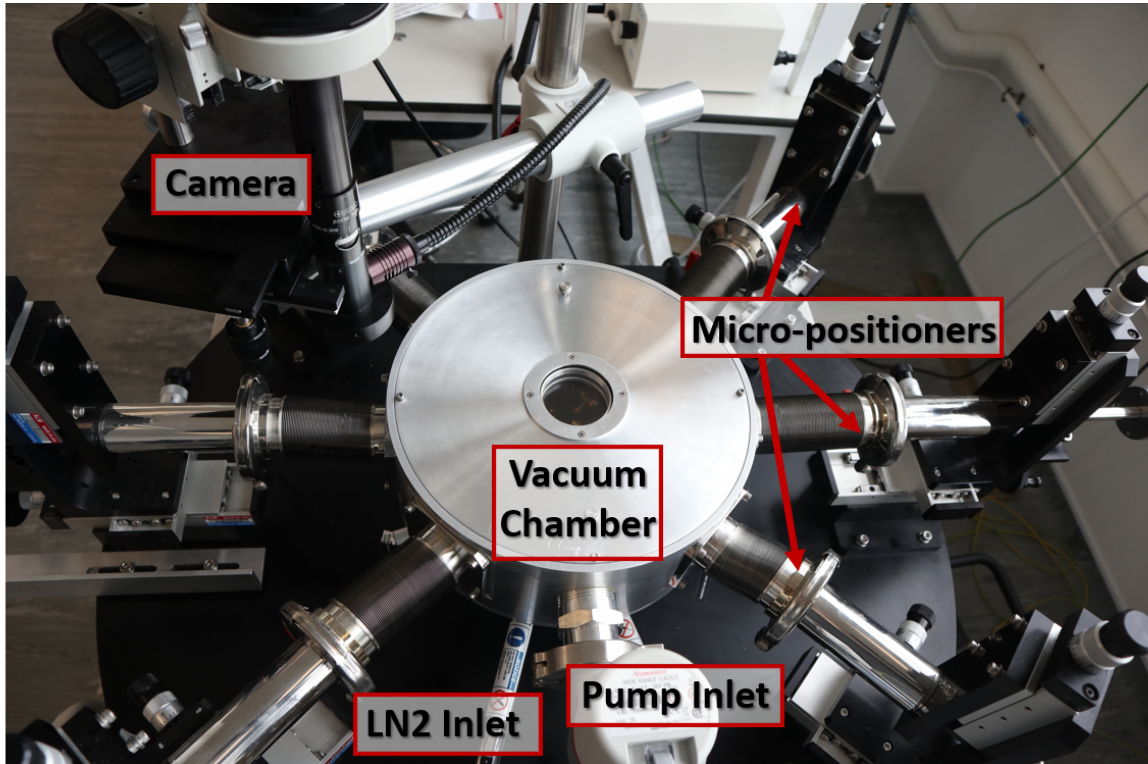

Figure 3.3: Cryogenic probe station Janis St-500, comprising of vacuum chamber with six micro-positioner arms attached to it. The vacuum is maintained by a turbo-molecular pump whereas temperature is controlled by a temperature controller and manual adjustment to the liquid nitrogen (LN2) flow.

Measurements requiring variation in device temperature were preformed in Janis Research Micromanipulated St-500 probe station containing six micro-positioner arms (shown in Figure 3.3), which was combined with Lake Shore Cryotronics's Model 336 temperature controller and Edwards T-Station 75 42 L/s turbomolecular vacuum pump. The probe station is capable of accommodating wafers with diameter up to 6 inch, while due to incorporation of triaxial connections inside the arms (guarded chuck included), the system is capable of performing low current measurements with internal leakage currents on the order of ~ few fA. The temperature control is achieved by combining the electronic heating system (based on a resistance heater) capable of operation between 3.5 K to 475 K (accuracy below 0.3 K), with the manual adjustment of liquid nitrogen flow from the Dewar container around the vacuum chamber. The electronic feedback system detects the cooling rate of liquid nitrogen and adjusts the heating power to achieve precise temperature inside the chamber. Presence of ultra high vacuum (pressure inside the chamber $\approx 5 \times 10^{-9}$ Pa) significantly reduces heat loss from the sample due to convection.

3.1.4 Probe Station for Thermal Measurements

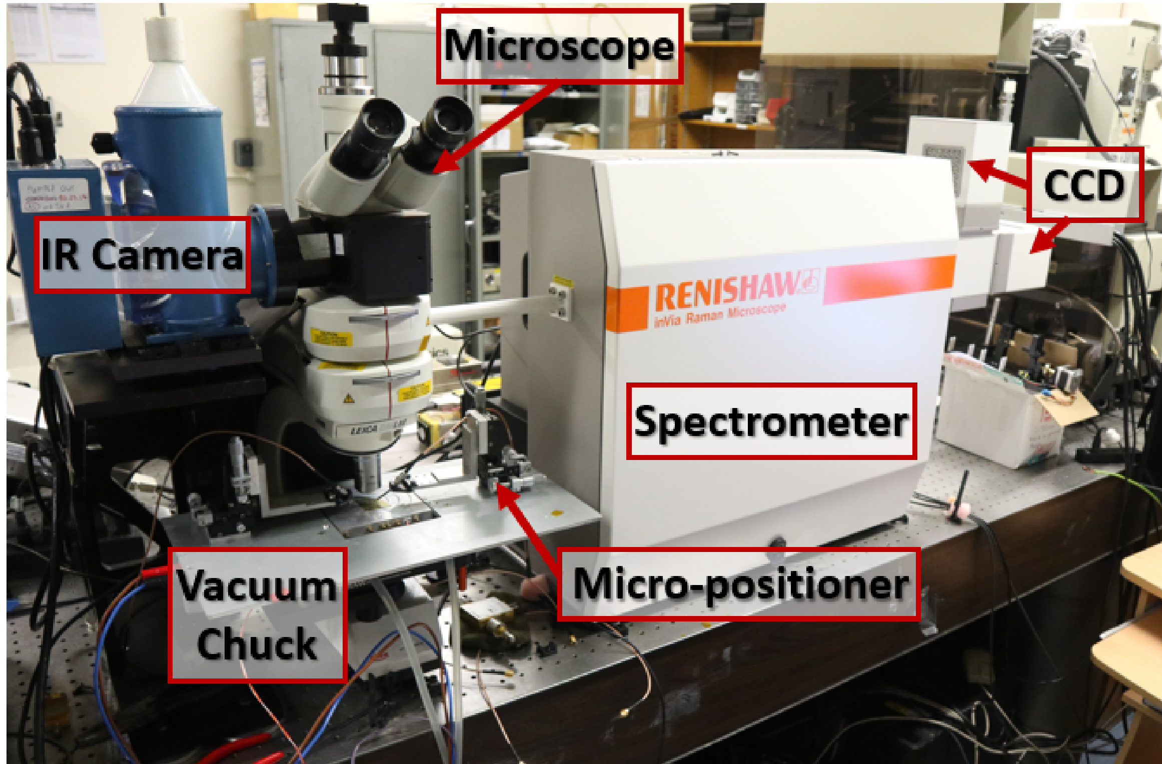

Figure 3.4: Probe station used for thermal measurements described in this chapter. The station consists of Raman spectrometer integrated with an optical microscope, video camera, IR camera and two CCDs. The micro-positioners are placed on the metal stage surrounding the thermo-electric vacuum chuck. The whole set-up is rested on an optical table.

Figure 3.4 shows the probe station used for thermal measurements. The set-up includes a spectrometer with two CCDs connected to an optical microscope and a video camera to deliver live images to the computer. The samples are rested on the thermo-electric vacuum chuck, which includes a resistive filament to offer heating up to 120°C. The cooling is achieved by pumping an ethylene glycole based coolant, which in combination with the heater allows for temperature control with the accuracy of ~ 0.2°C.

The thermo-electric vacuum chuck includes a metal stage to enable magnetic attachment of micro-positioners. The whole set-up rests on an optical table to reduce the effects of vibrations. In addition, all the cables are tied together and surrounded by foam to mitigate the vibrations mainly from the cooling system.

The probe station also includes the IR camera and a liquid nitrogen container allowing for a wide range of measurements to be performed at a single station. The entire set-up is connected to the computer which controls the spectrometer (and its various mechanical component), cameras and the thermo-electric vacuum chuck via appropriate software. The entire station is grounded and placed inside a dark room.

3.1.5 Measurement Instrumentation

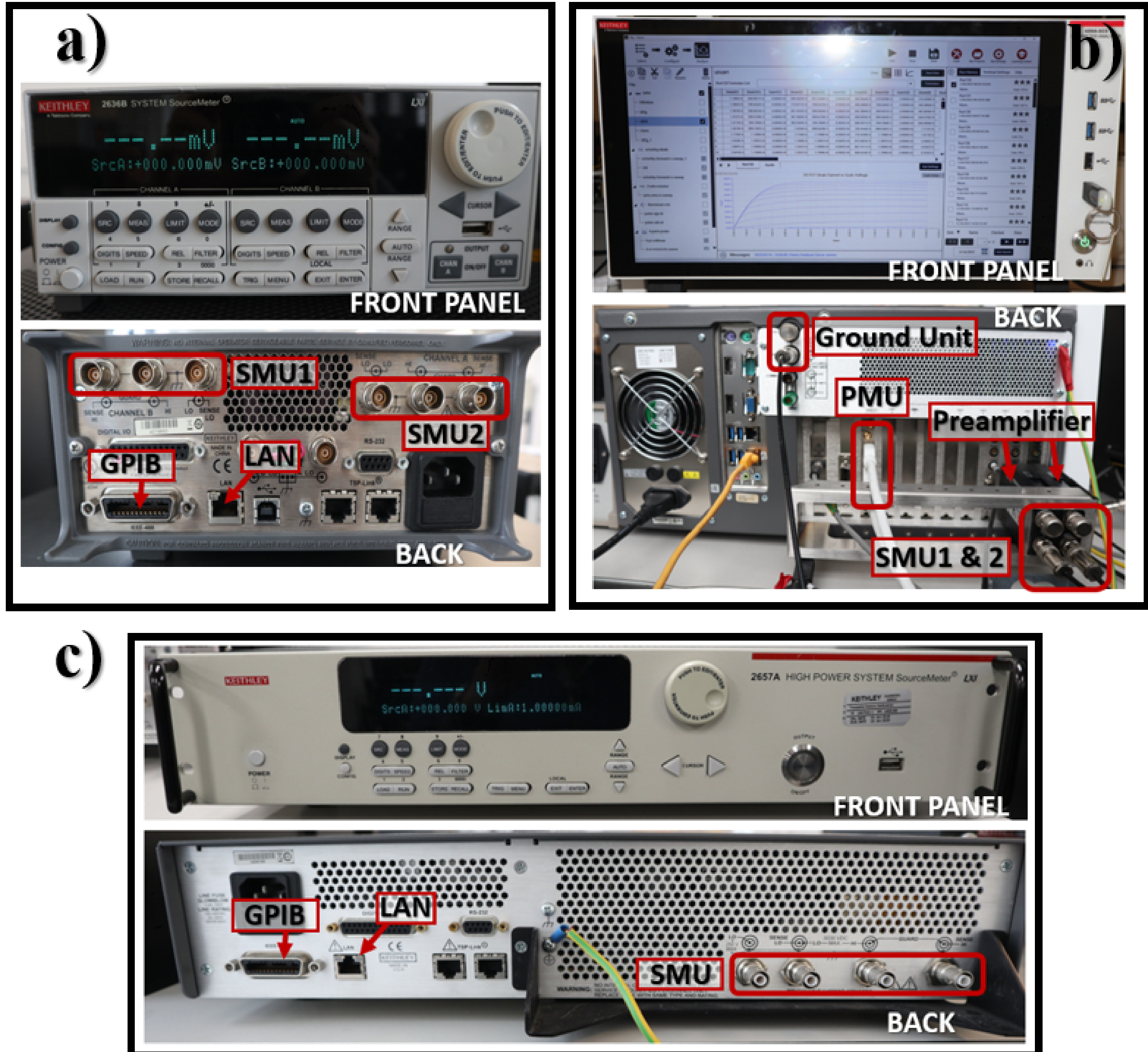

Figure 3.5: **a)** Keithley 2636B Source Meter Instrument equipped with two SMUs with triaxial connectors, GPIB bus for external control and LAN port for integration with other instruments. **b)** Keithley 4200A-SCS Parameter Analyser equipped with two low-power SMUs (and corresponding preamplifiers to increase the current resolution), one PMU and a high power ground unit. All of the above units are equipped with triaxial connectors. **c)** Keithley 2657B Source Meter Instrument equipped with high power SMU (triaxial connector), GPIB bus and LAN port.

Figure 3.5 shows three main instruments for electrical characterisation used to perform measurements presented in this thesis. Each of these instruments is equipped with source measurement units (SMUs) capable of sourcing voltage and measuring current (and vice versa) at the same time. The SMUs equipped with the instruments shown here possess triaxial connectors to allow for low current measurements. However, each of these instruments serves a different

purpose as their capabilities vary significantly in terms of current resolution and power handling ability.

The Keithley 2636B Source Meter Instrument shown in Fig. 3.5a is a small and compact unit containing two SMUs, each capable of delivering voltages up to 200 V with the current resolution on the order of ~ 100 pA, and the maximum power handling of 30.6 W per SMU. Due to its good current and voltage resolution this instrument is suitable for a variety of applications and can be easily programmed to run custom measurements.

The Keithley 4200A-SCS Parameter Analyser shown in Fig. 3.5b is equipped with two SMUs with the maximum voltage range of 210 V and maximum current of 105 mA, while being capable of measuring currents as low as 1 fA with the aid of preamplifier. The presence of ground unit gives an added ability to increase the current handling capabilities up to 2.6 A. The instrument is also equipped with a pulse measure unit (PMU) capable of delivering pulses as short as 100 ns for voltages up to 40 V. The inclusion of capacitance-voltage unit (CVU) for voltages up to 200 V and frequencies from 1kHz to 10 MHz, makes this instrument particularly versatile, allowing for DC, pulsed IV and CV characterisation to be performed on the devices in one swift sequence.

The Keithley 2657B Source Meter (shown Fig. 3.5c) contains one high power SMU with a triaxial connector, capable of delivering voltages as high as 3 kV and currents up to 120 mA. This instrument is particularly useful for vertical breakdown and leakage measurements, but is also often combined with Keithley 2636B to perform bidirectional substrate ramp sweeps.

All thermal measurements presented in this work were performed using Renishaw InVia Raman spectrometer combined with 488 nm frequency double diode laser. The photo of the spectrometer and the schematic diagram showing its main components are presented in Figure 3.6. Before entering the spectrometer, laser light passes through a neutral density filter in order to reduce the beam intensity to a desired level. Upon entering the spectrometer, the laser beam encounters the first beam steering mirror (A) which directs the light through the beam expander (B) consisting of two lenses with coinciding focal points. Laser beam travelling through the beam expander increases its diameter while maintaining its collimation. It then travels towards the second beam steering mirror (C) where it is directed vertically towards the Rayleigh filter (D) via a cylindrical lens, which reduces power density delivered to the DUT. The purpose of Rayleigh filter is to block wavelengths around the chosen beam wavelength, while allowing for efficient transmission of remaining frequencies. The light is reflected from the filter into Leica DMLM microscope where it is further directed and focused onto the sample via a Nikon 50x objective lens with a 0.5 numerical aperture (NA), which allows for sub-micron special resolution at the DUT surface.

The light back-scattered from the sample is collected by the objective lens and directed again towards the Rayleigh filter, which blocks Rayleigh scattered light while allowing Raman scattered light to pass further down the optical path. This light is then focused onto an adjustable slit (F) by

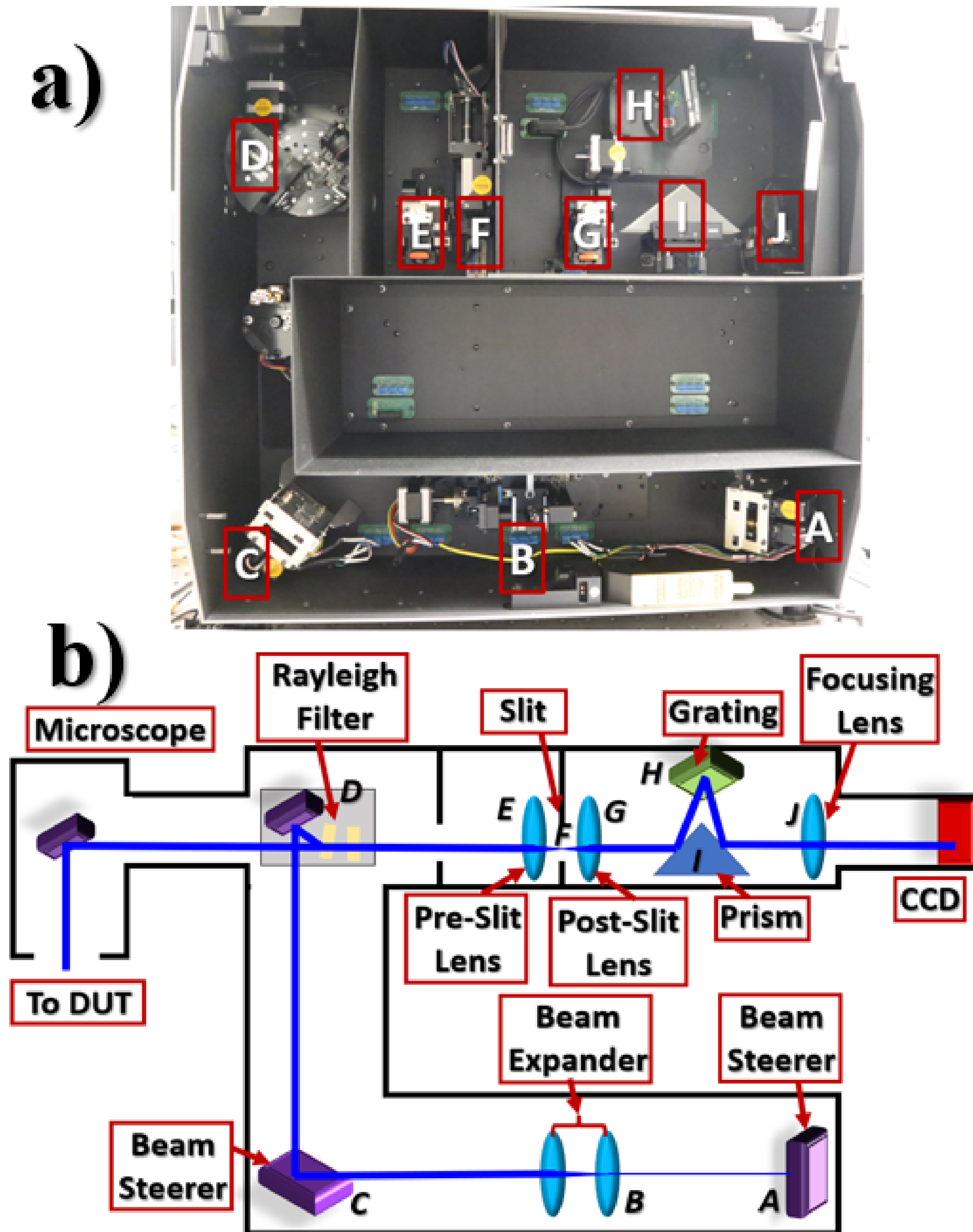

Figure 3.6: **a)** Photograph and **b)** schematic representation of Renishaw InVia micro-Raman spectrometer with the main components labelled and the corresponding laser path indicated.

a lens (E) which also serves to blocks off the ambient light entering through the objective lens. The slit width affects the spectral broadening, with the narrower slit reducing the broadening. The slit is motorised and its width is usually ~50 μm, with the fine tuning performed automatically by the Wire software operating the spectrometer.

The slit is followed by another lens (G) that collimates the travelling light and sends it towards the prism (I). The prism directs the light at an angle towards the diffraction grating (H) with the line density of 3000 lines/mm. Subsequently, the light is reflected towards a lens (J) which focuses it onto the CCD, which is equipped with a shutter to control the exposure time. Once the shutter is open, CCD accumulates electric charge proportional to the amount of incident light for each individual pixel, which after closing of the shutter amplifies the signal and converts pixel positions into frequency.

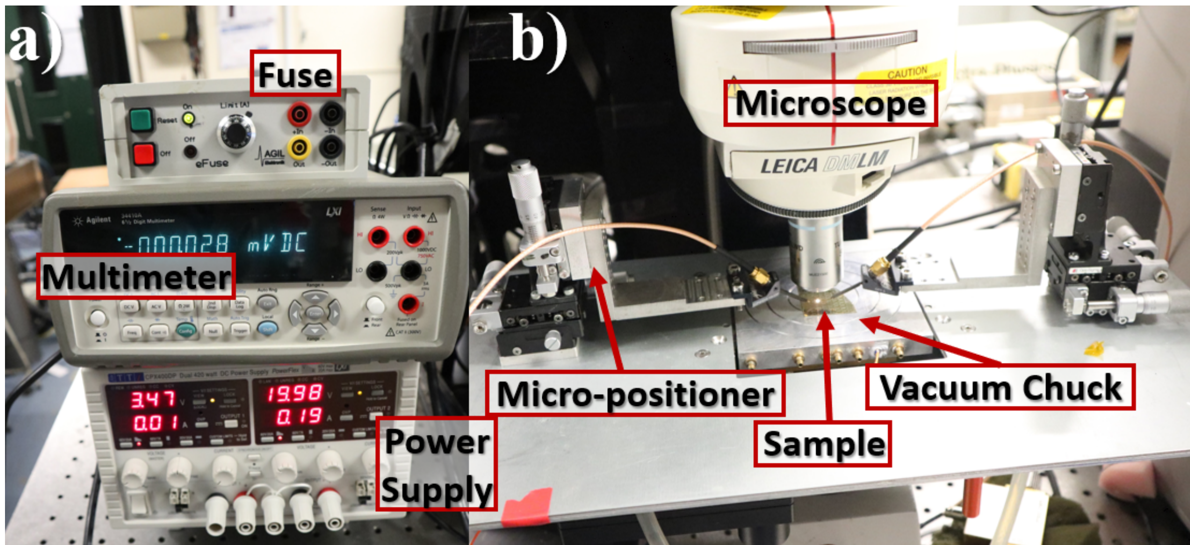

Figure 3.7: Instruments and general electrical set-up for thermal measurement. **a)** Instruments used to bias the devices for thermal characterisation: TTI CPX400DP power supply, Agilent 34410A Multimeter and Agil Elektonik AL-EFUSE2-200-10 electronic fuse. **b)** Sample containing RF GaN HEMTs prepared for micro-Raman thermography measurement.

In addition to Raman spectrometer, thermal measurements of operating devices require appropriate instrumentation for biasing of the devices (see Figure 3.7a). To control drain and gate terminals of the DUT, TTI CPX400DP power supply was used. This instrument is capable of delivering up to 60 V, while being able to handle currents up to 20 A, allowing for high power measurements of multifinger transistors. Due to its limited current resolution, Agilent 34410A Multimeter serves as an ammeter to ensure accurate power dissipation throughout the measurement. In addition, Agil Elektonik AL-EFUSE2-200-10 electronic fuse with adjustable current compliance ensures the safety of instruments and devices involved in thermal measurements. For smaller devices with low current outputs the power supply, multimeter and fuse combination can be replaced with a single Keithley 2636B instrument. The devices are contacted either by three separate tungsten probes mounted onto micro-positioners, or in case of RF devices (as shown in Figure 3.7b) using GSG probe tips. The devices are mounted onto a thermo-electric vacuum chuck positioned directly below Renishaw InVia Raman spectrometer.

3.2 Electrical Characterisation Techniques

This section describes key experimental techniques and computational tools for electrical and thermal characterisation of GaN-based devices for RF and power electronics,

3.2.1 DC & Pulsed Current-Voltage Measurements

DC current-voltage (IV) characterisation is one of the most basic and useful techniques to gain a good overall insight into device operation. The general idea behind IV measurements involves monitoring of the output current as a function of applied DC potential. The two most common types of IV characterisation performed on GaN HEMTs are IdVd and IdVg measurement: the first one involves sweeping of drain potential while recording drain current at a fixed gate voltage, while the latter is performed by maintaining constant drain potential and monitoring drain current while the gate voltage is swept. During a typical IV measurements currents at other electrodes are also monitored (eg. gate current or source current) and can therefore help easily identify the reason for deviation from ideal IV characteristics.

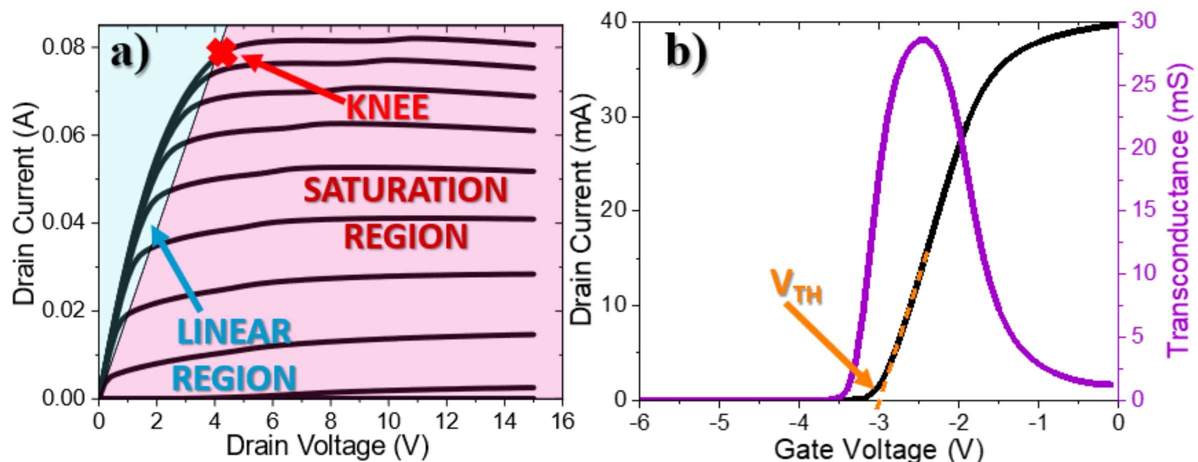

Figure 3.8: **a)** Typical DC IdVd characteristics showing linear region, saturation region and knee voltage. **b)** Typical DC IdVg characteristics with threshold voltage and transconductance.

Figure 3.8a shows typical DC IdVd characteristics for a GaN HEMT, which can be divided into three distinct regions: linear, knee and saturation region. The linear region provides information about On-resistance of the device, while knee voltage indicates the maximum drain current that can be achieved. Saturation region shows the effects of self-heating which result in reduction in drain current with increasing power dissipation. In addition, IdVg characteristics (shown in Fig. 3.8b) can provide information about transconductance g_M and threshold voltage V_{TH}. The latter can be extracted in a number of ways, but the most common techniques to calculate V_{TH} involve extrapolation of linear part of the IdVg curve as shown in Fig. 3.8b, or extraction of voltage at which drain current drops below a a certain value (usually 1 mA/mm).

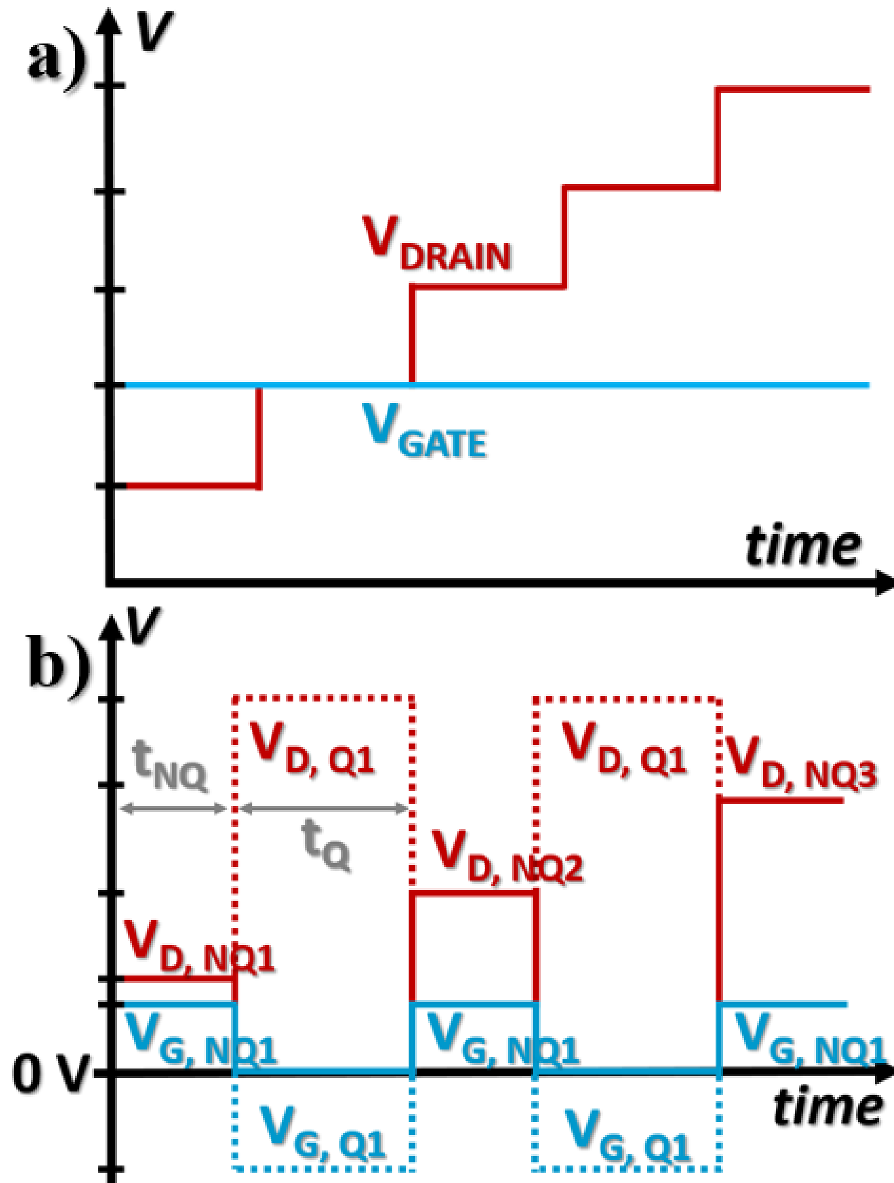

Figure 3.9: **a)** Schematic timeline of a DC IdVd measurement: drain voltage is gradually increased at a constant gate bias. **b)** Schematic timeline of a pulsed IdVd measurement. Quiescent drain ($V_{D,NQ}$) and gate voltages ($V_{G,NQ}$) are only applied for short periods of time t_{NQ} to measure the drain current. In between the measurements the applied voltage is completely removed (solid lines) or maintained at a chosen quiescent off-state stress point $V_{D,Q}$, $V_{G,Q}$ for a time period t_Q usually much longer than t_{NQ}.

Pulsed IV measurements are based on the identical premise to DC characterisation: output current is measured as a function of applied potential. The main difference between the two techniques lies in the manner in which the voltage is applied to the appropriate contacts. Figure 3.9 shows a schematic timeline of measurement as a comparison between the DC and pulsed measurements. For pulsed IV characterisation, the measurement is only taken during very

narrow time windows during which the device is in the On-state. The measurement period is known as non-quiescent state and its duration is usually as short as t_{NQ} (also referred to as t_{ON}) $\approx$ 1 μs, as prolonged on-state operation can induce significant self-heating.

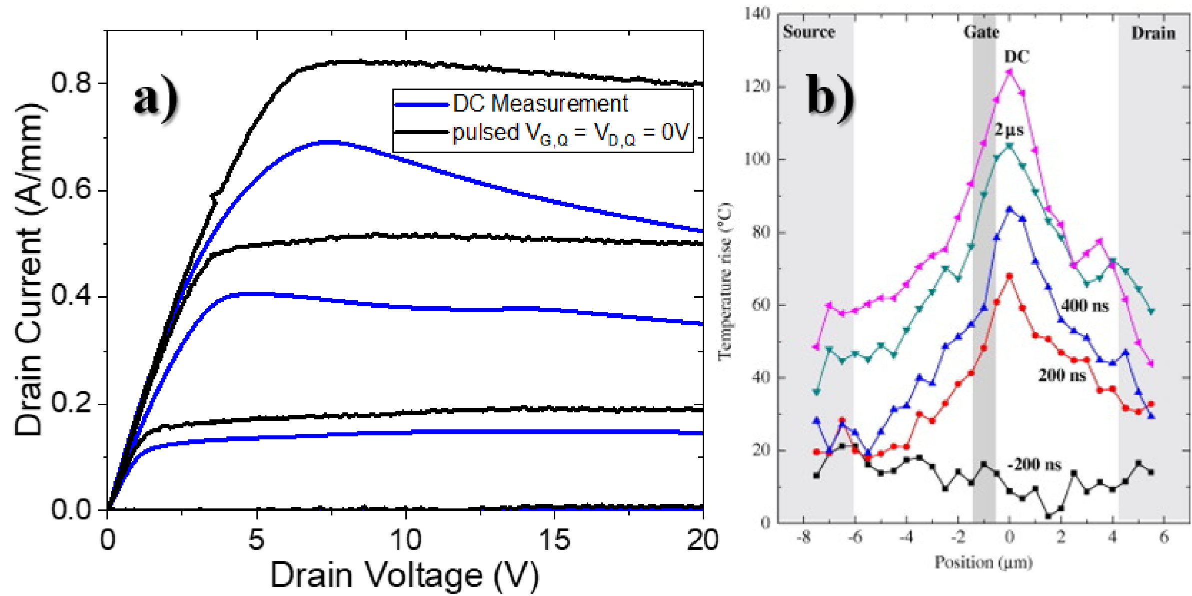

Figure 3.10: **a)** Comparison between a DC and a pulsed IdVd measurement from a quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0 V, 0 V] with the duty cycle of 0.1% (t_{NQ} = 1 μs, t_Q = 1 ms) performed on a two-finger GaN-on-Si HEMT with drain-gate spacing of 9.4 μm and gate length of 100 μm. **b)** GaN HEMT channel temperature profile for a single finger device with source-drain spacing of 10 μm and gate-length 125 μm for a range of pulse durations with power dissipation of 20 W/mm. Figure adapted from [211].

Figure 3.10a shows the effects of self heating on IV characteristics of a two-finger GaN-on-Si power HEMT resulting in reduction in saturation current up to ~ 38% in comparison with pulsed measurement with measurement window t_{NQ} = 1 μs and no stress applied in the in the quiescent state. As the non-quiescent measurement window becomes longer, the current measured in a pulsed IV measurement gradually decreases due to prolonged periods of power dissipation and increase in overall channel temperatures. This observation is aptly demonstrated in Fig. 3.10b, which shows variation in temperature profile across the source-drain gap with duration of non-quiescent bias point.

Pulsed IV measurements can be highly effective in identifying the locations of trapping in the DUT. This can be achieve by careful consideration of quiescent bias points and the duration of stress (t_Q or t_{OFF}). Considering electron capture by a trap state, if one assumes trap capture cross-section of 10^{-15} cm^2, thermal velocity of electrons as 10^7 cm/s and free electron concentration of 10^{11} cm^{-3} the resulting time constant for the electron capture is 1 ms. Due to low numbers of free carrier present in the wide bandgap semiconductors such as GaN, the above estimate of capture time constant is slightly exaggerated. Thus, quiescent time period t_Q = 1 ms is sufficient

to allow for carrier capture. The ratio t_{NQ}/t_Q is known as the duty cycle and is an important parameter describing pulsed IV measurement.

If the quiescent bias point [$V_{D,Q}$ = 0 V, $V_{G,Q}$] is chosen, such that $V_{G,Q} < V_{TH}$ the trapping current collapse in the pulsed IdVd measurement can result either from trapping in the vicinity of the gate or in the gate-drain access region. The trapping near the gate is characterised by a shift in V_{TH} in the corresponding pulsed IdVg measurement, and results in "virtual gate" formation at the gate edge locally depleting the 2DEG.

If the source of trapping is located in the gate-drain access region, the addition of drain stress will result in further current collapse and reduction in the transconductance peak accompanied by an increase in the measured R_{ON}. Trapping in the gate-drain access region should not have a significant effect of V_{TH} [164][143].

3.2.2 Substrate Ramp Sweeps

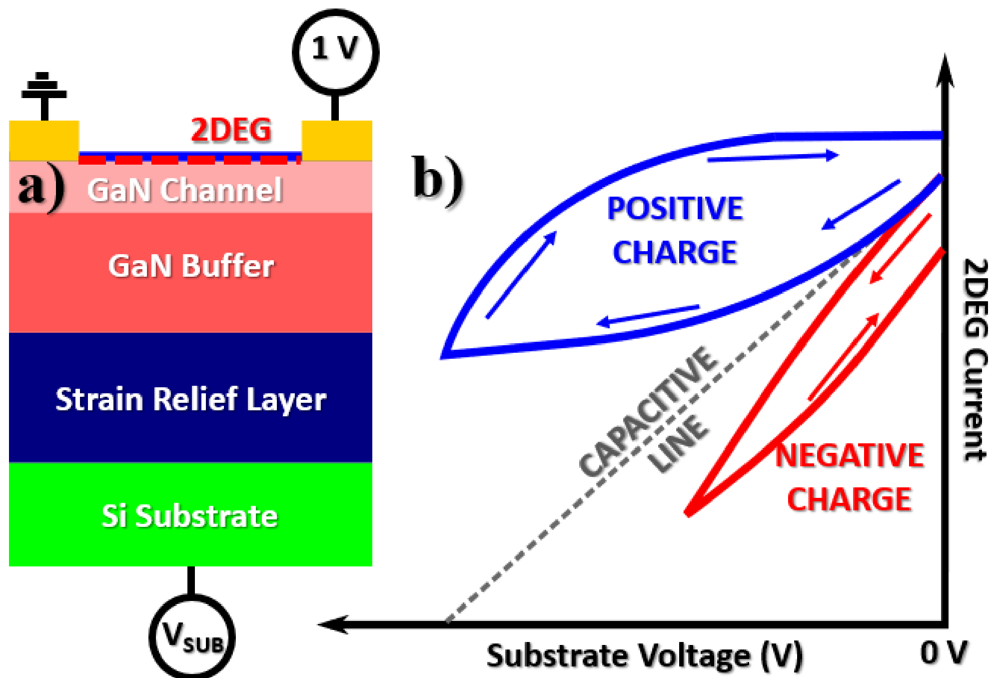

Figure 3.11: **a)** Schematic representation of substrate ramp sweep performed on a transfer length method (TLM) structure. The Ohmic contacts to the 2DEG are kept at a small potential difference, while the substrate voltage is swept from 0 V to a chosen potential and back at a constant rate. **b)** Schematic substrate ramp curves showing two possible scenarios: any response above capacitve line indicates positive charge storage in the buffer, while any response below the line suggest negative charge storage. The arrows indicate direction of the sweep.

Substrate ramp sweeps or back-biasing method is a useful tool to assess charge storage in the buffer and to monitor charge transport processes taking place in the epitaxy. Figure 3.11a shows a schematic representation of GaN-based transfer length method (TLM) structure with all the

relevant bias conditions for substrate ramp sweep measurement indicated on the plot. In this technique small potential is applied to one of the Ohmic contacts (with the other contact kept at 0 V), while the substrate is used as a back gate and is ramped at a constant rate from 0 V to a chosen negative bias point and back. The application of negative substrate potential serves to replicate electric fields present in the buffer during off-state transistor operation with large positive bias applied to the drain terminal.

Throughout the measurement 2DEG current is used as means of monitoring the electric fields in the buffer. It is important to maintain the 2DEG during the sweep, as it acts to shield the surface from the applied potential, rendering this technique especially useful for characterisation of buffers and insensitive to surface effects. The assessment of the buffer charging properties is carried out in relation to capacitive line, which describes a theoretical case in which the entire epitaxy acts as a ideal dielectric. Thus, when a potential is applied to one plate of a capacitor, charge equivalent to $q = C \times V$ is induced at the other plate. For a perfect capacitor, the capacitance per unit are can be expressed as ϵ/d where ϵ denotes permittivity of the dielectric and d is its thickness. Therefore, the position of the capacitive line is calculated from the 2DEG carrier concentration at a given potential $n_{2DEG}(V)$, assuming it is depleted with applied voltage according to the equation:

$$n_{2DEG}(V) = n_{2DEG}(V = 0) - \frac{\epsilon|V_{SUB}|}{d} \tag{3.1}$$

where V_{SUB} denotes the applied substrate potential.

In reality, the epitaxy consists of semiconductor layers and their behaviour can differ drastically from an ideal case. The ramp rate of the sweep will determine the displacement current $I_{DIS} = C_{TOT} \cdot dV_{SUB}/dt$, where C_{TOT} denotes total capacitance of the epitaxy. Once the leakage across a layer exceeds the displacement current, deviation from the ideal capacitive line is to be expected. If the 2DEG current exceeds this line, this indicates positive charge storage in the epitaxy. If however, the measured response dips below the capacitive line, negative charge accumulation in the structure is to be expected. Both of these cases are schematically shown in Fig. 3.11b.

In addition to assessing charge storage properties of the epitaxy, substrate ramp measurements can also be applied to investigate lateral and vertical leakage paths within the structure, that can have a significant impact on electrical performance of the operating device. In the absence of such leakage paths the substrate ramps should show little variation with the size of the active area or contact spacing, however some notable examples of deviations from the expected behaviour are demonstrated in [212] and [213].

3.2.3 Current Transient Measurements

Pulsed IV measurements can deliver broad and quick overview of the trapping in the buffer, while substrate ramp sweeps can provide a qualitative description of charge storage in the epitaxy. To

gain a detailed understanding about the nature of trapping present in the buffer or to observe charge transport processes taking place in the epitaxy, current transient measurements are most suitable for these purposes. The general idea behind the measurement involves application of stress voltage followed by measurement aimed at monitoring the detrapping (or in some cases trapping) processes to extract their time constants. This technique, however, can also be applied to study trapping behaviour as both trapping and detrapping dynamics can be describe by the equation:

$$\tau^{-1} = \gamma T^2 \sigma_\infty exp\left(-\frac{E_A}{k_B T}\right) \tag{3.2}$$

where τ denotes the capture (or detrapping) time constant, σ_∞ is the capture cross-section at temperature $T = \infty$, E_A stands for activation energy and γ is a constant.

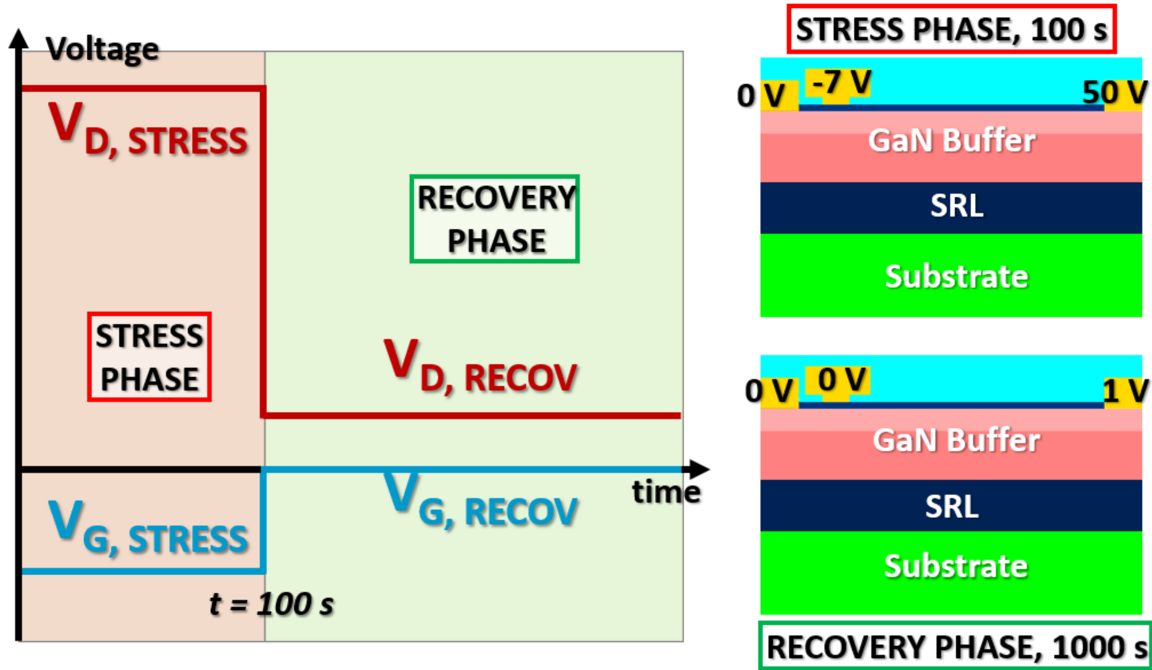

Figure 3.12: Schematic timeline of a current transient measurement where stress [$V_{D,STRESS}$ = 50 V, $V_{G,STRESS}$ = -7 V] is applied for 100 s followed by a recover phase at the bias point [$V_{D,RECOV}$ = 1 V, $V_{G,RECOV}$ = 0 V] during which drain current is measured for 1000 s.

Figure 3.12 shows a schematic timeline of a current transient measurement performed on a D-mode GaN HEMT. The stress phase involves application of Off-state stress for 100 s, followed by an On-state recovery phase which lasts 1000 s, during which the 2DEG current is monitored. In order to minimise the impact of the measurement on device recovery it is of crucial importance to apply only small bias to the electrodes (in this example V_G = 0 V and V_D = 1 V), to avoid self-heating and further trapping [214] (see Fig. 3.13a). However, it has also been proposed by Bisi *et al.* that measurements in saturation regions, as opposed to linear region, have greater sensitivity to recovery processes taking place after application of stress [143]. A comparison

between current transients measured in linear and saturation regions following off-state stress is shown in Fig. 3.13b & c. Compared to the measurement taken in linear region, the differential signal collected in saturation shows trapping states T1 and T2 much more clearly.

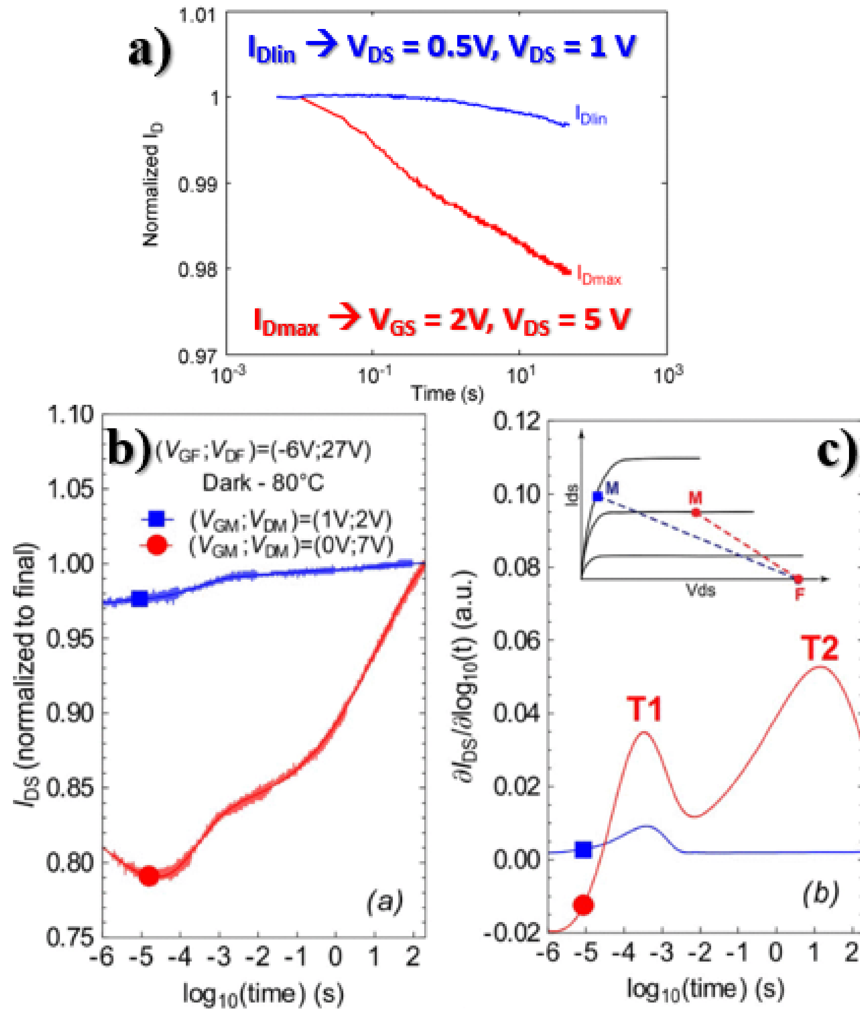

Figure 3.13: **a)** Drain current variation over time measured under applied bias in the linear region (I_{Dlin}) and in the maximum drain current region (I_{Dmax}). Figure adapted from [214] © IEEE (2011). **b)** Drain current transient after following stress [$V_{D,STRESS}$ = 27 V, $V_{G,STRESS}$ = -6 V] measured in linear region (blue) and in saturation region (red). **c)** Corresponding differential signal from current transients measure in linear (blue) and saturation regions. The inset shows relative positions along IdVd characteristics from which the transients were measured. Plots shown in a) and b) are adapted from [143] © IEEE (2013).

Figure 3.14 shows an overall outline of transient measurements and following data analysis. The data collection was performed using a combination of Keithley 2636B and (depending on the intended voltage range) Keithley 2657A instruments, which were remotely controlled using a PC via Keithley Test Scrip Builder (TSB) software (Fig. 3.14a). Figure 3.14b shows an example of current transient measured on a TLM structure. The 2DEG current was recorded during the

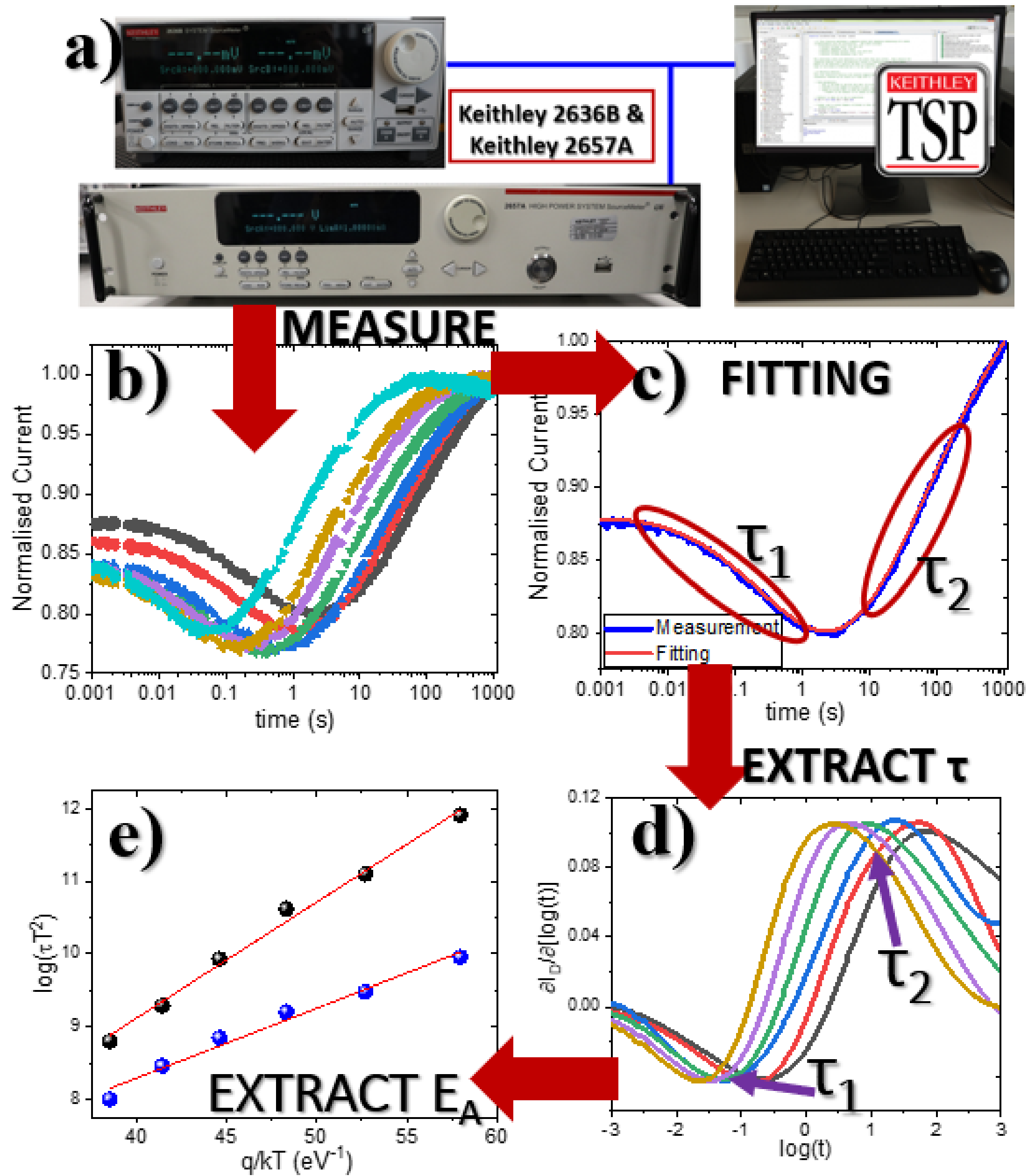

Figure 3.14: **a)** General overview of transient measurement and data analysis process. **a)** Keithley 2636B and (in some cases) Keithley 2657A instruments are controlled with Keithley Test Script Builder (TSP) software to collect the data. **b)** Example of trapping transient collected over a range of temperatures. **c)** The data is fitted using stretched multi-exponential function. **d)** The fitted curves are differentiated with respect to time to extract the time constant across the temperature range. **e)** The activation energy for investigated processes is calculated from the Arrhenius plot based on extracted time constants.

stress phase, which involved application of stress voltage of V_{STRESS} = -70 V to the substrate. The measurement is performed across a range of temperature (usually around 100 °C)

This transient shows two time constants highlighted in Fig. 3.14c. In order to extract time constants of investigated trapping (or detrapping) processes, the data needs to be fitted to eliminate the effects of noise from data analysis. The choice of the fitting method can have a significant impact on the extracted time constants and the three main methods involve:

- **polynomial fitting** - this technique uses a polynomial expression of the form

$$I_D = a_0 + x \cdot a_1 + ... + x^{n-1} a_{n-1} \quad (3.3)$$

  where n denotes the order of the polynomial function and a_i is a constant; this method works well for trapping/recovery processes involving a single time constant, however if the data contains multiple time constants or if the current follows a stretched exponential function this method is less accurate than the alternatives; an example of polynomial analysis is shown in [79];

- **multiple exponentials** - this method is based on the assumption that current transient consists of a variety of trapping and detrapping processes decaying in time exponentially; therefore transient current I_D can be described as:

$$I_D = \sum_{i=1}^{n} a_i exp\left(-\frac{x}{\tau_i}\right) + I_{fin} \quad (3.4)$$

  where a_i denotes the prexponential constant, τ_i is a predefined time constant, I_{fin} is the maximum current (fully recovered current) and n is the order of the function denoting the number of exponentials used for fitting (usually n = 100); this method is described in more detail in [214];

- **stretched multi-exponential fitting** - this fitting function treats transient current as consisting of multiple (usually between 2 and 4) stretched exponentials and can be represented as:

$$I_D = I_{fin} + \sum_{i=1}^{n} a_i exp\left(-\frac{x}{\tau_i}\right)^{\beta_i} \quad (3.5)$$

  with β denoting the nonexponetial stretching factor between 0 and 1; the value of β is of particular interest as significant deviations from unity can indicate the transient response results from superposition of multiple emission/capture processes [215] or can suggest high density of the trap states in the material [216] [168].

The stretched multiexponential fitting is the method of choice in this thesis as it shows highest degree of accuracy for fitting transient current data and especially when the processes involved are non-exponential in nature [143]. Figure 3.14c shows an example of data fitted using this function.

After the experimental data is fitted with an appropriate function, the result if differentiated with respect to log_{10} of time to find the time constants from the peaks and troughs (depending if

carrier emission or capture are investigated) of the data as shown in Fig. 3.14d. Time constants are calculated from a so-called Arrhenius plot (see 3.14e) which shows the dependence of time constant τ multiplied by the temperature squared on the inverse of thermal energy $k_B T$ according to 3.2. The activation energy E_A is calculated from the gradient of the linear function fitted to the data, whereas the intercept can provide the information about the capture cross-section σ_∞. The combination of activation energy and capture cross-section are considered the trap signature, with a list of notable examples given in [143].

3.3 Raman Spectroscopy for Temperature Measurements

Raman spectroscopy is a powerful tool to observe phonon frequencies and their shifts resulting from change in the internal and external conditions. This section outlines some key theoretical concepts behind Raman spectroscopy and describes how these ideas can be applied to temperature measurements in operating GaN-based devices.

3.3.1 Raman Scattering

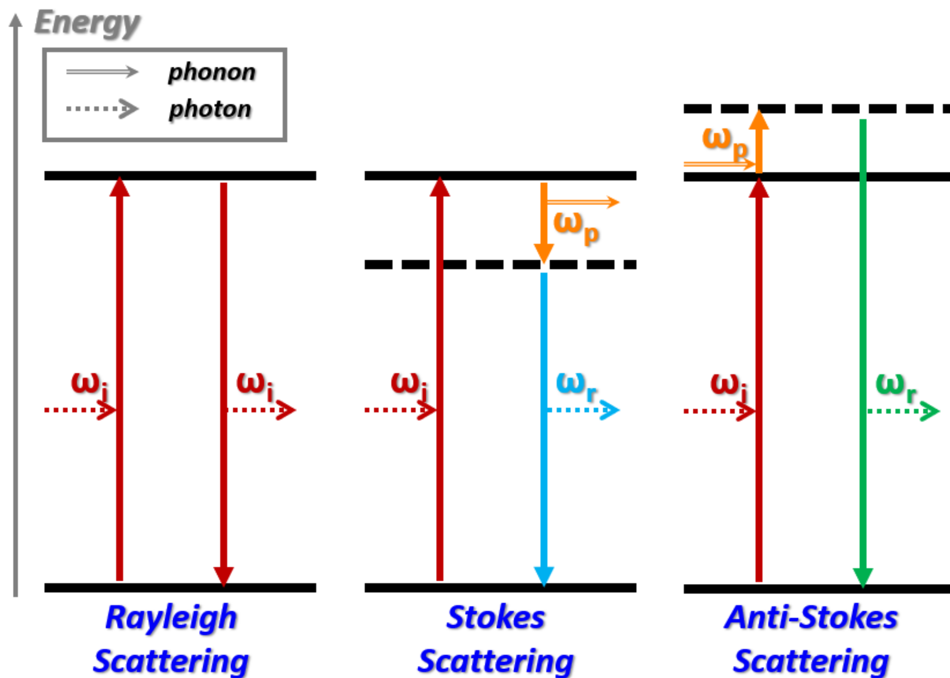

Figure 3.15: Three different modes of light interacting with matter. Elastic Rayleigh scattering releases photon with the same frequency ω_i as the incoming photon. Inelastic Raman scattering results from release of a phonon (Stokes scattering) or annihilation of an incoming phonon (anti-Stokes scattering).

Raman scattering describes inelastic scattering of light interacting with matter, where the energy from the incoming radiation is converted in molecular vibrations. When an incoming

photon with a frequency ω_i interacts with matter, an electron can be promoted to an excited state. In case of elastic scattering, the relaxation of the electron results in release of a photon with identical frequency to the original photon (ω_i) - the process known as Rayleigh scattering. However, it is also possible for the excited electron to release some of its energy in the form of lattice vibration with frequency ω_p corresponding to a normal mode of the lattice. In this case, the relaxation of the electron results in release of a photon with the frequency: $\omega_r = \omega_i - \omega_p$. Conversely, the excited electron can interact with an incoming phonon with frequency ω_p, annihilating it. In this case, the excited electron gains energy and its relaxation will release a photon $\omega_r = \omega_i + \omega_p$. The two scenarios of inelastic scattering described above are known as Stokes and anti-Stokes Raman scattering processes and are schematically shown in Fig. 3.15.

At temperatures most relevant for operating devices the intensity of signal due to Stokes scattering is significantly greater than that of anti-Stoke processes and so further discussion will revolve around the first type of Raman scattering. It is indeed possible to use the ratio of Stokes and anti-Stokes signals for device temperature measurements, however it is not a widely employed method due to long integration times required to measure the anti-Stokes signal as well as significant errors associated with such measurement especially at high temperatures [217] [218].

The Raman modes of a material can be explored by considering polarisation $\vec{P}$ induced by incident electromagnetic radiation, which can be described according to:

$$\vec{P} = \vec{E}\mathbf{R}e^{-i\omega t} \tag{3.6}$$

where $\vec{E}$ and $\mathbf{R}$ denote electric field and polarizability tensor, which can be derived based on mathematical group theory. In general, the vibrational modes that result in greater polarization will lead to greater scattering intensity and therefore can be described according to the equation:

$$I_R \propto |\vec{e_r}\mathbf{R}'\vec{e_i}|^2 \tag{3.7}$$

where $\mathbf{R}'$ denotes polarizability vector normalised to volume, while $\vec{e_i}$ and $\vec{e_r}$ describe polarisation of incoming and scattered photons respectively. For devices measured in back-scattering geometry (i.e. probe laser is incident at the right angles to the sample with scattered radiation travelling back along the same path), assuming the DUT lies in the xy plane with the incident radiation travelling along the z axis, the polarisation vectors can be described as:

$$\vec{e_i} = [cos(\theta\hat{e_{ix}}), sin\left(\theta\hat{e_{iy}}\right), 0] \tag{3.8}$$

$$\vec{e_r} = [-sin(\theta\hat{e_{rx}}), cos\left(\theta\hat{e_{ry}}\right), 0]. \tag{3.9}$$

For wurtzite crystal structure the analysis of symmetries based on group theory predicts crystallographic point group C_{6v}, which at the centre of Brillouin zone can be expressed as $2A_1 \bigoplus 2B_1 \bigoplus 2E_1 \bigoplus 2E_2$, however only $A_1 \bigoplus 2B_1 \bigoplus E_1 \bigoplus 2E_2$ (shown in Fig. 3.16) correspond to

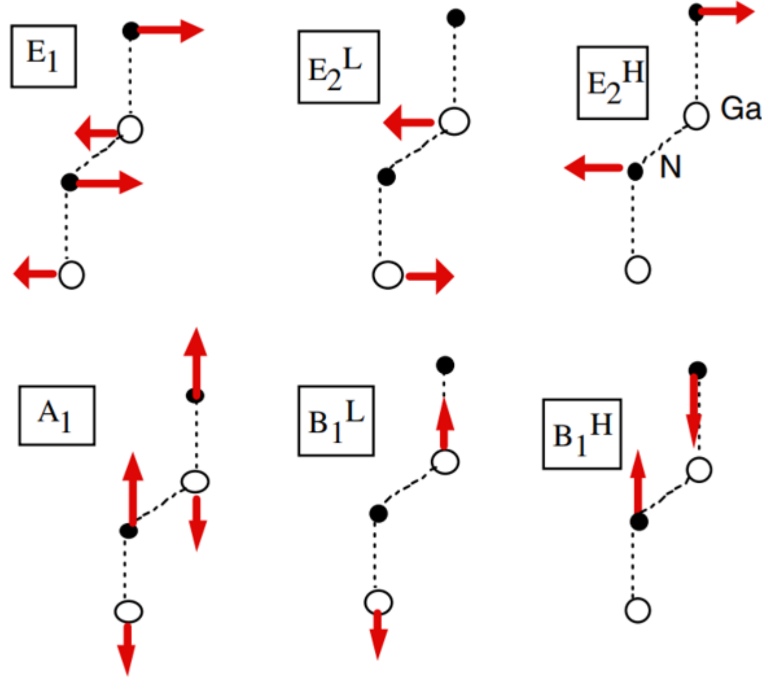

Figure 3.16: Schematic representation of optical phonon modes in GaN (wurtzite) unit cell, with nitrogen atoms marked in black and gallium in white. Superscripts H and L indicating high and low frequency vibrations respectively. The diagram has been adapted from [219]. Reprinted with permission from AIP Publishing.

optical phonons out of which only the modes A_1, E_1 and E_2 are Raman active. The normalised polarizability tensors for these modes are given by:

$$A_1 = \begin{pmatrix} k & 0 & 0 \\ 0 & k & 0 \\ 0 & 0 & k \end{pmatrix}, \quad E_2^L = \begin{pmatrix} l & 0 & 0 \\ 0 & -l & 0 \\ 0 & 0 & 0 \end{pmatrix} \quad and \quad E_2^H = \begin{pmatrix} 0 & m & 0 \\ m & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \tag{3.10}$$

where k, l and m are constants. Superscripts H and L refer to high and low frequency vibrational modes respectively, while A_1 is a longitudinal mode (LO) with vibrations propagating in the direction of wave propagation. B_1 modes are Raman inactive, as they do not result in change in polarisability of the unit cell.

3.3.2 Raman Thermography

In this work, Raman spectroscopy is used to measure device temperatures based on the shifts in A_1 (LO) and E_2 high Raman modes in GaN based micro-electronic devices, as these phonons exhibit best combination of intensity and temperature dependence in comparison to other GaN Raman active modes [220]. As the temperature of the device increases, the vibrational frequency of the phonons changes due to increased damping, strain and changes in the volume of the solid.

Therefore, phonon frequency at a given temperature $\omega(T)$ can be described as a sum of these effects according to:

$$\omega(T) = \omega_0 - \Delta\omega_d(T) - \Delta\omega_s(T) - \Delta\omega_v(T) \tag{3.11}$$

where $\Delta\omega_d(T)$, $\Delta\omega_s(T)$ and $\Delta\omega_v(T)$ denote the changes in frequency due to damping, strain and volume of the lattice respectively, while ω_0 describes harmonic phonon frequency.

Each of the contributions mentioned above has its own complex temperature dependence. The contribution due to strain can be described according to:

$$\Delta\omega_s(T) = 2\left(a - b\frac{C_{13}}{C_{33}}\right)\epsilon(T) \tag{3.12}$$

where a and b denote deformation potentials, C_{13} and C_{33} describe elastic constants, while $\epsilon(T)$ is the thermal expansion coefficient. The damping contribution to phonon frequency can be derived from the cubic and quartic terms of the Hamiltonian of lattice vibrations, which leads to:

$$\Delta\omega_d(T) \propto [1 + 2n(T, {}^{\omega_0}\!/\!_2)] \tag{3.13}$$

where $n(T,\omega)$ describes the statistical factor of Bose-Einstein distribution [221]. Finally, the $\Delta\omega_v(T)$ term depends on the thermal expansion coefficients according to:

$$\Delta\omega_v(T) = \omega_0\gamma \int_0^T \left[\alpha_c(T') + 2\alpha_a(T')\right] dT' \tag{3.14}$$

with α_a and α_c denoting linear thermal expansion coefficients perpendicular and parallel to the c-axis of the structure and γ stands for Grueneisen parameter, which describes phonon frequency dependence on volume [222].

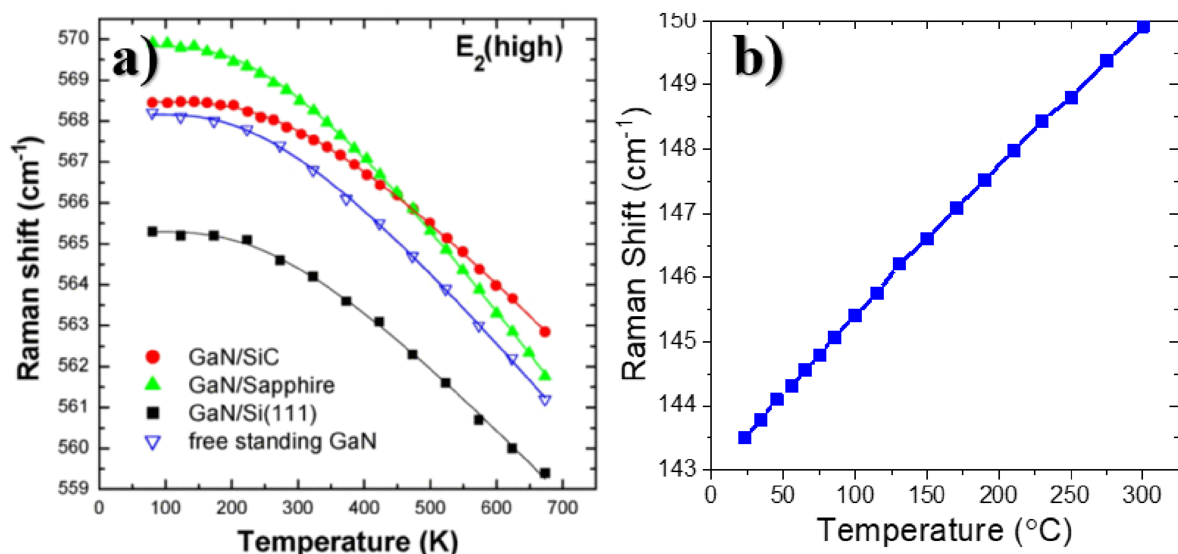

Figure 3.17: **a)** Temperature dependence of E_2 high phonon mode on temperature for GaN grown on different substrates. The figure has been adapted from [223] © IEEE (2006). **b)** Temperature dependence of a E_g Raman phonon of TiO_2 nanoparticles.

Due to complexity of the analytical solution to the temperature dependence of phonon frequency shown in the Eq.3.11, a more convenient empirical expression has been proposed by Cui *et al.*, where the Raman shift in phonon frequency with temperature can be described as:

$$\omega(T) = \omega_0 - \frac{A}{e^{Bhc\omega_0/k_B T} - 1} \tag{3.15}$$

where A, B and ω_0 are fitting parameters [224]. In the high temperature region, Eq. 3.15 can be simplified to:

$$\omega(T) = \frac{-Ak_B \Delta T}{Bhc\omega_0} \tag{3.16}$$

where ΔT denotes temperature change. Figure 3.17a shows a measurement of E_2 high phonon mode for GaN grown on different substrates [223]. Such curves would be fitted with Eq. 3.15 to extract the fitting coefficients A, B and ω_0, which will be used to calculate the GaN temperatures of operating devices.

In this work, micro-Raman thermography measurements are performed in back-scattering geometry, which involves perpendicular illumination of an AlGaN/GaN - based device with 488 nm laser, with the Raman scattered signal travelling along the same path as the laser beam as shown in Fig. 3.6. The device rests on a thermo-electric vacuum chuck maintained at 25°C. Contacting is performed with tungsten probes and the device is operated at a chosen power dissipation, while the shifts in A_1(LO) and E_2 high modes are measured. For micro-Raman measurements of HEMT, the laser beam is focused 0.5 μm away from the gate edge on the drain side in order to measure the temperatures as close as possible to the hotspot position, while avoiding light scattering from the metal contact itself.

Temperatures calculated from the shift in GaN A_1 (LO) and E_2 peaks during device operations are depth averaged across the entire thickness of GaN in the structure. In addition, despite the proximity to the main source of heating in the device this technique by itself cannot deliver values for maximum operating temperature, however it can be used to compared different structures or epitaxies [225], for temperature mapping [223], to monitor transient temperature profiles in operating devices [204] and many more.

A variation on micro-Raman thermography involves deposition of TiO_2 nanoparticles onto the device surface or on the gate. This technique is particularly useful when the access to GaN channel is restricted by metalisation or field plates. The principle behind nanoparticle assisted micro-Raman thermography is identical to conventional temperature measurement. Figure 3.17b shows temperature dependence of the E_g Raman mode measured for the TiO_2 nanoparticles. The shift of this phonon is measured during device operation and the local temperatures are calculated based on the calibration line shown in the figure. Figure 3.18a shows an example of a Raman spectrum taken for a TiO_2 nanoparticle deposited on a GaN-on-SiC HEMT. The temperatures derived using nano-Raman thermography are accurate to $\sim \pm 5$°C.

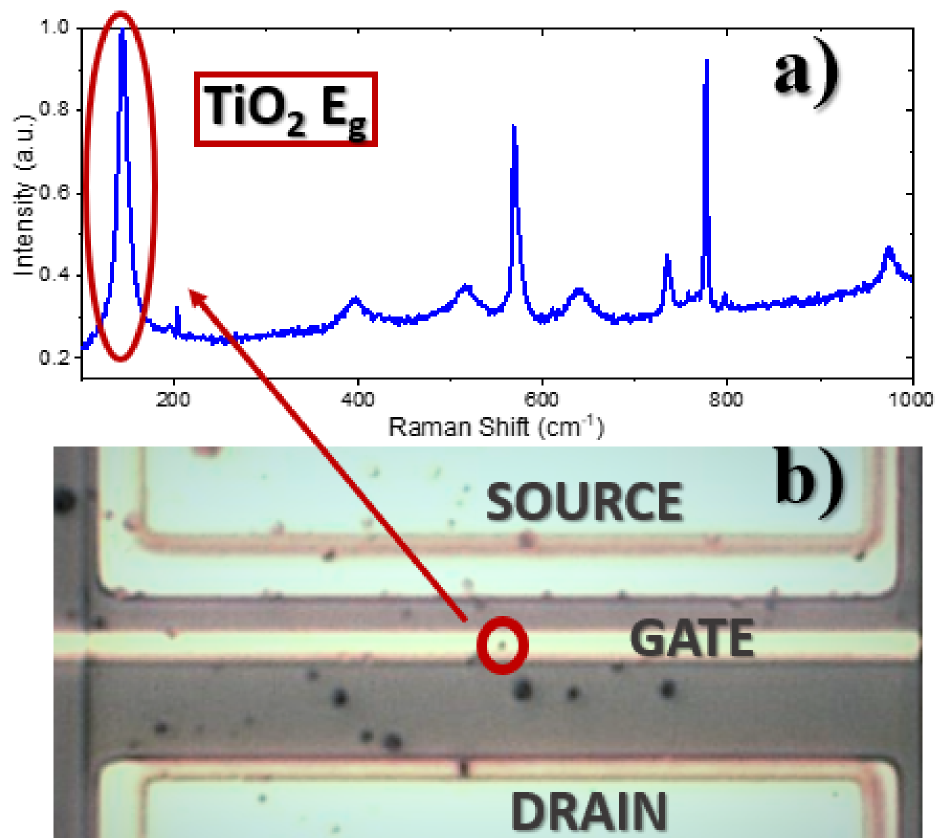

Figure 3.18: **a)** Raman spectrum of a TiO_2 nanoparticle deposited on a GaN-on-SiC HEMT. The position of the E_g Raman mode is monitored to calculate temperature profile of the operating device. **b)** Image of a nanoparticle deposited on the gate of a single finger GaN-on-SiC transistor taken with a 50× lens with optical aperture NA = 0.5.

3.3.3 Mechanical Strain Correction

Growth of AlGaN/GaN heterostructures on foreign substrates with different lattice parameters results in significant amounts of stress in the eptiaxy. During device operation, the temperature profiles across the device are not uniform, providing yet another source of strain due to different thermal expansion coefficients. In addition, application of bias voltage will lead to piezoelectric strain in the lattice. Thus in many cases, device operation results in mechanical strain present in the epitaxial layers that is not present during temperature calibration, and the total phonon shift measured experimentally can be expressed as:

$$\Delta\omega = \Delta\omega_T + \Delta\omega_\epsilon \tag{3.17}$$

where $\Delta\omega_T$ and $\Delta\omega_\epsilon$ stand for phonon frequency shift due to lattice temperature and total strain respectively. The strain generated in the experiment will affect the position of Raman active modes and can therefore result in misleading temperature calculations. In GaN and other

wurtzite materials, the phonon shift resulting from strain can be expressed as:

$$\omega_\epsilon = a\left(\epsilon_{xx} + \epsilon_{yy}\right) + b\epsilon_{zz} \pm c\sqrt{\left(\epsilon_{xx} - \epsilon_{yy}\right)^2 + 4\epsilon_{xy}^2} \quad (3.18)$$

where a, b and c are phonon deformation potentials and ϵ_{xx}, ϵ_{yy} and ϵ_{zz} are the components of strain tensor [226].

The effects of strain on Raman mode frequencies can to a good approximation be expressed by considering exclusively biaxial strain [227]:

$$\Delta\omega_{biax} = 2a'\epsilon_{xx} \quad (3.19)$$

where a' denote phonon deformation potential per unit area. In piezoelectric materials such as GaN, the application of voltage will additionally generate an internal strain ϵ_{zz} due to inverse piezoelectric effect, which can be expressed as:

$$\epsilon_{zz} = \left(d_{33} - \frac{2S_{13}}{S_{11} + S_{12}} d_{31}\right) E_z = \frac{\omega_{piezo}}{b}, \quad (3.20)$$

where d_{33}, d_{31} denote piezoelectric modulus components, S_{11}, S_{12}, S_{13} are the components of elastic compliance tensor and E_z denotes the component of electric field in the vertical direction, assuming $\epsilon_{xx} = \epsilon_{yy}$ [228]. The strain resulting from the inverse piezoelectric effect is highest under the drain due to high vertical electric fields present in this region. To account for this strain component, temperatures derived from micro-Raman thermography measurements of operating devices are calculated relative to the measurement of the device in the Off state, as the electric field distribution under the drain is very similar in both cases. This approach is also valid when attempting to account for any other form of strain resulting from applied electric field [229].

In practical term, in order to factor in the effects of thermomechanical strain present in an investigated sample, it is necessary to separate the temperature and strain contributions as expressed in Eq. 3.24. This can be achieved by considering temperature and stress dependence of each individual phonon mode measured. The temperature dependence of GaN A_1(LO) peak is almost three times stronger than that of the E_2 high mode, however it is the latter that shows more significant dependence on strain present in the GaN layers [217]. By combining Eq. 3.24 with Cui equation 3.15, the total frequency shift of a phonon $\Delta\omega$ can be expressed as:

$$\Delta\omega = \Delta\omega_0 - \frac{A}{exp\left({}^{B\hbar\omega_0}\!/\!_{k_B T}\right) - 1} + 2a\epsilon_{xx}. \quad (3.21)$$

The phonon deformation potential a is used to find the biaxial stress coefficient $d\omega/d\sigma$, where σ denotes thermomechanical stress in the device. The deformation potentials for GaN A_1 and E_2 phonon modes are 1.91 cm^{-1}/GPa and 2.41 cm^{-1}/GPa respectively [226]. By considering the first term of Taylor expansion of Eq. 3.21, the effects of thermomechanical strain on the temperatures derived from A_1 or E_2 phonons can be described as:

$$T_M = T_{act} + \Delta\sigma \frac{d\sigma}{dT_M} \quad (3.22)$$

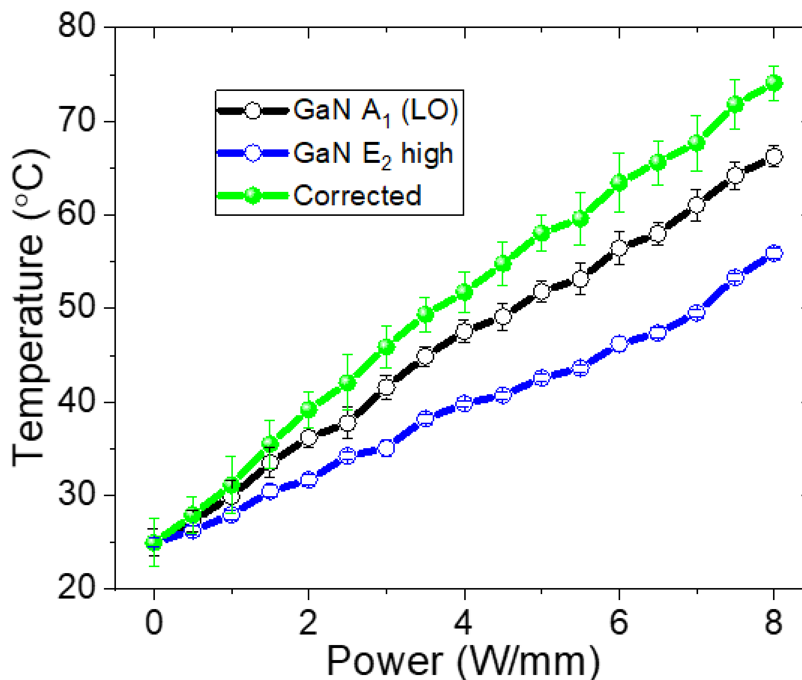

Figure 3.19: Temperature as a function of power dissipation for a GaN-on-SiC HEMT as derived from GaN A_1 (black) and E_2 (blue) Raman modes compared to results corrected for thermomechanical strain (green).

where T_M denote temperatures measured from A_1 or E_2 peak and T_{act} is the actual "unknown" temperature. The $\frac{d\sigma}{dT_M}$ term is obtained by combining the deformation potential with the $d\omega/dT$ term, which can be calculated from the slope of the calibration function. By applying equation 3.22 to A_1 and E_2 peaks, the strain – corrected channel temperature can be expressed as:

$$T_{act} = T_{A1} + \frac{T_{E2} - T_{A1}}{\frac{\frac{d\sigma}{dT_{E2}}}{\frac{d\sigma}{dT_{A1}}} - 1}. \tag{3.23}$$

In most devices it is very important to correct for thermomechanical stress, as failure to do so will result in significant discrepancy in temperatures derived from shifts in different Raman modes. Figure 3.19 shows an example of temperatures derived from shifts in GaN A_1 (LO) and E_2 high Raman modes compared to temperatures calculated using strain correction formula. Due to sensitivity of the E_2 peak to strain, there is a significant discrepancy between temperatures derived from this mode as compared to A_1 phonon. However, as the frequency of A_1 mode is less sensitive to strain, this peak alone can be used as a reasonable approximation of device temperature in cases where it is not possible to perform the correction analysis. The discrepancy between temperatures derived from the Raman shifts of A_1 (LO) and E_2 peaks depends on the strain present in the operating device, thus both modes should give similar temperatures for devices experiencing little stress.

3.4 Computational Simulations

This section outlines the main computational tools and methods applied for simulations of GaN-based power and RF devices. To aid electrical analysis of investigated devices Silvaco Atlas TCAD software was used. Meanwhile, thermal analyses and parameter optimization studies have been performed using Ansys 3D Finite Element Analysis software.

3.4.1 Electrical 2D TCAD Simulations

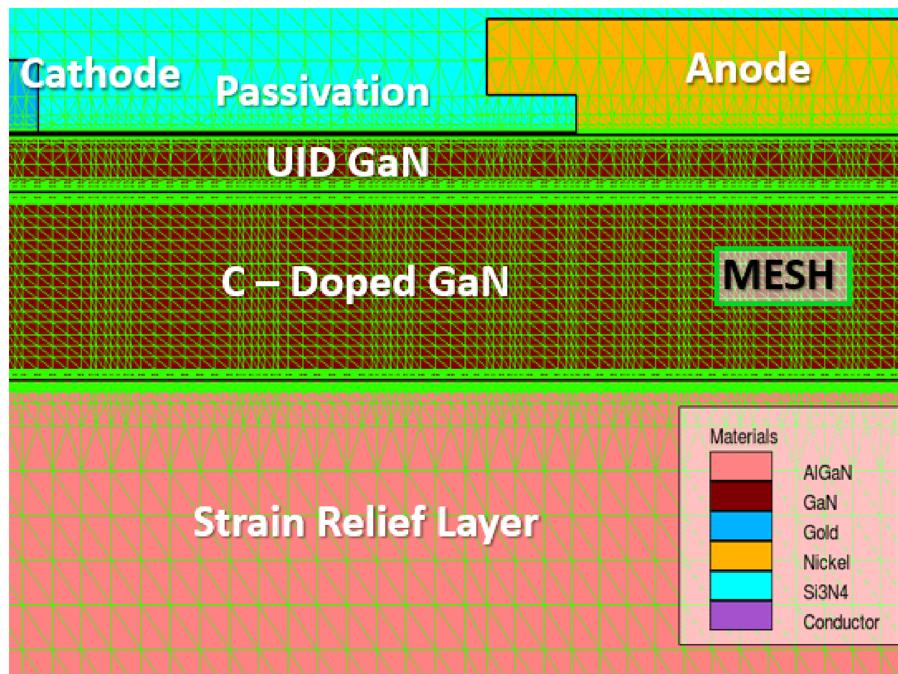

Figure 3.20: A section of a GaN-on-Si Schottky barrier diode simulated in Silvaco Atlas, with mesh displayed over the structure. All the relevant equations are solved for the nodes of the shown mesh. Mesh density increases significantly in the vicinity of the 2DEG and other relevant interfaces.

In order to gain a better understanding of electrical performance of investigated micro-electronic devices most experimental measurements were combined with computational simulations. Electrical simulations presented in this thesis have been performed using Silvaco Atlas Technology Computer-Aided Design (TCAD) Software, which was designed specifically for electrical simulations of semiconductor devices and contains a wide range of models specific to GaN-based electronics.

The process of creating a model begins in the programme called *DevEdit*, where 2D device cross-sections of investigated devices are created and meshed by creating triangluar connections between individual points. Meshing is one of the most important steps in the entire simulation process as the mathematical calculations are performed at the nodes created by the mesh. Thus,

due care must be taken when specifying mesh dimensions, especially when considering corners and regions where high electric fields are present. Figure 3.21 shows an example of a meshed structure, with particularly high mesh density at the 2DEG and other interfaces. Failure to create appropriate mesh can result in convergence issues and simulations not completing. In some cases, poorly meshed structures can still be simulated, however the results obtained from such simulations can bear large error, e.g. lowered 2DEG density or artificially reduce electric fields. However, as the mesh density increases so does the time taken by the simulator to calculate the results. Therefore, meshing needs to be done in a way that incorporates high density regions for accurate simulation results but also contains regions of thin meshing to increase computational efficiency of the model. DevEdit contains an extensive library of standard materials, each of which comes with associated physical properties such as bandgaps, carrier mobilities, affinities and more. These properties do not need to be specified at any point during the simulation process, but they can be altered at later stages.

Simulations are handled by the programme called *Deckbuild*. Here, the complete structure can be uploaded and selected physical models can be activated for all or selected device regions. Similar to meshing, the choice of physical models is of tremendous importance to simulation results, however inclusion of excessive number of physical models will significantly increase the simulation time and can lead to convergence issues. The addition of doping (or trapping) can also be included at this stage. This can be achieved by specifying the region and corresponding dopant density, capture cross-section, degeneracy and energy level (which is specified in relation to valence band or conduction band for donors and acceptors respectively). Polarization charges can be implemented manually at appropriate interfaces or calculated by the simulator by including appropriate polarization models.

The simulations are performed by specifying the experimental conditions in Deckbuild: for static simulations this includes designating bias conditions (or currents) to appropriate electrodes, while transient measurements also requiring specification of time-dependence parameters such as rise time, ramp rate etc. In its basic operation the simulator self-consistently solves the Poisson equation, current continuity and transport equations, which together combine into drift-diffusion equations describing current densities and movement of charges under applied electric field, according to the expression:

$$J_{n,p} = q\rho_{n,p}\mu_{n,p}E_{n,p} + qD_{n,p}\nabla\rho_{n,p} \tag{3.24}$$

where J, ρ, μ, E and D denote current density, carrier density, carrier mobility, effective electric field and the diffusion coefficient respectively. The subscripts n and p indicate this quantity can refer to either electrons or holes. Drift - diffusion equation, together with any other models specified in the input file are solved at each node of the mesh.

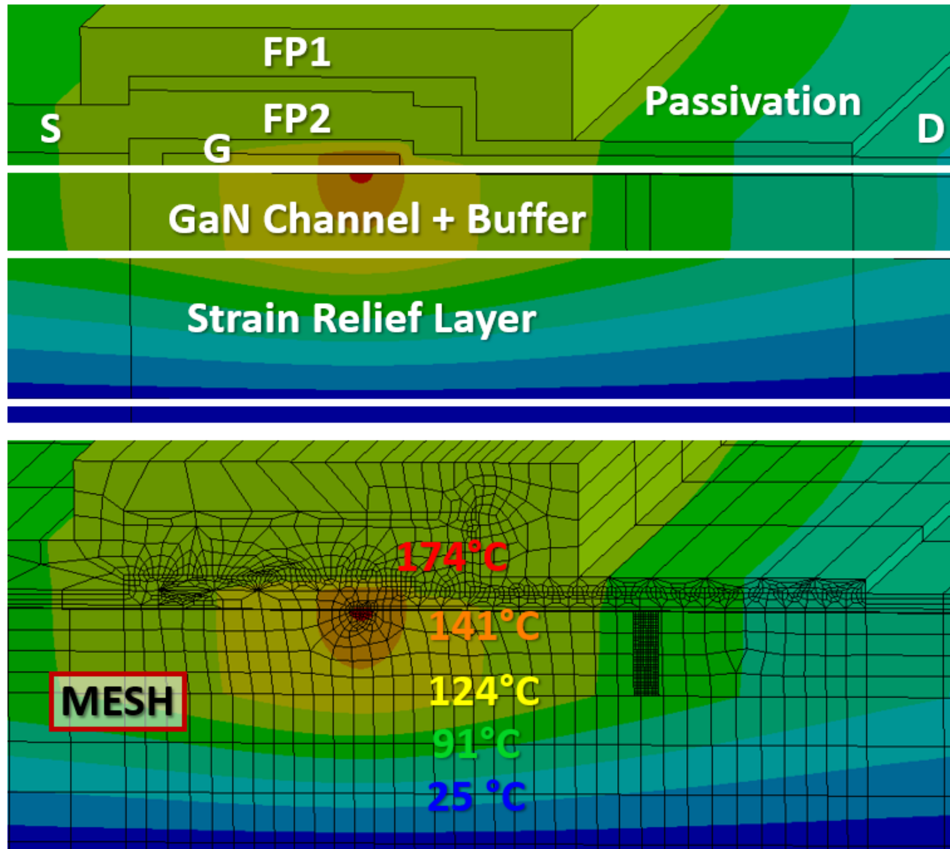

Figure 3.21: Temperature distribution of GaN-on-Si HEMT simulated in Ansys and corresponding mesh. Higher mesh density is required in the regions of high temperature flux (mainly near the hot spot at the gate edge).

3.4.2 Thermal 3D FEA Simulations

To gain a better understanding of thermal performance of GaN-based electronic devices Ansys finite element analysis (FEA) multiphysics engineering simulation software is employed. Just like in case of electrical simulations, the general idea behind Ansys simulations involves discretising a geometry by means of meshing, where finite elements of the body are connected at the nodes of the mesh. Relevant physical models and equations are solved at the nodes and the results are interpolated within the elements either linearly or using a higher order approximation. When deciding on the order of interpolation the accuracy and computational power need to be considered: the former will suffer for lower order approximations, while the latter will increase significantly as higher order interpolation is used. To achieve the right balance, some areas experiencing the largest temperature gradients and energy flux include very fine mesh, while in the remaining areas the mesh will be more relaxed. Figure 3.21 shows an example of a meshed GaN-on-Si HEMT with the corresponding temperature profile.

In this thesis Ansys was employed to perform steady-state thermal analysis, which calculates heat flow and temperature profiles for a 3D body. For solid where heat is generated in one area of

the body, the first law of thermodynamics can be expressed as (assuming conservation of mass):

$$\rho c\left(\frac{\partial T}{\partial t}+\vec{v}\nabla T\right)+\nabla\vec{q}=U \tag{3.25}$$

where ρ, c, T, $\vec{v}$, $\vec{q}$ and U denote mass density, specific heat, temperature, heat velocity, heat flux and rate of heat generation respectively. By combining Eq. 3.25 with the expression for heat transfer according to Fourier's law:

$$\vec{q}=-\kappa\nabla T \tag{3.26}$$

where κ denotes thermal conductivity matrix to account for anisotropic behaviour, the followig equation is solved by Ansys to calculate heat flux at the nodes of the mesh:

$$\rho c\left(\frac{\partial T}{\partial t}+\vec{v}\nabla T\right)=\nabla(\kappa\nabla T)+U. \tag{3.27}$$

Eq. 3.27 requires specification of material densities, specific heats and thermal conductivities, however for steady-state thermal simulations the above expression is effectively reduced to Fourier's law shown in Eq. 3.26, thus requiring only the thermal conductivity matrix.

The creation of the model takes place is SpaceClaim computer-aided design (CAD) programme, which is followed by assignment of materials to all the layers and meshing. Ansys contains extensive material libraries, however the software allows for modification of existing materials and creation of new entries. Once the model is complete, the boundary conditions are established and energy input is assigned either to points, lines, surfaces or volumes. For a typical HEMT simulation, initially the device temperature is set to 25°C and the bottom of the HEMT is fixed at this temperature for the duration of the experiment (this is known as Dirchlet boundary condition). Heat generation is assigned to a small body with the approximate dimensions 10nm × 400 nm position at the drain-side gate edge to simulate heat generation during device operation. The temperature profiles and heat flux are calculated as describe above across a range of power dissipations according to the value used in the actual experiment.

Chapter 4

Low-Field Vertical Charge Transport Processes in GaN Channel and Buffer Layers

This chapter presents an investigation of vertical charge transport processes taking place in the UID GaN channel and the C – doped (GaN:C) buffer in the low-filed regime, and is based on experimental measurements of TLM structures and TCAD simulations. Substrate ramps were used to determine the main voltage points at which dominant vertical charge transport processes can be singled out and studied individually. These points were subsequently used to perform substrate stress transient measurements, which show two distinct transient behaviours: negative going (decreasing) transient with the activation energy E_A = 0.28 eV and a positive going (increasing) transient with E_A = 0.38 eV. Temperature and field dependence of the time constants of each transient reveal 1D hopping along dislocations is responsible for transport across the UID GaN channel, while charge redistribution across the GaN:C buffer takes place via 3D variable range hopping. Current transients obtained from bidirectional voltage steps of the magnitude of 10 V between 0 and -140 V show transport via the dislocations exhibit non-Ohmic behaviour especially at low substrate biases. We therefore propose an existence of previously unobserved diode junction between the dislocation core and the 2DEG.

The structures used in this study were grown and processed by Interuniversity Micro-Electronics Centre (imec). All the experimental work and simulations were performed by the author. This chapter contains significant portions of the article published in IEEE Electron Device Letters [230]. Some figures have been reproduced with permission from IEEE.

4.1 Introduction

Currently, one of the major issues affecting the operation of GaN power HEMTs is the dynamic R_{ON}, which can be defined as a temporary increase in On-resistance of the device caused by the Off-state stress. At present, surface trapping can be effectively managed by optimized passivation and carefully engineered field plates [173][170], however the effects of buffer trapping on the output characteristics of GaN power HEMTs have been widely observed and demonstrated in the literature [174][231][232]. The issue of dynamic R_{ON} still remains one of the main challenges for realisation of highly efficient power GaN devices.

Uren *et al.* have demonstrated that the variation observed between devices with similar epitaxial structures and doping profiles can be explained in terms of the availability of vertical leakage paths between the C – doped buffer and the 2DEG [92]. Application of large Off state drain bias results in the formation of reverse biased pn – junction between the channel and the buffer. In this case, the floating GaN:C buffer will act as a back-gate and its effects can only be managed by providing an electrical connection between the buffer and the 2DEG.

Previous work on GaN vertical pn – diodes and LEDs has demonstrated that the vertical leakage can be associated with screw dislocations [233][154]. In addition, experimental measurements and simulations of vertical GaN power pn – diodes indicate the charge transport via dislocations is consistent with hopping conduction [234]. Although dislocation can have an adverse effect on electrical performance of GaN-based devices, their presence can also provide an electrical connection to otherwise floating C-doped GaN buffer resulting in reduction in phenomena such as dynamic R_{ON} [92].

In case of C – doped GaN buffer, charge transport across this layer is most often described in terms of activation of holes from the carbon acceptor (C_N) into the valence band. The activation energy for this process has been predicted theoretically as well as measured experimentally as 0.9 eV [86][87]. However, the apparent activation energy of carbon strongly dependes on the dopant concentration, as demonstrated by Koller *et al.* in their work on GaN pn-junctions with C as the acceptor in the p-layer. By investigating the charging and discharging properties of the p-type GaN layer at carbon concentrations between 10^{17} cm^{-3} to 2×10^{19} cm^{-3}, they have demonstrated the apparent activation energy becomes temperature dependent and can vary between 0.05 and 0.8 eV. It has been proposed, that charge transport across GaN:C layer takes place via a defect band (DB) [30].

This aim of this work is to investigate vertical charge transport processes in the UID GaN channel and the C – doped GaN buffer in the low field regime most relevant to the dynamic R_{ON}. The measurements are performed on the state-of-the-art 200 mm GaN-on-Si HEMT epitaxial stack rated for 200 V provided by imec. We propose a new method for investigation of vertical charge transport processes in the GaN layers and show that charge redistribution across GaN:C is consistent with 3D variable range hopping in the DB, while transport across UID GaN takes place via 1D hopping along the dislocation cores. The non-Ohmic characteristics of the 1D hopping

process at low voltages is explained by the presence of previously unrecognised diode junction between the dislocation core and the 2DEG.

4.2 Experimental Details

4.2.1 Sample Description

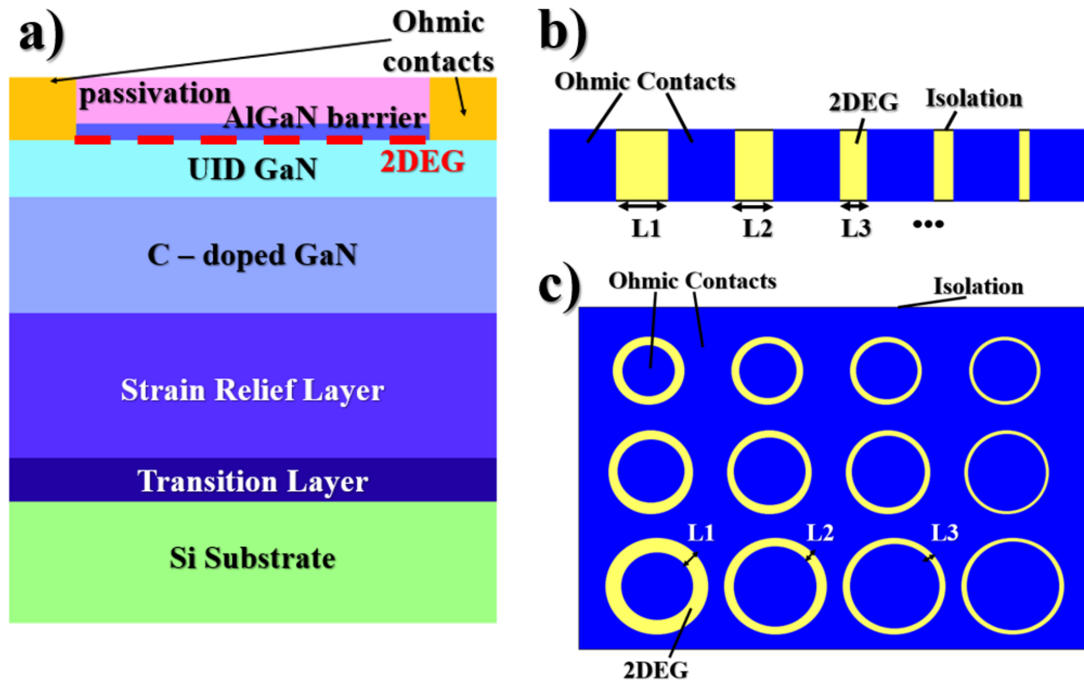

Figure 4.1: **a)** Schematic diagram of the epitaxial structure investigated in this study. **b)** Schematic representation of a transfer length model (TLM) structure with decreasing contact spacing L1 > L2 > ... **c)** Schematic representation of a circular transfer length model (cTLM) structure with decreasing contact spacing L1 > L2 > L3.

This work has been performed on a typical AlGaN/GaN-on-Si HEMT epitaxy optimised for power applications up to 200 V. The epitaxial stack was grown by metal organic chemical vapour deposition (MOCVD) method on a conductive p-type silicon substrate with resistivity > Ω·cm. The structure consists of AlN and AlGaN transition layers followed by AlN/AlGaN superlattice strain relief layer (SRL). Total thickness of the transition layer and the strain relief layer is 1.9 μm. 1 μm of C – doped GaN buffer was grown on top of the SRL with the C concentration of 2×10^{19} cm^{-3} measured by secondary ion mass spectroscopy (SIMS). The unintentionally doped GaN channel of the thickness of 0.3 μm and 13 nm of $Al_{0.27}Ga_{0.73}N$ barrier were grown over the buffer to form the 2DEG. Al_2O_3 and SiO_2 were used to passivate the epitaxy. The sheet resistance of the 2DEG was measured to be 550 Ω/sq. The Ohmic contacts were fabricated using low temperature method as described by Firrincieli *et al.* [235] which involves full recess of AlGaN barrier before the deposition of the Ti/Al/TiN stack with the Ti to Al ratio of 0.05. The contacts were annealed

at 550°C and the contact resistance was measured as 0.6 Ω·cm. Figure 4.1a shows a schematic representation of the sample structure. The structures were isolated using nitrogen implantation method. The maximum energy of the ions was 375 keV corresponding to maximum implantation depth of 550 nm.

In this study all the experiments were performed on the transfer length model (TLM) structures, which consist of a series Ohmic contacts with the width of 100 μm deposited along the active area. The spacing between adjacent contacts varies from 1 to 18 μm (see Fig. 4.1b). In addition, circular transfer length model (cTLM) structures were also measured (see Fig. 4.1c). These structures were fabricated on an active area with the dimensions 1200 × 1600 μm with the contact diameter of 100 μm. The contact spacing of cTLM structures varies from 1 to 18 μm.

4.2.2 Experimental Method

Bidirectional substrate ramp sweeps were performed on TLM and cTLM structures across the wafer using Keithley 2636B to assess uniformity of the samples. This technique is performed by applying small potential difference of 0 and 0.5 V to the Ohmic contact while gradually sweeping the substrate up to -200 V and back at a constant rate of 1 V/s. The polarity of the field inducted in the buffer by applying negative substrate stress is equivalent to drain stress, while remaining insensitive to surface effects.

To investigate potential leakage paths under the contacts [91] TLMs with contact length from 2 μm to 100 μm were measured. In addition, the effects of contact spacing between 1 to 18 μm on the substrate ramp characteristics were investigated. Finally, substrate ramps were measured for TLMs and cTLMs with different size of active areas in order to rule out (or otherwise) the presence of 2D hole gas (2DHG) present in the epitaxy [213].

Subsequently, substrate stress transient measurements were performed on TLM structures with the contact dimensions 100 × 100 μm and contact spacing of 8 μm. This measurement is a variation on classic current transient measurement. Here, small potential difference of 0.5 V is applied to the electrodes in order to monitor the 2DEG current, while the substrate is rapidly (10s of μs) switch from 0 V to a chosen negative bias point. The measurement timeline is shown in Figure 4.2a.

In addition, stepped substrate stress transient measurements were performed on the TLM structures. This measurement involves biasing the substrate for 1000 s at a chosen initial bias (V_{SUB} = V_i), which is followed by a rapid switch to the final bias point V_{SUB} = V_f for further 1000 s. The 2DEG current is measured for the duration of V_f bias point to investigate the change in the electric field in the buffer between the two chosen bias points V_i and V_f. The measurement timeline is shown in Figure 4.2b.

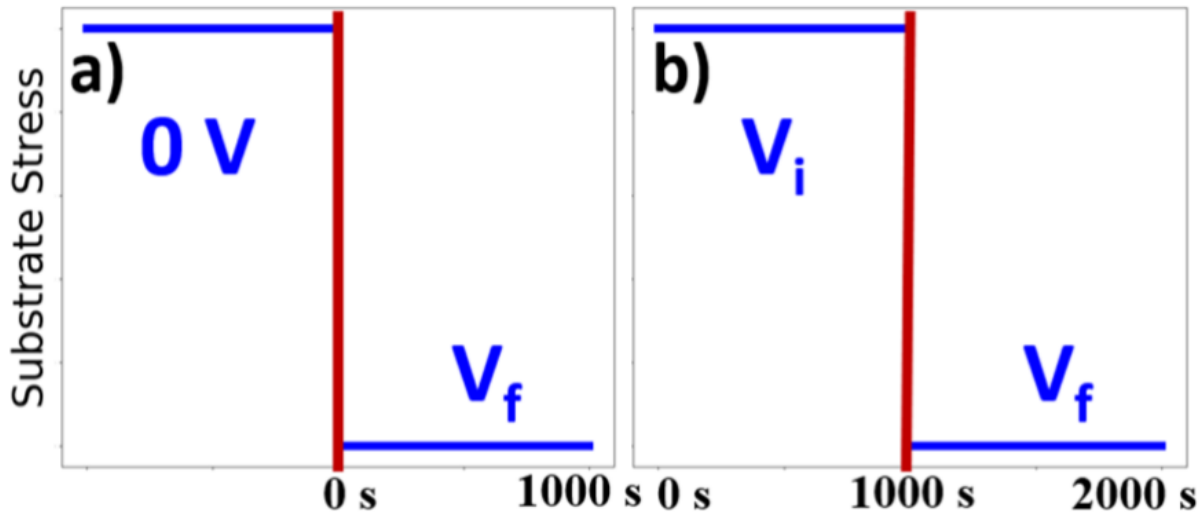

Figure 4.2: **a)**Schematic representation of the measurement timeline of the substrate stress transient measurement, where substrate voltage is rapidly switched to the stress point (V_f) for 1000 s. **b)** Schematic representation of the stepped substrate stress transient measurement, where the device is biased at the initial stress voltage (V_i) for 1000 s before the substreate stress is rapidly switched to the final bias point (V_f) for another 1000 s at during which time the measurement is performed.

4.3 Results

Substrate ramps were performed on TLM structures at different locations on the sample showing uniform behaviour across the wafer with little device to device variation. Likewise, no significant variation with contact spacing or contact area has been observed indicating a uniform conductivity across the entire length of the channel as described in [90]. This result also suggests there are no significant leakage paths under the contacts, which would manifest itself by negative correlation between contact spacing and magnitude of the normalised 2DEG current during the sweep. Similarly, active area of the device had a little effect on substrate ramp characteristics, suggesting there are no significant internal lateral leakage paths associated with 2DHGs and 2DEGs at heterojunctions. Therefore, the absence of lateral conduction channel in the expitaxy implies the transport across the epitaxy can be approximated as 1D (purely vertical).

Figure 4.3 shows a bidirectional substrate ramp sweep measured for a TLM structure with the contact spacing of 8 μm and contact dimensions 100 × 100 μm at the rate of 1 V/s. The grey dashed line indicates and ideal capacitive response of the epitaxial stack (i.e. each layer acting as a perfect dielectric) and can be used as an indicator of charge storage in the buffer. Any response below the capacitive line suggests negative charge storage in the buffer, while any response above the line indicates positive charge storage. This technique is described in more detail in Chapter 3. The areas of positive and negative charge storage have been marked out in Fig. 4.3. Substrate stress transient measurements were performed at bias point V_1 = -10 V, V_2 = -70 V and V_3 = -140 V. These points correspond to negative charging (V_1), positive charging of the buffer (V_3) and an

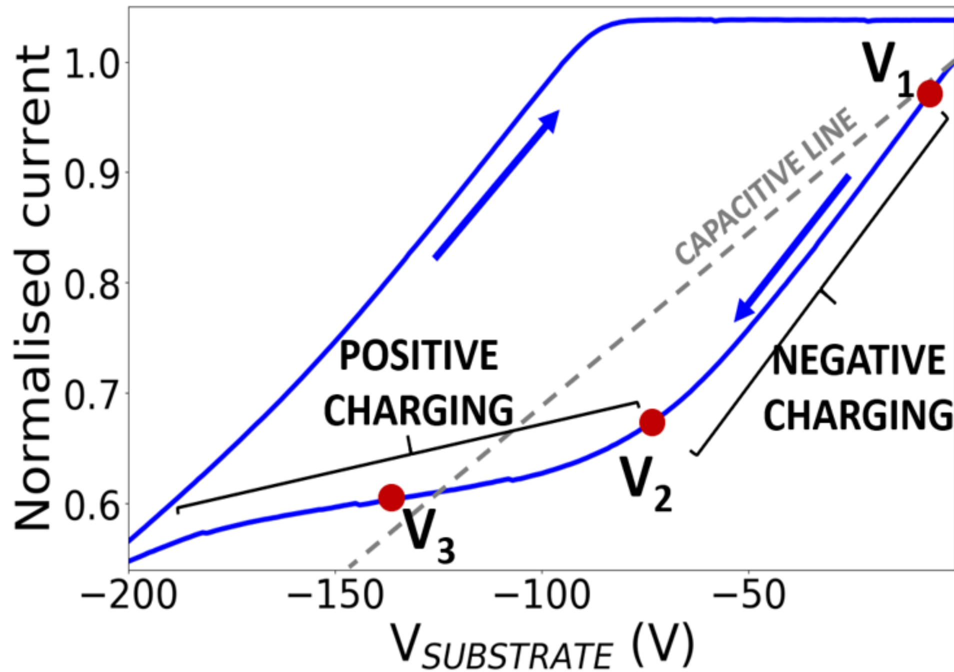

Figure 4.3: Bidirectional substrate ramp measurement performed on a TLM structure with contact dimensions 100 × 100 μm and contact spacing of 8 μm at the ramp rate of 1 V/s (arrows indicate the direction of voltage sweep). Capacitive line indicates ideal dielectric behaviour of the stack. The regions of positive and negative charging are indicated on the plot, with point V_1, V_2 and V_3 marking out the main points of positive and negative charging taking place in the epitaxy.

intermediate point between the two regions (V_2).

Figure 4.4 shows a substrate stress transient measurement performed over a range of temperatures between 30°C to 120°C for the bias point V_{SUB} = V_2. The measurement shows two distinct regimes: τ_1 which can be described as a negative going (decreasing) transient and τ_2 – characterised by a positive going (increasing) transient. The activation energies for each regime have been calculated from an Arrhenius plot as 0.29 eV for τ_1 and 0.38 eV for τ_2. As transient measurements are performed closer to the bias point V_1, the process τ_1 becomes more prominent while τ_2 diminishes. Conversely, the measurements performed closer to the bias point V_3 show significant increase in magnitude of the process τ_2 accompanied by reduction in magnitude of τ_1.

Figure 4.5 shows the data from stepped substrate stress transient measurements for a range of bias points (V_i, V_f) with the potential difference of 10 V. The time constant for the process τ_1 show very little variation with the applied electric field, whereas a significant shift in the time constant τ_2 can be observed as the applied substrate potential is increased. The results therefore indicate the process τ_2 is characterised by much stronger dependence on applied field compared to process τ_1.

Figure 4.6a shows the substrate stress transients for bidirectional voltage steps, where the transients are first performed by stepping the voltage up from V_i to V_f and vice versa (τ_1’ and τ_2’

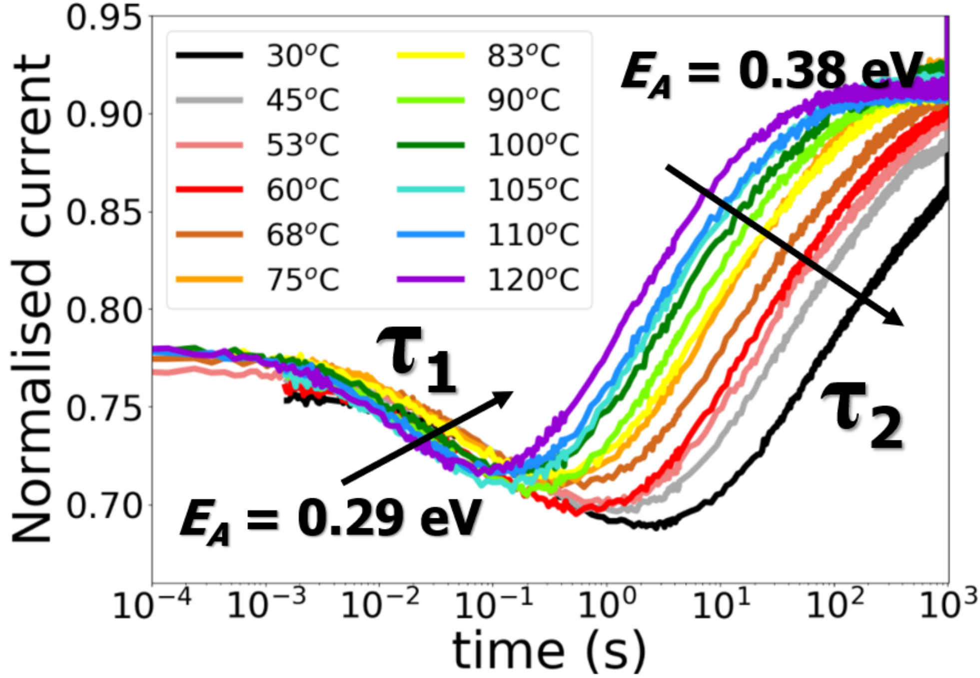

Figure 4.4: Substrate stress transient measurement performed following bias step V_i = 0 V → V_f = V_2 between 30°C and 120°C. Negative going (decreasing) and positive going (increasing) transients are labelled τ_1 and τ_2 respectively with corresponding activation energies (data captured at V_{SUB} = V_2).

indicate the time constants of the reverse steps). The transient response of the process τ_1 shows high degree of symmetry between the forward and reverse bias steps (i.e. the ratio τ_1'/τ_1 1). On the other hand, the process τ_2 is shows highly asymmetric characteristics between forward and reverse voltage steps, which become increasingly symmetric with applied substrate voltage as shown in Fig. 4.6b (i.e. τ_2'/τ_2 tends to unity).

The temperature and field dependence of the processes τ_1 and τ_2 have been measured in the range 200 – 450 K for substrate stress $|V_{SUB}|$ between 10 and 140 V. These are shown in Figures 4.7 and 4.8 for τ_1 and τ_2 respectively. The voltage dependence of τ_1 and τ_2 can be approximated as $\tau^{-1} \propto \log(V_{SUB})$ for the entire range of τ_1 (Fig 4.7b) and most of the range of τ_2 (Fig. 4.8b). Process τ_1 shows weak dependence on the applied filed, as the time constant shifts by only one decade over 100 V of applied potential (see Fig. 4.7b). In contrast, the time constant for process τ_2 spans over two decades across the 100 V of applied substrate voltage (see Fig. 4.8b).

4.4 Discussion

The measurements of TLM structures with variable contact spacing and active area suggest charge transport in the epitaxy can be approximated as 1D. Figure 4.9 shows an equivalent 1D lump element diagram of the epitaxial structure. The substrate ramp shown in Figure 4.3 can be

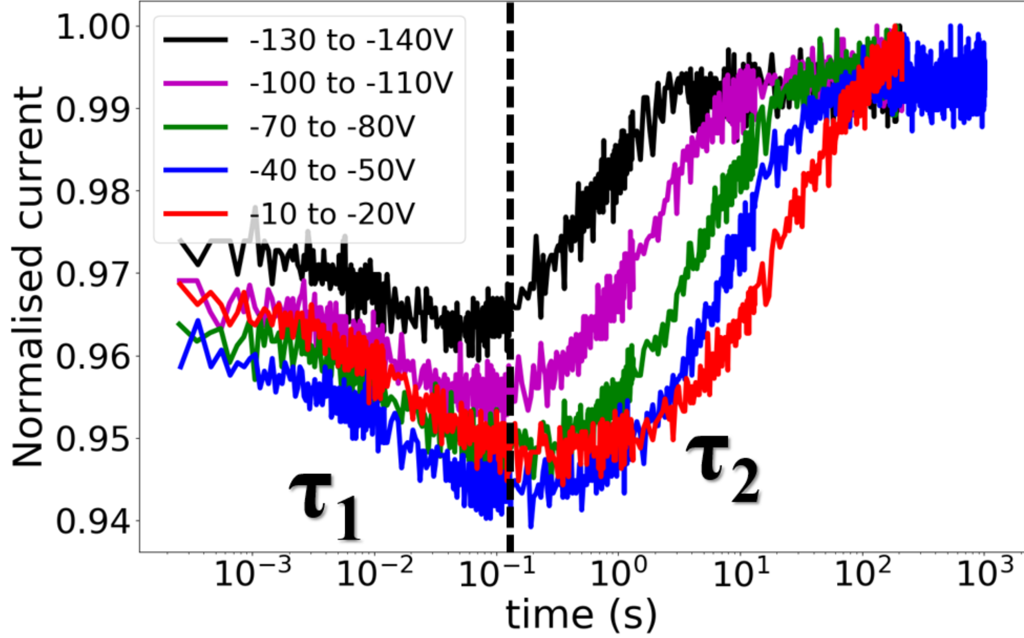

Figure 4.5: Forward stepped substrate stress transient measurements of the potential difference V_f - V_i = 10 V between -10 to -140 V. The positive and negative going transients τ_1 and τ_2 are indicated on the plot.

explain with the aid of 1D model by considering only the vertical movement of charges in the epitaxy.

In a 1D model the resistance and capacitance per unit area can be described as $R = \rho \times \epsilon$ and $C = \epsilon/d$, where ρ, d and ϵ denote resistivity, thickness and permittivity of a given layer. Thus, the time constant time constant τ for a vertical charge transport process across a given layer is given by τ = RC = $\rho \times \epsilon$, implying these processes depend on the resistivity of the layer and not on its thickness. If we consider each layer of the expitaxy as a dielectric material, then charges will accumulate at the interfaces due to the difference in dielectric constants of the materials and their conductivity according to the Maxwell – Wagner effect, which can be expressed as:

$$Q = \left(\epsilon_2 - \epsilon_1 \frac{\sigma_2}{\sigma_1}\right) E_2 = \left(\epsilon_2 \frac{\sigma_1}{\sigma_2} - \epsilon_1\right) E_1 \tag{4.1}$$

where indices 1 and 2 denote the top and bottom layers respectively [236]. When the field of standard polarity is applied across a dielectric, a positive charge equal to $Q = CV = CIR = \epsilon \rho I$ will accumullate at the top and identical negative charge at the bottom of the layer. Thus, when the field is applied across two layers of differing resistivity, the charge accumulated at the interface can be expressed as:

$$Q_2 – Q_1 = (\epsilon_2 \rho_2 – \epsilon_1 \rho_1) I \tag{4.2}$$

where I is the vertical current density. As the dielectric constant of materials present in the AlGaN/GaN HEMT epitaxy is very similar, the relationship described in equation 4.2 suggests

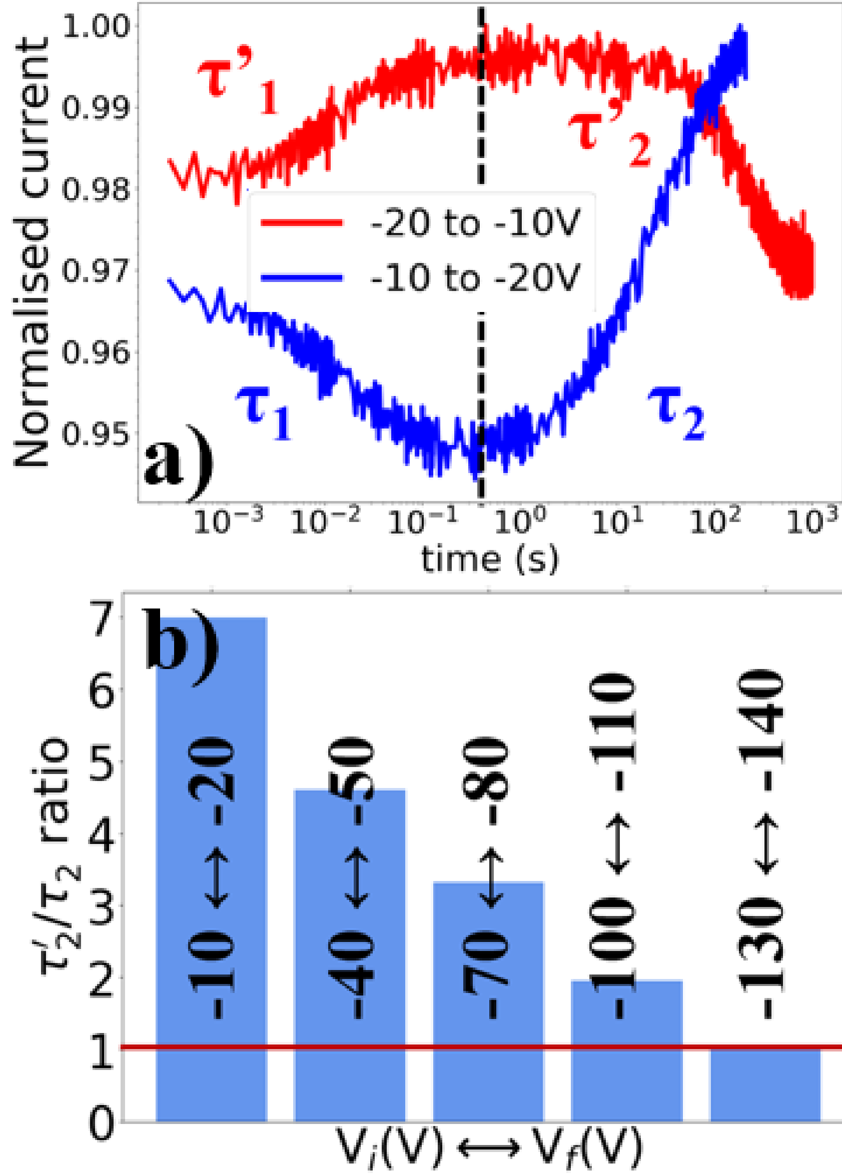

Figure 4.6: **a)**Forward (blue line) and reverse (red line) stepped substrate stress transient measurements between V_{SUB} = -10 V and -20 V. τ_1 and τ_2 indicate the transient response for forward voltage steps, while τ_1' and τ_2' denote equivalent processes for the reverse voltage step. **b)** Ratio of time constants (τ_2'/τ_2) for bidirectional voltage steps for substrate stress from V_{SUB} = -10 V to -140 V.

that at any point charge accumulation at any interface in an epitaxial stack will depend on resistivities of materials creating this interface.

The back-gating threshold voltage resulting from the application of substrate stress can be described as V_{TB} = -q_n/C_{TOT} where C_{TOT} denotes the combined capacitance of UID GaN, GaN:C and SRL. Similarly, the displacement current in the epitaxy $I_{DISS} = C_{TOT} \times dV_{SUB}/dt$. For a substrate ramp with the sweep rate of 1 V/s the corresponding displacement current is on the

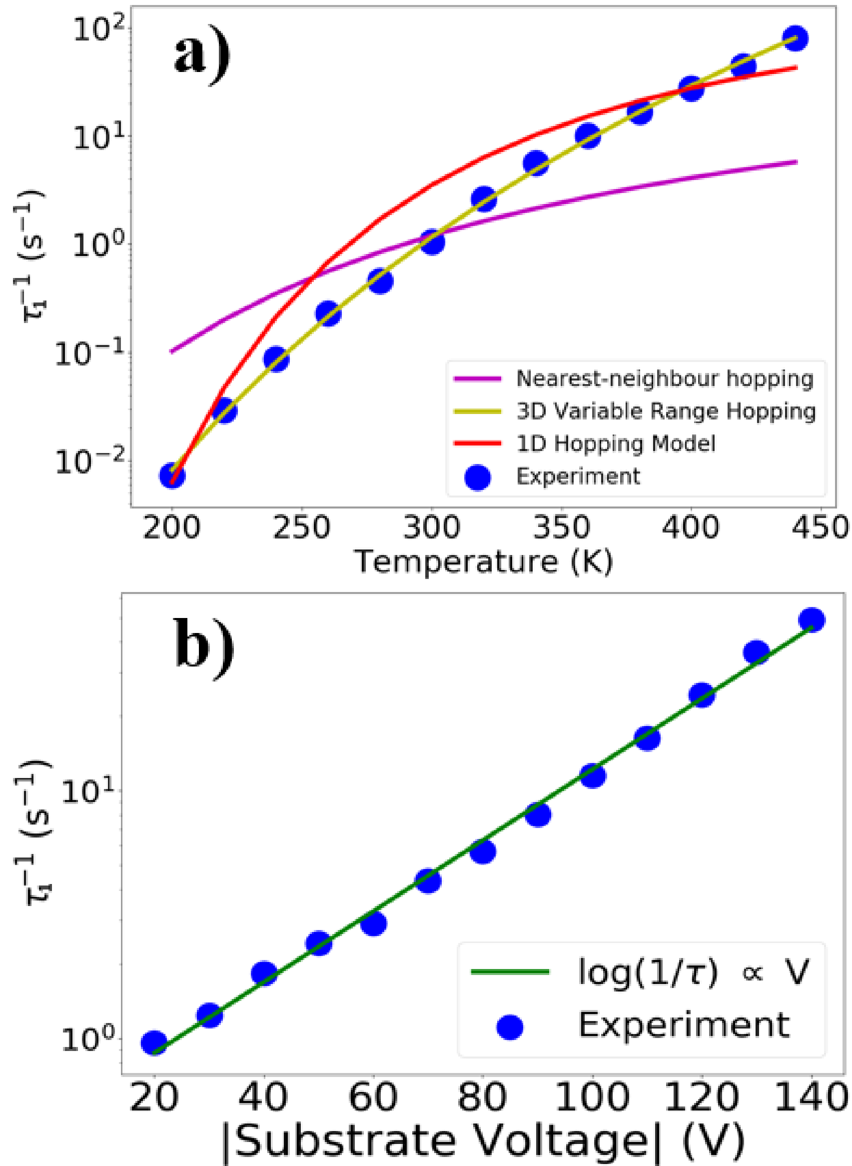

Figure 4.7: **a)** Inverse time constant as a function of temperature for the process τ_1 (measured for $|V_{SUB}|$ = 10 V).**b)** Inverses time constant as a function of applied substrate stress for the process τ_1 (measured at 380 K).

order of 2 nA/cm^2. For very small voltages ($|V_{SUB}| < V_1$) capactive coupling can be observed where the entire stack acts as an insulator and follows the capacitive line. The measured response starts deviating from the ideal capacitve behaviour as soon as leakage in one of the layers exceeds the displacement current. The initial drop in 2DEG conductivity seen at V_1 results from the leakage across the GaN:C layer which exceed the displacement current. In this region we can observe charge redistribution across C – doped GaN buffer which results in the dipole formation. The positive charge at the bottom of GaN:C and the negative charge at the UID GaN/GaN:C

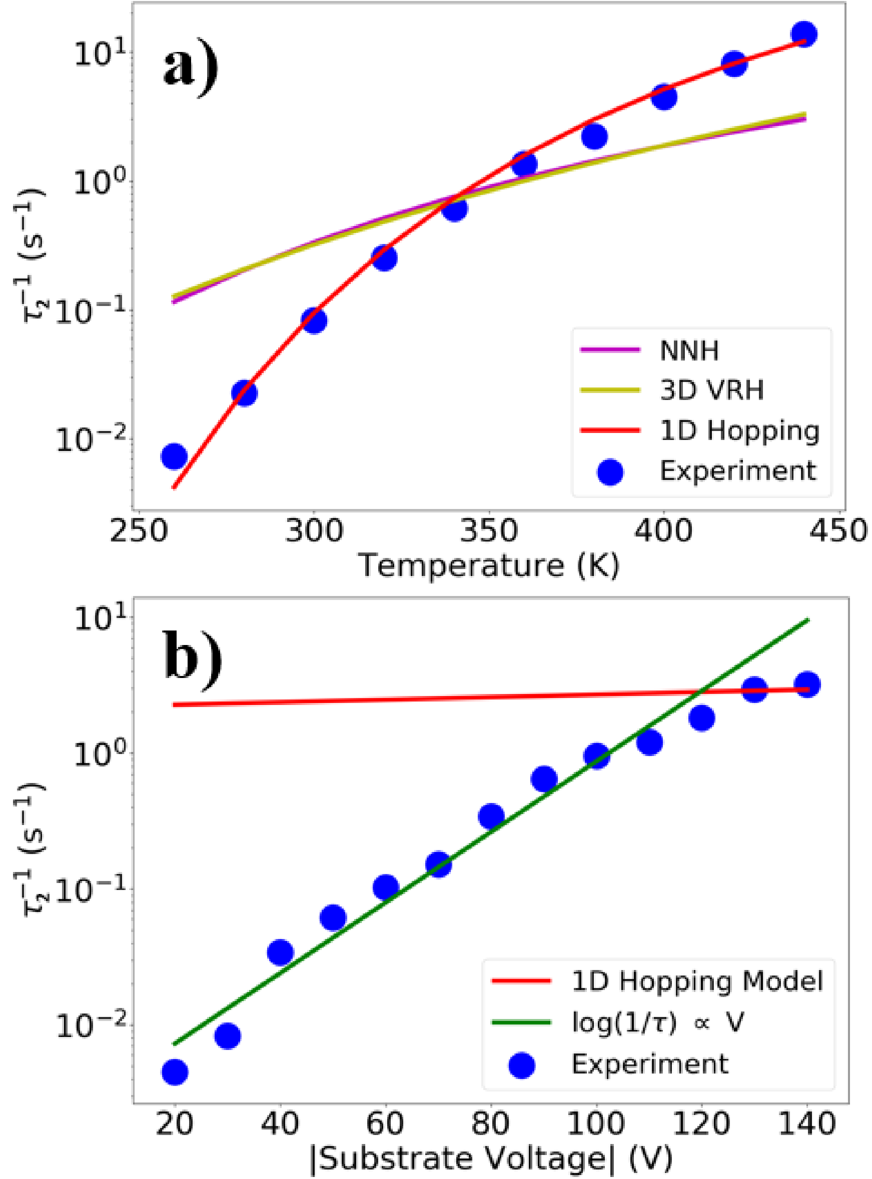

Figure 4.8: **a)** Inverse time constant as a function of temperature for the process τ_2 (measured for $|V_{SUB}|$ = 140 V). **b)** Inverses time constant as a function of applied substrate stress for the process τ_1 (measured at 300 K).

interface are confined to very narrow depletion regions.

This process is shown in Figure 4.9b and can be associated with the negative going (decreasing) transient τ_1 shown in Figure 4.4. The charge redistribution across GaN:C buffer results in accumulation of negative charge at the UID/GaN:C interface and leads to a decrease in the 2DEG conductivity. The measured activation energy E_A = 0.29 eV indicates activation of holes from the C acceptors into the valence band is not the dominant charge transport process, as its signature $E_A \approx 0.9$ eV.

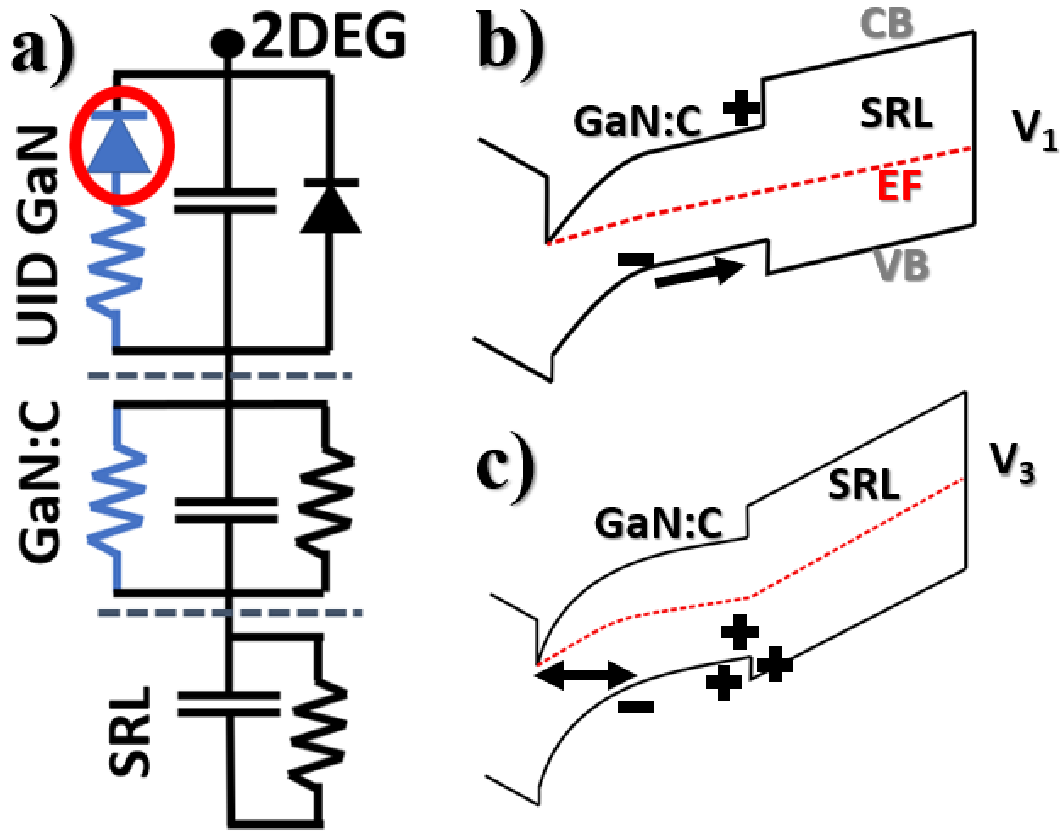

Figure 4.9: **a)** 1D lump element diagram of the transistor. The leakage paths due to dislocations are highlighted in blue, while the activation barrier between the dislocation core and the 2DEG is represented as a diode junction circled in red. **b)** Schematic representation of charge redistribution across GaN:C when the substrate stress V_{SUB} = V_1 is applied. **c)** Schematic representation of band-to-band leakage across UID GaN channel when the substrate stress V_{SUB} = V_3 is applied.

As the substrate potential is increased form the point V_2 to V_3, the substrate ramp starts plateauing indicating positive charge accumulation in the buffer. According to eq. 4.2 this is only possible if the resistivity of UID GaN is lower than the resistivity of GaN:C, which previously has been explained with a trap assisted band-to-band hopping mechanism [92][237]. This trap assisted mechanism allows for charge flow across the reverse biased pn – junction, with electrons injected into the 2DEG while the holes flow back into the GaN:C buffer. These holes will gather at the bottom of the GaN:C at the heterointerface with the SRL either neutralising the ionized acceptors or accumulating as free charge.

This process is schematically depicted in Figure 4.9c and can be attributed to the positive going (increasing) transient shown in Fig. 4.4 with the activation energy E_A = 0.38 eV. The band-to-band leakage mechanism results in the vertical leakage across UID GaN channel with the holes gathering at the bottom of GaN:C buffer. The accumulation of positive charge acts to shield the 2DEG from the applied potential leading to the observed increase in the measured

Table 4.1: Hopping Conductivity Models

1D Hopping Conduction	$\tau^{-1} = \frac{v_0 N_{TD} e}{\epsilon E}\left[1 + \frac{2exp\left(\frac{eE_\sigma}{k_B T}\right)^2}{exp\left(\frac{ebE}{k_B T}\right)-1}\right]^{-1}$
3D Variable Range Hopping	$\tau^{-1} = A_V exp\,(-{}^{T_0}\!/_{T})^{0.25}$
Nearest Neighbour Hopping	$\tau^{-1} = A_N exp\,(-{}^{E_A}\!/_{k_B T})$

Time constant dependence (τ) on temperature (T) for charge transport mechanisms with fitting parameters given in the brackets. A denotes preexponential factors with A_V and A_N equal to 1.69×10^{20} s^{-1} and 163.2 s^{-1} respectively, T_0 (1.4×10^9 K) is the Mott temperature, N_{TD} (6×10^8 cm^{-1}) is the dislocation density, e is the elctron charge, b (1.1 nm) is the trap separation, E is the electric field, μ_0 (1 GHz) is the hopping frequency and E_σ (60 meV) is the trap characteristic energy distribution [238][239][240][241]

drain current.

To identify charge transport processes responsible for charge redistribution across C – doped buffer (process τ_1) and band-to-band leakage across UID GaN channel, the most likely vertical transport processes were fitted to the experimental data for temperature and field dependence. Table 4.1 gives an outline of the investigated charge transport processes. Based one the assumption of linearised transport in the epitaxy, the conductivity associated with each process can be related to the theoretical time constant according to $\tau^{-1} = \sigma/\epsilon$ where σ denotes conductivity. The fitting parameters were extracted from the data based on the relationship between the time constant τ and the temperature. All the fitting parameters are quoted in the caption to Table 4.1.

The earliest of these models is the nearest neighbour hopping (NNH) model, which was proposed by Miller and Abrahams in 1960 to serve as an explanation for conduction in doped semiconductors. This model describes a thermally activated hopping into a nearest neighbour state where the thermal energy is delivered by a phonon. The excited electron below the Fermi level will move to the nearest unoccupied centre with the conductivity proportional to -$E_A/k_B T$, with the E_A being inversely proportional to the cube of the distance to the nearest neighbour [242].

The 3D variable range hopping (3D VRH) was first proposed by Nevill Mott in 1969 [243] and is based on the idea that the charge will hop into one of the states in its vicinity based on how far away this state is and the energy separation between the states. By evaluating the availability of states around the charge, the conduction in a semiconductor is proportional to $T^{1/_{1+d}}$ where d denotes the number of dimensions considered.

The 1D hopping conduction model assumes Ohmic conduction through dislocation cores. The current density for a dislocation density N_{TD} can be expressed as:

$$J = N_{TD} e n_d \mu E \tag{4.3}$$

where n_d, μ and E denote the linear carrier density along the dislocation, carrier mobility and electric field respectively. Assuming a single carrier for each trap state along the dislocation, $n_d = 1/b$ where b is the trap separation. In addition, the electron mobility mu is based on the theoretical calculations for one-dimensional transport in a disordered solid [240] and can be expressed as:

$$\mu = \frac{v_0 b}{E}\left[1 + \frac{2exp\left(\frac{qE_\sigma{}^2}{kT}\right)}{exp\left(\frac{ebE}{kT} - 1\right)}\right]^{-1} \tag{4.4}$$

where v_0 and E_σ denote hopping frequency and energy distribution of trap states. By combining both equations 4.3 and 4.4 the theoretical time constant can be calculated as shown in Table 4.1.

Based on the models described above and experimental data for the temperature dependence of time constant τ_1, the charge redistribution across GaN:C buffer is best described by 3D variable range hopping (Fig. 4.7a). This is consistent with the observations presented in [30] and the conduction via the defect band discussed there, suggesting primarily conduction through the bulk rather than via the dislocation (as 1D characteristics should be expected from in such case). The results from stepped and bidirectional substrate stress transient measurements suggest weak dependence of the time constant on the applied stress for small forward and reverse voltage steps (Fig. 4.5 and 4.6). However, there is still a gradual and noticeable decrease in time constant with the applied substrate voltage (Fig. 4.7b) which is not expected for one-dimensional hopping conduction.

In contrast, based on the temperature dependence of the process τ_2 the band-to-band leakage across the UID GaN channel is best described by the 1D hopping along dislocations (shown in Fig. 4.8a). However, we observe a strong asymmetry in conduction at low fields (see Fig. 4.5 and 4.6), implying very strong non-Ohmic character of this conduction process. Theoretical prediction indicates the 1D hopping mechanism should be Ohmic (i.e. time constant τ independent of the applied voltage as shown in Fig. 4.8b), so this model cannot explain these observations especially in the low voltage range.

A plausible explanation for the non-Ohmic character of the conduction across the UID GaN channel is presented in Figure 4.10. Fig. 4.10a shows a simulated vertical band diagrams including the channel and GaN:C buffer layers for substrate voltages V_1 and V_3 10s after stress is applied. Charge redistribution across the C – doped buffer (τ_1 in Fig. 4.4) results in almost complete suppression of the electric field across this layer. The blue arrows indicate band-to-band leakage associated with the 1D hopping along the dislocations, providing an electrical connection between the 2DEG and the buffer. Figure 4.10b shows a horizontal cut-line along the 2DEG. A dislocation passing through the 2DEG can be associated with a depletion region around its core (assuming Fermi level pinning at the defect band in the dislocation core), resulting in a Schottky barrier in series with the dislocation core. This junction is indicated by the diode highlighted in the lump element diagram shown in Figure 4.9a.

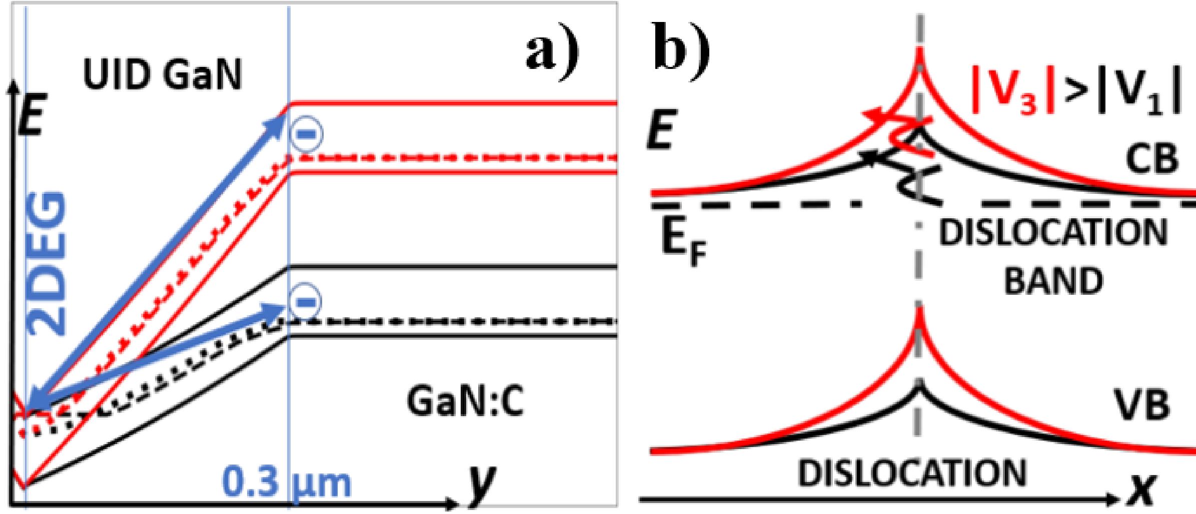

Figure 4.10: **a)** Simulated vertical band diagram of the device 10 s after substrate stress $V_{SUB} = V_1$ (black) and $V_{SUB} = V_3$ is applied. Dashed and dotted lines indicate the position of electron and hole quasi Fermi levels respectively. **b)** Schematic representation of the horizontal band diagram along the 2DEG when it intersects a dislocation core; it is easier for electrons to enter the 2DEG at higher substrate bias as the depletion region around the dislocation core is thinned by the applied field. Dimensions y and x represent the depth and length of the device.

Application of negative substrate bias results in a reverse biased Schottky barrier junction. However, increase in electric field results in current flow through the barrier likely facilitated by processes such as Fowler-Nordheim tunneling or trap assisted tunneling. Thus, the differential resistance of the junction will decrease with applied bias until the vertical transport is dominated by the Ohmic hopping conduction via the dislocations. This provides an explanation for strong asymmetry that decreases with applied substrate potential shown in Fig. 4.6b.

Figure 4.11 shows activation energy of the band-to-band leakage process (τ_2) measured for substrate stress $|V_{SUB}|$ between 20 and 140 V. It can be observed that the in this voltage range the activation energy decreases by ~ 0.1 eV, which provides further support for this model. Interestingly, we note a similar discrepancy at low voltages between the experimental measurements and 1D hopping model that has been observed by Moroz *et al.* in GaN pn diodes [234], however no explanation was offered by the authors.

4.5 Simulations

In order to explain and verify the experimental measurements 2D TCAD simulations were performed using Silvaco Atlas software. The simulated device structure is shown in 4.1a and includes 300 nm UID GaN channel and 1μm C – doped GaN buffer, with the exception of superlattice strain relief layer which instead was represented as consisting exclusively of AlN with the thickness of 1.9 μm. This substitution was introduced for the purpose of simplicity and

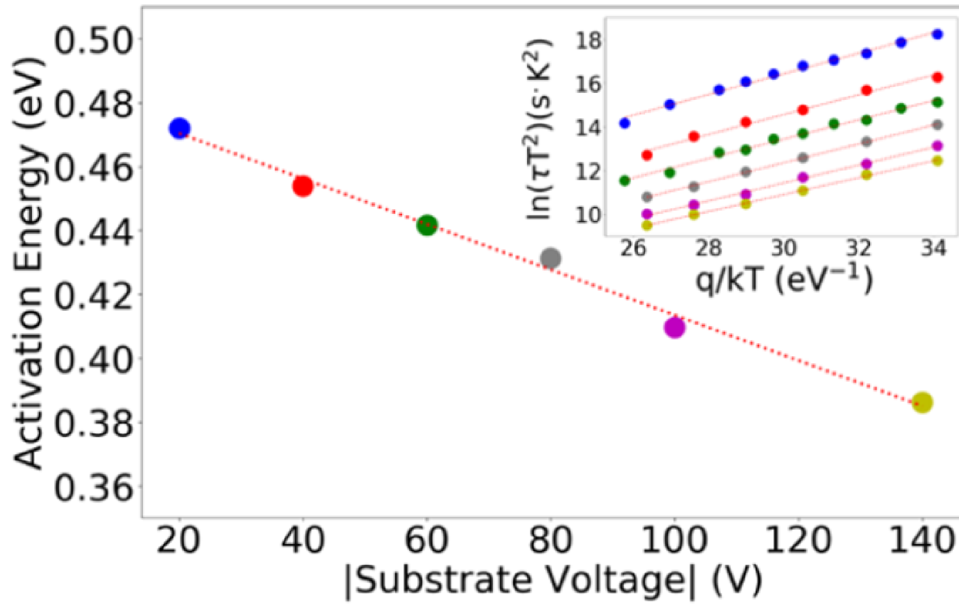

Figure 4.11: Activation energy of the band-to-band leakage across the UID GaN channel (process τ_2) measured for a range of substrate stress voltages $|V_{SUB}|$ = 20 V 140 V. The inset shows Arrhenius plots used for extraction of these activation energies.

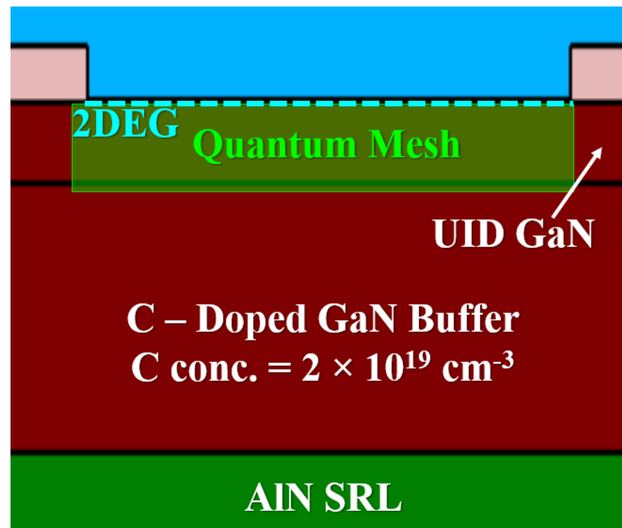

Figure 4.12: TLM structure simulated in the Silvaco Atlas TCAD software. The quantum mesh was introduced across UID GaN channel allow for novel model describing 1D hopping along the dislocations between the GaN:C and 2DEG. Device parameters such as geometry, epitaxy and doping profiles have been replicated based on measured structure.

computational efficiency, whilst having no effect on the simulation results in the investigated field regime. Total carbon concentration in the buffer was set to 2×10^{19} cm^{-3} with the acceptor level at 0.8 eV above the valence band. The electron and hole capture cross-sections were set to 10^{-15} cm^2. Deep acceptors were compensated by shallow donors at 0.05 eV below the conduction

band with the compensation ratio of shallow donors to acceptors of 0.5 [177]. Figure 4.12 shows the simulated structure described above.

The models used in the simulation included Fermi – Dirac and Shockley–Read–Hall statistics. For electron mobilities Caughey-Thomas velocity saturation law was applied (which relates to doping and temperature dependence in low field regime), with 2DEG mobility of 1800 cm^2 V^{-1} s^{-1} and bulk hole mobility of 8 cm^2 V^{-1} s^{-1}. In addition, novel non-local 1D hopping model was included between the 2DEG and GaN:C to simulate vertical band-to-band leakage along the dislocations, with the hopping current given by:

$$J = \frac{N_{TD} e v_0}{1 + \frac{2exp\left(\frac{eE_\sigma}{kT}\right)^2}{exp\left(\frac{ebE}{kT}-1\right)}} \tag{4.5}$$

where the trap density N_{TD} = $10^7 cm^{-2}$, hopping frequency v_0 = 10^{11} Hz, energy width of the defect band is set to E_σ = 0.06 eV and the separation between hopping sites b = 1.1 nm. This was achieved by introducing an additional level of meshing (so called “quantum mesh”). The full description of this computational model can be found in [241].

Figure 4.13a shows the simulated bidirectional substrate ramp (red) compared to the experimentally measured substrate ramp (blue) at the ramp rate of 1 V/s. The simulations show good qualitative agreement with the measurement especially in the forward sweep. The reverse sweep show some degree of variation from the experiment: simulated current increases at a decreasing rate (in the region -150 to -100 V), while the measured current increases at an increasing rate in the same region. This reason for this discrepancy lies in the Ohmic nature of the simulated hopping along the dislocation, whereas in fact we have previously demonstrated its non-Ohmic character.

This point is particularly evident for the simulation of bidirectional stepped substrate stress transient measurements show in Figure 4.13b. The measurement (see Fig. 4.6a for comparison) shows strong asymmetry between forward and reverse voltage steps characteristic of non-Ohmic transport process, which is not present in the simulated transients.

4.6 Conclusions

The understanding of vertical charge transport processes in the GaN-on-Si power devices is of crucial importance to better manage dynamic On-resistance. In this work, we used a combination of bidirectional substrate ramp sweeps and substrate stress transient measurements to separate the dominant charge transport processes in state-of-the-art GaN HEMT epitaxy.

Based on the substrate ramp measurement we established the main bias points at which two different charge transport processes are dominant, while substrate stress transient measurements enabled separation of these processes. The measurements show to distinct conduction regimes: negative going (decreasing) transient response with the activation energy E_A = 0.28 eV

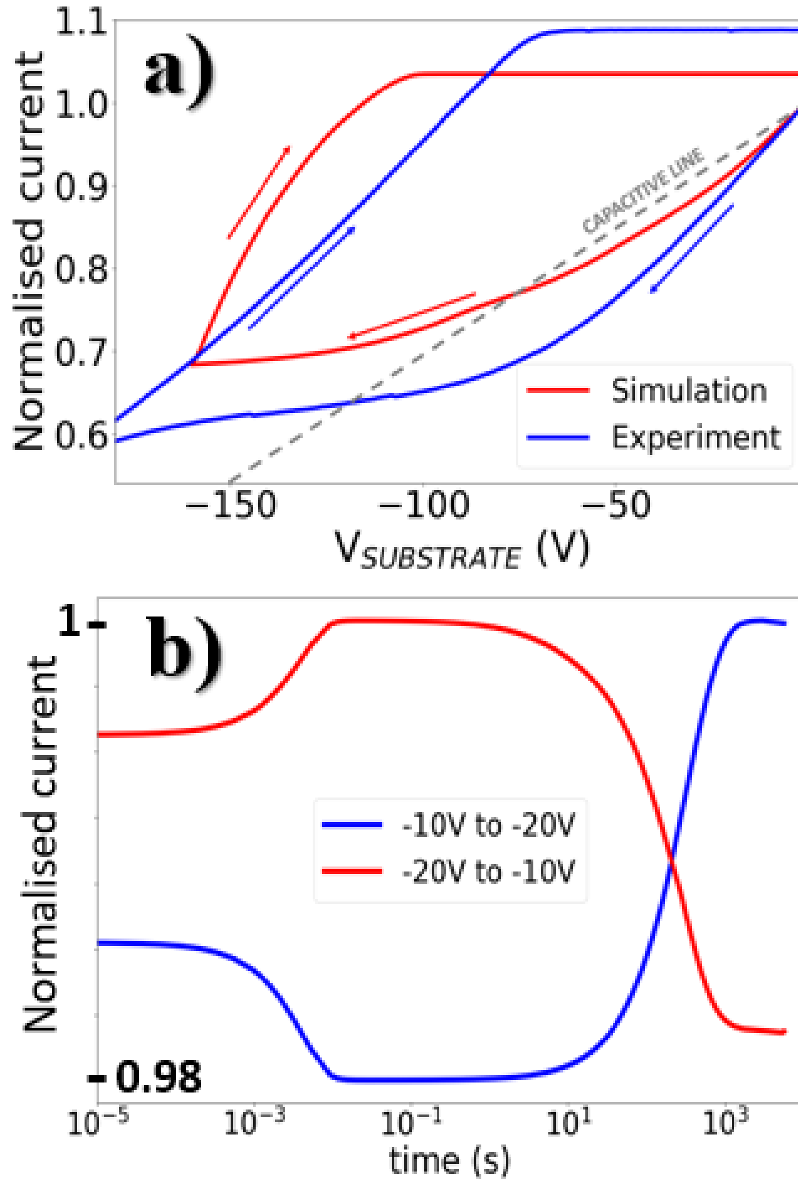

Figure 4.13: **a)** Substrate ramp simulation as compared to the experimental measurement at the ramp rate of 1 V/s. **b)** Simulated forward (blue line) and reverse (red line) stepped substrate stress transient measurements between V_{SUB} = -10 V and -20 V. The arrows indicate the direction of the sweep.

responsible for charge redistribution in the C - doped GaN buffer and a positive going (increasing) transient with the activation energy $E_A = 0.29$ eV corresponding to band-to-band leakage across the UID GaN channel.

By investigating the temperature dependence of the time constants, theoretical expressions for the most likely vertical charge transport processes were fitted to the experimental data. The results indicate that charge redistribution across GaN:C buffer is best described by 3D variable

range hopping within the bulk, while band-to-band leakage process across the UID GaN channel corresponds to the 1D hopping along the dislocations.

Bidirectional substrate stress transient measurements show mild non-Ohmic character for the charge redistribution across GaN:C. In contrast band-to-band leakage across UID GaN channel exhibits strong non-Ohmic character, which is confirmed by investigating the field dependence of this process. To explain these observations, we propose an existence of previously unobserved activation barrier between the dislocation core and the 2DEG, which decreases with the applied field.

In addition, we demonstrate implementation of a novel 1D hopping model into TCAD simulations performed in Silvaco Atlas software. The simulations show good qualitative agreement with the measurements, however due to Ohmic character of the theoretical hopping model the effects of non-linearity observed for the band-to-band leakage model cannot be reproduced in the simulator.

The results presented in this chapter constitute a significant step towards a better understanding of the role carbon doping and dislocation play in phenomena such as dynamic R_{ON}, and how they affect the electrical characteristics of operating GaN based devices. The ideas and concepts developed in this chapter will be further investigated in the next section of this thesis, where the link between dynamic R_{ON} and GaN-on-Si Schottky barrier diodes is explored.

CHAPTER 5

The Effects of Charge Transport Processes on Dynamic On-Resistance in GaN-on-Si Schottky Barrier Diodes

This work focuses on the effects of charge transport processes present in carbon doped GaN buffers on the electrical performance of power devices. In the previous chapter, we identify the dominant vertical charge transport processes present in GaN layers of the investigated epitaxial structure as 1D hopping along the dislocations across UID GaN channel and 3D variable range hopping in the defect band across the C-doped buffer. This chapter constitutes a continuation of that work, demonstrating evidence that vertical and lateral charge transport processes and not buffer trapping are predominantly responsible for temperature and field dependence of On-resistance in GaN-on-Si Schottky barrier diodes.

Bidirectional substrate ramps and substrate stress transient measurements were performed on transfer length model (TLM) structures based on identical epitaxy to the Schottky diodes. This allows for separation of the dominant vertical charge transport mechanisms in the epitaxy according to their bias dependence. Temperature (200 - 450 K) and voltage (0 - 200 V) dependence of dynamic On-resistance (R_{ON}) of TLM structures shows strong dependence on the vertical charge transport processes across the investigated range of parameters. Comparison of recovery transients between TLM structures and Schottky diodes shows significant differences, with diodes exhibiting more complex behaviour and significantly larger increase in the dynamic R_{ON}. In addition, the temperature and field dependence of the dynamic R_{ON} show significant differences between the two investigated structures. 2D TCAD simulations of the investigated devices reveal the differences can be explained in terms of non-uniform field distribution during stress phase in Schottky barrier diodes. Thus, the observed two step recovery transient can be explain in terms of lateral charge redistribution followed by vertical reorganisation. Hence, the origin of the measured dynamic R_{ON} is attributed to vertical and lateral charge transport processes present

in the buffer.

The structures used in this study were grown and processed by Inter-university Micro-Electronics Centre (imec). All the experimental work and simulations were performed by the author. This chapter contains significant portions of the article has been submitted (currently under review) to IEEE Transactions on Electron Devices. Some figures have been reproduced with permission from IEEE.

5.1 Introduction

Electronic devices based on AlGaN/GaN hetereostructures demonstrate excellent properties for power switching applications. The figure of merit BV^2/R_{ON} for these devices is much higher in comparison with other competing technologies, whilst allowing for manufacturing of more compact and efficient modules [68]. One of the main factors preventing widespread application of GaN based devices relates to buffer induced dynamic R_{ON}, which can be observed even in the commercially available transistors and diodes.

Schottky barrier diodes (SBDs) based on AlGaN/GaN heterostructure are perfect candidates for power switching applications due to the presence of 2DEG and outstanding material properties as outlined above. An efficient SBD requires low off-state leakage current and low voltage drop across the device in the on-state operation in order to minimise static power loss. Thus, increase in On-resistance of the operating device can have a dramatic effect on the power dissipation of a converter and has to be mitigated to achieve maximum efficiency.

The origin of dynamic R_{ON} can be in most cases attributed to heavily doped buffer layers, which are necessary for growth of good quality GaN-on-Si devices. However, in the literature the discussion of dynamic R_{ON} is dominated by references to trap states, activation energies and capture cross-sections, with some examples including [232], [244] and [245].

In the previous chapter we have identified the dominant vertical charge mechanisms taking place in the buffer and demonstrated their significance to electrical performance of the GaN-based power devices. In this work, we investigate the effects of charge transport processes on dynamic R_{ON} in TLM structures and in Schottky barrier diodes. The temperature and field dependence of dynamic R_{ON} in both types of structures are discussed with the aid of TCAD simulations.

5.2 Experimental Method

5.2.1 Sample Description

This study was performed on TLM structures and Schottky barrier diodes grown and fabricated by imec on the same wafer (Figure 5.1 shows a schematic representation of the structures), based on a typical AlGaN/GaN-on-Si epitaxy optimised for power applications up to 200 V. The epitaxial stack was grown on the Si (111) substrate using metal-organic chemical vapour deposition method

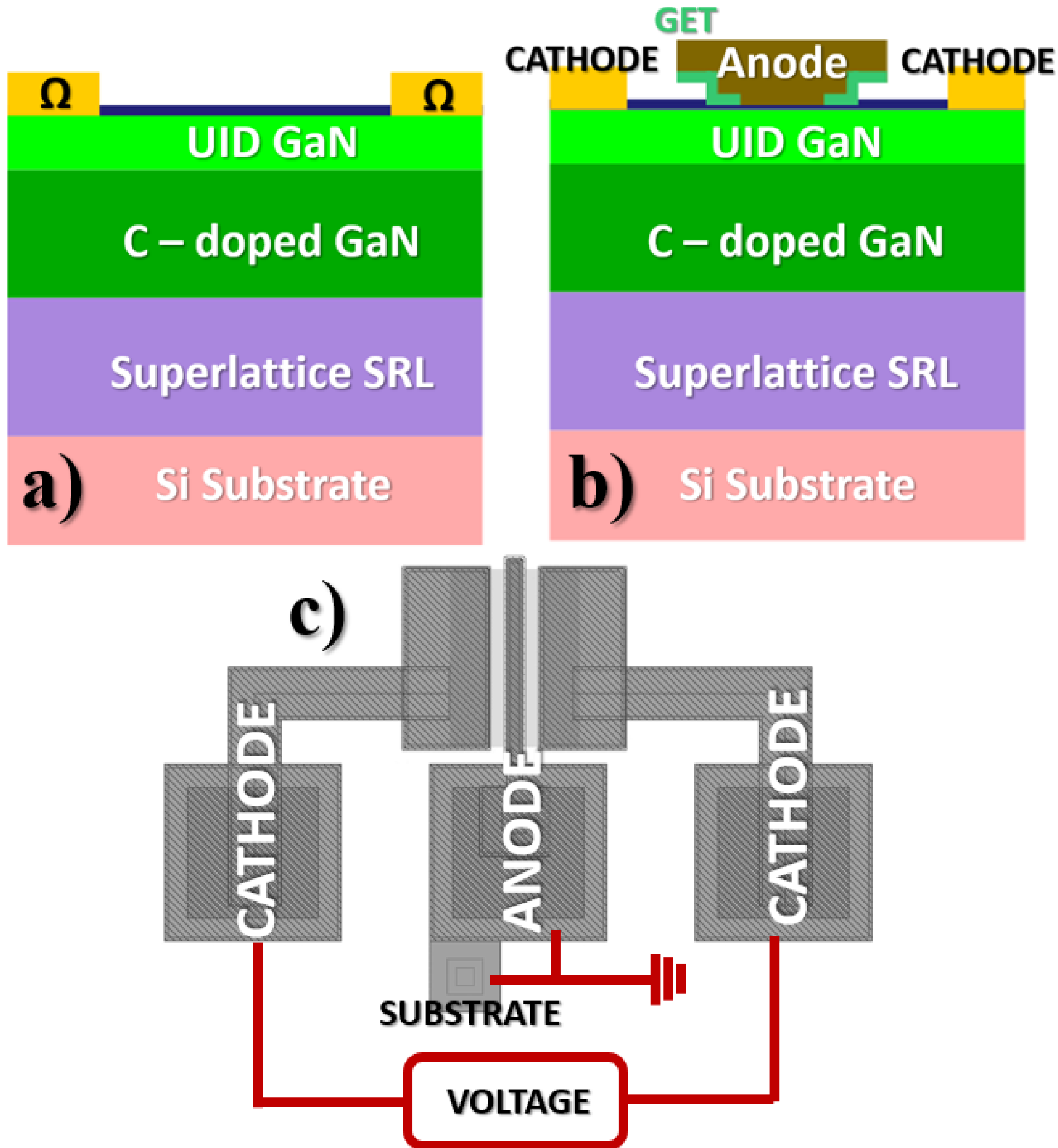

Figure 5.1: Schematic representation of structures investigated in this study: **a)** transfer length model structure and **b)** Schottky barrier diode with gated edge termination (GET). Both structures were fabricated on identical epitaxial stack. **c)** Top view of the Schottky barrier diode with schematic representation of bias configuration.

and consists of AlGaN and AlN transition layers followed by AlGaN/AlN superlattice strain relief layer (total thickness of these layers ≈ 1.9 μm), heavily C-doped GaN buffer (C concentration of 2 $\times$ 10^{19} cm^{-3} as measured by secondary ion mass spectroscopy) with the thickness of 1 μm and unintentionally doped GaN channel (0.3 μm thick). To enable 2DEG formation 0.5 nm-thick AlN spacer and 10 nm thick $Al_{0.25}Ga_{0.75}N$ barrier were grown on top of GaN channel followed by 5nm of SiN cap and passivated with SiO_2 by means of high-temperature oxide deposition method. In

case of Schottky barrier diodes, the AlGaN barrier was recessed in the anode region by ~ 6 nm by atomic layer etching, resulting in only ~ 4 nm AlGaN under the electrode. Plasma-enhanced atomic layer deposition was used to deposit 45 nm of Si_3N_4 followed by dry etching under the anode to create the gated edge termination (GET) of the length of 1 μm. GET structure effectively reduces leakage current under the reverse bias operation as outlined in more detail in [246].

The Au-free Schottky contact was formed by deposition of TiN (20 nm), Ti (20 nm), Al (250 nm), Ti (20 nm) and TiN (60 nm). The anode sheet resistance is 0.37 Ω/sq. The Au-free Ohmic contacts were fabricated with 20 nm of Ti, 200 nm Al, 20 nm Ti, 60 nm TiN and annealed at 565°C. The Ohmic contact resistance was measured as 0.14 Ω·cm.

This study was performed on 200 V rated single finger diodes, with anode length of 6 µm, anode to cathode spacing of 6 µm, and anode width of 100 µm. In addition, TLM structures with contact spacing between 1 μm and 18 μm and contact width of 100 μm were also studied to offer a comparison with Schottky barrier diodes.

5.2.2 Experimental Method

To assess the properties of vertical charge transport processes and uniformity of the sample, bidirectional substrate ramp sweeps were performed on TLM structures across the wafer by applying of small bias (0 and 0.5 V) to the Ohmic contacts while the substrate potential was gradually swept from 0 V to -20 V and back at a constant rate of 1 V/s. In this way, the polarity of the electric field in the buffer is equivalent to application of large Off-state anode stress. Due to the constant presence of the 2DEG this technique is insensitive to surface effects.

To investigate potential leakage paths under the contacts [91], TLMs with contact length from 2um to 100 um were measured. In addition, the effects of contact spacing between 1 to 18 μm on the substrate ramp characteristics were measured. In order to inspect the epitaxy for the presence of 2DEGs or 2D hole gases, substrate ramps were measured for TLMs with active areas of different size. Finally, the effects of temperature on ramp characteristics were studied in the range 300 - 450 K.

Subsequently, substrate stress and recovery transient measurements were performed on TLM structures with the contact dimensions 100 × 100 μm and contact spacing of 8 μm. The measurement timeline is shown in Fig. 5.2. Substrate stress transient measurement involves application of small bias across the Ohmic contacts to monitor the 2DEG conductance throughout the experiment while minimising the impact of the applied potential at the top of the epitaxy, at the same time the substrate potential is rapidly switched (~ 10 μs) to a chosen bias point V_f. The 2DEG conductivity is monitored for the duration of applied substrate bias (Fig. 5.2a). In contrast, the recovery transients involve monitoring of 2DEG conductivity immediately after the substrate stress V_f has been removed for up to 1000 s (Fig. 5.2b).

The measurements of dynamic R_{ON} were performed in the temperature range between 200 K and 450 K on TLM structures with the contact dimensions 100 × 100 μm and contact spacing of

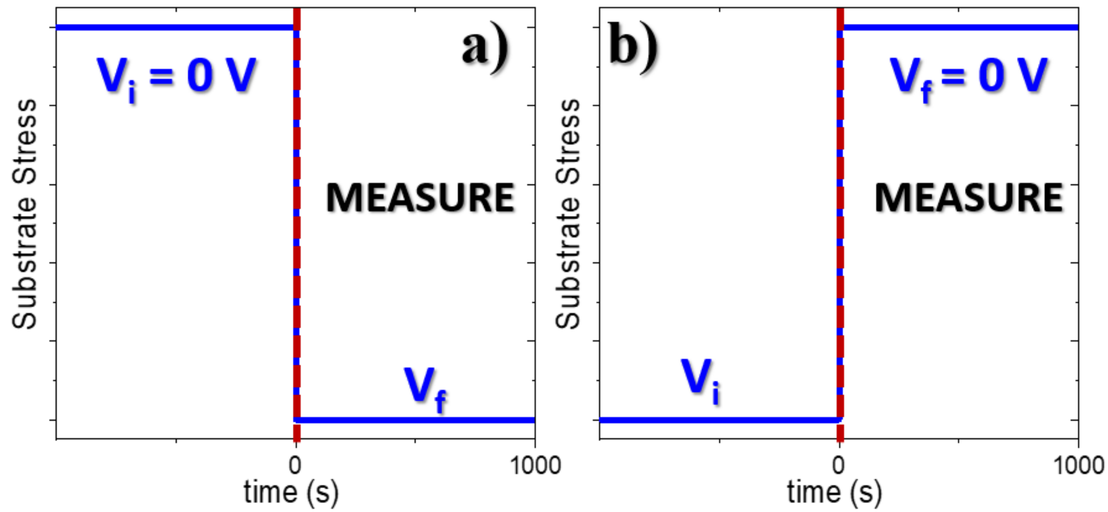

Figure 5.2: **a)** Schematic representation of the measurement timeline of the substrate stress transient measurement, where substrate voltage is rapidly switched to stress point V_f for 1000 s. The measurement begins at this point. **b)** Schematic representation of the substrate stress recovery transient measurement, where the device is biased at the stress voltage V_f for 1000 s before the substrate stress is rapidly switched to 0 V, at which point the measurement begins.

8 μm. In this experiment substrate stress of -50 V, -100 V and -150 V was applied for 1, 10 and 100 s across the temperature range from 200 - 450 K. The IV characteristics of the device were measured immediately after the stress was removed and the dynamic R_{ON} was calculated from the gradient of the linear region.

Characterisation of Schottky barrier diodes involved DC IV measurements in the temperature range between 200 - 450 K. The measurements were performed by grounding the anode and the substrate while applying negative potential to the cathodes (see Fig. 5.1c). This biasing scheme is chosen to match the intended device operation in the commercial applications. The recovery transients of SBDs were measured in a similar fashion to TLM structures, however the stress phase involves application of positive bias to the cathodes. In addition, dynamic R_{ON} measurements in the temperature range 200 - 450 K were performed by biasing the cathodes at 50 V, 100 V and 150 V for 1, 10 and 100 s; the IV characteristics were measured immediately after the stress phase to extract the dynamic R_{ON}.

All the experiments described in this section were performed using Keithley 2636B instrument. In addition, to achieve precise temperature conditions all the investigated devices was placed in the cryogenic vacuum probe station Janis ST-500, which is described in more detail in Chapter 3.

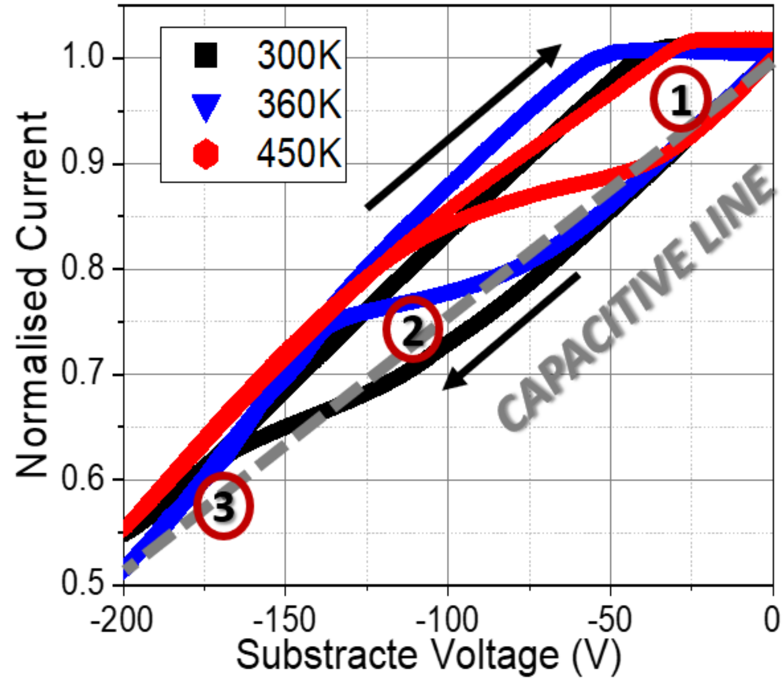

Figure 5.3: Substrate ramp measurements performed on TLM structure with contact spacing of 6 μm and contact area of 100 × 100 μm at 300, 360 and 450 K at the ramp rate of 1 V/s. The arrows indicate the direction of the sweep while the numbers 1-3 indicate regions dominated by different charge transport mechanisms.

5.3 Results

5.3.1 TLM Structures

Application of substrate stress to TLM structures enables clear characterization of buffer charging properties resulting from uniform lateral field distribution during stress, while creating bias conditions similar to off-state cathode stress. Substrate ramps performed on the devices different location on the wafer indicate uniform behaviour across the sample. Variation in contact spacing and contact surface area had little effect on measured device characteristics, indicating uniform vertical conduction across the entire length of the channel [90]. In addition, the size of active area had no significant effect on substrate ramp characteristics suggesting the vertical charge transport across the epitaxy can be approximated as 1D. This result also indicates no significant vertical leakage paths under the contacts or lateral conduction channels in the form of 2D hole gases or 2DEGs at heterojunctions [212] [213].

Figure 5.3 shows a representative set of substrate ramps performed on a TLM structure with contact spacing of 6 μm and contact area of 100 × 100 μm at temperatures between 300 K and 450 K and ramp rate of 1 V/s. The forward sweep shows three distinct regions labelled 1-3, with the capacitive grey dashed line (i.e. the line indicating the case where the whole epitaxy acts as a perfect insulator). This line acts as a reference for inferring charge storage in the epitaxy: any

response above the line suggests positive charge storage (which is the case for the investigated structures), while any response below the line indicates negative charge storage.

In region 1 we observe a gradual decrease in the 2DEG current with the applied substrate potential. At 300 K this region extends up to $|V_{SUB}| \approx 125$ V and drops as the temperature is increased (down to $|V_{SUB}| \approx 40$ V at 450 K). The observed decrease in 2DEG current can be attributed to charge redistribution across C-doped GaN buffer, in which the holes accumulate at the bottom of the GaN:C layer while the negative charge builds up at the the UID GaN/GaN:C interface.

As the substrate potential is increased further, region 2 shows a reduction in the rate at which 2DEG conductivity decreases, in some cases showing a plateau. This observation indicates accumulation of positive charge in the buffer that at least partially screens the applied substrate voltage. This charge accumulation can be attributed to band-to-band leakage process across the UID GaN channel. The decrease in resistivity of this layer allows for positive charge build-up at the interface. Similar to region 1, increase in temperature leads to positive charge accumulation at lower voltages. Eventually, positive charge accumulated in the buffer is insufficient for further screening of the applied potential and the gradual decrease in 2DEG current continues (region 3). At 300 K this region can be observed at $|V_{SUB}| \approx 175$ V and its origin can be attributed to the leakage across the SRL.

Substrate stress transient measurements can be used to separate the dominant vertical charge transport processes in the buffer corresponding to the regions described above [230]. Figure 5.4 shows substrate stress transients related to "trapping" phase and corresponding recovery transients, with currents normalised against 2DEG conductivity with no stress applied. The "trapping" transients in Figure 5.4a exhibits two distinct regions: the negative going (decreasing) transient τ_1 and the positive going (increasing) transient τ_2, with the corresponding activation energies extracted from the Arrhenius plots of E_A = 0.21 eV and E_A = 0.31 eV respectively. Performing substrate stress transient measurements at higher voltages results in reduction in the magnitude of τ_1, while the process τ_2 becomes more prominent. The reverse is true for transients measured at lower substrate voltages.

Figure 5.4b shows a substrate stress recovery (or "detrapping") transient following 100 s of substrate stress V_{SUB} = -50 V across the temperature range between 300 K - 450 K (stress duration is marked on Fig. 5.4a by dashed vertical line). Removal of the stress results in immediate increase in current up to 2.5% above the baseline. The activation energy for this process has been extracted from the Arrhenius plot as E_A = 0.46 eV. Increase in current after stress is followed by gradual return to the equilibrium. The initial current reading at ~ 1 ms shows non-linear dependence on temperature: for temperatures between 300 K to 340 K we observe reducing in the initial current due to increased extent of "trapping"; at temperatures above the 340 K initial current reading increases and exceeds the baseline at 380 K.

Figure 5.5a shows IV characteristics of the TLM structure with contact spacing of 6 μm

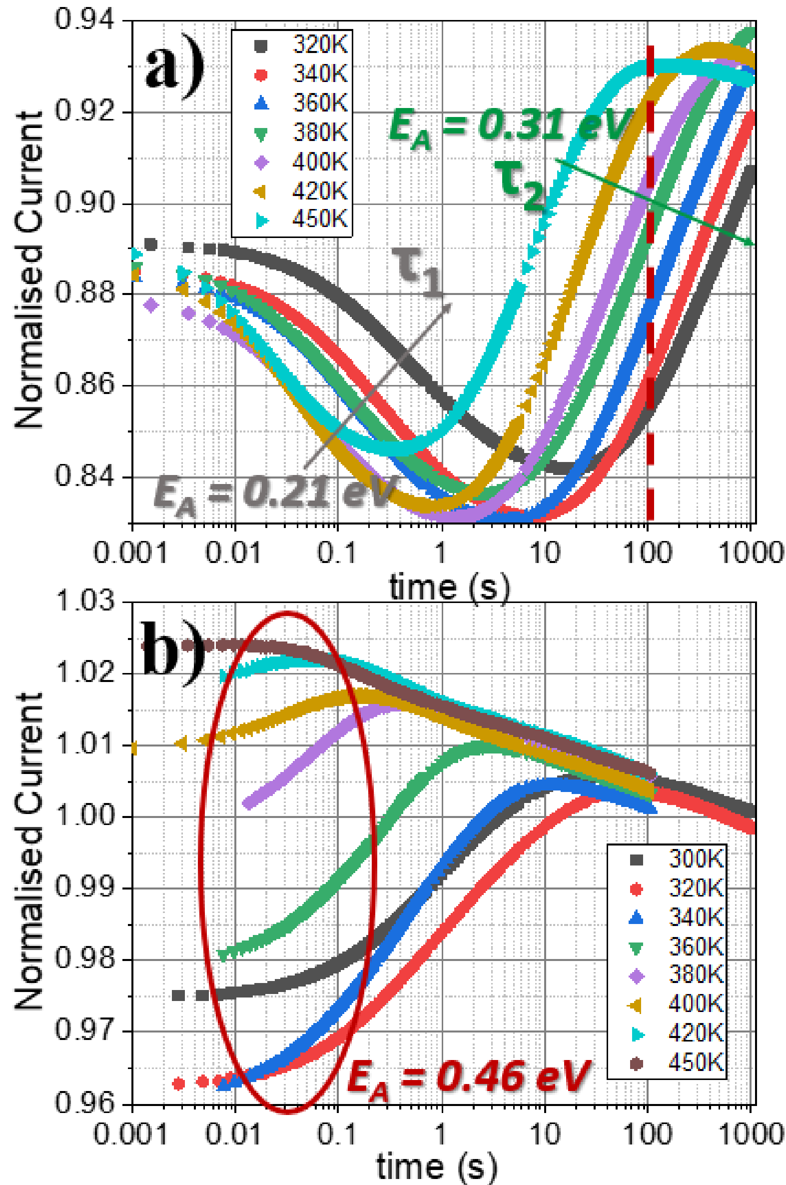

Figure 5.4: **a)** Substrate stress transient measurement in the temperature range between 320 - 450 K showing "trapping" at V_{SUB} = -50 V for TLM structure with contact spacing of 6 μm and contact area of 100 × 100 μm. Negative (decreasing) and positive (increasing) going transients τ_1 and τ_2 are shown in the graph with their corresponding activation energies. **b)** Recovery transient from 100 s of V_{SUB} = -50 V stress (marked by dashed line in **a)** for a TLM structure measured in the temperature range 300 - 450 K. The activation energy of the recovery process is indicated on the plot.

and contact area of 100 × 100 μm in the temperature range between 300K - 450 K, while the corresponding On-resistance of the structure over an extended range is shown in Fig. 5.5b. The R_{ON} of the devices increases almost linearly across the temperature range from 1.77 Ω·mm at 300 K to 6.46 Ω·mm at 450 K. These results were used as a baseline for normalisation of dynamic

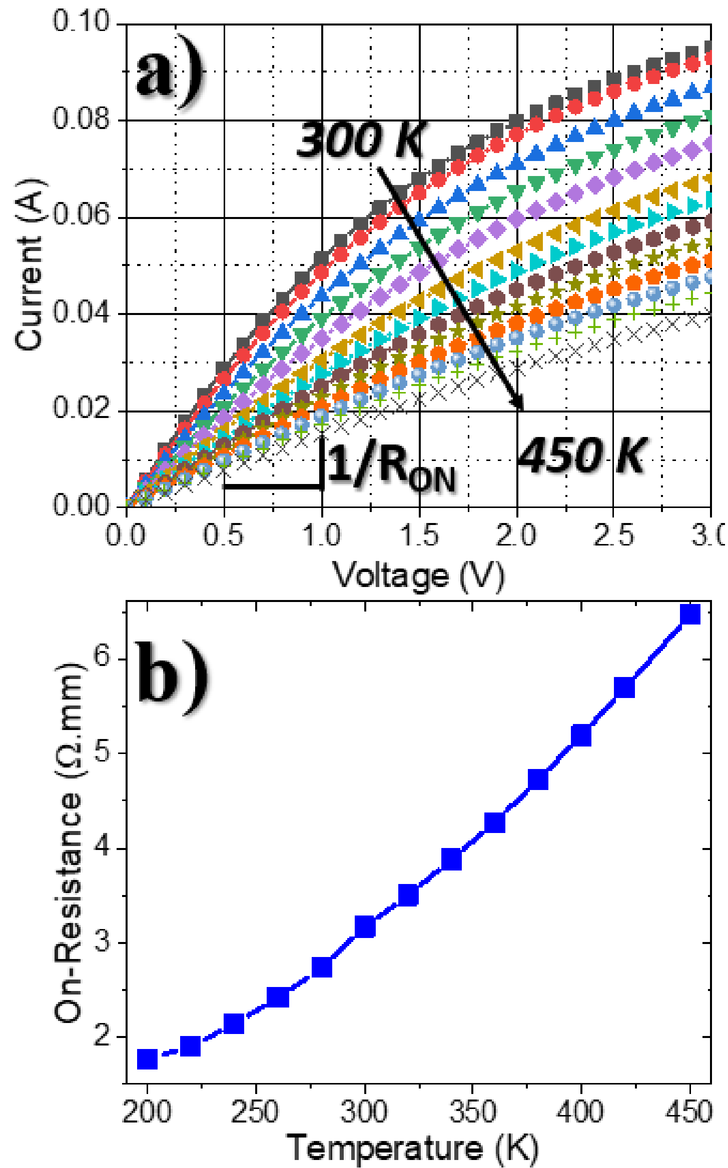

Figure 5.5: **a)** IV characteristics of a TLM structure with contact spacing of 6 μm and contact area of 100 × 100 μm across the temperature range 300 - 450 K. The R_{ON} was measured from the slope of the linear region. **b)** On-resistance of the TLM structure between 200 K and 450 K.

R_{ON} in the field and temperature dependence experiments.

Figure 5.6 shows the temperature and field dependence of the dynamic R_{ON} measured for the TLM structures. The field dependence on the dynamic R_{ON} (Fig. 5.6a) shows two distinct regions: initially the dynamic R_{ON} increases by up to 6.5% followed by a gradual decrease. As the duration of stress is increased, the peak in the On-resistance shifts towards lower voltages and eventually, for stress duration of 100 s the substrate potential appears to have little effect of the measured dynamic R_{ON}. The temperature dependence of dynamic R_{ON} shown in Fig.

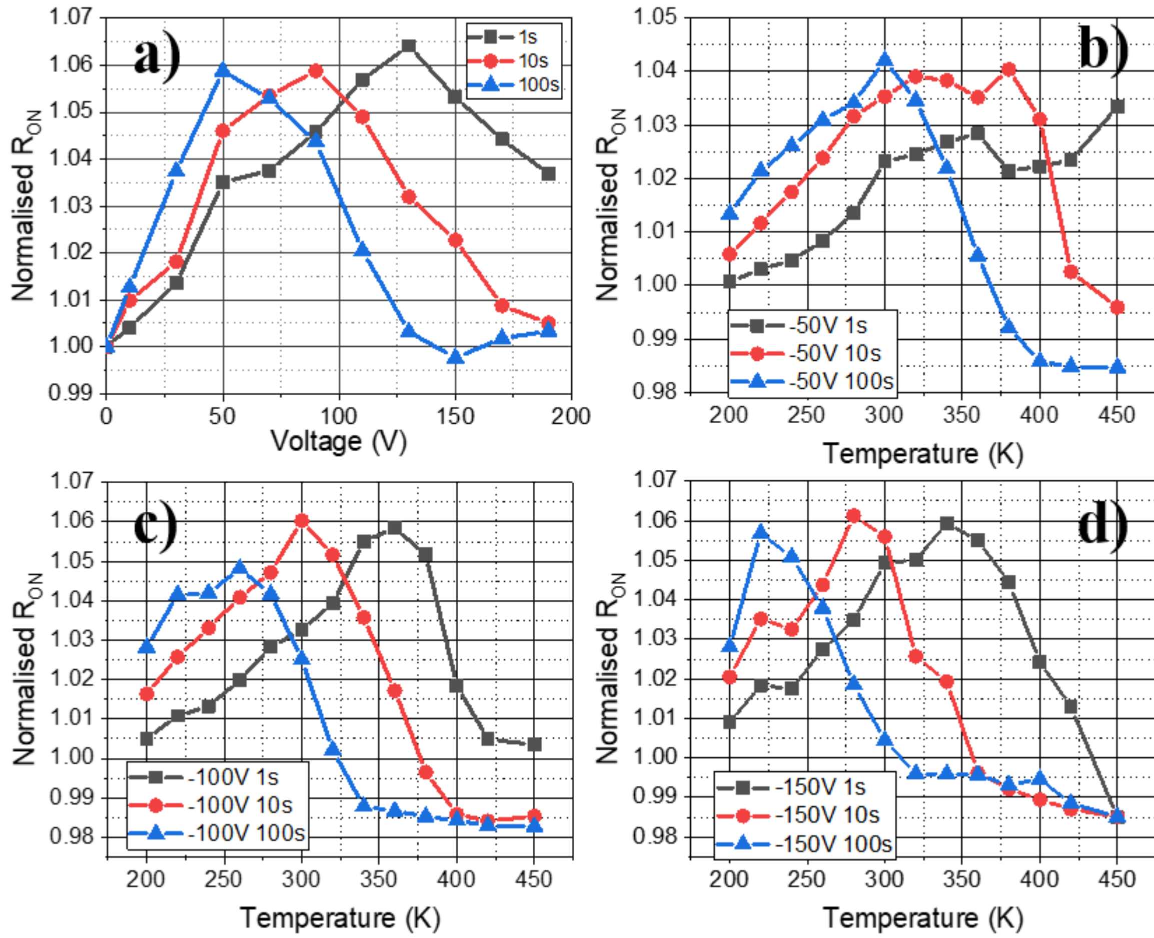

Figure 5.6: Dynamic R_{ON} measurements of a TLM structure with contact spacing of 6 μm and contact area of 100 × 100 μm . **a)** Normalised dynamic R_{ON} as a function of applied substrate stress V_{SUB} at 300 K for stress duration of 1, 10 and 100 s (measured immediately after stress). Normalised dynamic R_{ON} measured immediately after stress as a function of temperature for stress voltages V_{SUB} = -50 V, -100 V and -150 V (stress duration of 1, 10 and 100 s) are shown in **b)**, **c)** and **d)** respectively.

5.6b-d exhibits similar trends to those described above: initial increase in R_{ON} is followed by a gradual decrease, with the peak value shifting towards lower temperatures with increased stress duration.

5.3.2 Schottky Barrier Diodes

Figure 5.7 shows typical IV characteristics measured for a Schottky barrier diode with contact spacing of 6 μm and anode length of 100 μm. Here, we define the threshold voltage as potential difference between cathode and anode V_{AC} at which the anode current falls below 1 mA/mm. The threshold voltage of the investigated devices was measured as 0.8 V at 300 K and decreases to 0.74 V at 450 K. The On-resistance of SBDs was measured as 2.12 Ω·mm at 300 K and increases

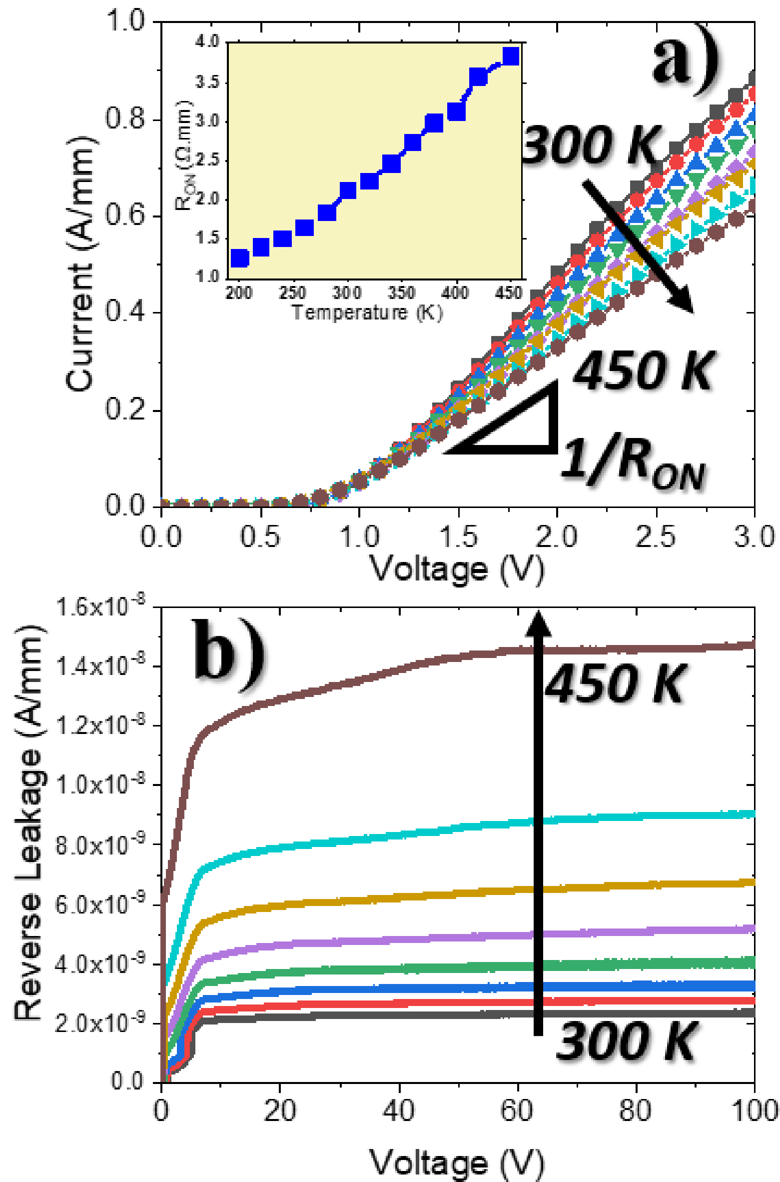

Figure 5.7: **a)** Forward IV characteristics of a Schottky barrier diode with anode-cathode spacing of 6 μm and anode length of 100 μm across the temperature range 300 - 450 K. The R_{ON} was measured from the slope of the linear region between 1.5 V and 2 V. Inset: R_{ON} as a function of temperature. **b)** Reverse leakage current of a Schottky barrier diode with anode-cathode spacing of 6 μm and anode length of 100 μm across the temperature range 300 - 450 K.

roughly linearly to 3.83 Ω·mm at 450 K as shown in the inset to Fig. 5.7a. The results show in Fig. 5.7 were used as a baseline for normalisation of dynamic R_{ON} in the temperature and field dependence experiments.

Similarly to TLM structures, the effects of stress on diode recovery were studied by subjecting the SBDs to 100 s of reverse bias stress at voltages V_{STRESS} = 50 V and 150 V. The corresponding recovery (or "detrapping") transients are shown in Figure 5.8a and b respectively. The readings

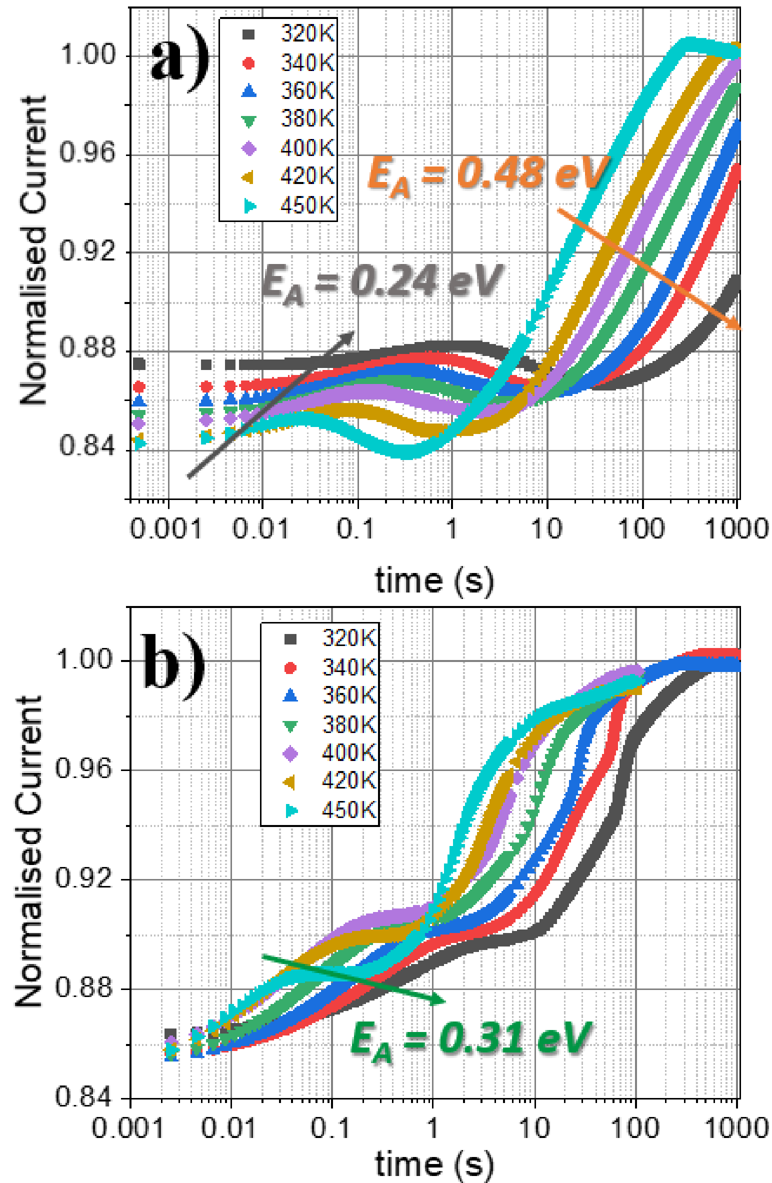

Figure 5.8: Schottky diode recovery transients measured from 100 s of stress voltage **a)** V_{STRESS} = 50 V and **b)** V_{STRESS} = 150 V for temperatures between 320 K and 450 K. Activation energies of some key processes are indicated on the plots.

were normalised to anode current measured prior to applied stress. The recovery from stress V_{STRESS} = 50 V (see in Fig. 5.8a) shows initial small positive going (increasing) transient with the activation energy of E_A = 0.24 eV, followed by a momentary slump in current before further recovery with the activation energy E_A = 0.48 eV (as before, activation energies have been extracted from the Arrhenius plot) characterised by time constants τ > 1000 s for temperatures below 380 K. Application of V_{STRESS} = 50 V results in current reduction up to 16%, which is much more significant in comparison to TLM structure under equivalent substrate stress (see

Fig. 5.4b). In addition, the recovery times for SBDs are much longer and do not tend to exceed the baseline.

When the applied stress is increased to V_{STRESS} = 150 V (see in Fig. 5.8b) two positive going (increasing) transients can be observed: first one consisting of a single time constant with activation energy E_A = 0.31 eV and second one consisting of multiple time constant, that cannot be explained by Shockley–Read–Hall recombination of carriers. The current decrease up to 15% is of similar magnitude to the current collapse induced by V_{STRESS} = 50 V, however recovery times from larger applied stress are shorter in comparison.

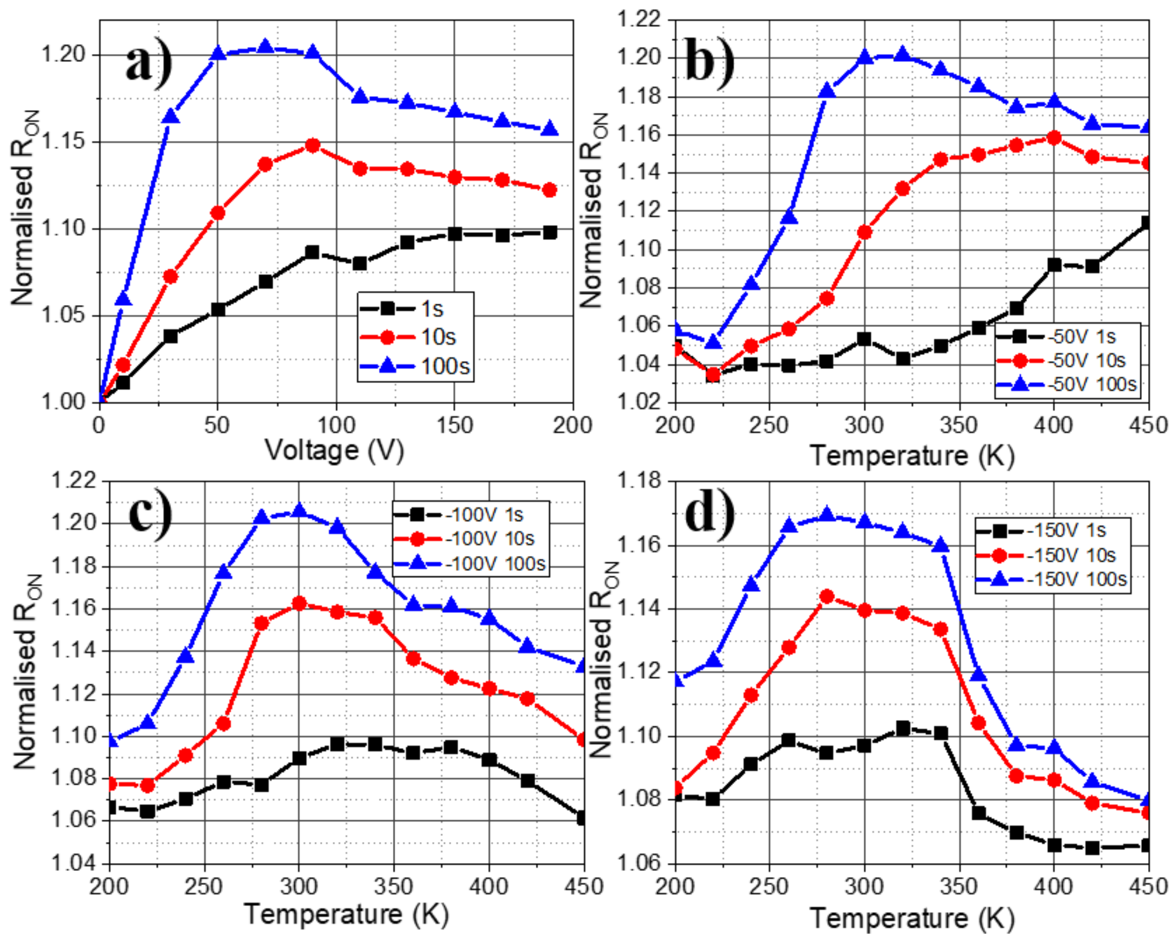

Figure 5.9: Dynamic R_{ON} measurements of a Schottky barrier diode with anode-cathode spacing of 6 μm and anode length 100 μm. **a)** Normalised dynamic R_{ON} as a function of applied reverse bias stress V_{STRESS} at 300 K for the duration of 1, 10 and 100 s. Normalised dynamic R_{ON} as a function of temperature for reverse bias stress V_{STRESS} = 50 V, 100 V and 150 V (stress duration of 1, 10 and 100 s) are shown in **b)**, **c)** and **d)** respectively.

Figure 5.9 shows the temperature and field dependence of dynamic R_{ON} in SBDs for stress duration of 1, 10 and 100 s. As the substrate stress is increased the diodes show a corresponding increase in dynamic R_{ON} followed by very gradual decline (see Fig. 5.9a). Prolonging the stress

duration results in increase in magnitude of the On-resistance (from < 10% to 20%), with the position of its peak relatively unchanged. The temperature dependence of dynamic R_{ON} shown in Fig. 5.9b-d shows similar trends: a rapid increase with temperature followed by steady reduction in measured dynamic R_{ON}. Longer stress phase results in increased dynamic On-resistance, while having little effect on the position of the peak. In comparison to TLM structure (see Fig. 5.6), the magnitude of the stress-induced On-resistance is more significant in Schottky diodes, which can be as high as 21%.

5.4 Discussion

5.4.1 TLM Structures and Vertical Transport Mechanisms

Each of the three regions shown in Figure 5.3 corresponds to a different dominant vertical charge transport process in the epitaxy and is directly related to transients τ_1 and τ_2 shown in Fig. 5.4a. Region 1 (Fig. 5.3) corresponds to charge redistribution across the C-doped buffer, which results in formation of a dipole across C - doped buffer. Negative charge accumulates at the interface between UID GaN channel and GaN:C leading to the negative going (decreasing) transient τ_1 in Fig. 5.4a. The measured activation energy of E_A = 0.21 eV indicates that activation of holes to the valence band is not the dominant charge transport mechanism, as the signature activation energy for this process is ~ 0.9 eV. Previous work on temperature and field dependence of vertical charge transport processes suggests 3D variable range hopping via the defect band is the dominant charge transport mechanism [230][92].

Increasing the substrate bias results in the increase in magnitude of transient τ_2 relative to τ_2. Likewise, the process τ_2 becomes dominant in the region 2 shown in the bidirectional substrate sweep in Figure 5.3. This mechanism is best described by band-to-band leakage across the UID GaN channel that takes place via 1D hopping along the threading dislocations. This process results in the electron flow across the channel into the 2DEG while the corresponding holes are transported to the bottom of the GaN:C buffer partially screening the GaN layers from the applied substrate potential.

As the substrate potential is increased further, eventually the positive charge accumulated at the bottom of C-doped buffer is insufficient for continued screening of the potential. Region 3 (Fig. 5.3) indicates onset of vertical leakage across the entire epitaxial stack including the strain relief layer. This process is beyond the scope of this work as it has little effect on electrical characteristics of the devices in the investigated field regime, with its time constants exceeding 1000s of seconds by a significant margin.

The recovery transients shown in Fig. 5.4b can be interpreted by considering charge transport mechanisms τ_1 and τ_2. The application of constant substrate stress over 100 s will result in variation in charge storage in the buffer depending on temperature and applied stress, as these conditions will determine how far along the processes τ_1 and τ_2 the "trapping" phase ends. Based

on the trapping transients shown in Fig. 5.4a, the "trapping" phase for applied stress V_{SUB} = -50 V for 100 s at 320 K ends shortly after completion of process τ_1. In contrast, for the same stress applied at 450 K the "trapping" phase ends soon after completion of process τ_2. As process τ_2 results in positive charging of the buffer, while process τ_1 promotes negative charging in the buffer, the recovery transient from stress applied at 450 K will show higher current than the transient measured at 300 K (as is the case in Fig. 5.4b).

Similar argument can be used to interpret the temperature and field dependence of dynamic R_{ON} in TLM structures shown in Figure 5.6. The voltage dependence of the processes τ_1 and τ_2 shows reduction in the time constants with the applied potential. This leads to initial increase in dynamic R_{ON} followed by a decrease as seen in Fig. 5.6a. Increasing the duration of the stress allows more time for the transport processes to progress, thus the peak in the R_{ON} will shift towards lower voltages for longer stress durations. Similarly, elevated temperatures lead to shorter time constants for both processes, leading to an increase followed by a drop in the dynamic R_{ON} with temperature (Fig. 5.6b-d). Increase in stress magnitude and duration results in the the peak of R_{ON} shifting towards lower temperatures.

In comparison, Schottky barrier diode show more complex recovery behaviour for equivalent applied stress. In order to gain a better understanding of the processes behind trapping and recovery in SBDs, TCAD simulations were performed in Silvaco Atlas software and analysed to explain the difference between the two structures grown on identical epitaxy.

5.4.2 Schottky Barrier Diodes - Computational Simulations

To gain a better understanding of temperature and field dependence of dynamic R_{ON} in Schottky barrier diodes, investigated structure was simulated in Silvaco Atlas TCAD software and is shown in Figure 5.10. The simulated structure consisted of 300 nm UID GaN channel, 1 μm C - doped buffer and 1.9 μm $Al_{0.7}Ga_{0.3}N$ strain relief layer. The substitution of AlN/AlGaN superlattice SRL increases computational efficiency of the model while having no appreciable effect on simulation results under investigated conditions. Total carbon concentration in the buffer was set to 2×10^{19} cm^{-3} (in agreement with SIMS profiles) with the compensation ratio of donors to acceptors equal to 0.5 [177]. The deep donors were introduced 0.8 eV above the valence band while the acceptors are situated 0.05 eV below the conduction band. The electron and hole capture cross-sections were set to 10^{-15} cm^2. The key models used in the simulation include Shockley–Read–Hall and Fermi-Dirac statistics, with the carrier mobilities governed by Caughey-Thomas velocity saturation law. In addition, 2DEG mobility was set to 1800 cm^2 V^{-1} s^{-1} and bulk hole mobility was 8 cm^2 V^{-1} s^{-1}. Finally, the non-local 1D hopping model [241] across UID channel was included (indicated by the "Hopping Model" in Fig. 5.10) to allow for electrical connection between 2DEG and GaN:C buffer that would be provided by dislocations across the channel.

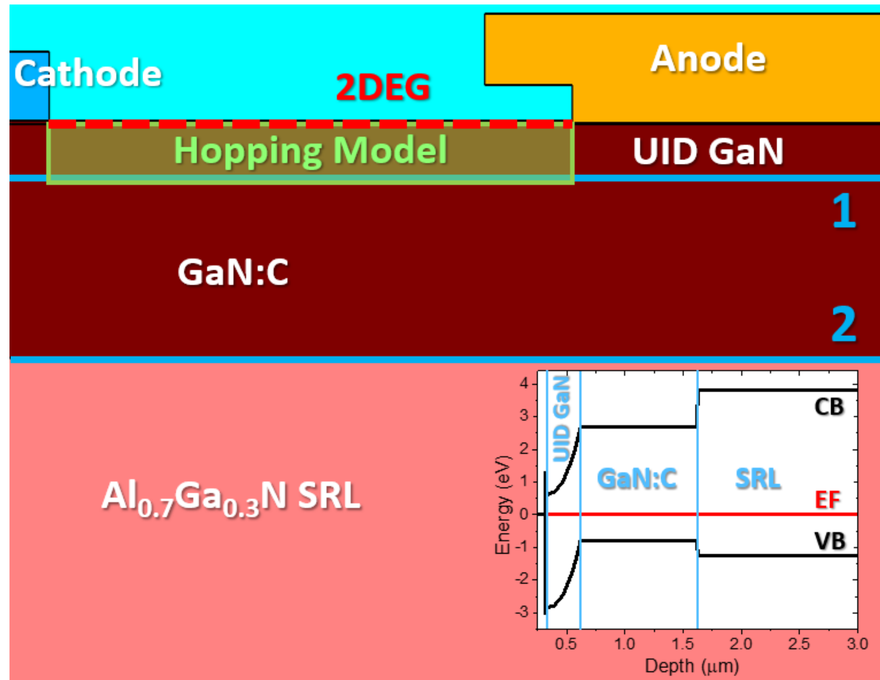

Figure 5.10: Schottky barrier diode simulated with Silvaco Atlas TCAD software. Inset: simulated vertical band diagram of the SBD. Labels 1 and 2 indicate two main cutlines (interfaces) along which charge distribution is analysed. The device parameters including the structure and doping profiles have been replicated based on the measured devices.

5.4.3 Schottky Barrier Diodes - Trapping Phase

Figure 5.11 shows simulated total net charge distribution along UID/GaN:C buffer and at the bottom of C-doped buffer during the trapping phase with the duration of 100 s for a diode shown in Fig. 5.10. The total net charge distribution was calculated by integrating charge concentration across these interfaces every 0.5 m along the length of the device. Application of large positive stress bias to the cathode (while anode and substrate are grounded) results in formation of relatively uniform dipole across the C - doped GaN buffer along the entire length of the device, with the negative charge concentration at the UID/GaN:C interface (Fig. 5.11a) initially significantly exceeding the positive charge at the bottom of C-doped buffer (Fig. 5.11b).

As the duration of the applied stress increases, charge concentration along the interfaces begins to shown non-uniform lateral distribution. Negative charge concentration at the UID/GaN:C interface increases significantly with time in the access region between the electrodes, while a small positive charge gradually builds up under the anode. Similarly, positive charge at the bottom of C-doped GaN increases in the access region and a small concentration of negative charge build us at the foot of the anode to support high lateral electric fields. Unlike in TLM structures, applied stress potential results in a non-uniform lateral field distribution in Schottky diodes. At short stress durations there is a significant electric field present across the GaN:C buffer resulting in charge redistribution and dipole formation across this layer. However, as the

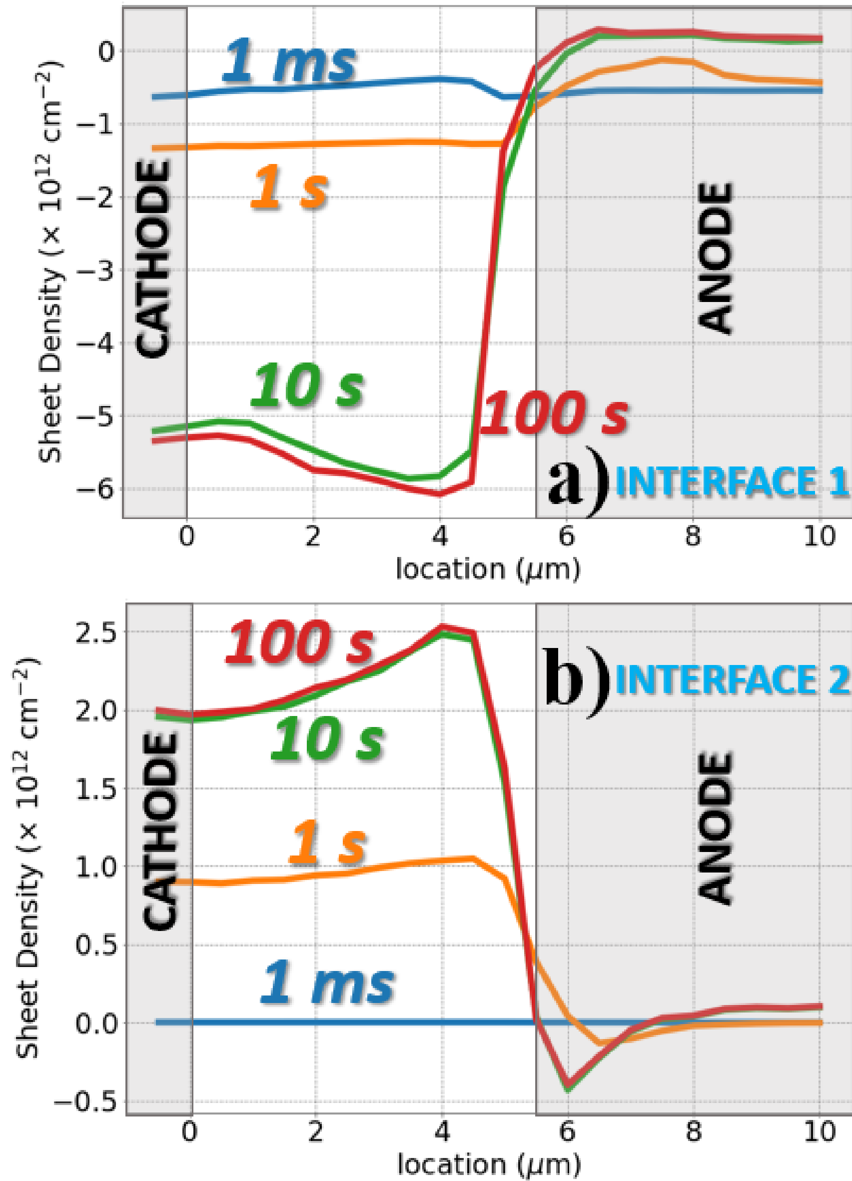

Figure 5.11: Total net sheet charge density along during trapping process along **a)** UID/GaN:C interface (1) and **b)** at the bottom of GaN:C buffer (interface 2) for trapping voltage of 150 V at 300 K. Shaded areas represent the location of cathode and anode.

stress continues the electric field builds up across UID GaN channel in the access region between the electrodes, leading to conduction via the dislocations. The charges present at interfaces also experience significant lateral electric fields, which result in non-uniform charge distribution along the investigated interfaces.

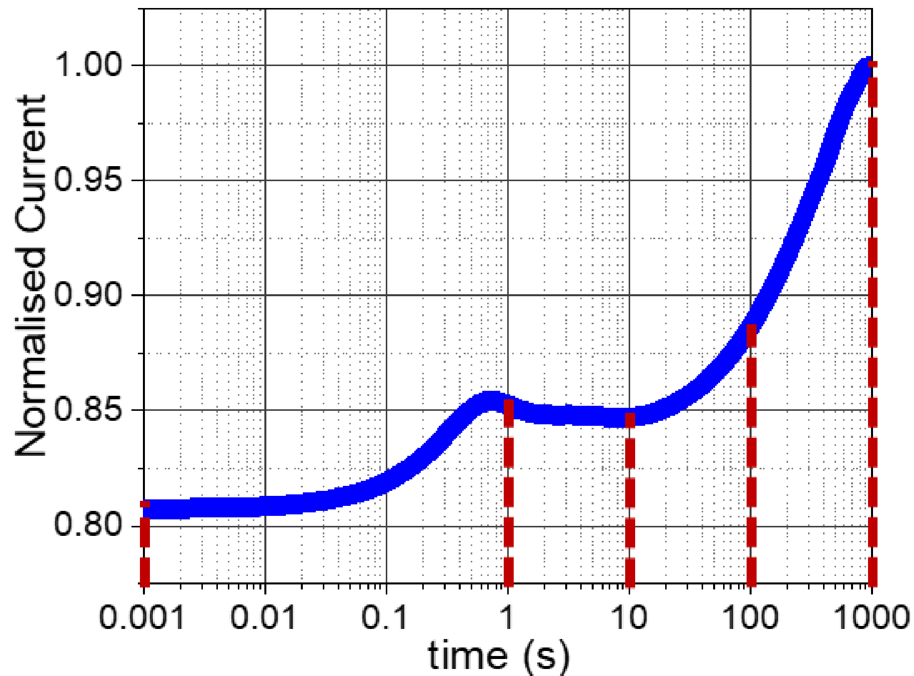

Figure 5.12: Simulated recovery transient of the SBD from 100 s of reverse bias stress V_{STRESS} = 150 V at 300 K.

5.4.4 Schottky Barrier Diodes - Recovery Phase

Figure 5.12 shows an example of a simulated recovery transient for Schottky barrier diode after 100 s of reverse bias stress V_{STRESS} = 150 V. The simulation shows good qualitative agreement with the experimental measurements (see Fig.5.8), demonstrating two distinct time constants leading to recovery. To better understand the device recovery from reverse bias stress, charge distribution along UID/GaN:C interface and at the bottom of GaN:C layer were calculated for times indicated by dashed red lines shown in Fig. 5.12. This was done by integrating charge concentration across the interface every 0.5 μm along the interface.

Figure 5.13 shows total charge concentration along the interface between UID GaN channel and GaN:C buffer and at the bottom of GaN:C buffer as outlined by cutlines 1 and 2 in Fig. 5.12 immediately after stress. Considering the charges at the UID/GaN:C interface (Fig. 5.13a), we observe high initial (at 1 ms after stress) negative charge concentration in the access region between the electrodes which drops abruptly under the anode. As more time is allowed for recovery, the difference in charge concentration between these two region reduces gradually leading to uniform charge distribution for recover times t > 10 s. Further recovery results in overall reduction in charge concentration at the interface back to the equilibrium position.

In contrast, the bottom of C-doped buffer shows initial (at 1 ms after stress) high concentration of positive charge in the access region between electrodes (however smaller than negative charge concentration at interface 1), with a small area of negative charge at the foot on the anode

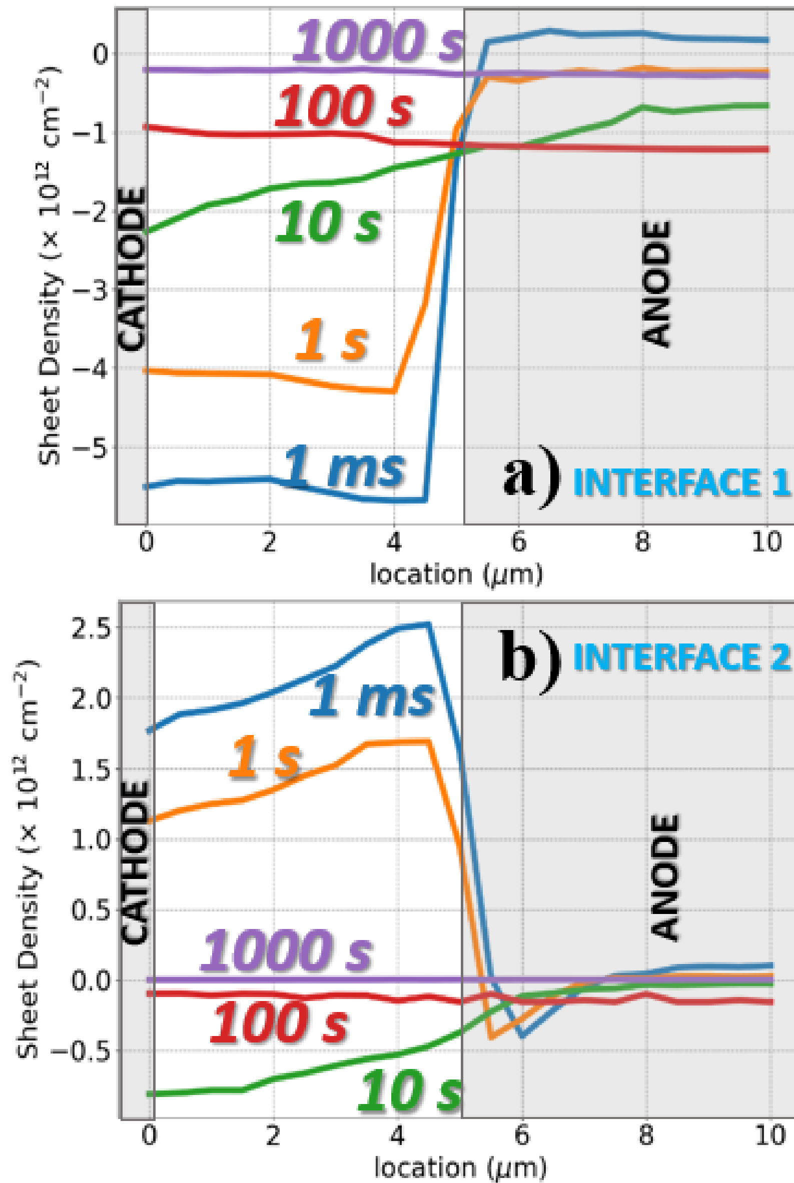

Figure 5.13: **a)** Total net sheet charge density along the UID GaN/GaN:C interface during recovery process. **b)** Total sheet charge density at the bottom of GaN:C buffer during recovery process. Shaded areas represent the location of cathode and anode.

to support high lateral electric fields (see Fig. 5.13b), followed by another region with low concentration of positive charge directly under the anode. Similar to the situation described for UID/GaN:C interface, the high positive charge concentration in the access region decreases over time leading to uniform charge distribution at times $t > 10$ s, followed by a period of slow recovery back to equilibrium with the original charge concentration of ~ 5×10^{10} cm^{-2}.

Figure 5.14 shows the simulated Schottky barrier diode immediately after reverse bias stress V_{STRESS} = 150 V with a schematic representation of the recovery process as indicated by the

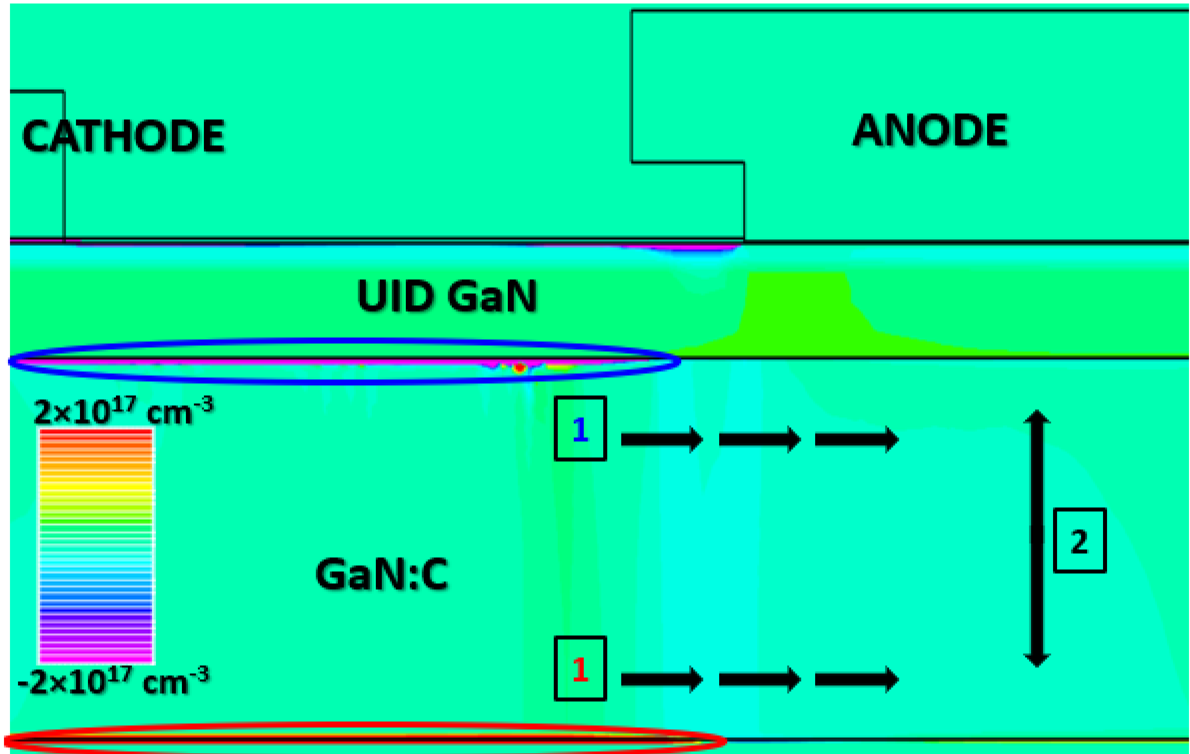

Figure 5.14: Simulated total net charge distribution immediately after 100 s of reverse bias stress V_{STRESS} = 150 V. Positive and negative charges accumulated at the bottom of GaN:C and the UID/GaN:C interface are highlighted in red and blue respectively. The arrows give a schematic representation of charge redistribution taking place in the buffer during the recovery process: lateral charge redistribution (1) is followed by vertical redistribution (2) to reach the equilibrium state.

arrows. The simulations suggest the recovery takes place via a two-step process that can be interpreted in terms of vertical and lateral charge redistribution across the buffer. Thus, the first time constant shown in Figure 5.12 represents lateral charge redistribution within the buffer at the UID/GaN:C interface and at the bottom of GaN:C layer. This process corresponds to high charge concentration in the access region between the electrodes transitioning towards the uniform charge distribution at the interfaces. Once the uniform charge distribution at the top and bottom of GaN:C buffer is achieved, the vertical charge redistribution takes place, which restores the diode to the equilibrium condition. This process corresponds to the second time constant in Fig. 5.12.

In case of TLM structures, application of substrate stress leads to uniform field distribution and hence only vertical charge redistribution takes place in the buffer, leading to significantly different recovery transient and dynamic R_{ON} dependence on applied field and temperature as compared to Schottky diodes.

In general, the recovery across the range of stress voltages and temperatures can be explained

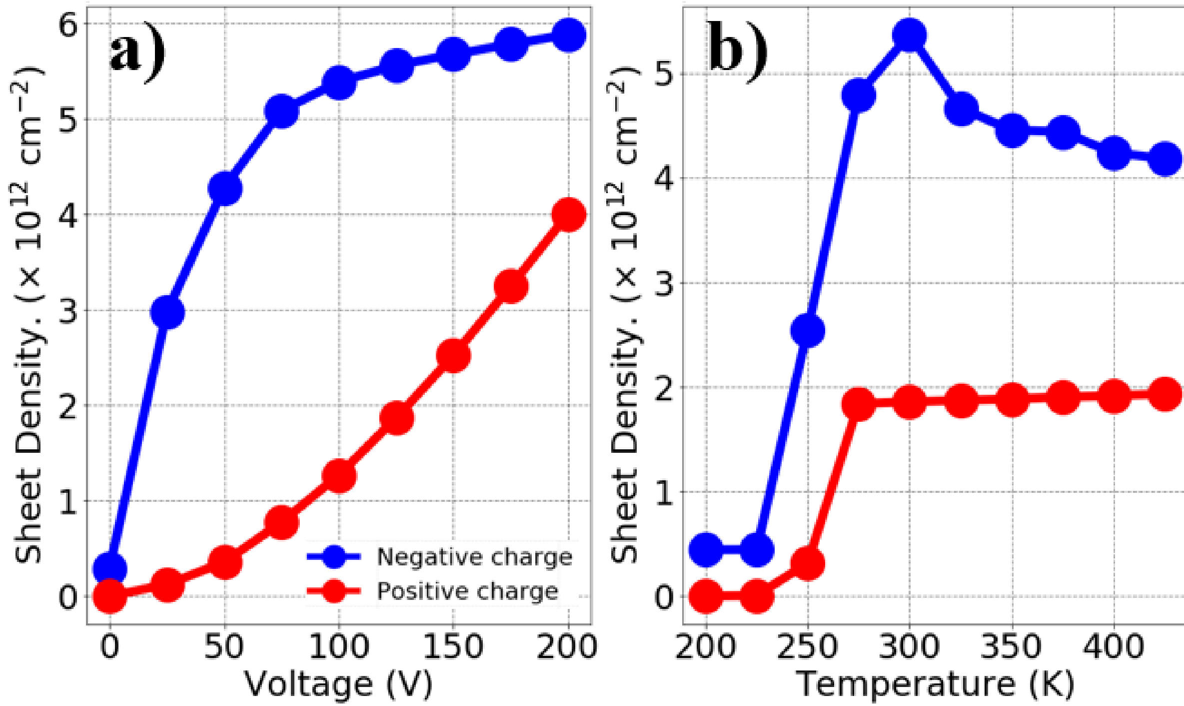

Figure 5.15: Simulated maximum total net charge concentration at the UID/GaN:C interface (negative charge) and at the bottom of GaN:C buffer (positive charge) in a Schottky barrier diode immediately after 100 s of reverse bias stress as a function of **a)** applied stress at 300 K and **b)** temperature for applied stress of 100 V. Blue data points indicate negative charge, red correspond to positive charge.

in terms of relative concentrations of positive and negative charges accumulated at the interfaces of C-doped GaN buffer during the stress phase. Figure 5.15 shows simulated maximum total net charge concentration in the access region of a Schottky barrier diode at the UID/GaN:C interface and at the bottom of C-doped buffer as a function of applied reverse bias stress (Fig. 5.15a) and temperature (Fig. 5.15b). The dependence of dynamic R_{ON} on the applied stress shown in Fig. 5.9a can be interpreted in terms of relative concentration of charges accumulated at the top and bottom of GaN:C layer. The initial sharp increase in dynamic R_{ON} can be associated with significant increase in negative charge concentration at the UID/GaN:C interface with applied potential. This observation can be explained by charge redistribution across C-doped buffer, which takes place at lower stress voltages. As the reverse bias stress is increased beyond V_{STRESS} = 75 V the rise in net negative charge concentration gradually slows down. At the same time, the positive charge at the bottom of GaN:C buffer steadily increases with the applied potential (roughly as ${V_{STRESS}}^{1.5}$), as at conduction via dislocations becomes the dominant charge transport process at higher stress voltages. The change in relative charge concentrations immediately after stress results in slow reduction in R_{ON} observed in the experiment.

Similarly, the variation of dynamic R_{ON} with temperature (see Fig. 5.9b-d) can be associated

with a sudden increase in negative charge concentration at the UID/GaN:C interface, reaching its peak value at 300 K followed by a gradual decline. Meanwhile, the positive charge concentration at the bottom of GaN:C buffer slowly builds up leading to a gradual reduction in the observed R_{ON}.

5.5 Conclusions

The understanding of the origins of dynamic On-resistance in GaN-based power devices is of crucial importance for designing highly efficient and commercially competitive power devices. In the previous chapter we have identified key vertical charge transport processes taking place in GaN buffers. Here, the relationship between the dynamic R_{ON} and charge transport processes is explored in more detail.

Bidirectional substrate ramp sweeps are performed on TLM structures across a wide range of temperatures, which in combination with substrate stress transient measurements allow for separation of key charge transport processes in the buffer. Temperature and field dependence of dynamic R_{ON} in the TLM structures is measured and the results can be accounted for by considering variation in time constants of vertical charge transport processes taking place in the GaN buffer with the applied stress and temperature conditions.

In contrast to TLM structures, Schottky barrier diodes grown on identical epitaxy show more severe current collapse in response to equivalent stress with two-step recovery transients. In addition, dynamic R_{ON} shows more significant increase across the investigated range of temperatures and stress potentials, with overall response different to TLM structures.

Computational simulations of Schottky diodes reveal that the applied reverse bias stress results in non-uniform charge distribution across the UID/GaN:C interface and at the bottom of GaN:C buffer. The two-step recovery from stress can be explained in terms of lateral charge redistribution, followed by vertical redistribution restoring the device to equilibrium state. Temperature and field dependence of dynamic R_{ON} in SBDs results from variation in concentration of positive and negative charges accumulated at the top and bottom of GaN:C in the access region between the electrodes.

We therefore demonstrate, that the dynamic R_{ON} in the TLM structures and Schottky barrier diodes is dominated by vertical and lateral charge transport processes and not buffer trapping as is often suggested. %

CHAPTER 6

Electrical and Thermal Characterisation of "Buffer-Free" GaN-on-SiC HEMTs

This chapter focuses on thermal and electrical characterisation of early generation high performance microwave GaN-on-SiC GaN HEMTs fabricated on a heterostructure without the conventional thick, highly-doped buffer ("buffer-free" design also known as QuanFINE technology) grown by the novel transmorphic process [247]. Micro-Raman thermography measurements were performed on the "buffer-free" and conventional GaN HEMT structures for power dissipation up to 8 W/mm. Experimental results were combined with 3D Ansys FEA simulations to analyse the temperature profiles in the investigated devices. Conventional GaN-on-SiC HEMTs show peak channel temperature of 141.8 °C at 8 W/mm and the effective thermal boundary resistance between the GaN buffer and the substrate (TBR_{eff}) was calculated as 30 m^2 K GW^{-1}. In contrast, peak channel temperature of "buffer-free" HEMTs was determined as 155.6 °C at 8 W/mm with the TBR_{eff} of 10 m^2 K GW^{-1}, indicating high quality interface between the channel and the substrate. The effects of GaN thickness and effective thermal boundary resistance between GaN and the substrate are analyzed suggesting the latter to be a critical parameter for thermal performance for “buffer-free” epitaxy.

The electrical measurements are performed on both sets of devices: "buffer-free" HEMTs and conventional devices with thick buffer for comparison. Electrical characteristics of the structures with thick buffer shows conventional drain-induced barrier lowering (DIBL) with little hysteresis or stretch-out in the IV characteristics. In contrast, "buffer-free" GaN HEMTs show significant DIBL and stretching of the IdVg characteristics with applied drain bias especially for gate length L_G = 150 nm. Experimental results are combined with electrical simulations performed using Silvaco Atlas TCAD software indicating compromised confinement of electrons in the channel due to reduced polarization charge of the AlN nucleation layer. Further analysis reveals methods

for improved channel control.

The structures used in this study were grown by SweGaN AB, while the fabrication was performed by Leonardo S.p.A. All the experimental work and simulations were performed by the author.

6.1 Introduction

GaN-based High Electron Mobility Transistors (HEMTs) possess a range of advantages over competing materials for RF applications including high electron mobilities, large breakdown fields and power outputs on the order of 30 W/mm [248][29]. However, DC-RF dispersion (or "current collapse") caused by charge trapping in the buffer still poses a major issue for GaN based RF devices [249]. Conventional GaN HEMT epitaxy requires introduction of thick GaN buffer which serves two main purposes. Firstly, it provides a physical separation between 2DEG and the interface between the GaN buffer and the AlN nucleation layer (NL). Due to lattice mismatch and thermal expansion coefficient difference between GaN and SiC, the GaN/AlN NL interface shows high concentrations of dislocations, pits and defects that could compromise the electrical performance of the device and lead to reduction in 2DEG density [250]. Thicker GaN buffer allows for reduction in crystalline defects formed during nucleation [251][252]. Secondly, the buffer serves to provide vertical insulation. Reduced leakage currents (and thus higher breakdown voltage), better carrier confinement in the channel and suppression of the short channel effects are among the most important advantages of the thick GaN buffer.

Buffer insulation is commonly achieved by introduction of intentional dopants such as C and Fe, with the latter being a preferred for RF applications as C doping results in more significant current collapse in RF operation [85]. Even with Fe doping present in the buffer, charge trapping in this layer and consequent DC-RF dispersion is still an issue affecting RF devices [253]. One solution to the issue of buffer trapping involves complete removal of thick doped buffer layer and growth of the GaN channel directly on the nucleation layer. Previous attempts to grow think GaN layers directly on the nucleation layer show significantly increased numbers of defects and threading dislocations resulting in deterioration of carrier density and mobility as shown in [254] and [255]. However, recently Chen *et al.* have successfully fabricated high performance microwave GaN-on-SiC HEMT without a conventional thick buffer structure, with extrinsic f_T of 70 GHz and f_{MAX} of 130 GHz [256].

However, in addition to electrical benefits resulting from removing the highly doped buffer, the main motivation behind creating a "buffer-free" design relates directly to thermal management and costs of production. By growing thinner GaN layers the peak of the Joule heating present during device operation lies closer to high thermal conductivity substrate. Provided the defect formation at the NL/UID GaN interface is managed well, the heat dissipation should be more effective than in conventional GaN HEMTs alleviating the issue of self-heating. In addition,

growth of thin GaN layers results in reduction of raw materials used for growth (including precursor gases) by 90% and in shorter deposition times [257]. Thus, the manufacturing costs are significantly minimized while the uptime of the MOCVD reactor is increased.

The main objective of this work is a comprehensive electrical and thermal analysis of the early generation "buffer-free" GaN-on-SiC HEMTs provided by SweGaN AB. Thermal analysis was performed using a combination of Raman thermography measurements and Ansys simulations. The electrical measurements rely on DC and pulsed IV characterisation in tandem with TCAD simulations. The results show excellent thermal performance of the devices due to high quality AlN nucleation layer (and thus low TBR_{eff}), however the electrical measurements indicate compromised carrier confinement especially for the devices with short gate lengths.

6.2 Experimental Details

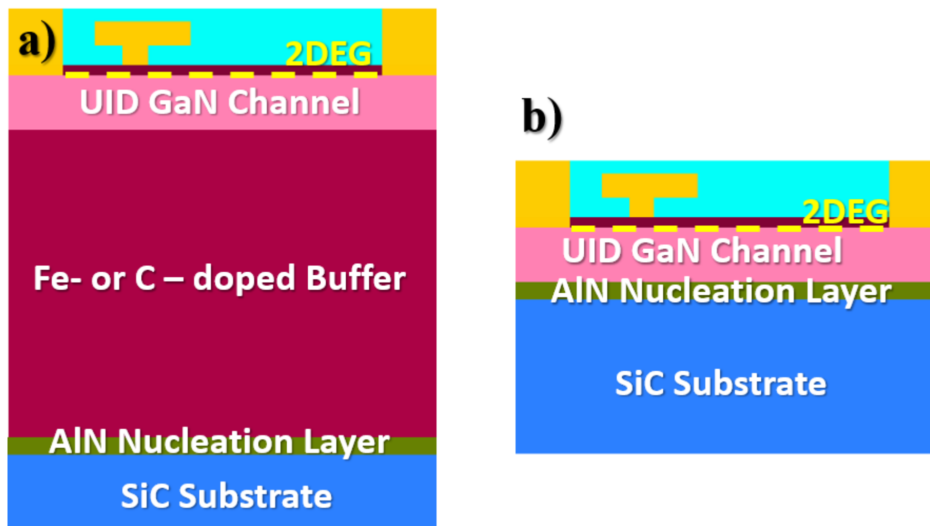

Figure 6.1: Comparison between **a)** conventional GaN HEMT design featuring thick doped buffer and **b)** QuanFINE technology described in this chapter.

Figure 6.1 shows the general concept of the QuanFINE ("buffer-free") GaN-on-SiC HEMT technology compared to conventional device design. The epitaxial structure consists of 480 μm vanadium doped 4H on-axis SiC semi-insulating substrate, 60 nm AlN nucleation layer and 250 nm UID GaN channel, 14 nm AlGaN barrier (with the Al content of 29%) and 2 nm GaN cap. The nitride layers were grown on top of Si-face of the substrate in a commercial hot-wall metal-organic chemical vapour deposition (MOCVD) reactor using high-purity (>99.999%) ammonia (NH_3), trimethylaluminium (TMAl) and trimethylgallium (TMGa) as precursor gasses for N, Al and Ga, diluted in the mixture of H_2 and N_2 carrier gasses at the pressure of 50 mbar. To achieve high quality thin AlN nucleation layer, the growth was performed at elevated temperatures in comparison to conventional MOCVD deposition.

In this study, the measurements were performed on 2-finger transistor with gate lengths of 150 nm and 250 nm and gate width of 50 μm. The channel length of the devices was 4 μm and 3 μm for gate lengths of 250 nm and 150 nm respectively. The fabricated structures did not possess field plates to allow for laser access to the gate-drain access region. In addition to "buffer-free" transistors, a set of control devices containing thick 2 μm Fe-doped buffer with identical geometry to QuanFINE devices and processed in the identical way (see Fig. 6.1a) were also measured for comparison.

The main techniques used for electrical characterisation of the GaN HEMTs involved DC and pulsed IV measurements. Dimensions of the devices under test are: two 50 μm-wide gate fingers, pitch of 12 μm, gate length 150 nm and 250 nm and channel lengths of 3 μm and 4 μm respectively. Figure 6.2 shows a schematic representation of a pulsed IV measurement. In this experiment the duty cycle was set to 0.1% with non-quiescent (ON) time of 1 μs and quiescent (OFF) time of 1 ms. The rise time was set to 50 nm. To avoid hard switching time offset between the drain and gate pulses has been introduced, such that the gate stress $V_{G,STRESS}$ below threshold was present for the entire duration of the drain stress pulse $V_{D,STRESS}$. The aim of electrical characterisation was to investigate the output characteristics of the devices, with particular focus on short-channel effects and carrier confinement.

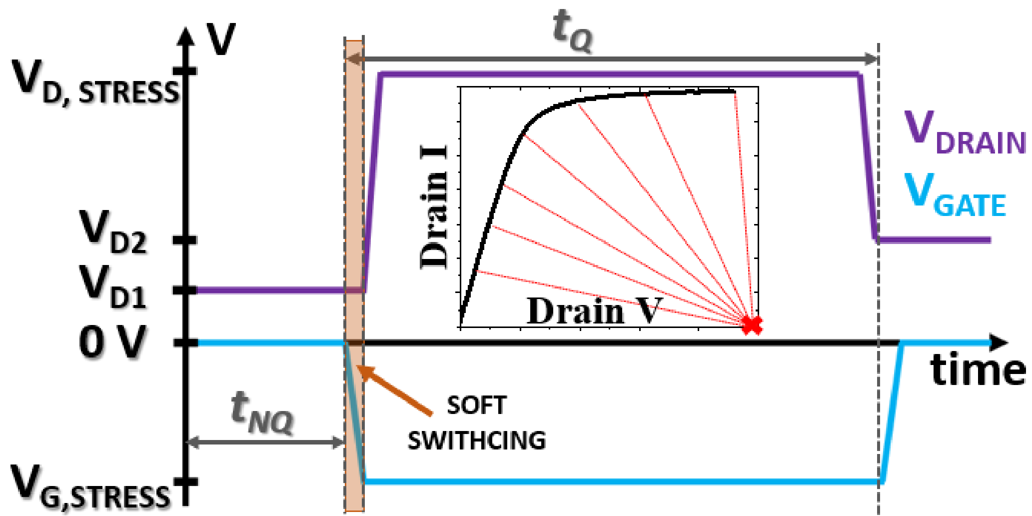

Figure 6.2: Schematic representation of measurement timeline of a pulsed IV measurement. The duty cycle is determined by the ratio of time spent in the non-quiescent state (t_{NQ}) to time spent in the quiescent state (t_Q). The inset shows the relationship between the IV measurement (measured in NQ) state and the OFF state (Q state with gate voltage $V_{G,STRESS} < V_{TH}$ and large drain bias $V_{D,STRESS}$).

GaN temperatures were measured by micro-Raman thermography, using a 488 nm frequency double diode laser and an 0.5 NA objective lens. The temperature was measured close to the hot spot at a distance of 0.5 μm from the gate edge by a diffraction limited lateral focal spot with the diameter of 0.5 μm. Figure 6.3 shows a schematic representation of the experimental

measurement. The temperature dependence of GaN E_2 high and A_1 (LO) phonons was calibrated for in the range of 25 - 120°C. The measurement was performed by operating the devices at power dissipations up to 8 W/mm (V_{DRAIN} = 15 V) while recording the shift in E_2 and A_1 modes in relation to pinch off. This was done to account for phonon frequency change induced by the strain resulting from inverse piezoelectric effect. Throughout the experiment, the base temperature of the transistors was kept at 25 °C using a thermo-electric vacuum chuck. For each sample three device were measured and each measurement repeated 3 times, resulting in a mean standard error of approximately ±5°C.

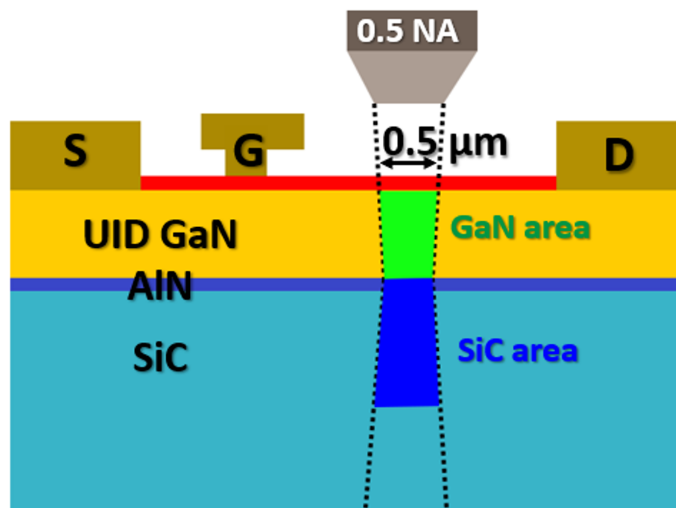

Figure 6.3: Schematic representation of micro-Raman thermography measurement performed om the "buffer-free" structure using a 488 nm frequency double diode laser and the 0.5 NA objective lens. The measurement is depth averaged as indicated by the shaded areas.

Additional compressive thermomechanical strain is induced by the high temperature gradient around the hot spot during device operation, which is not present during temperature calibration [258]. If not corrected for, this causes the temperatures derived from micro-Raman thermography measurement to underestimate the real temperatures of the transistor. To account for any strain present in the epitaxy during device operation, thermomechanical strain temperature correction is applied to the results as outlined in section 3.3.2. This method is based on examining the difference between temperatures derived from Raman shifts of E_2 high and A_1(LO) modes relative to the Off-state measurement. By considering the temperature and strain dependence of phonon frequency for each mode, the corrected (real) GaN temperature can be calculated.

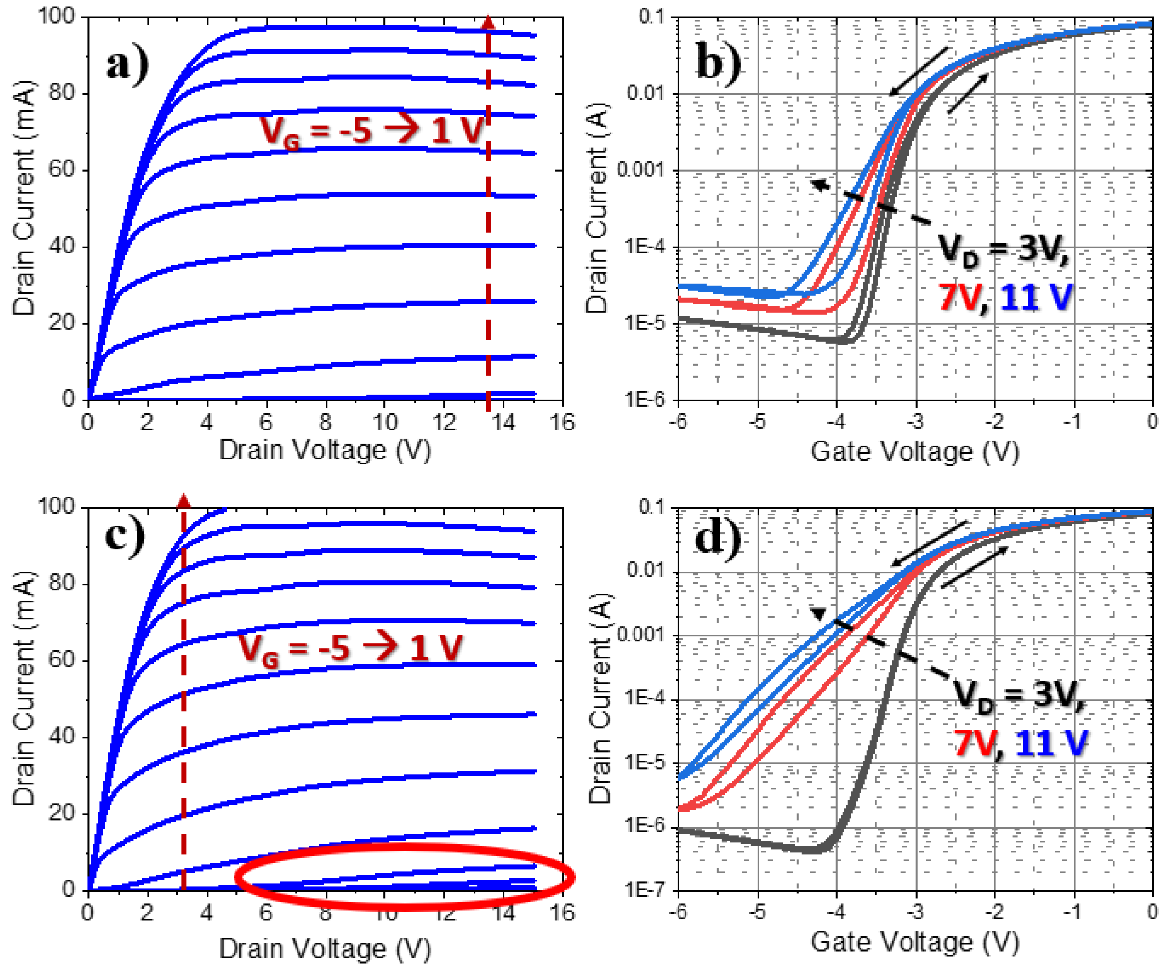

Figure 6.4: **a)** DC IdVd measurement of "buffer-free" GaN HEMT with gate length L_G = 250 nm for gate voltages V_G = -5 V → 1 V in steps of 0.5 V. **b)** Bidirectional DC IdVg sweep (arrows indicate the direction of the sweep) measured for "buffer-free" GaN HEMT with gate length L_G = 250 nm for drain voltages V_D = 3 V, 5 V and 7 V. **c)** DC IdVd measurement of "buffer-free" GaN HEMT with gate length L_G = 150 nm for gate voltages V_G = -5 V → 1 V in steps of 0.5 V; the red circle highlights punch through observed in the devices with L_G = 150 nm. **d)** Bidirectional DC IdVg sweep (arrows indicate the direction of the sweep) measured for "buffer-free" GaN HEMT with gate length L_G = 150 nm for drain voltages V_D = 3 V, 5 V and 7 V.

6.3 Results

6.3.1 Electrical Characterisation

This section describes DC and pulsed IV characterisation of early generation QuanFINE "buffer-free" GaN-on-SiC HEMTs in comparison with conventional GaN-on-SiC HEMT with thick doped buffer. Figure 6.4 shows DC IV measurements performed on the "buffer-free" GaN-on-SiC HEMTs for devices with gate lengths L_G = 250 nm (Fig. 6.4a b) and L_G = 150 nm (Fig. 6.4c d). Two devices with gate length of 150 nm and three devices with gate length of 250 nm were tested,

showing uniform behaviour within individual sets. The IdVd (Fig. 6.4a & c) measurements for both sets of devices show clear transition from linear to saturation regions with very little self-heating present. The On-resistance was measured as 2.48 Ω·mm and 2.13 Ω·mm for L_G = 250 nm and 150 nm respectively. However, devices with shorter gate length show signs of punch-through as highlighted in Fig. 6.4c, which is manifested by significant increase in drain current with applied drain voltage for gate voltages below threshold.

Both sets of devices show significant decrease in threshold voltage with the applied drain potential, however this effects if more prominent in the devices with shorter gate lengths (see Fig. 6.4b d for comparison). In both cases, this results in a shift in the transconductance peak without affecting its magnitude. In addition, transistors with gate length L_G = 150 nm exhibit sizeable stretch-out in the IdVg characteristics, which does not seem to affect the devices with L_G = 250 nm to a similar extent.

Figure 6.5 shows IV characteristics for conventional GaN HEMTs with thick GaN buffer. The On-resistance for devices with gate length of 250 nm and 150 nm was measured as 3.00 Ω·mm and 2.58 Ω·mm respectively. In contrast to "buffer-free" devices, the conventional GaN HEMTs show no significant punch-through or other short channel effects even for gates lengths as short as 150 nm. In addition, IdVg characteristics show noticeable difference between "buffer-free" (Fig. 6.4 b & d) and conventional GaN HEMTs with thick buffer (Fig. 6.5 b & d). In case of the conventional devices, increase in drain potential results in relatively minor shift in threshold voltage even for structures with gate length L_G = 150 nm. Moreover, the IdVg characteristics show little stretching or hysteresis contrary to "buffer-free" HEMTs.

Figure 6.6 shows a comparison of gate leakage currents between "buffer-free" GaN HEMT (Fig. 6.6a) and a conventional device with thick buffer (Fig. 6.6b). The leakage currents for both sets of devices are at a similar level of a few micro amperes, suggesting the differences in the measured IdVg characteristics (and in particular the stretch-out observed in the "buffer-free" devices) cannot be attributed to the gate leakage. The exponential increase in gate current for both sets of devices indicates gate leakage becomes the dominant contribution to the Off-state current at gate voltages below the threshold.

Figure 6.7 shows the dependence of threshold voltage on the applied drain potential for "buffer-free" GaN HEMTs (Fig. 6.7a) and conventional GaN HEMTs with thick buffer (Fig. 6.7b). In this work, we define threshold voltage as gate voltage at which drain current reaches 10 mA/mm. In addition, drain-induced barrier lowering (DIBL) is defined as the change in threshold voltage shift between applied drain bias of 1 V and 12 V.

Both "buffer-free" and conventional GaN-on-SiC HEMTS show initial rapid decrease in threshold voltage with applied drain potential. As the drain bias is increased further, its effect on V_{TH} becomes weaker. The DIBL values measured for "buffer-free" GaN HEMTs are 42 mV/V and 95 mV/V for devices with gate length of 250 nm and 150 nm respectively. In contrast, the conventional GaN devices show roughly half of DIBL values for the corresponding gate lengths:

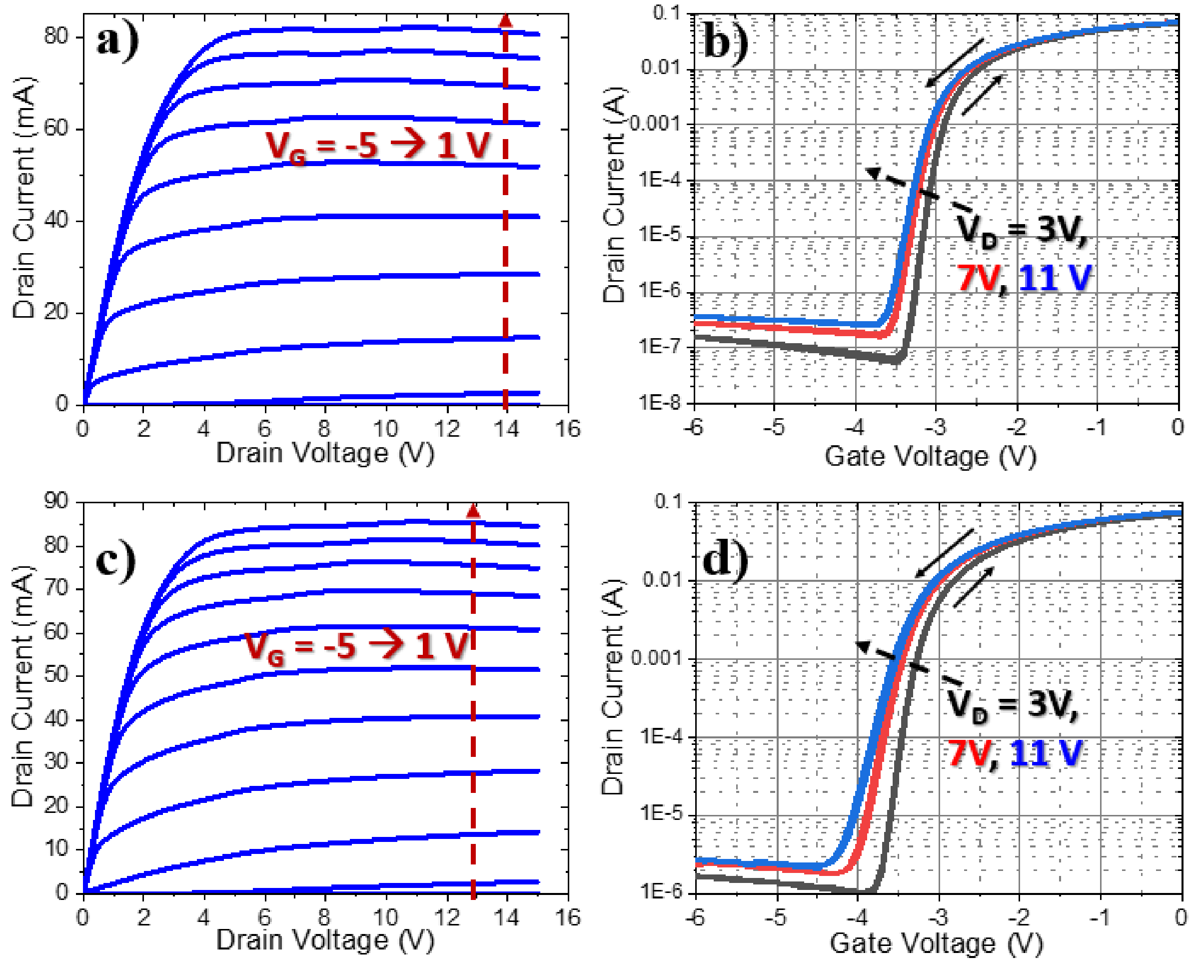

Figure 6.5: **a)** DC IdVd measurement of conventional GaN HEMT with gate length L_G = 250 nm for gate voltages V_G = -5 V → 1 V in steps of 0.5 V. **b)** Bidirectional DC IdVg sweep (arrows indicate the direction of the sweep) measured for conventional GaN HEMT with gate length L_G = 250 nm for drain voltages V_D = 3 V, 5 V and 7 V. **c)** DC IdVd measurement of conventional GaN HEMT with gate length L_G = 150 nm for gate voltages V_G = -5 V → 1 V in steps of 0.5 V. **d)** Bidirectional DC IdVg sweep (arrows indicate the direction of the sweep) measured for conventional GaN HEMT with gate length L_G = 150 nm for drain voltages V_D = 3 V, 5 V and 7 V.

26 mV/V and 40 mV/V for L_G = 250 nm and 150 nm respectively.

To investigate the effects of trapping on the observed DC IV characteristics, pulsed measurements were performed on both sets of samples. Figure 6.8 shows a set of pulsed IV characteristics for devices with gate length of 250 nm and 150 nm. All the measurements were performed at the duty cycle of 0.1% (t_{ON} = 1 μs, t_{OFF} = 1 ms). For IdVd measurements, three distinct stress conditions were chosen: [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V], [0V, -6V] and [15V, -6V]. The results indicate the application of gate stress has little effect on the output characteristics, while additional drain stress results in only a small current decrease for both L_G = 150 nm and 250 nm sets of devices (Fig 6.8a & c). Similar to DC measurements (see Fig. 6.4), the devices with L_G = 150 nm show

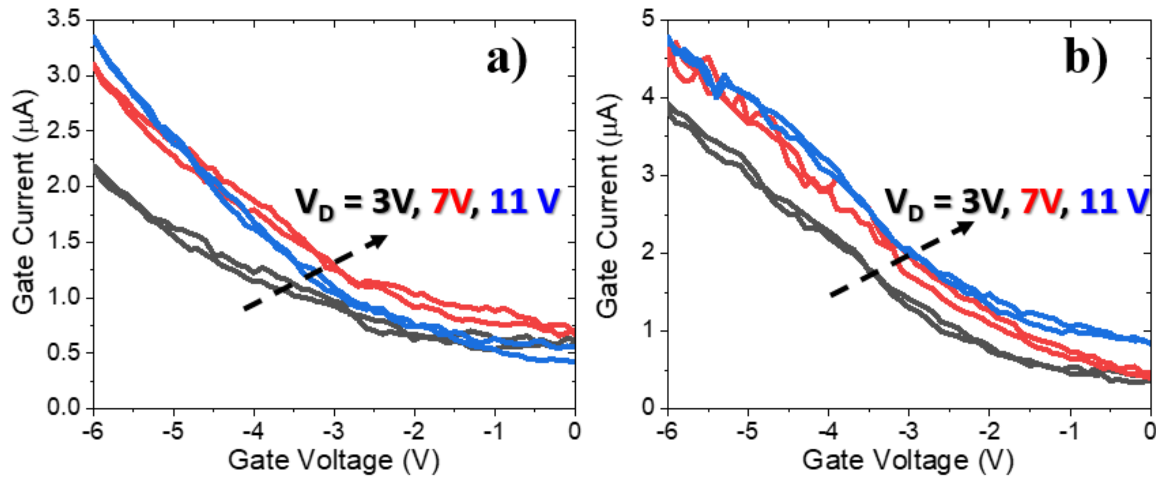

Figure 6.6: **a)** Gate leakage current of a "buffer-free" GaN HEMT as a function of gate voltage for a DC sweep at drain voltages of 3 V, 7 V and 11 V. **b)** Gate leakage current of a conventional GaN HEMT with a thick buffer as a function of gate voltage for a DC sweep at drain voltages of 3 V, 7 V and 11 V.

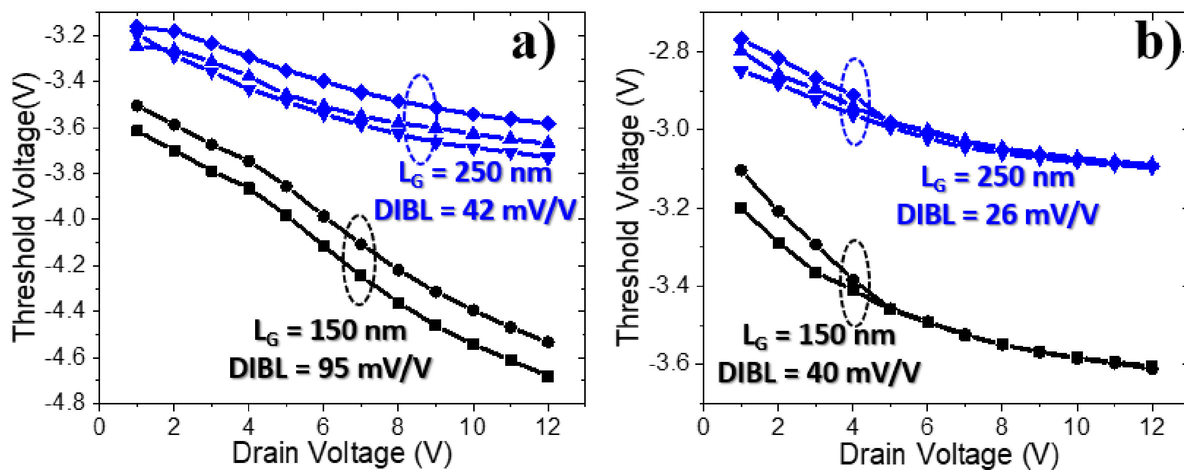

Figure 6.7: **a)** Threshold voltage as a function of applied drain bias for "buffer-free" GaN HEMTs with gate length of L_G = 150 nm (2 transistors) and 250 nm (3 transistors). **b)** Threshold voltage as a function of applied drain bias for conventional GaN HEMT devices with thick buffer for gate length of L_G = 150 nm (2 transistors) and 250 nm (3 transistors).

punch-through at gate voltages below threshold (highlighted in Fig 6.8c).

Pulsed IdVg measurements were performed from the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V] to reduce the effects of self-heating and potential trapping on the output characteristics (Fig 6.8b & d). The devices with gate length of 150 nm show more significant threshold voltage shift compared to devices with L_G = 250 nm, which has also been observed in the DC measurements. However, even the transistors with longer gate lengths show stretch-out in pulsed IdVg characteristics. In addition, the devices show higher off-state leakage than in the DC sweep.

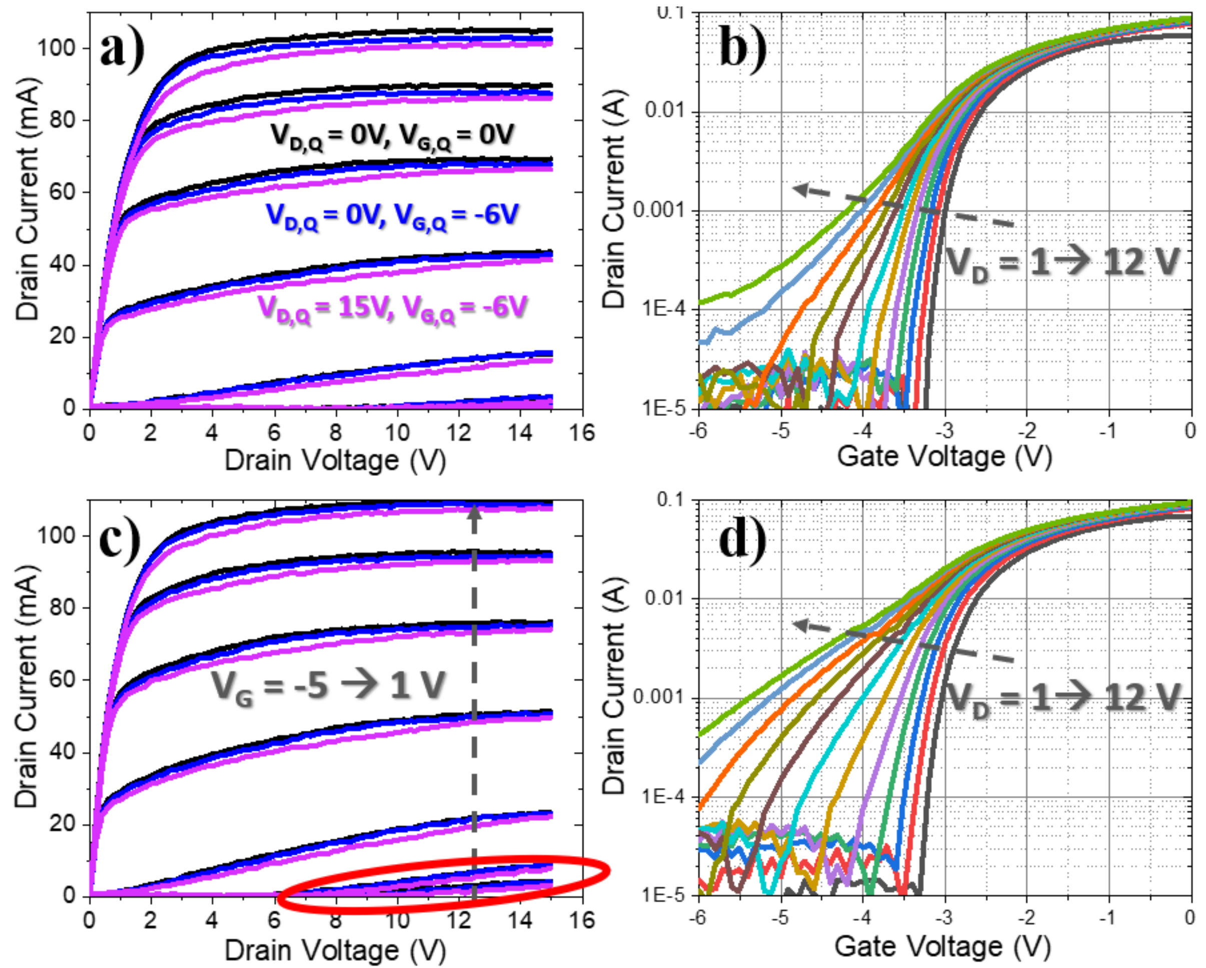

Figure 6.8: **a)** Pulsed IdVd measurement of "buffer-free" GaN HEMT with gate length L_G = 250 nm for gate voltages V_G = -5 V → 1 V in steps of 1 V. Measurement duty cycle = 0.1% (t_{ON} (non-quiescent) = 1 μs, t_{OFF} (quiescent) = 1ms); quiescent (stress) points are [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V], [0V, -6V] and [15V, -6V]. **b)** Pulsed IdVg sweep measured for "buffer-free" GaN HEMT with gate length L_G = 250 nm for drain voltages V_D = 1 V → 12 V in steps of 1 V. Measurement duty cycle = 0.1%, Quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V]. **c)** Pulsed IdVd measurement of "buffer-free" GaN HEMT with gate length L_G = 150 nm for gate voltages V_G = -5 V → 1 V in steps of 1 V; the red circle highlights punch through observed in the devices with L_G = 150 nm. Measurement duty cycle = 0.1%; quiescent (stress) points are [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V], [0V, -6V] and [15V, -6V]. **d)** Pulsed IdVg sweep measured for "buffer-free" GaN HEMT with gate length L_G = 150 nm for drain voltages V_D = 1 V → 12 V in steps of 1 V. Measurement duty cycle = 0.1%, Quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V].

Pulsed IdVd measurements of conventional GaN-on-SiC HEMTs with thick buffer show little change in current with the application of quiescent gate stress of -6 V (Figure 6.9a & c). However, unlike for "buffer-free" devices, the application of quiescent stress [$V_{D,Q}$, $V_{G,Q}$] = [15 V, -6 V] results in noticeable current collapse up to 12%. Figure 6.9b & d shows pulsed IdVg measurements performed on the conventional GaN HEMTs from the quiescent bias point [$V_{D,Q}$,

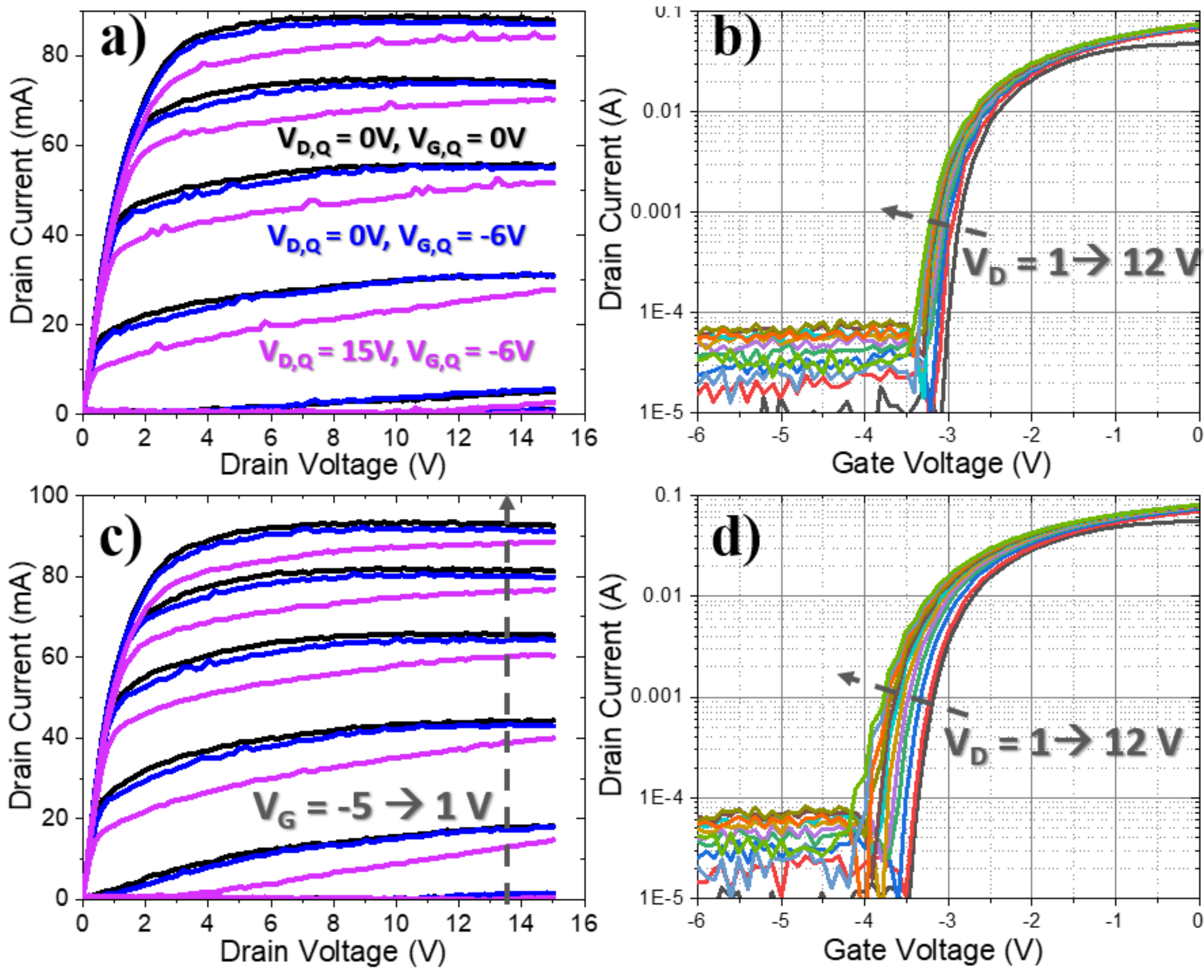

Figure 6.9: **a)** Pulsed IdVd measurement of conventional GaN HEMT with gate length L_G = 250 nm for gate voltages V_G = -5 V → 1 V in steps of 1 V. Measurement duty cycle = 0.1% (t_{ON} (non-quiescent) = 1 μs, t_{OFF} (quiescent) = 1ms); quiescent (stress) points are [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V], [0V, -6V] and [15V, -6V]. **b)** Pulsed IdVg sweep measured for conventional GaN HEMT with gate length L_G = 250 nm for drain voltages V_D = 1 V → 12 V in steps of 1 V. Measurement duty cycle = 0.1%, Quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V]. **c)** Pulsed IdVd measurement of conventional GaN HEMT with gate length L_G = 150 nm for gate voltages V_G = -5 V → 1 V in steps of 1 V. Measurement duty cycle = 0.1%; quiescent (stress) points are [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V], [0V, -6V] and [15V, -6V]. **d)** Pulsed IdVg sweep measured for conventional GaN HEMT with gate length L_G = 150 nm for drain voltages V_D = 1 V → 12 V in steps of 1 V. Measurement duty cycle = 0.1%, Quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V].

$V_{G,Q}$] = [0V, 0V] for drain voltages between 1 V and 12 V. In comparison to "buffer-free" HEMTs these devices show little to no signs of stretch-out indicating good carrier confinement in the channel. However, similar to DC measurements, the devices with shorter gate length show bigger change in threshold voltage than the transistors with L_G = 250 nm. In contrast to "buffer-free" HEMTs, the comparison between DC and pulsed IdVg measurements of the conventional devices shows little variation in the measured drain current.

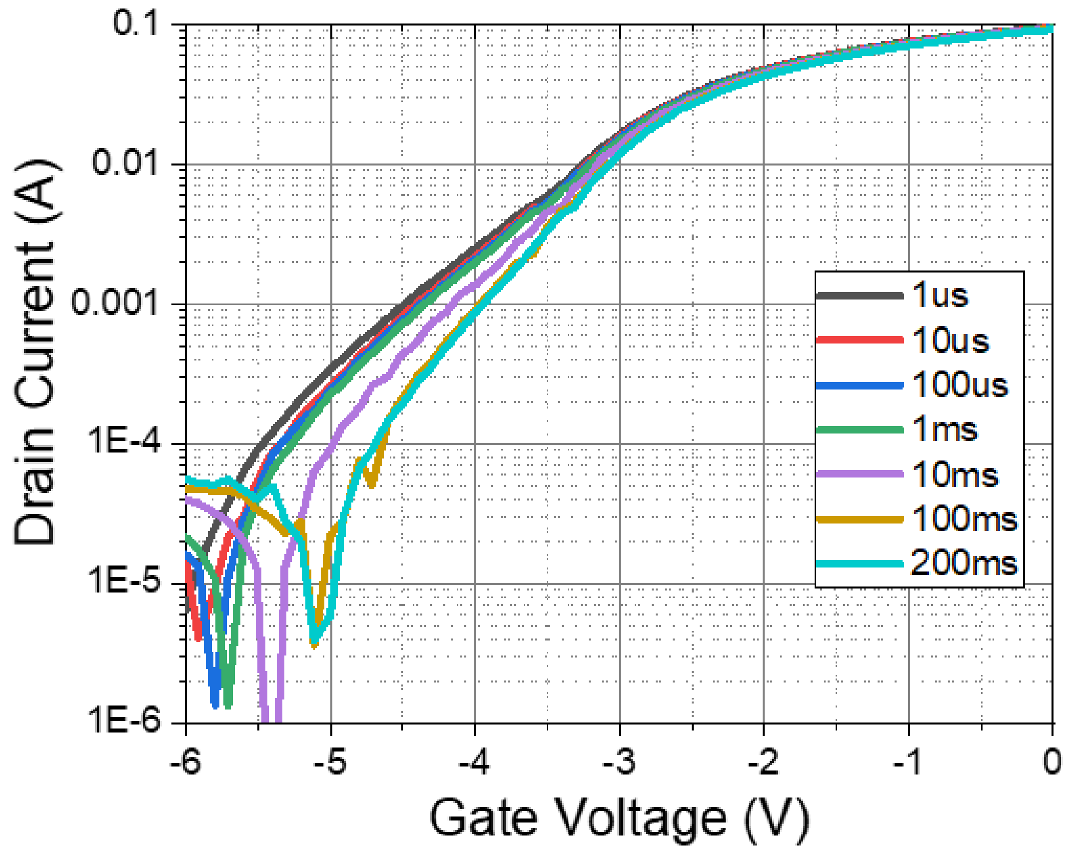

Figure 6.10: Pulsed IdVg measurement of the "buffer-free" GaN HEMT for the drain voltage of 7 V from the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [15V, -7V] over a range of duty cycles from 0.1% to 0.0005% (constant t_{ON} = 1 μs, t_{OFF} = 1 ms → 200 ms).

To gain better understand of the observed drain current increase in pulsed IdVg characteristics of "buffer-free" GaN HEMTs (Fig 6.8) in comparison to the DC measurement (Fig 6.4), the effects of the Off-state drain stress duration (for the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [15V, -7V]) were measured and are shown in Fig. 6.10. For quiescent stress times between 1μs to 1 ms there is little change in the IdVg characteristics. As the stress duration is increased to 100 ms, the threshold voltage shifts towards more positive value in line with the DC measurement. No further shift in threshold voltage can be observed for stress times longer than 100 ms.

6.3.2 Thermal Characterisation

To evaluate the thermal performance of "buffer-free" GaN HEMTs micro-Raman thermography measurements were performed on the samples with gate length L_G = 250 nm and source-to-drain spacing of 4 μm. Figure 6.11 shows an example of the Raman spectrum obtained for an unbiased device at 25°C. To measure channel temperatures of the devices shift in GaN E_2 high and GaN A_1 (LO) peaks were recorded as a function of power dissipation.

Figure 6.12 shows the channel temperatures of the 2-finger QuanFINE GaN HEMTs extracted

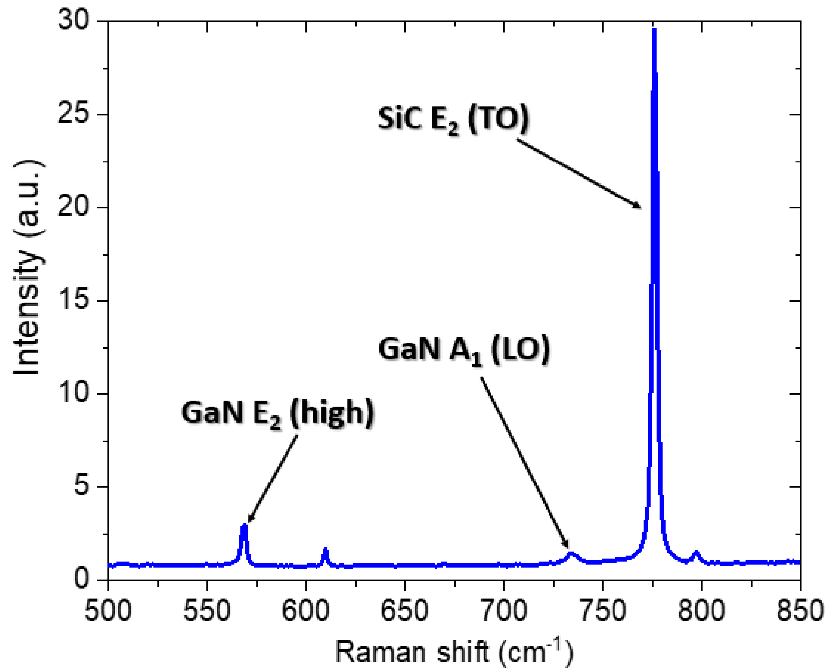

Figure 6.11: Raman spectrum of the "buffer-free" GaN-on-SiC HEMT with source-drain spacing of 4 μm and gate length L_G = 250 nm at 25°C when no extrnal potential is applied (main peaks from GaN and SiC are labelled).

from GaN E_2 high and GaN A_1 (LO) peaks. The channel temperatures derived from the shift in the frequency of the investigated Raman modes at 8 W/mm are 69.5 ± 2.7°C from A_1 peak and 65.7 ± 0.7°C E_2 peak. The thermal resistance of GaN channel was calculated 8.3 ± 0.3 W^{-1} °C mm and 8.7 ± 0.4 W^{-1} °C mm for E_2 and A_1 peaks accordingly. Further evaluation of the thermal performance of the "buffer-free" GaN HEMTs including extraction of the effective thermal boundary resistance (TBR_{eff}) and the peak channel temperatures relies on combination of experimental results and computational simulations as described in the next section. Good agreement between the temperatures measured from the shift in E_2 and A_1 modes indicates little thermomechanical strain present in the channel during device operation.

Figure 6.12 shows the channel temperatures of a conventional 2-finger GaN-on-SiC HEMT with thick buffer (L_G = 250 nm, 4 μm channel) derived from the shift in GaN E_2 high and GaN A_1 (LO) Raman modes for power dissipation up to 8 W/mm. The temperatures measured for each mode at 8 W/mm are 68.7 ± 2.1°C for A_1 mode and 57.0 ± 1.0°C for E_2 mode. The discrepancy in the temperatures derived from the frequency shift of A_1 and E_2 modes results from a significant thermomechanical strain present in the epitaxial structure during device operation, with the former mode being less susceptible to the effects of strain. Thus, temperatures calculated from the Raman shift of A_1 are closer to the true lattice temperature.

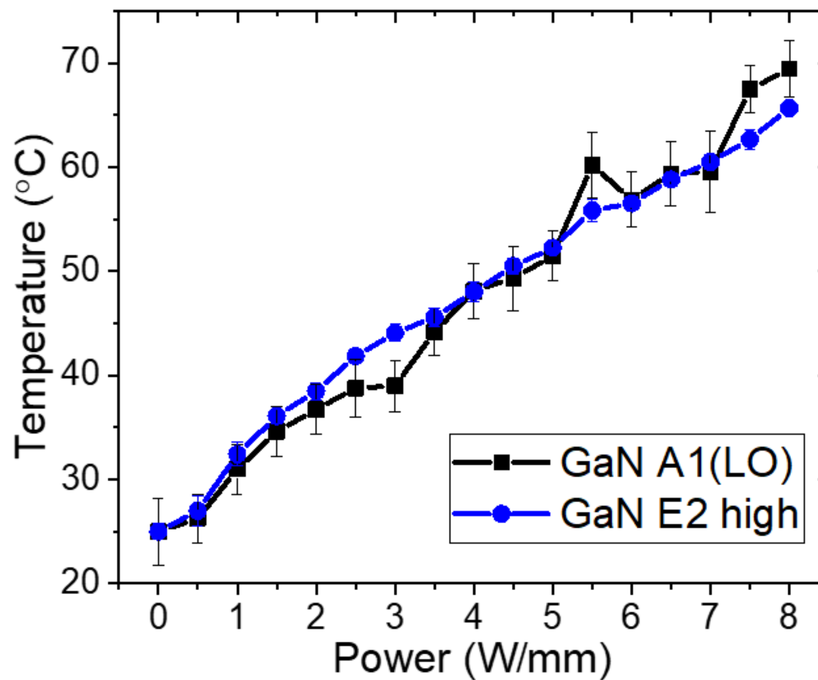

Figure 6.12: Average channel temperature of 2-finger "buffer-free" GaN-on-SiC HEMTs with channel length of 4 μm and gate length L_G = 250 nm as a function of power dissipation extracted from Raman shifts of GaN E_2 high and GaN A_1 (LO) peaks. The calibration coefficients for both peaks are:for GaN E_2 (high) A = 19.1, B = 1.2, ω_0 = 568.5; for GaN A_1 (LO) A = 18.6, B = 0.54, ω_0 = 736.4.

6.4 Discussion

6.4.1 Electrical Measurements

The comparison of DC IdVd measurements between "buffer-free" GaN HEMTs and conventional transistors with thick GaN buffer suggest potential issues with carrier confinement, which are particularly prominent in case of devices with short gate lengths (L_G = 150 nm) and are manifested by the punch-through shown in Fig. 6.4c. Compromised confinement of electrons in the channel could also account for stretch-out observed in the IdVg sweeps (Fig. 6.4b & d) but it could also result from trapping present in the epitaxy or from gate leakage. None of these features have been observed in the conventional GaN HEMTs with thick buffer. Gate leakage measurements presented in Figure 6.5 show similar gate leakage for both conventional and "buffer-free" devices. This result suggests gate leakage cannot account for the stretch-out in the DC IdVg sweeps of QuanFINE GaN HEMTs. The results, however, indicate the gate current is responsible for off-state leakage at gate voltages below threshold.

To investigate the effects of trapping pulsed IV measurements were performed on both sets of devices. The duty cycle of 0.1% (t_{ON} = 1 μs, t_{OFF} = 1 ms) ensures the non-quiescent bias conditions do not result in self-heating or additional trapping. By applying appropriate quiescent stress, the

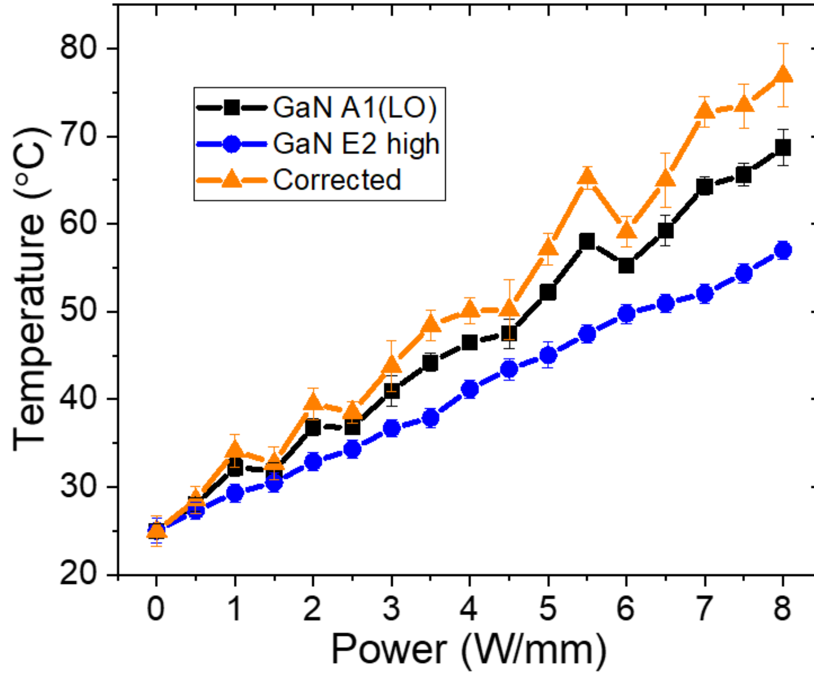

Figure 6.13: Average channel temperature of 2-finger conventional GaN-on-SiC HEMTs with channel length of 4 μm and gate length L_G = 250 nm as a function of power dissipation extracted from Raman shifts of GaN E_2 high and GaN A_1 (LO) peaks. The results were corrected for thermomechanical strain as described in section 3.3.3. The calibration coefficients for both peaks are:for GaN E_2 (high) A = 19.1, B = 1.2, ω_0 = 568.5; for GaN A_1 (LO) A = 18.6, B = 0.54, ω_0 = 736.4.

effects of different regions within the expitaxial structure can be investiagted separately. The quiescent stress point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V] serves as a reference point for further measurement, as no stress is applied between very short measurement windows. By setting the quiescent stress to [$V_{D,Q}$, $V_{G,Q}$] = [0V, -6V] the effects of trapping in the gate region are investigated. Both "buffer-free" and conventional HEMTs show little current decrease for this stress condition regardless of the gate length (see Fig. 6.8a & c and Fig. 6.9a & c), indicating little trapping in the vicinity of the gate.

The quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [15V, -6V] is conventionally chosen to look at the effects of trapping in the gate-drain access region, especially in the buffer. The "buffer-free" devices show an additional small decrease in the drain current with the application of quiescent drain stress. In comparison, conventional devices with the thick GaN buffer show current collapse on the order of 12% indicating significant buffer trapping. This result suggests QuanFINE devices offer significant advantages over conventional GaN HEMT design that relies on heavily doped thick buffers.

Pulsed IdVg sweeps from the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0V, 0V] (duty cycle 0.1%) for "buffer-free" transistors presented in Fig. 6.8b & d show stretch-out similar to that observed in

the DC measurements, suggesting trapping cannot account for this feature. The off-state current measured for these devices is slightly higher (moderate decrease in threshold voltage) than in the DC measurement. This is likely caused by activation of trap states located in the gate-drain access region during the DC sweep, resulting in current reduction as compared to pulsed IV. Figure 6.10 shows the drain current dependence on the duty cycle of the measurement for the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [15V, -6V]. The change in threshold voltage for stress times between 1 ms and 100 ms suggest some small concentration of trap states with the time constant on the order of 10s of ms. These trap states can become populated during a DC sweep resulting in small increase in threshold voltage. During pulsed IdVg sweep, the measurement window of 1 μs is to short to allow for activation of these traps.

Pulsed IV measurement suggest the main cause of the stretch-out observed in particular in the short gate QuanFINE devices (L_G = 150 nm) can be attributed to the insufficient carrier confinement in the channel. Considering both conventional and QuanFINE HEMTs have undergone the identical fabrication process, the issues observed in the "buffer-free" devices are expected to stem from the expitaxy.

6.4.2 Electrical Simulations

To gain a better understanding of the IV characteristics of the "buffer-free" GaN HEMTs, Silvaco's Atlas TCAD software was employed to create an accurate model of the investigated device. The simulated device structure is shown in Figure 6.14a and includes 4H-SiC substrate followed by 60 nm of AlN nucleation layer, 250 nm of UID GaN channel, 14 nm AlGaN barrier (29% Al contents) and passivisation. The GaN channel includes 10^{16} cm^{-3} of shallow donors (at 0.05 eV below the conduction band) compensated by 10^{15} cm^{-3} C acceptors 0.9 eV above the valence band. The electron and hole capture cross-sections were set to 10^{-15} cm^2.

The key models used in these simulations include Fermi-Dirac and Shockley–Read–Hall statistics. To accurately simulate carrier mobilities of the simulated devices Farahmand Modified Caughey Thomas model was used in the low field regime (this model includes temperature and doping dependence), while high field mobility was simulated using nitride specific field dependent mobility model based on the work by Farahmand *et al.* [259]. In addition, piezoelectric and spontaneous polarization effects were included in the simulation using appropriate models specific for polarization in wurtzite structures.

Figure 6.14b shows two proposed band diagrams for the simulated structure. Case 1 includes full polarisation charge present at the GaN/AlN NL interface and at the bottom of the nucleation layer (which is defined as the polarization charge expected at the interface of perfect crystalline AlN NL), similar to band diagram proposed by Chen *et al.* in [256], while case 2 shows a situation where the concentration of the polarisation charge across the AlN nucleation layer is reduced, thus resulting in lower internal potential across GaN layer as compared to case 1.

Figure 6.15 shows the simulated IdVg characteristics for band diagrams corresponding to

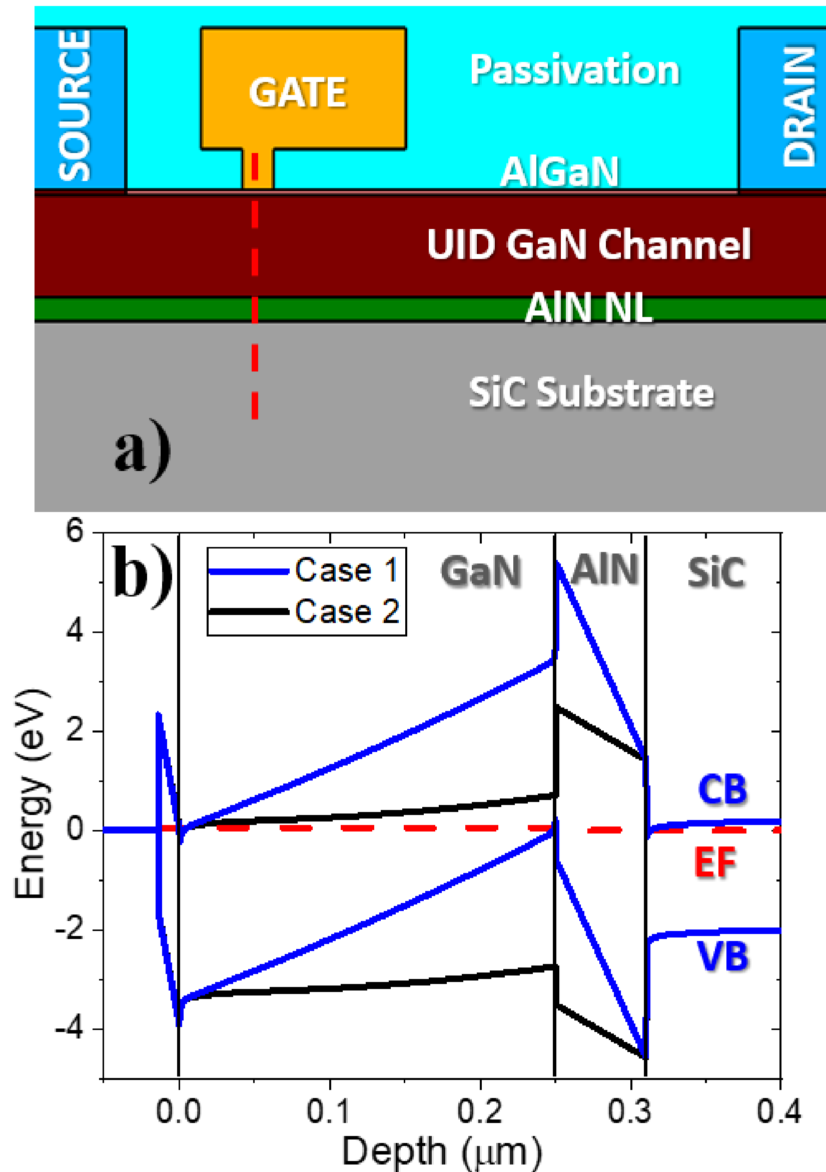

Figure 6.14: **a)** Structure of "buffer-free" GaN-on-SiC HEMT with channel length of 3 μm and gate length L_G = 150 nm simulated in Silvaco's Atlas TCAD software. The red line represents the cut-line along which the band diagrams shown in **b)** have been plotted. **b)** Simulated band diagrams of "buffer-free" GaN-on-SiC HEMT for two considered cases: **case 1** corresponds full polarisation charge present at the GaN/AlN interface (similar band diagram proposed by Chen *et al.* in [256]); **case 2** corresponds to band diagram with reduced polarisation charge at the GaN/AlN interface. The appropriate layers are indicated in the diagram, as well as valence band (VB), conduction band (CB) and electron Fermi level (EF).

case 1 and case 2. Case 1 (Fig. 6.15a) shows a slow and gradual shift in threshold voltage as observed in conventional devices with thick GaN buffer (see Fig. 6.5), with the DIBL calculated as 31 mV/V (compared to measure 95 mV/V). The stretch-out observed in the experiment is not

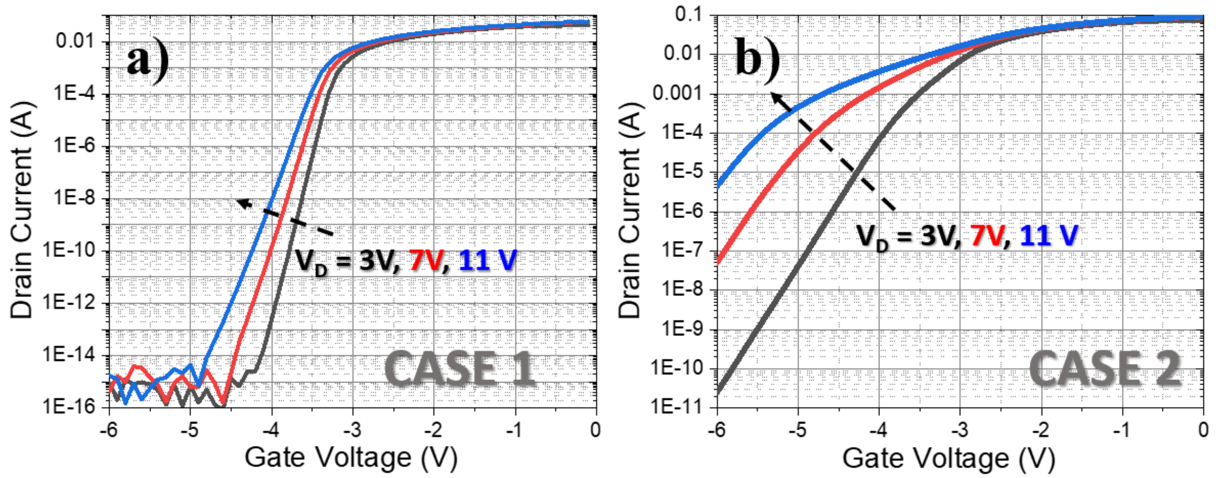

Figure 6.15: Simulated DC IdVg characteristics for band diagrams represented by **a)** case 1 and **b)** case 2 for drain voltages V_{DRAIN} = 3 V, 7 V and 11 V.

present here. In contrast, IdVg curves simulated for the band diagram represented by case 2 (Fig. 6.15b) show a significant stretch-out very similar to experimental observations. The difference in the off-state leakage current between the measurement and simulation results from the absence of gate leakage current, that is not trivial to reproduce in the simulator.

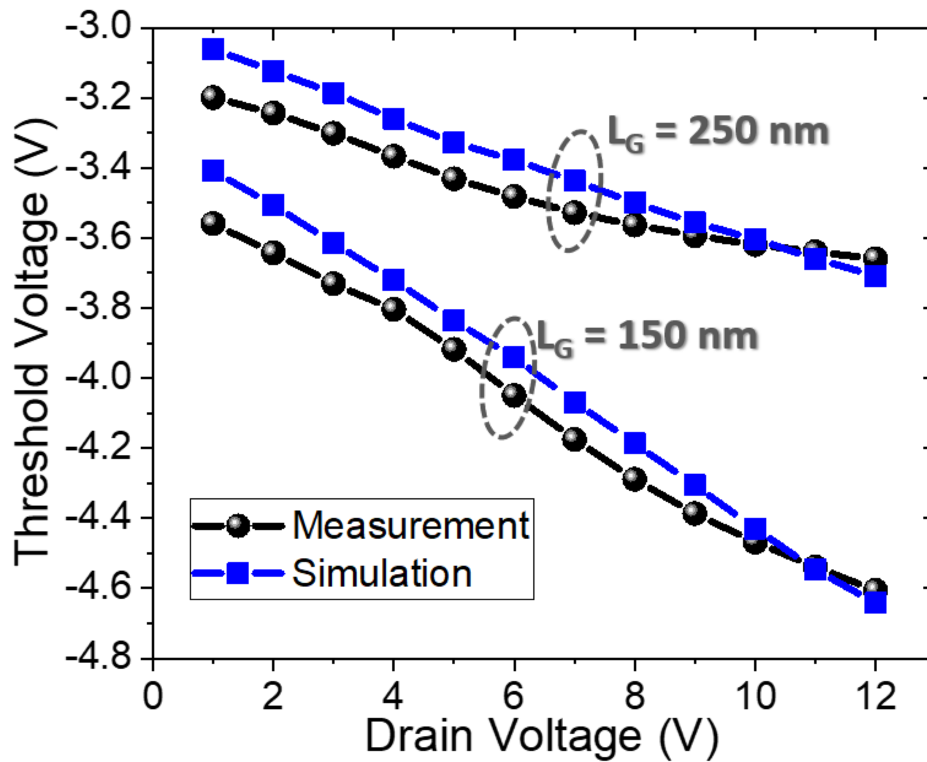

Figure 6.16: Average measured DIBL for "buffer-free" GaN-on-SiC HEMTs with gate length L_G = 150 nm and 250 nm compared to the simulations based on band diagram represented by Case 2.

In general, the simulations show good qualitative agreement with the measurement as demonstrated in Figure 6.16. The simulated shift in threshold voltage as a function of applied drain potential matches the experimental results well for devices with gate lengths of L_G = 150 nm and 250 nm. The shift in threshold voltage and the stretch-out observed in both DC and pulsed measurements can be explained in terms of punch-through effect. At higher drain voltages, the depletion region under the gate is insufficient to prevent the current flow between source and drain. The charges flow around the depletion region as shown in Fig. 6.17 resulting in stretch-out in the IdVg characteristics, especially prominent in devices with shorter gate lengths.

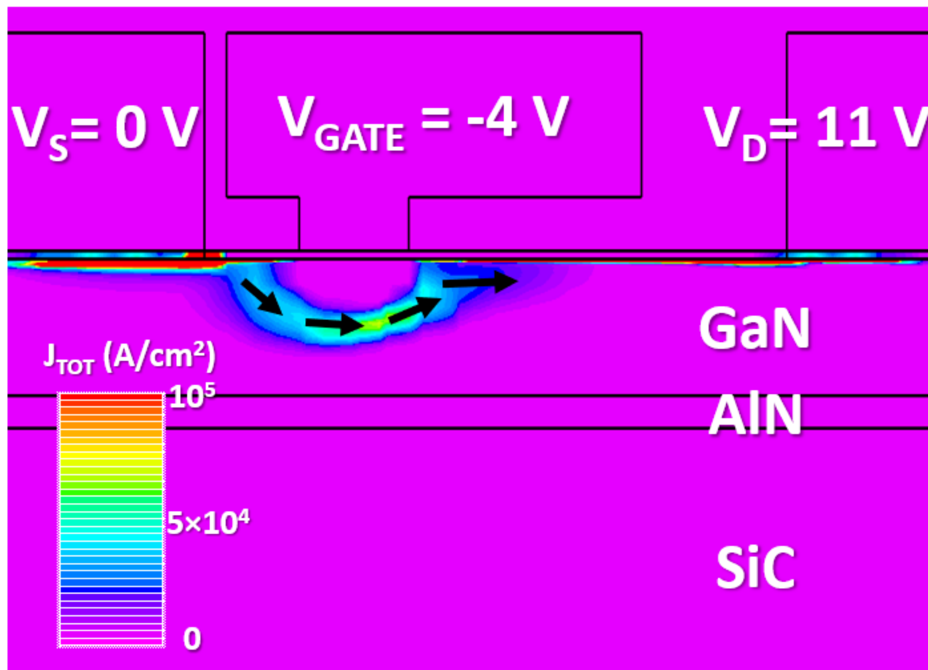

Figure 6.17: Simulated current density for "buffer-free" GaN-on-SiC HEMT with gate length L_G = 150 nm. At higher drain voltages, current can flow around the gate depletion region leading to strech-out in IdVg characteristics.

A possible explanation for reduction in polarisation charge at the GaN/AlN interface relate to the techniques utilised for growth of AlN nucleation layer. To achieve nucleation layers of highest quality in the devices, the AlN NL is grown transmorphically to include out-of-plane compositional-gradient with an in-plane vacancy-ordering resulting in atomic configuration adjustment between SiC and AlN on the order of 1 nm. This technique results in localisation of defects and dislocation to within 10 nm away from the interface as shown in Fig. 6.18a [247]. In contrast, conventional growth of AlN on SiC results in abrupt interface with extended defects and pits formation as shown in Fig. 6.18b. AlN nucleation layers grown transmorphically demonstrate outstanding quality and structural order, resulting in significant reduction in defect densities and strain in GaN layers grown over it. However, decrease in polarisation charge across the AlN could be a possible side effect resulting from reduced relative strain between AlN and GaN layers.

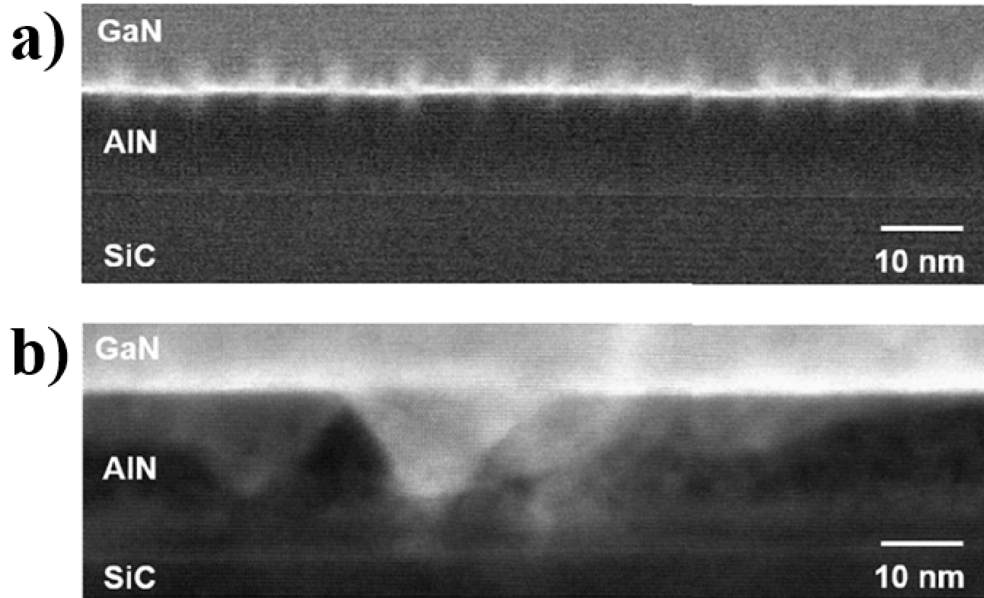

Figure 6.18: Cross-sectional TEM images of AlN nucleation layer and interfaces for **a)** NL grown transmorphically including out-of-plane compositional-gradient with an in-plane vacancy-ordering and **b)** NL grown by conventional methods with abrupt AlN/SiC interface. Bright contrast results from localised stress due to dislocations. Image adapted from [247].

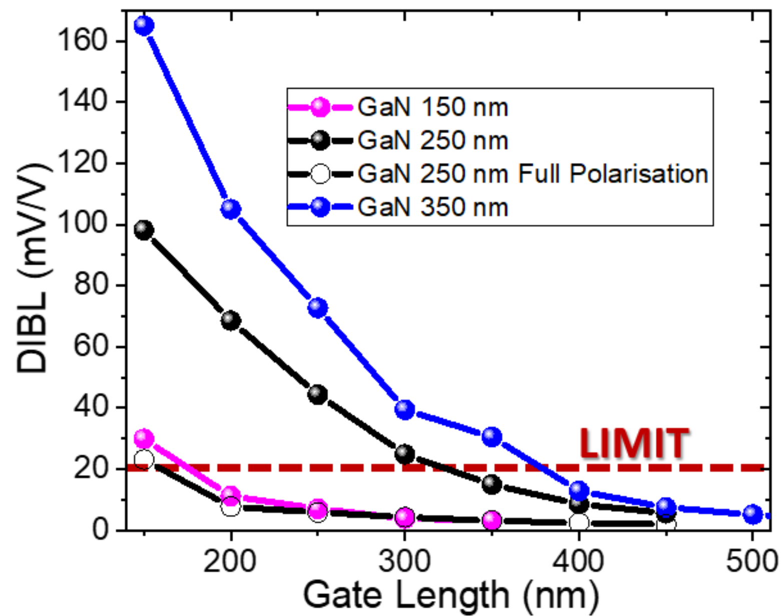

Figure 6.19: Simulated DIBL as a function of device gate length L_G for GaN channel thicknesses of 150, 250 and 350 nm for devices with reduced polarisation charge across AlN interlayer. Simulation of HEMT with GaN thickness of 250 nm and full polarisation charge (which represents the case of perfect single crystal AlN interlayer) included for comparison. The limit of 20 mV/V represents a general industrial standard for reliable device performance.

A possible avenue for mitigation of carrier confinement issues lies in adjusting the gate length of the "buffer-free" GaN-on-SiC HEMTs. Figure 6.19 shows simulated DIBL as a function of gate length for "buffer-free" GaN-on-SiC HEMTs with channel thickness of 150, 250 and 350 nm. The limit of 20 mV/V represents a general industrial standard for reliable device performance. The results indicate that regardless of channel thickness increasing the gate length results in better channel control and decrease in DIBL. The drawback to this approach involves reduction in maximum theoretical cut-off frequency f_T as it is inversely proportional to the gate length L_G. Therefore, an alternative solution could involve reduction in GaN thickness. Good electron confinement is easier to achieve in the thinner GaN channels as the proximity of gate depletion region and the AlN nucleation layer creates sufficient barrier for charge carriers. The simulations suggest that GaN HEMTs with a gate length of $L_G \approx 175$ nm requires a GaN channel thickness of 150 nm, while a gate length of Lg $L_G \approx$ nm requires a GaN channel thickness of 350 nm for DIBL to drop below 20 mV/V. However, reduction in GaN thickness should also be considered from the perspective of thermal performance as thinner GaN layers show significant reduction in thermal conductivity. The effects of GaN thickness on temperature profiles in operating devices will be fully discussed in section 6.4.4.

To avoid changes to device epitaxy and geometry, an improvement in electron confinement can be achieved by increase in polarization charge across the AlN nucleation layer (as shown in Fig. 6.19), which would involve growth process optimization aimed at lowering the position of Fermi level E_F in the AlN nucleation layer. "Buffer-free" GaN-on-SiC HEMTs investigated in this thesis constitute early generation QuanFINE devices, therefore further study of the properties of the GaN/AlN interface and the electrical properties of the defects located at this interface could provide attainable solutions to current issues with carriers confinement.

6.4.3 Thermal Analysis of Conventional GaN-on-SiC HEMTs

GaN temperatures derived from the measured Raman shifts of A_1(LO) and E_2 phonon modes in the conventional GaN-on-SiC HEMTs show significant discrepancy, which increases with power dissipation up to ~12 °C at 8 W/mm, indicating significant thermomechanical strain present in the epitaxy. To account for the strain present during measurement, the results were corrected for as described in section 3.3.2. Figure 6.13 shows operating device temperatures derived from A_1(LO) (black) and E_2 high (blue) modes as well as GaN temperature after correction for thermomechanical stress (orange).

Further analysis of temperature profiles of the investigated conventional GaN-on-SiC HEMTs was performed using 3D finite element analysis (FEA) Ansys software. A detailed device model was created to accurately represent all device dimensions and measurement conditions. The epitaxial structure consisted of 4H-SiC substrate, 60 nm of AlN nucleation layer and 2 μm GaN buffer. The channel width was set as 4 μm with the gate length L_G = 250 nm. Table 6.1 outlines the thermal conductivity parameters and their temperature dependence for the key materials

Table 6.1: Thermal Conductivity Values for Ansys Simulations I

Material	Thermal Conductivity [W/mK]
GaN (Isotropic)	$160 \times (298/T)^{1.4}$
4H-SiC (In-plane)	$390 \times (298/T)^{1.15}$
4H-SiC (Out-of-plane)	$490 \times (298/T)^{1.15}$
AlN NL	$2 \times (298/T)^{0.9}$
AlGaN	14
Contacts	315

Thermal conductivity parameters used in the simulations of GaN-on-SiC HEMTs. Temperature dependence from [260] and [205].

used in the simulation. The heater with the dimension of 400 nm × 10 nm was introduced at the gate edge to replicate Joule heating during GaN HEMT operation [190]. To simulate temperature measurement based on micro-Raman thermography, a flat block with the width of 500 nm (corresponding to laser spot diameter) was inserted and the average temperature across this area was monitored as a function of power dissipation up to 8 W/mm. Simulations were calibrated based on the experimental measurements to extract the effective TBR between the GaN buffer and the substrate.

Figure 6.20 shows a comparison between measured GaN temperatures and Ansys simulation of conventional GaN-on-SiC HEMT for power dissipations up to 8 W/mm. The simulation indicates the devices with thick buffer reach the maximum temperature of 141.8 °C at 8 W/mm, with the effective thermal boundary resistance calculated as 30 m^2 K GW^{-1}.

6.4.4 Thermal Analysis of "Buffer-Free" GaN HEMTs

The temperature dependence of GaN A_1(LO) peak position is almost three times strong than that of the E_2 high mode, however it is the latter that shows more significant dependence on strain of the GaN layer [217]. The similarity in temperatures extracted from micro-Raman thermography measurements of A_1(LO) and E_2 high peaks (see Fig. 6.12) indicates relatively little stress present in the UID GaN channel.

Further analysis of temperature profiles of "buffer-free" GaN-on-SiC HEMTs was performed using 3D FEA Ansys software. As in the case of conventional devices, an accurate model of the transistor was prepared taking into account geometry, epitaxy and measurement conditions. The epitaxial structure consisted of 4H-SiC substrate, 60 nm of AlN nucleation layer and a 250 nm GaN channel. The channel width was set as 4 μm with the gate length L_G = 250 nm. Table 6.2 outlines the thermal conductivity parameters and their temperature dependence for the key materials. The reduction in out-of-plane thermal conductivity of GaN channel in QuanFINE

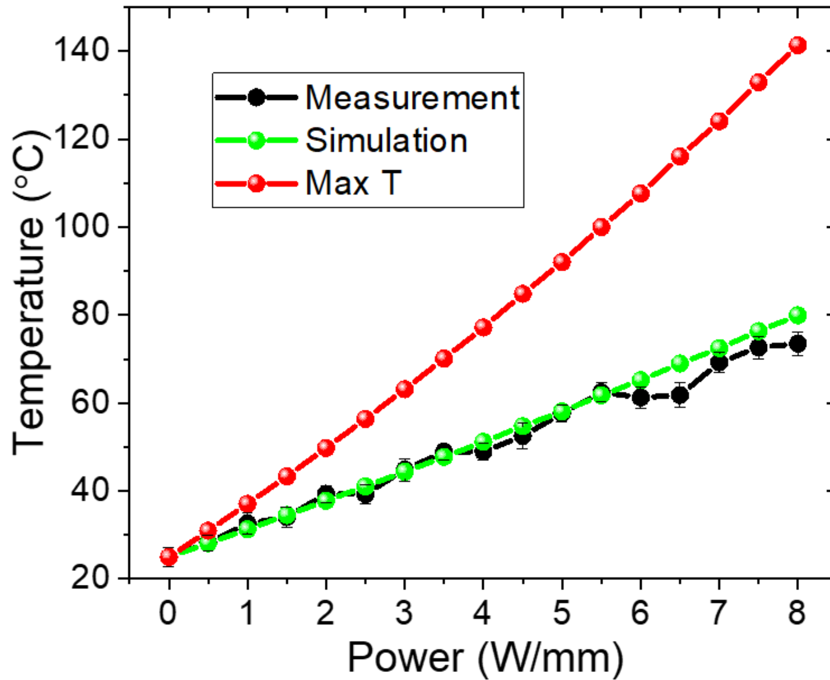

Figure 6.20: Comparison between GaN buffer temperature measured for conventional GaN-on-SiC HEMTs using micro-Raman thermography (black) and Ansys simulation based on the parameters shown in Table 6.1 (green) for power dissipations up to 8 W/mm. Simulated maximum channel temperature is shown in red.

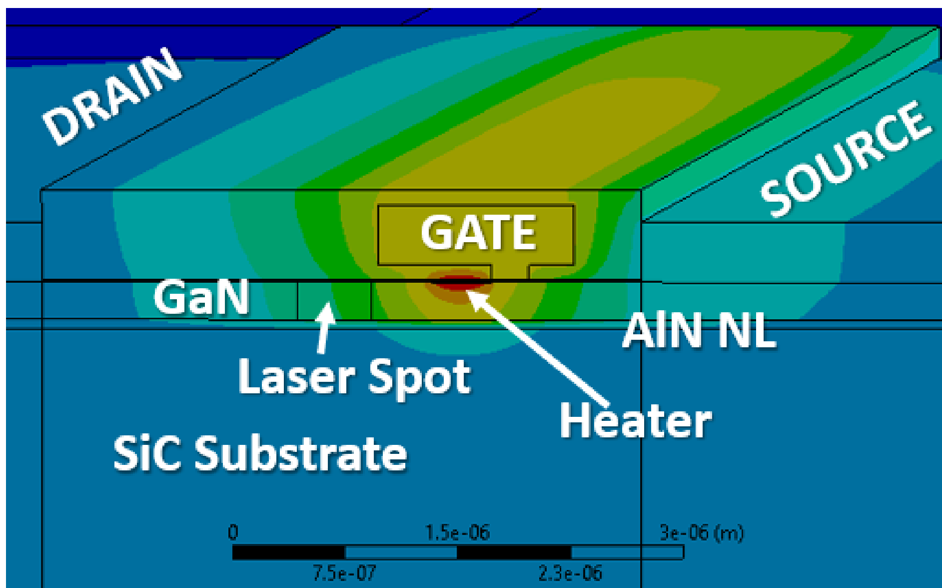

Figure 6.21: Structure of "buffer-free" GaN-on-SiC HEMT with channel length of 4 μm and gate length L_G = 250 nm simulated in 3D Ansys FEA software. All further simulations are based on the structure presented in this figure.

Table 6.2: Thermal Conductivity Values for Ansys Simulations II

Material	Thermal Conductivity [W/mK]
GaN (Out-of-plane)	$82 \times (298/T)^{1.4}$
GaN (In-plane)	$160 \times (298/T)^{1.4}$
4H-SiC (Isotropic)	$390 \times (298/T)^{1.15}$
AlN NL	$6 \times (298/T)^{0.9}$
AlGaN	14
Contacts	315

Thermal conductivity parameters used in the simulations of a "buffer-free" GaN-on-SiC HEMTs. Temperature dependence from [260] and [205].

devices results from increased phonon scattering at the boundaries as outlined in [57], with phonon relaxation time $\tau^{-1} \propto d^{-1}$ where d is GaN thickness. As above, the heating element was introduced at the drain-side gate edge and the micro-Raman measurement was simulated by including a 500 nm wide rectangular block spanning across the entire channel thickness. Figure 6.21 shows an image of the Ansys model. Simulations were calibrated based on the experimental measurements to extract TBR_{eff} between the GaN channel and the substrate. Further analysis was performed on the "buffer-free" HEMT model to study the effects of GaN thickness across a wide range of TBR_{eff} values on temperature profiles of the operating devices.

Figure 6.22 shows a comparison between channel temperatures measured using micro-Raman thermography based on shift in A_1(LO) and E_2 high Raman modes with channel temperatures simulated in Ansys. The results indicate a low effective thermal boundary resistance (TBR_{eff}) between GaN and SiC of 10 m^2 K GW^{-1} (at 25°C, assuming the $T^{-0.9}$ temperature dependence of ref. [260]), which stands in agreement with previous measurements of this technology [206] and is lower than reported values for conventional commercially available devices which are normally larger than 20 m^2 K GW^{-1} at 25 °C [205]. The simulation suggest peak channel temperature of 155.6 °C for power dissipation of 8 W/mm.

To study the effects of GaN thickness on the thermal performance of the GaN-on-SiC HEMTs, the structures with total GaN thickness between 0.2 μm and 2 μm were simulated, while all the other parameters were kept constant. Figure 6.23a shows a temperature profile along the AlGaN/GaN interface between source and drain for total GaN thickness (channel + buffer) between 0.25 μm and 1.5 μm. For very thin GaN layers, a small increase in the channel thickness can result in significant reduction of peak channel temperature. As the total GaN thickness increases further, the resultant reduction in temperature becomes less significant. However, thin GaN devices demonstrate lower temperatures under source and drain contacts, reducing the chances of thermal degradation of the contacts and potentially increasing device lifetime.

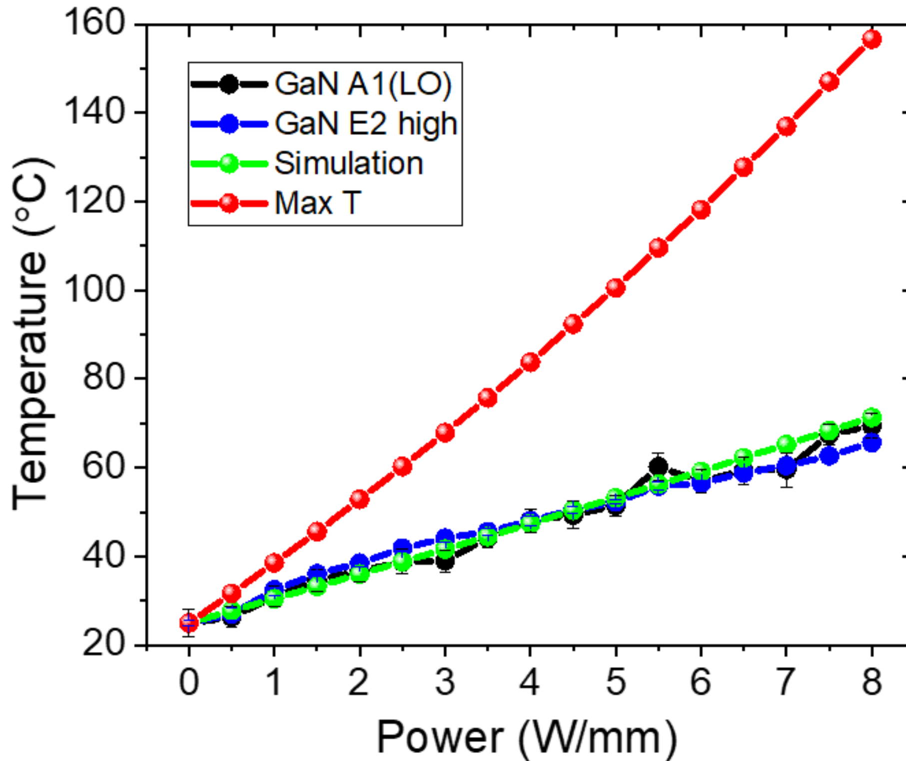

Figure 6.22: Comparison between GaN channel temperature measured for "buffer-free" GaN HEMTs using micro-Raman thermography (black and blue lines) and Ansys simulation based on the parameters shown in Table 6.2 (green) for power dissipations up to 8 W/mm. Simulated maximum channel temperature is shown in red.

The effects of GaN thickness on peak channel temperatures are examined more closely in Figure 6.23b. The difference in maximum temperature between GaN HEMT with thick buffer and a QuanFINE device is denoted by ΔT. To reduce this difference by 50% it is sufficient to increase the GaN thickness by only ~100 nm (up to 360 nm). The inset to Fig. 6.23b shows the variation in out-of-plane thermal conductivity of GaN as a function of the layer thickness. The steep reduction in thermal conductivity for GaN layers thinner than 1 μm results from phonon scattering at interfaces, which becomes a dominant scattering mechanism for thin semiconductor films [61].

The effects of GaN thickness on peak channel temperature can seem counter-intuitive considering the proximity of high thermal conductivity 4H-SiC substrate. By examining vertical temperature profiles across the device, the importance of an excellent thermal interface between GaN channel and the substrate becomes immediately apparent. Figure 6.23 shows the percentage temperature drop across GaN, AlN and SiC substrate as a function of GaN thickness. In case of structures with higher TBR_{eff} (solid lines) and GaN thickness < 400 nm, the biggest temperature drop occurs across the AlN nucleation layer indicating higher thermal resistance in this region. The presence of thermally resistive barrier between GaN and SiC results in compromised heat

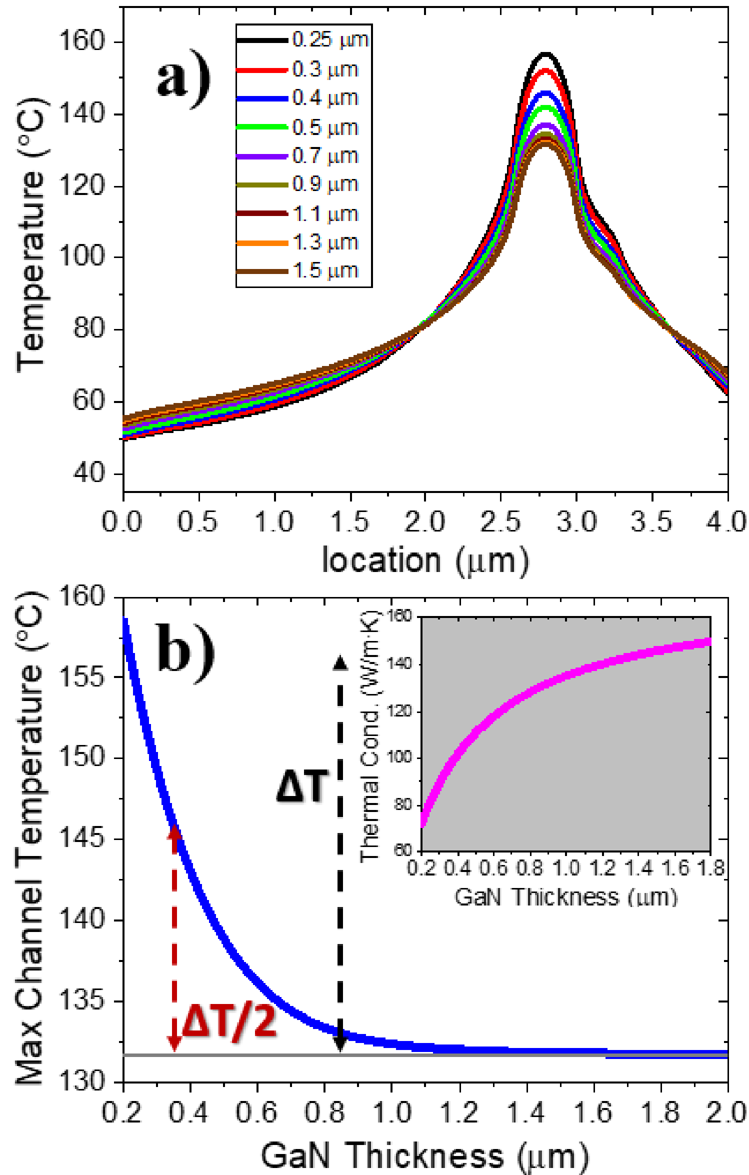

Figure 6.23: **a)** Simulated temperature profiles along the AlGaN/GaN interface between the drain (x = 0 μm) and source (x = 4 μm) with the peak at the drain-side gate edge for total GaN thickness (channel + buffer) between 0.25 μm and 1.5 μm for power dissipation of 8 W/mm. **b)** Peak channel temperature at power dissipation of 8 W/mm as a function of total GaN thickness between 0.2 μm and 2 μm. ΔT indicates the peak channel temperature difference between "buffer-free" device and conventional thick buffer HEMT (all other parameters remain unchanged) Inset: Thermal conductivity as a function of GaN thickness; adapted from [57].

conduction away from the hot spot under the gate edge. Thus, the potential advantages from the proximity of the SiC substrate are diminished in terms of their effect on thermal management of the device. Reduction in effective thermal boundary resistance between the substrate and the channel (dashed lines in Fig. 6.23) shows significant decrease in temperature drop across the AlN

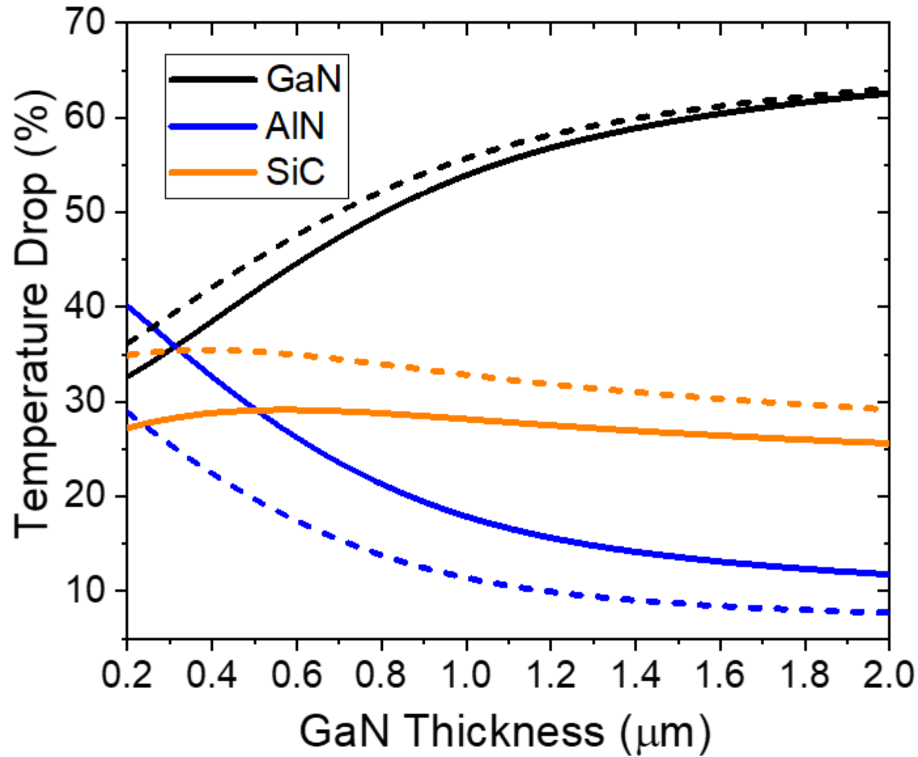

Figure 6.24: Percentage temperature drop across GaN, SiC and AlN NL (TBR_{eff}) as a function of total GaN thickness. Solid lines show the results for TBR_{eff} = 10 m^2 K GW^{-1} (measured for the investigated structure), dashed line show reduced TBR_{eff} = 5 m^2 K GW^{-1} for comparison.

layer allowing for more effective heat diffusion into the substrate, and thus higher temperature gradient across GaN and SiC layers.

The combined effects of GaN thickness and TBR_{eff} on the peak channel temperature are shown in Figure 6.24. The simulations emphasise the importance of excellent quality thermal interface between GaN and SiC substrate especially for devices with very thin GaN layers, where relatively small increase in TBR_{eff} can result in a significant increase in peak channel temperature. To fully utilize the advantages of “buffer-free” technology and to increase the device lifetime it is crucial to fabricate high quality nucleation layers with very low TBR_{eff}. For this reason, QuanFINE technology design offers a highly competitive thermal performance in comparison with conventional GaN-on-SiC HEMTs, with the added benefit of reduction in manufacturing costs and elimination of buffer trapping.

The ideal "buffer-free" GaN-on-SiC HEMT combines excellent electrical and thermal performance to create reliable, robust and highly-efficient device. The total GaN thickness of 350 nm results in significant reduction in peak channel temperature compared to current samples, while still offering lower temperatures under the contacts. However, from the electrical perspective, assuming optimized AlN nucleation layer with Fermi level in the lower half of the band, the gate length required to provide adequate carrier confinement would have to increase to ~200 nm,

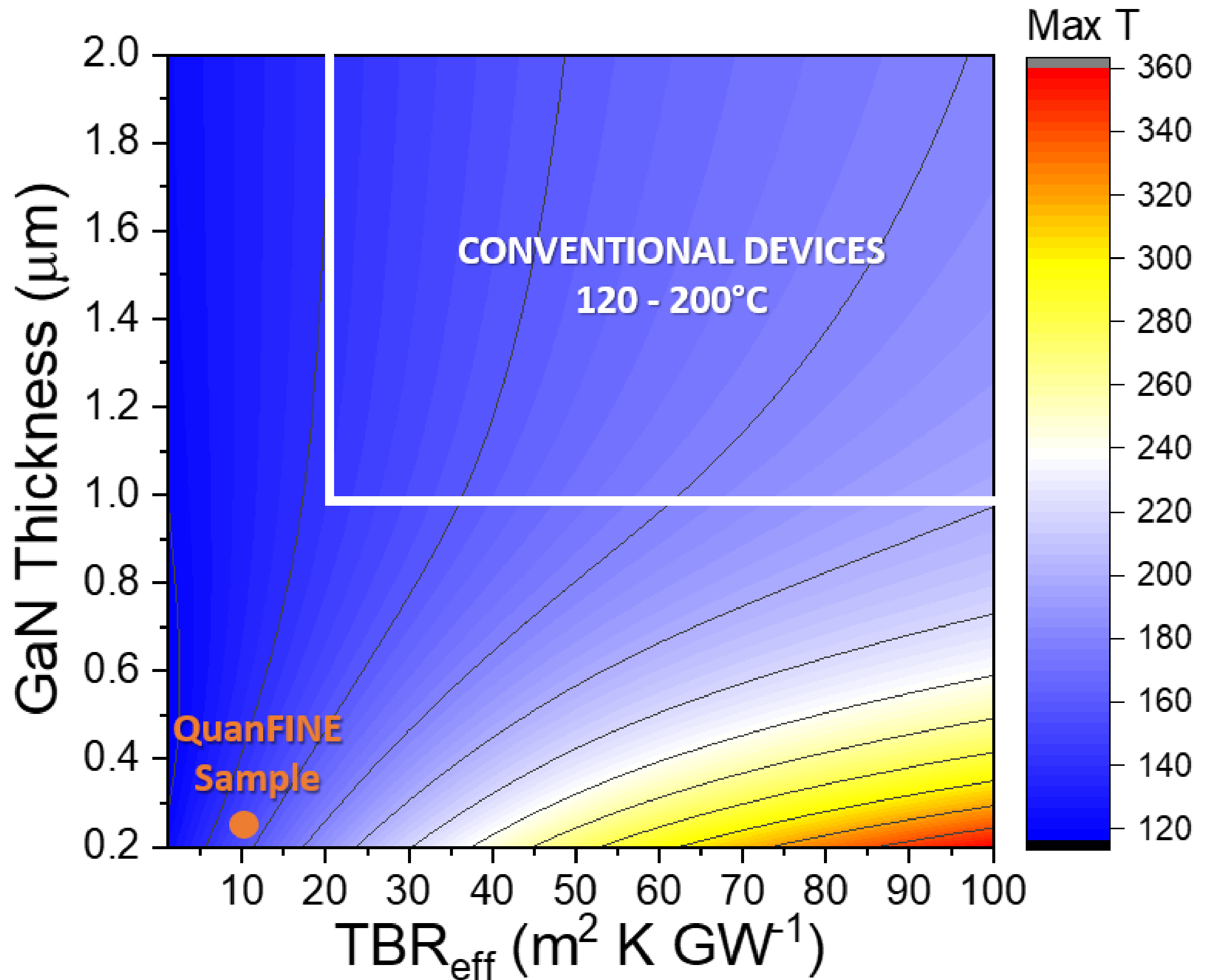

Figure 6.25: Peak channel temperature as a function GaN thickness and the effective thermal boundary resistance between GaN and SiC substrate for power dissipation of 8 W/mm. Isotherms (black lines) are spaced 20 °C apart.

resulting in reduction of attainable cut-off frequency f_T. For this reason, the ideal "buffer-free" GaN-on-SiC HEMT design would strongly depend on intended application with factors such as target power densities and operating frequencies playing a critical role in the design. Higher frequency applications will push the device design towards thinner GaN layers with shorter gates, while larger power dissipation will require slightly thicker channel with longer gates.

6.5 Conclusions

This chapter demonstrates an electrical and thermal characterisation of "buffer-free" (QuanFINE) GaN-on-SiC RF HEMTs developed by SweGaN AB. For comparison, identical GaN HEMTs with thick GaN buffer were also provided. The electrical characterisation of "buffer-free" devices shows signs of short channel effects especially for gate lengths L_G = 150 nm. In addition, the DC

IdVg sweeps show stretch-out in the output characteristics that is not present in conventional devices with the thick buffer. The pulsed IV measurements show little trapping either in the vicinity of gate or in the gate-drain access region, suggesting carrier confinement could be a viable explanation for the observed short-channel effects. Electrical simulations performed in Silvaco's Atlas TCAD software confirm the experimental observation suggesting punch-through effect as the primary cause for the stretch-out in IV characteristics. Improved carrier confinement in the channel can be achieved by increasing gate length or reduction in GaN channel thickness, however this latter option would have major implications on thermal performance of the devices. In contrast to "buffer-free" devices, despite good carrier confinement in the channel, conventional GaN HEMTs shows signs of buffer trapping due to high doping concentrations needed for buffer insulation.

Thermal analysis of QuanFINE devices involved a combination of micro-Raman thermography measurements and 3D FEA Ansys simulations. The results indicate peak channel temperature of 155.6 °C for power dissipation of 8 W/mm, with extracted effective thermal boundary resistance between GaN channel and the SiC substrate of TBR_{eff} = 10 m^2 K GW^{-1}, suggesting very competitive thermal performance in comparison to conventional GaN HEMTs with thick buffer. Further computational analysis shows the importance of low TBR_{eff} particularly for thin GaN layers. Despite the proximity of high thermal conductivity substrate TBR_{eff} can impede the effective heat diffusion away from the hot spot. Due to reduced thermal conductivity of thin GaN layers, the peak channel temperature can be reduced by 50% as compared to conventional devices with thick GaN buffer by increasing the GaN thickness by only ~ 100 nm.

The ideal "buffer-free" GaN HEMT design combines excellent electrical and thermal performance. However, while better carrier confinement and higher operating frequencies require thinner GaN layers with shorter gate lengths, thermal performance can be boosted by increasing GaN thickness, thus requiring longer gate lengths for good channel control. Design of the ideal transistor will therefore strongly depend on the intended device application, since for "buffer-free" HEMTs small changes in the discussed parameters can have a significant effect on device performance.

CHAPTER 7

ELECTRICAL AND THERMAL CHARACTERISATION OF GaN-ON-SiC HEMTs COVANLENTLY BONDED BY ADAPTIVE LOW-TEMPERATURE METHOD

This chapter describes electrical and thermal characterisation of a GaN-based power devices bonded onto SiC substrate as a proof of concept of a novel low-temperature bonding technique. AlGaN/GaN-on-Si HEMTs are chemically treated to remove the Si substrate and are subsequently bonded onto conductive 4H-SiC substrate via adaptive low-temperature covalent bonding technique by extremely thin water interlayers. DC and pulsed measurement techniques are used to characterise the HEMTs before and after bonding. DC IdVd characteristics of bonded devices show increase in drain current up to 20% in comparison with the original transistors resulting from reduction in self-heating. Pulsed IV measurements show both sets of devices suffer from mild current collapse due to trapping in the gate-drain access region, however the results suggest bonding does not increase trapping in the buffer. Bidirectional substrate ramp sweeps indicate increase in positive charge storage in the buffer in bonded devices, however the vertical leakage currents remain unchanged as compared to unbonded GaN-on-Si HEMTs. In addition, micro-Raman thermography was performed on the samples before and after bonding. Average GaN temperatures were calculated from the Raman shift of the A_1 (LO) and E_2 high phonons. Moreover, the surface temperatures of HEMTs were measured by monitoring the Raman shift of TiO_2 nanoparticles deposited on the device surface, showing reduction in measured temperatures from 154 °C to 116 °C at 5 W/mm. Ansys simulations of the devices indicate bonding of the devices onto 4H-SiC substrate (including the strain relief layer) results in the peak channel temperature at 5 W/mm dropping from 201.3°C to 174.4°C. Further improvement in the thermal performance of the devices can be achieved by removal of strain relief layer before bonding.

The original GaN-on-Si devices have been grown and fabricated by NXP Semiconductors, while bonding was performed by Thomas Gerrer with some assistance from the author. All the electrical and thermal measurement and simulations have been performed by me.

7.1 Introduction

III-nitride such as AlN, GaN and InN, as well as their tertiary and even quaternary alloys are important for development of wide range of semiconductor technologies including power converters, microwave amplifiers, light-emitting diodes, solar cells, sensors and many more. These materials are predominantly grown on substrates such as sapphire, Si and SiC due to limited availability of native large area substrates.

The ability to directly transfer III-nitride films onto different substrates can lead to integration of wide range of device technologies for improved device performance. For example, GaN-based power amplifiers for high frequency and high power outputs could benefit tremendously from availability of reliable transfer methods. Since thermal management is still a primary limiting factor for achieving higher power densities in GaN-based RF devices, the ability to bond AlGaN/GaN heterostructures onto substrates with high thermal conductivity (e.g. diamond) would allow more efficient devices with longer mean time to failure. For this reason, several groups have been exploring transfer techniques with some notable examples given in [261][262][263][264], however despite successful separation of nitride layers from the original substrate, it is the subsequent bonding process that still remains a crucial challenge for successful device transfer.

To achieve good quality interface between the transferred device and the target substrate, strong covalent bonding is needed to ensure robust mechanical and thermal interface between the two materials. However, to achieve high quality direct covalent bond, high smoothness (ideally Rq < 0.5 nm) and flatness is required from both surfaces. Homogeneous polishing is a common method to achieve good quality, smooth interfaces and can be applied to bond substrate. However, this technique is not suitable for thin film heterostructures consisting of complex epitaxy and layers with different chemical composition and under different degree of mechanical stress as this can lead to irreparable damage to the transferred layers.

Common techniques employed to overcome the issues relating to roughness of transferred heteroepitaxial films involve introduction of thin interlayers (some common choices include polymers, dielectric materials and metals [14][265][266][267]) to create a robust mechanical interface that can adapt to the surface topology on the atomic level, creating a strong bond between the transferred film and the bond substrate. However, the materials used for bonding interlayers can often be thermally insulating, mechanically soft and electrically active, significantly counteracting the benefits introduced by new high-performance substrates. Thus, the perfect bonding technique would involve formation of a bond layer that does not involve introduction of foreign materials, but rather involves restructuring of the surface involved in bonding on a nanometer

scale without affecting other parts of the thin film.

Such technique was first introduced by Gerrer *et al.*, who managed to successfully transfer AlGaN/GaN RF HEMTs from SiC to diamond substrate [268] using extremely thin water films. This method was further investigated revealing presence of covalent bond (and not van der Waals as initially reported) between the substrate and the transferred film, resulting in ~ 30 nm aluminium hydroxide layer [269]. This chapter describes first of its kind electrical and thermal analysis of GaN-based power HEMTs bonded using the method described by Gerrer *et al.*. We show that this bonding technique results in improved thermal performance of the devices, while having no adverse effect on electrical characteristics of the investigated devices.

7.2 Experimental Details

7.2.1 Sample Description

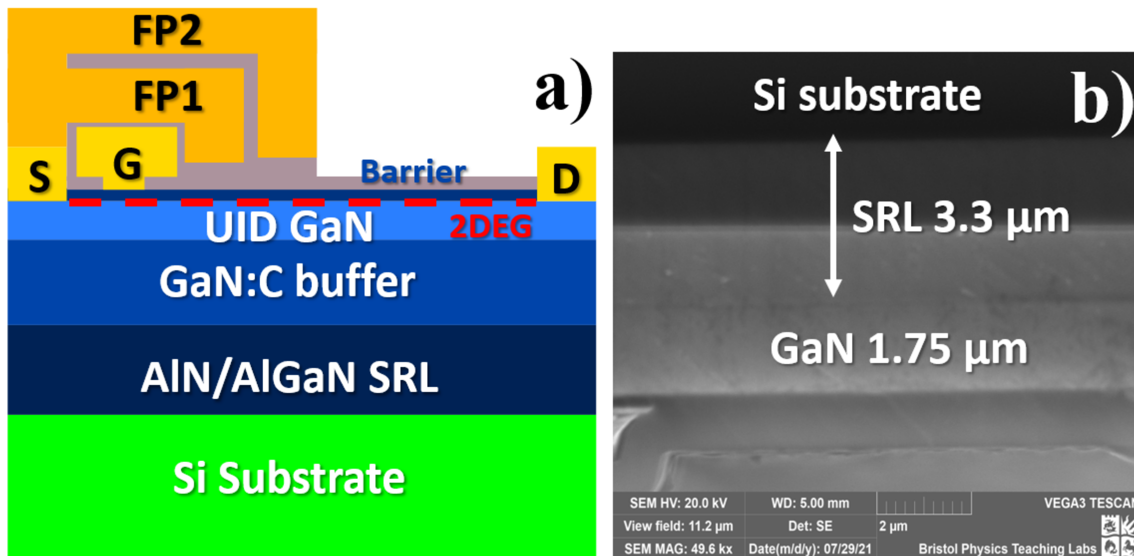

Figure 7.1: **a)** Schematic representation of the expitaxial structure of the power HEMTs before bonding. **b)** Scanning electron microscopy (SEM) image of the expitaxy with key layers labelled.

This study was performed on 150 mm-diameter GaN-on-Si wafers grown and fabricated by NXP Semiconductors. The epitaxy was grown by metal-organic chemical vapour deposition (MOCVD) method, and consisted of p-type Si substrate followed by AlN transistion layer and step-graded AlGaN strain relief layer (total thickness of transition layer and SRL is 3.3 μm), C-doped doped GaN buffer and UID Gan channel (total thickness of GaN is ~1.75 μm). 20 nm AlGaN barrier was grown over the GaN channel to form 2DEG with carrier density of 5.9×10^{12} cm^{-2}. 3-nm thick GaN cap was deposited on top of the barrier.

The devices were passivated with 70 nm of silicon nitride deposited by low-pressure chemical vapour deposition (LPCVD) at 850°C and pressure of ~100 mTorr in a horizontal LPCVD

furnace. The introduction of dichlorosilane (DCS) was preceded by soaking in NH_3 solution. The stoichiometry of the passivation was controlled by DCS to NH_3 precursor ratio, which for investigated samples was 3.3. The stress in the passivation and its refractive index were 275 MPa and 2.14 respectively.

This study was performed on HEMT structures with gate-source spacing of 0.7 μm and gate-drain spacing on 9.4 μm. The T-gate has the length of L_G = 3.4 μm, with gate fieldplate of 1 μm. The gate width is W_G = 100 μm. The devices are equipped with double source filed plate extending up to ~ 3 μm beyond the edge of the T-gate. Most measurements were performed on two-finger devices, however the effects of device active areas were studied using single-finger, 6-finger and 12-finger transistors. Figure 7.1 shows a schematic diagram of the epitaxy and the device structure.

7.2.2 Bonding Technique

Figure 7.2 shows a schematic flow diagram of the bonding process investigated in this study. Prior to bonding selected devices and bond substrate have to be prepared appropriately. The preparation process involves wafer dicing into chips of the size 12 × 12 mm^2, as well as laser cutting and polishing of the bond SiC substrate.

The bonding process begins with application of wax onto the chip and sapphire carrier at 80°C to form a homogeneous contact to the surface. The temperature is increased to 120°C and then further to 160°C to reflow the wax and make sure the adhesive is uniformly distributed across the chip surface, without forming bumps or regions of larger thickness. Sapphire handle and the chip are joint together at 140°C by the thermoplastic adhesive with the overall thickness of ~ 1 μm. This step is summarised in Fig. 7.2a. In the subsequent step, teflon tape is used to passivate the rim around the 9 mm diameter circle at the bottom of GaN-on-SiC samples in preparation for substrate etching. The etching mixture contains HF (49%) and HNO_3 (69%) in the ratio 1:3. The passivated chip is immersed in the mixture and the substrate is etched at the rate of ~16 μm per minute. This step is shown in Fig. 7.2b.

After etching is complete the sample is rinsed in deionized water to remove any residual acid. In the meantime, bond substrates are cleaned chemically in the RCA1 solution. After removing the teflon tape the chip is submerged in the fresh beaker with deionized water and the SiC bond substrate is contacted to the bottom of a chip as shown in Fig. 7.2c. The sample is then placed in the spin-coater and held together with magnets as shown in Fig. 7.2d. The spin coating takes place at 3000 rpm for 5 minutes to allow for capillary bonding of the chip and the bond substrate.

The chip and substrate are then placed in a bonding apparatus and tightened to exert a force on the sample stack. This setup is placed in the vacuum oven for 72 hours: 48 hours are spent at 80°C while for the final 24 hours the temperature is increased to 140°C (Fig. 7.2e). The handle wafer is removed by heating up the sample to 160°C to dissolve the temporary adhesive. Finally, the sample undergoes ultrasonic cleaning in acetone solution to remove any residual wax. Figure

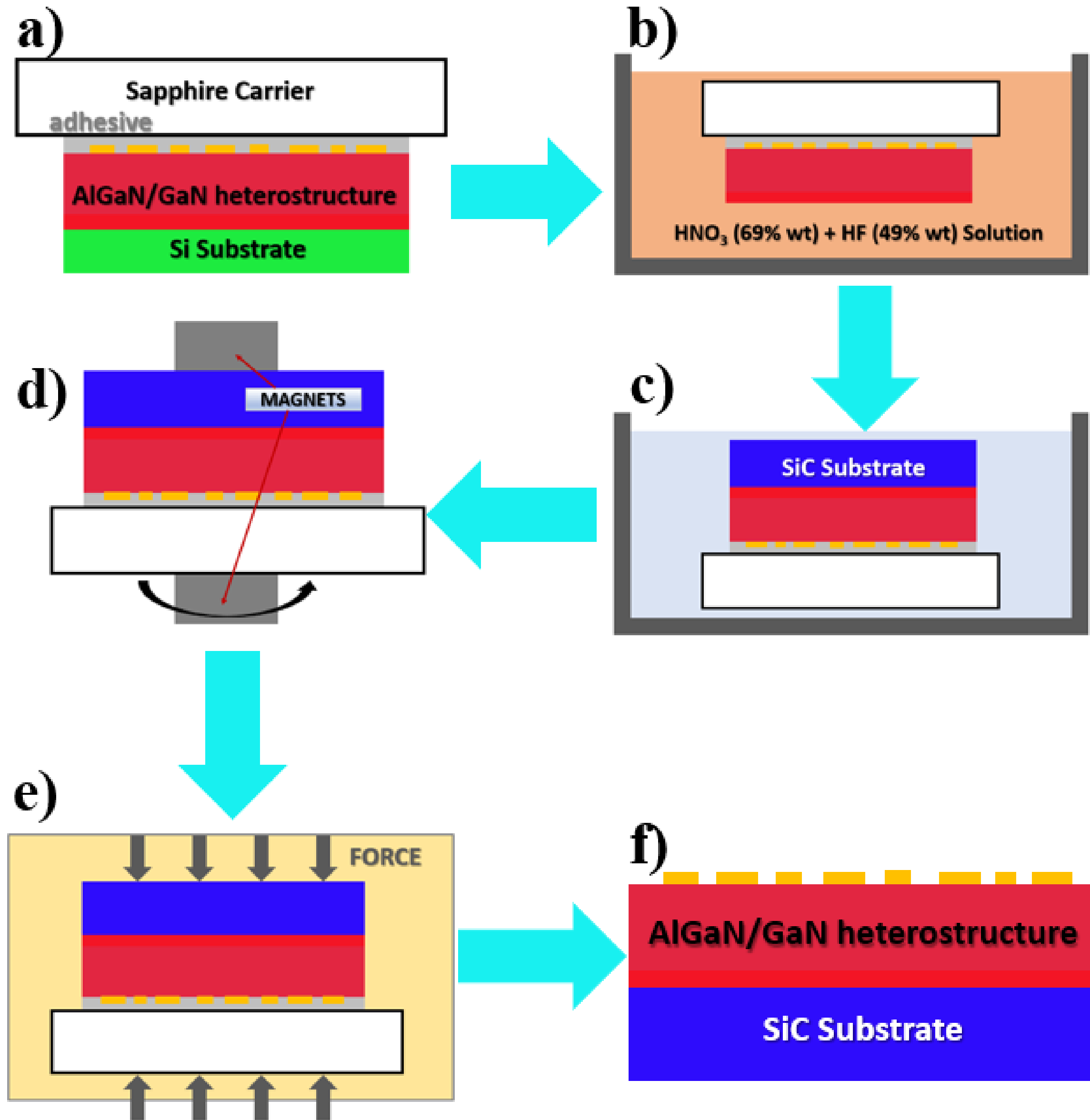

Figure 7.2: Schematic representation of key steps involved in the bonding technique investigated in this study. **a)** Heterostructure stabilisation by mounting the chip onto carrier wafer using temporary adhesive. **b)** Removal of Si substrate by etching in the acid mixture. **c)** SiC (bond) substrate contacted to the heterostructure in deionized water. **d)** Spin-coating of the sample to allow for capillary bonding. **e)** Annealing in the vacuum oven with applied pressure. **f)** Carrier wafer removed.

7.2f shows the final result of the bonding process. In this study, the bonded devices still contain the original transition layer and SRL.

Figure 7.3a shows a TEM image as an example of the solid bond interface with the thickness of ~ 30 nm between AlGaN/GaN heterostructure thin film and bond diamond substrate formed using bonding technique described above [269]. The chemical reaction involved in formation of

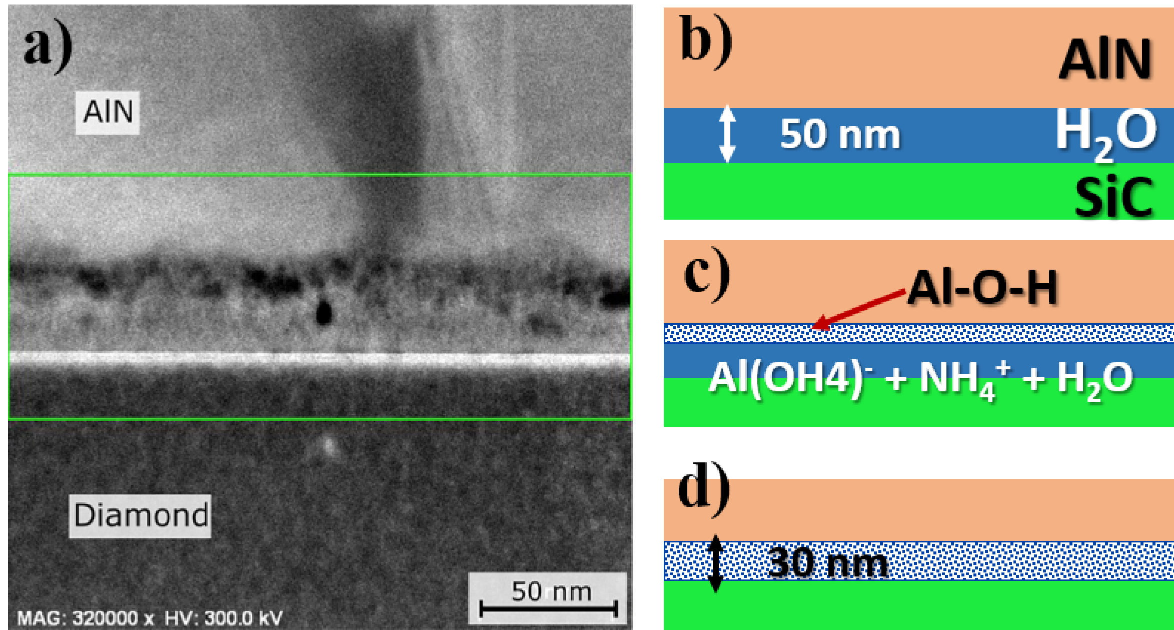

Figure 7.3: **a)** TEM image of bonded interface between AlN (bottom of AlGaN/GaN heterostructure thin film) and diamond bond substrate. The green box indicates the covalently bonded aluminium hydroxide layer. Image adapted from [269]. Diagrams **b) - d)** show a schematic formation of bond interface between AlGaN/GaN heterostructure thin film and SiC bond substrate, where: **b)** initial water layer trapped at the interface, **c)** reaction between water and AlN takes place, **d)** final bond layer of solid aluminium hydroxide is formed. In this study, strain relief layer is present throughout the entire process.

this interface is schematically represented in Fig. 7.3b-d. Following the spin-coating step of the bonding process (Fig. 7.3d) a thin layer of water becomes trapped between the heterostructure and the bond substrate (Fig. 7.3b). At room temperature no chemical reaction between water and AlN takes place, however as the temperature is increased AlN starts dissolving in water, creating alkaline solution of $Al(OH)_4^-$ and NH_4^+, which further accelerates the reaction, with small amounts of solid aluminium hydroxide forming at the interface (Fig. 7.3c). When all the water is consumed in the reaction, the chemical process stops resulting in solid aluminium hydroxide layer (Fig. 7.3d), which covalently bonds the substrate to the thin film with the AlGaN/GaN heterostructure. The same process is expected to take place in this experiment.

7.2.3 Experimental Details

The main objective of this study is electrical and thermal characterisation of the GaN-on-Si power HEMTs before and after Si substrate removal and subsequent bonding onto a SiC substrate. The electrical measurements consist of DC and pulsed IV (duty cycle = 0.1 %, with 1 μs t_{ON} and 1 ms t_{OFF}) characterisation of two-finger GaN HEMTs with gate length L_G = 3.4 μm, gate width W_G = 100 μm and gate-drain spacing of 9.4 μm. All IV measurements were performed using Keithley

4200-SCS Parameter Analyzer.

To further investigate the effects of bonding on electrical properties of the bonded devices, the dynamic On-resistance measurements were performed on two-finger GaN HEMTs before and after bonding. The procedure involved application of off-state stress with drain bias up to 400 V (V_G = -5 V during stress phase). The stress duration of 1 s was chosen for this experiment, which was performed using a combination of high voltage Keithley 2657A instrument to deliver drain stress and Keithley 2636B for biasing of the gate and source contacts. Both instruments were controlled via Keithley Test Scrip Builder software.

In addition, bidirectional substrate ramp sweeps were performed on the devices before and after bonding. This technique involves application of small bias between source and drain (V_{SOURCE} = 0 V, V_{DRAIN} = 0.5 V) with the gate grounded throughout the measurement, while the substrate potential is gradually swept at a constant rate from 0 V to a chosen negative bias point and back to 0. This experiment was performed using the combination of Keithley 2636B (to bias the source and drain) and high voltage Keithley 2657A (to supply substrate bias) instruments, which were controlled via Keithley Test Scrip Builder software. For the entire duration of the experiment vertical leakage currents were monitored using guarded chuck. Substrate ramp sweeps were performed across multiple samples and for single finger, 2-finger, 6-finger and 12-finger devices to assess the uniformity of electrical performance and the effects of active area on substrate ramp characteristics.

To assess the effects of bonding on vertical leakage currents through the epitaxy 15 single finger devices were biased via the substrate through a triaxial chuck at the voltage V_{SUB} = 400 V for 300 s (with source, drain and gate grounded) using high voltage Keithley 2657A instrument and the vertical leakage currents were measured. The experiment was performed on the devices before and after bonding to provide a reliable comparison. Similarly, dynamic R_{ON} measurement was performed on devices before and after bonding, which involved application of Off-state drain stress up to 400 V for 10 s, followed by measurement of On-resistance immediately after removal of the stress.

The thermal characterisation consisted of micro-Raman thermography assisted by deposition of TiO_2 nanoparticles on the device surface. The deposition was performed by heating up the sample to 95°C, followed by dropwise deposition of anatase nanoparticle (particle diameter = 30 nm) solution with the concentration of 0.012 mmol/cm^{-3} and 99.98% purity. A Renishaw InVia system with 488 nm frequency double diode laser (laser spot diameter = 0.5 μm) and an 0.5 NA objective lens were used to measure the shift in Raman E_g mode of TiO_2 naoparticles as a function of power dissipation, with the sample mounted on a thermo-electric vacuum chuck maintained at 25°C. Prior to the experiment the temperature coefficients of Raman modes of TiO_2 nanoparticles were obtained from calibration in the temperature range between 25°C - 300°C. In addition, the Raman shifts of A_1 (LO) and E_2 high peaks of GaN were measured and the average channel temperatures of GaN (UID GaN channel and C-doped GaN buffer together) were derived.

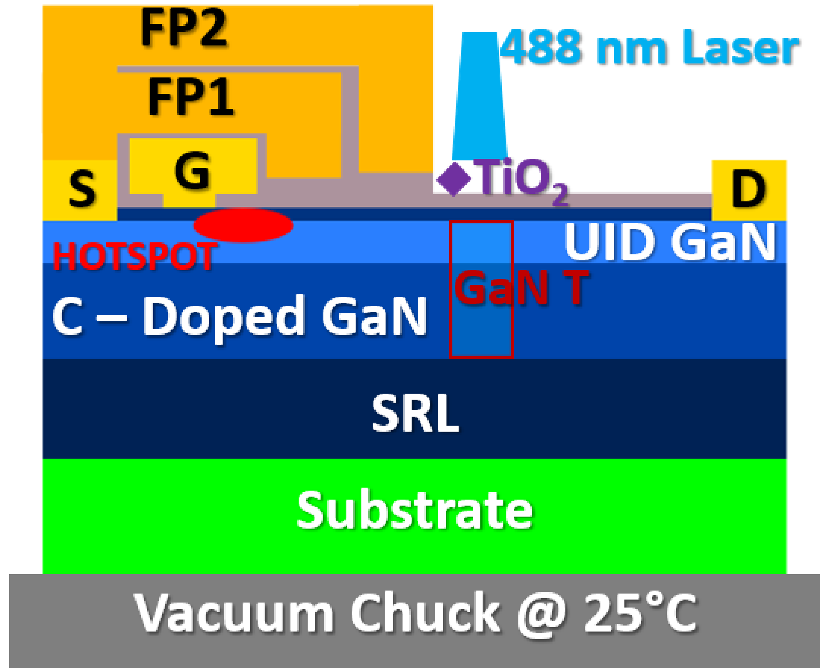

Figure 7.4: Schematic diagram showing micro-Raman thermography measurement of GaN HEMTs before and after bonding. TiO_2 were used to measure the surface temperature at the edge of the second field plate FP2, while GaN A_1 (LO) and E_2 high peaks were used to extract the average GaN temperature (marked by the red "GaN T" box).

Figure 7.4 shows schematic diagram of the Raman measurement performed on the GaN HEMTs before and after bonding. To account for the effects of strain on the frequency of investigated Raman modes, thermomechanical stress correction was implemented as outlined in section 3.3.2.

7.3 Results

Figure 7.5 shows DC measurements of two-finger GaN HEMTs performed on the same device before and after it was bonded to the 4H-SiC substrate. After transferring the AlGaN/GaN heterostructure films onto SiC substrate from Si, IdVd measurements (Fig.7.5a) show consistently higher drain currents than before bonding (up to ~ 20% current increase at V_D = 20 V, V_G = 1 V). In addition, at higher gate voltages the drain current of bonded devices shows slower decrease with applied drain potential in comparison to measurements taken before device transfer. The On resistance of bonded devices remains unchanged with average R_{ON} measured for original devices as 6.08 ± 0.3 Ω·mm and 6.17 ± 0.2 Ω·mm for GaN HEMTs bonded to SiC. The IdVg measurements shown in Fig.7.5b demonstrate little variation before and after bonding. The threshold voltage V_{TH} (here defined as the voltage at which drain current drops below 1 μA) remains relatively unchanged, with V_{TH} = -2.1 V before bonding and V_{TH} = -2.2 V after.

Figure 7.6 shows a pulsed IV measurement of two-finger (gate length L_G = 100 μm) GaN-

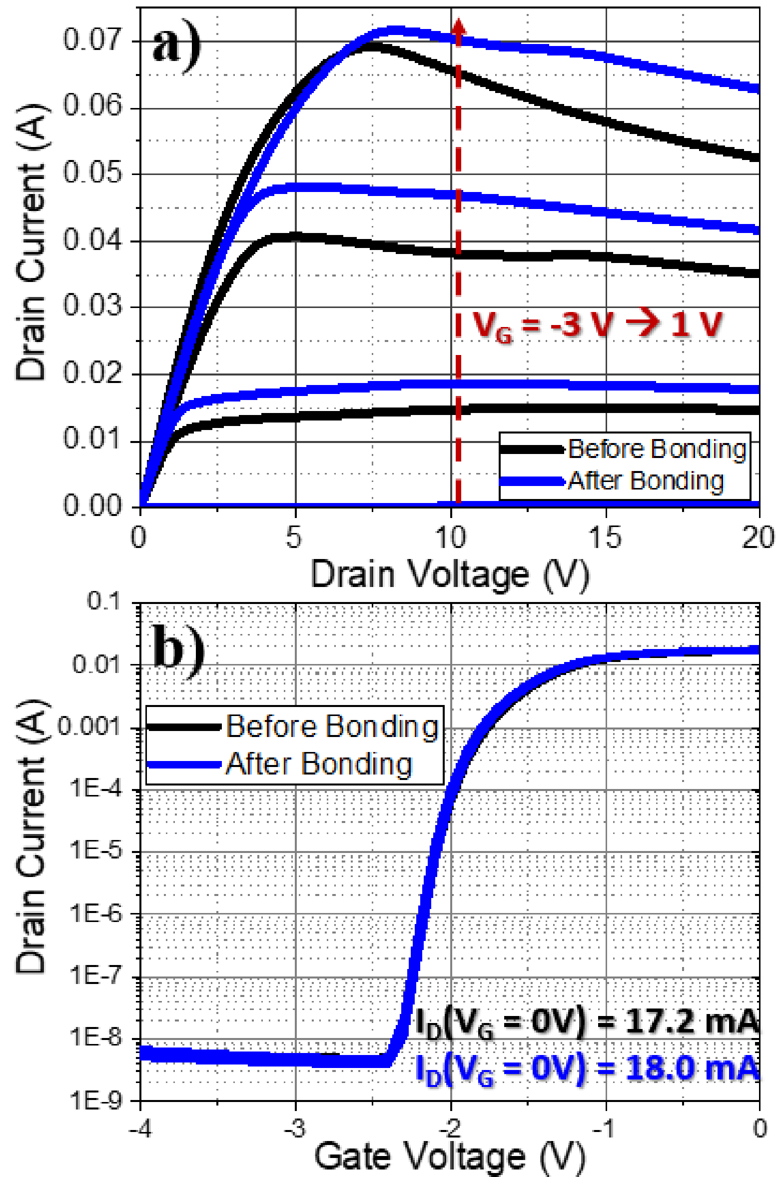

Figure 7.5: **a)** DC IdVd measurements of the two-finger GaN HEMT with gate length L_G = 100 μm and gate-drain spacing of 9.4 μm before and after bonding for gate voltages V_G = -3 V → 1 V in steps of 1 V. **b)** DC IdVg measurements of the two-finger GaN HEMT before and after bonding at drain voltage V_D = 1 V.

on-Si HEMTs (before bonding) and after the device was transferred onto a 4H-SiC substrate for quiescent bias points [$V_{D,Q}$, $V_{G,Q}$] = [0 V, 0V] and [40 V, -7 V]. Measurement duty cycle was set to be 0.1 % (t_{ON} = 1 μs, t_{OFF} = 1 ms). The drain current measured for pulsed IV characteristics from the queiescent bias point [0 V, 0V] (no stress applied) exceeds the values measured in the DC mode by 47% and 29% for HEMTs before bonding and for bonded devices respectively (at non-quiescent drain bias of $V_{D,NQ}$ = 20 V). As the quiescent stress is increased to [$V_{D,Q}$, $V_{G,Q}$]

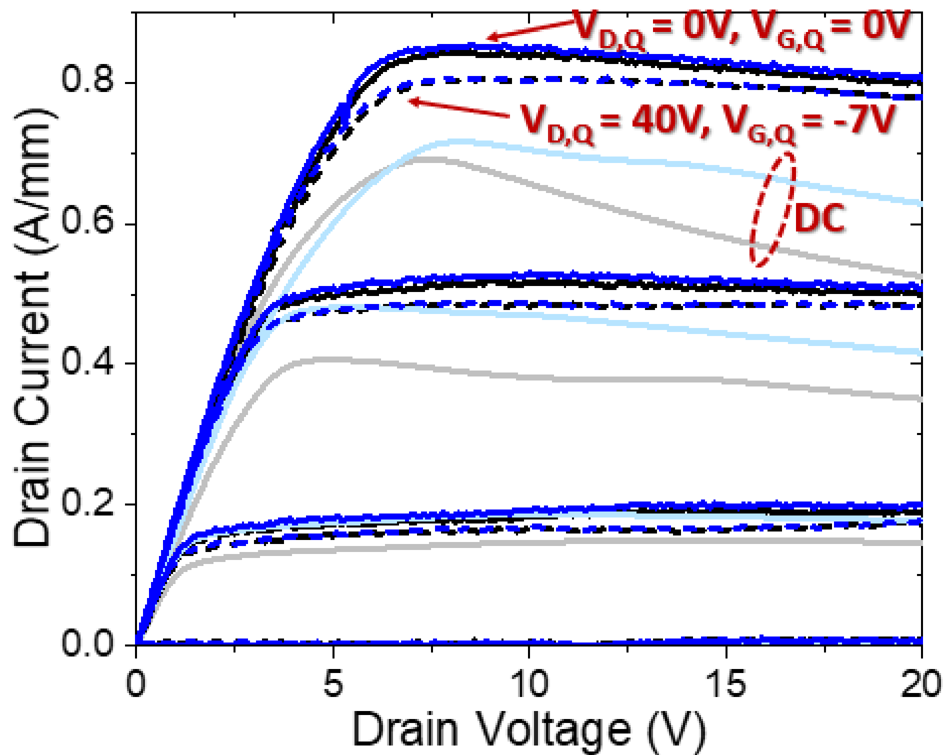

Figure 7.6: Pulsed IV measurement of two-finger GaN-on-Si HEMTs (before bonding, black lines) and transistors bonded onto 4H-SiC substrate (blue lines) for quiescent bias points [$V_{D,Q}$, $V_{G,Q}$] = [0 V, 0V] and [40 V, -7 V] for non-quiescent gate voltages $V_{N,Q}$ = -3 → 1 V. Measurement duty cycle = 0.1 % (t_{ON} = 1 μs, t_{OFF} = 1 ms). DC IV characteristics are shown for comparison.

= [40 V, -7 V], measured drain current for both sets of devices dropped by 5%, however there is no significant difference in drain current between bonded devices and original GaN-on-Si transistors.

To further assess the electrical performance of the GaN HEMTs before and after bonding, the effects of off-state drain stress on dynamic R_{ON} were measured for both sets of devices. Figure 7.7 shows normalised On-resistance as a function of off-state drain stress (with gate voltage V_G = -5 V during stress), which was calculated from the slope of IV characteristics for V_D = 1 V, V_G = 0 V. The values were normalised against the baseline described by R_{ON} measurement with no stress applied. Both sets of HEMTs before and after bonding show very similar patterns: initial decrease in dynamic R_{ON} below the baseline (up to drain stress $V_{D,STRESS}$ = 200 V) followed by a sharp increase of up to 37% in the range 200 V < $V_{D,STRESS}$ < 320 V. As drain voltage is increase further up to 400 V (not shown in the figure), the dynamic R_{ON} increases exponentially for GaN-on-Si transistors and the bonded devices to reach values as high as 348% and 353% in comparison to the baseline respectively. The bonded devices record moderately lower dynamic R_{ON} values for stress up to 200 V, but show slightly quicker increase for higher drain stress biases.

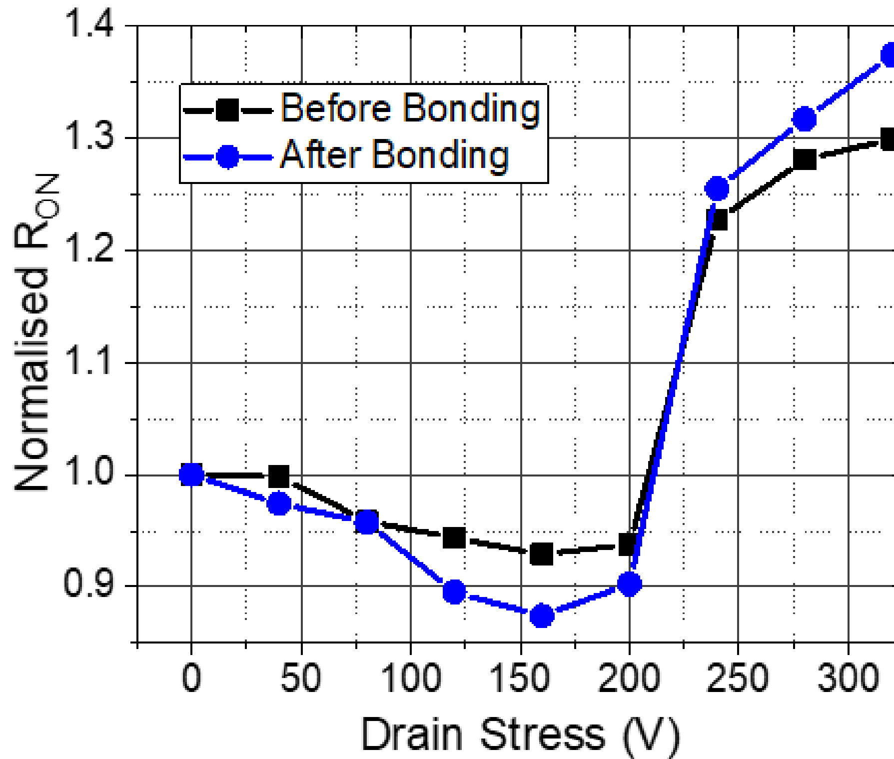

Figure 7.7: Normalised R_{ON} as a function of off-state drain stress for single finger GaN HEMTs before and after bonding onto SiC substrate (gate voltage during stress V_G = -5 V.

Bidirectional substrate ramp sweeps were performed on 15 different single finger HEMTs before and after bonding showing little variation in displayed characteristics, indicating uniform behaviour across both samples before and after bonding. Figure 7.8 shows a comparison between typical bidirectional substrate ramp sweeps for a single finger HEMT on Si and 4H-SiC substrates. The capacitive line indicates a theoretical case where the entire epitaxial stack acts as a perfect dielectric.

Both sets of curves show similar qualitative behaviour across the measured voltage range: both lines initially show gradual drop in the measured 2DEG current, followed by a minor slowing down in the current decrease for substrate voltages $|V_{SUB}|$ > 200 V. The reverse sweep is characterised by steady increase in current above the level of shown in the forward sweep, followed by eventual current saturation. The final current at 0 V in each case is ~ 2% higher than the starting value. However, despite similar trends observed for both sets of devices, HEMTs bonded to SiC substrates show higher overall currents throughout the sweep: when the 2DEG current of the original HEMTs drops to 5% of the original value at V_{SUB} = -400 V, the bonded devices record the normalised current of 20%.

To assess the effects of variation in active area on the substrate ramp characteristics, bidirectional substrate ramp sweeps were performed on single-finger devices as well as multifinger HEMTs (the active area varied from 940 μm^2 to 10,340 μm^2. Example of the data from substrate

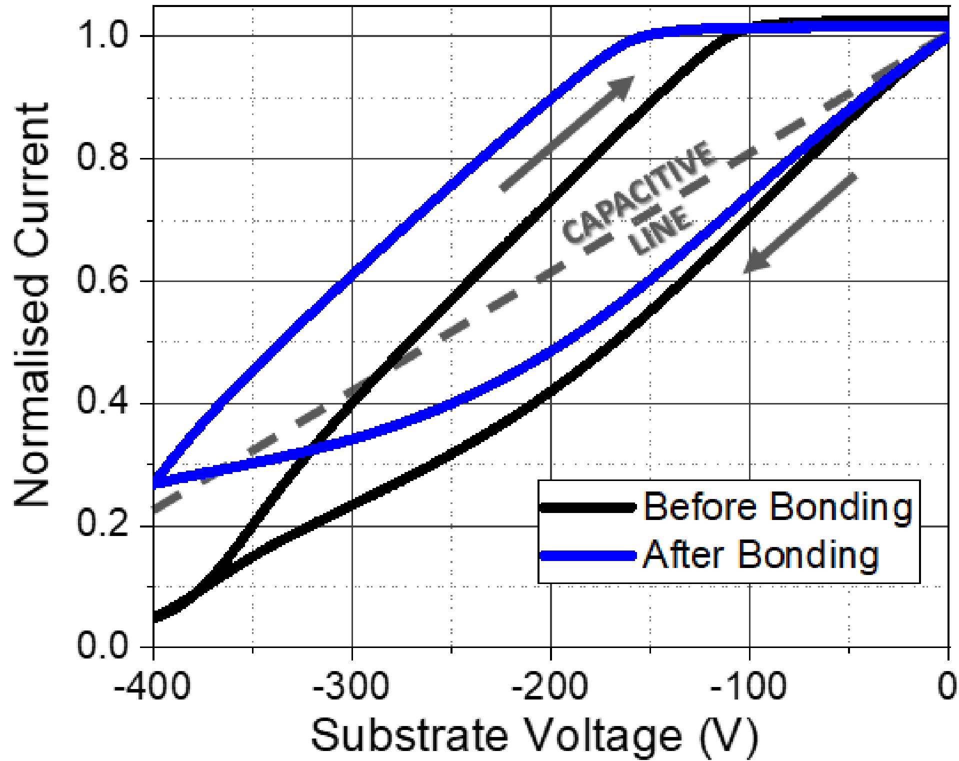

Figure 7.8: Bidirectional substrate ramp sweep performed on a single finger GaN HEMT with gate length L_G = 100 μm and gate-drain spacing of 9.4 μm before and after bonding at a constant rate of 1 V/s. The arrows indicate the direction of the sweep. The capacitive line indicates theoretical perfect dielectric response of the epitaxial stack.

ramp measurements of bonded GaN HEMTs is shown in Figure 7.9. Despite over 10 fold increase in the active area, the devices show little variation in substrate characteristics, which is also observed in the unbonded devices.

Figure 7.10 shows average the vertical leakage current measurements for 15 single finger devices before and after bonding. The inset to Fig. 7.10 shows an example of collected data for GaN HEMTs before bonding, which shows high uniformity in measured currents (bonded devices show similar degree of uniformity) to justify averaging of the measurements. The results suggest minor reduction in the vertical leakage current on the order of 10^{-11} A for bonded devices in comparison with the original sample.

Figure 7.11 shows Raman spectra of investigated two-finger GaN HEMTs on Si (before bonding) and SiC substrates (after bonding). GaN E_2 high and A_1(LO) peaks are present in both spectra and the shift in these Raman modes is used to extract the average channel and buffer temperatures. The position of GaN E_2 mode at 568.8 cm^{-1} indicates biaxial stress of 0.6 GPa presnent in this layer and is not affected by bonding. As expected, the Si peak at 520 cm^{-1} is not present in the Raman spectra of bonded samples indicating complete removal of the original substrate (see Fig. 7.11a). Instead, the spectra of bonded devices show strong peak at 778 cm^{-1}

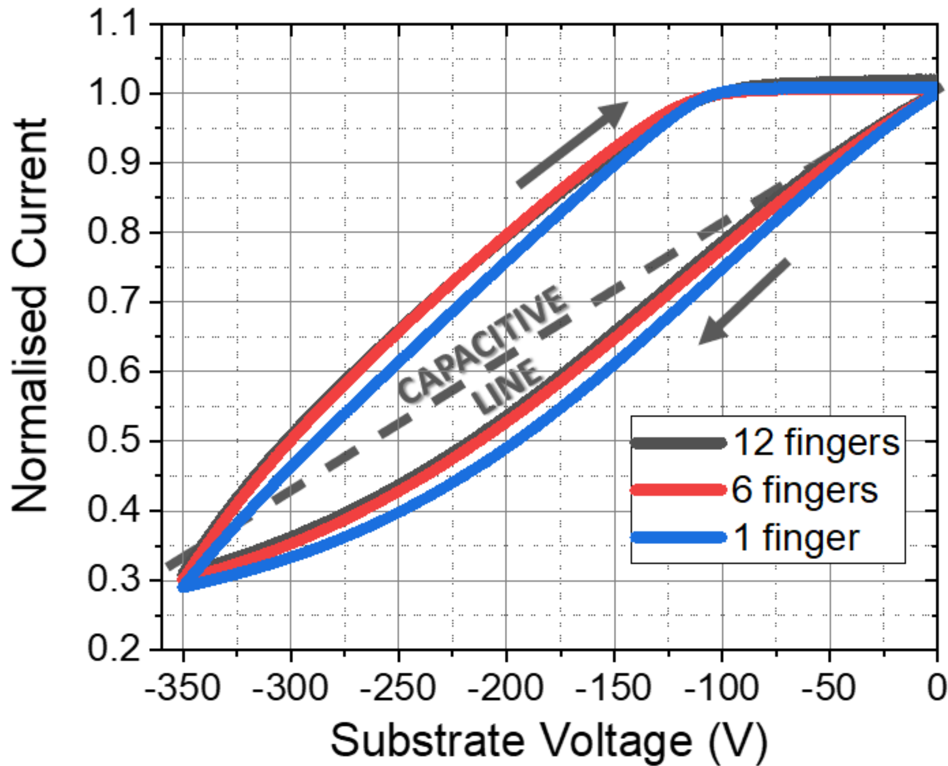

Figure 7.9: Bidirectional substrate ramp sweep performed on a single finger, 6-finger and 12-finger GaN HEMTs with gate width W_G = 100 μm bonded onto SiC at the ramp rate of 1V/s. Arrows indicate the direction of the sweep.

corresponding to 4H-SiC E_2 (TO) mode associated with the new substrate. After suspension of anatase nanoparticles is deposited on the device surface, the Raman spectrum also includes modes associated with TiO_2 as shown in Fig. 7.11b. The strongest E_g peak at 144 cm^{-1} (circled in red) is used to extract surface temperatures of the devices, however the B_{1g}, A_{1g} another E_g mode are present at 393 cm^{-1}, 517 cm^{-1} and 638 cm^{-1} respectively.

Micro-Raman thermography measurement of average GaN temperatures (including UID GaN channel and C-doped GaN buffer) for power dissipations up to 4 W/mm derived from Raman shift of A_1 (LO) and E_2 high peaks are shown in Figure 7.12. Table 7.1 gives a summary of fitting parameters used for temperature calculations. The temperature measurements were corrected for thermomechanical strain present in the epitaxy, by considering the temperature and strain dependence of vibrational frequency of each mode in relation to a measurement taken in the Off state. The full details of this technique are given in section 3.3.2. The result indicate bonding results in decrease in average GaN temperature from 111.1 ± 5 °C to 94.5 ± 6 °C at 4 W/mm. These values correspond to thermal resistance of GaN layers of 27.8 °C mm W^{-1} before bonding and 23.6 °C mm W^{-1} after bonding. In addition, device surface temperatures before and after bonding were calculated from Raman shift of E_g mode of the TiO_2 nanoparticles deposited at the edge of the second field plate for power dissipations up to 5 W/mm. The Raman shift of TiO_2 E_g

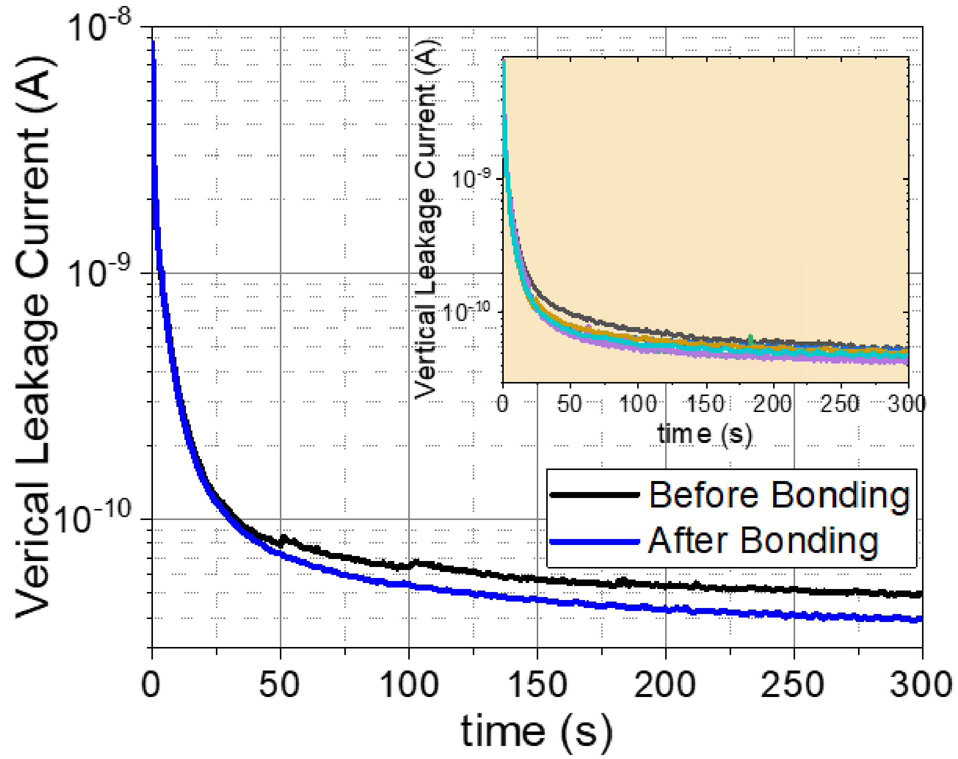

Figure 7.10: Average vertical leakage current for 15 single finger GaN HEMTs before and after bonding for the substrate bias V_{SUB} = 400 V. Inset: example of leakage currents measured for HEMTs before bonding.

mode increases linearly with applied temperature and can be described according to the equation: T(°C) = 143.0 [cm^{-1}] + 0.0234·ω, where ω denotes the Raman shift of the E_g peak. Fig. 7.13 shows the comparison between surface and corrected GaN temperatures measure for the investigated devices before and after bonding.

Table 7.1: GaN Phonon Temperature Dependence Coefficients

Material & Phonon	A	B	ω_0 (cm^{-1})
GaN-on-Si **A_1 (LO)**	23.3	0.68	736.3
GaN-on-Si **E_2 high**	20.6	1.33	568.0
GaN-on-SiC **A_1 (LO)**	15.9	0.51	736.5
GaN-on-SiC **E_2 high**	19.1	1.20	568.5

Temperature coefficients taken from [217].

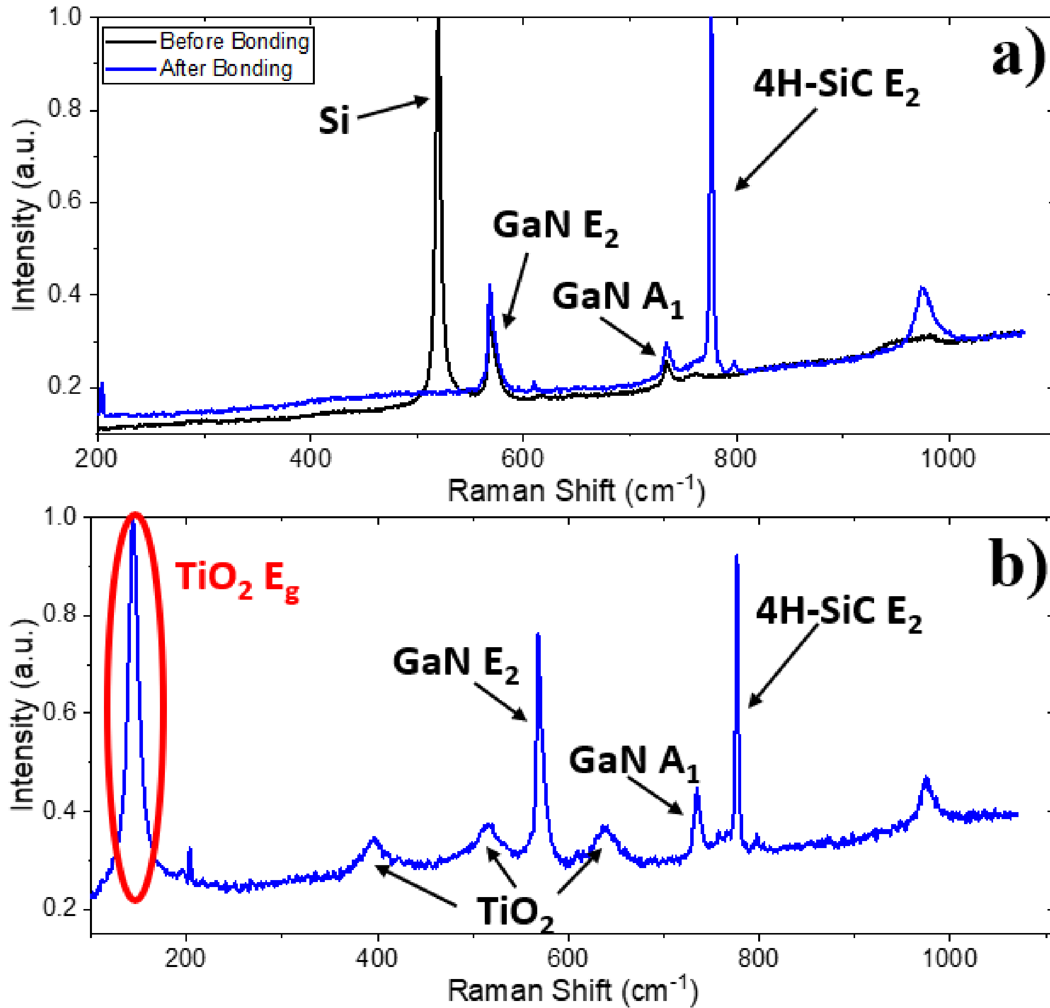

Figure 7.11: **a)** Raman spectrum taken for a single finger GaN HEMT on Si substrate (before bonding) and after bonding onto 4H-SiC substrate. All the major Raman active modes are indicated in the figure. E2 (high) and A1 (LO) peaks are used to extract average GaN temperature of the operating devices. **b)** Raman spectrum of a TiO_2 nanoparticle deposited on a single finger GaN HEMT bonded onto 4H-SiC substrate. TiO_2 E_g peak are used to extract surfaces temperatures of the operating devices.

7.4 Discussion

DC IV characteristics were measured for number of samples before and after bonding, in each instance showing little variation within the investigated device group. This result suggests the bonding process has a consistent effect on the GaN HEMTs studied in this chapter. Figure 7.5 shows a comparison between a typical GaN-on-Si HEMT and a device transferred onto SiC substrate. Increase in drain current observed in the bonded devices (Fig. 7.5a) can be attributed to reduced self-heating, resulting from incorporation of substrate with a higher thermal conductivity (see Fig. 7.13). The bonding technique has little effect on threshold voltage of the device (Fig.

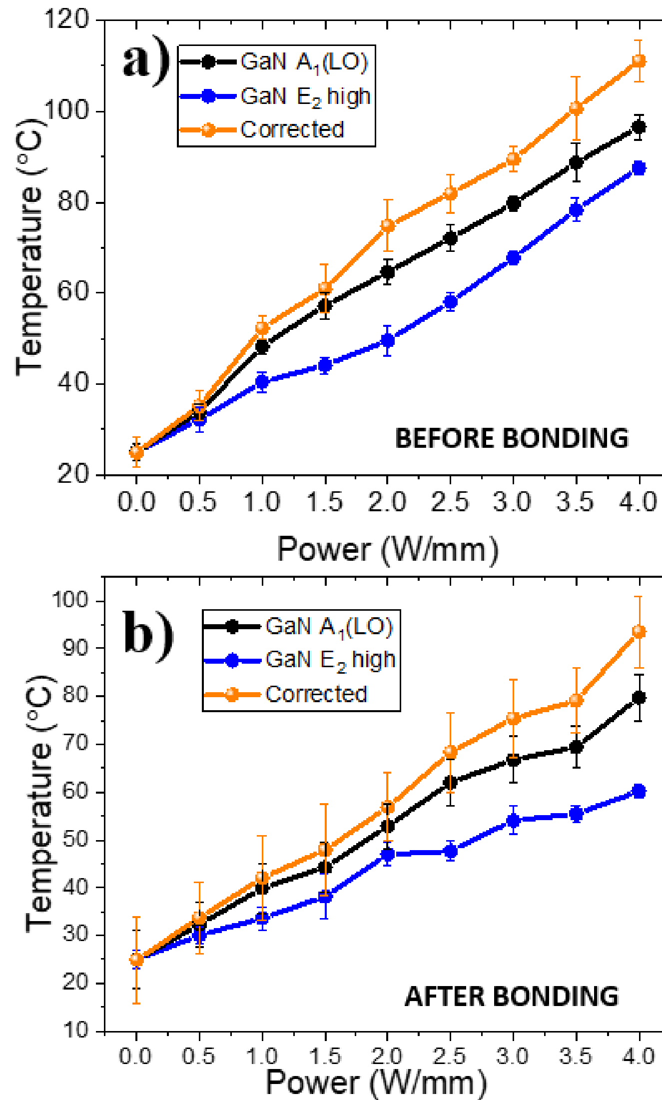

Figure 7.12: GaN temperatures derived from A_1(LO) and E_2 high Raman modes for two-finger GaN HEMTs **a)** before bonding and **b)** after bonding. The results were corrected for thermomechanical strain present during device operation (shown in orange).

7.5b) and the slight increase in drain current also attributed to reduction in self-heating. The DC IV characterisation shows no adverse effects of bonding on the overall device performance after its transfer onto the bond substrate.

Pulsed IV characterisation involves delivery of short period (yet of sufficient duration to allow for trapping) stress pulses (quiescent bias points), with even shorter measurement windows (non-quiescent bias points) as not to induce further trapping or cause self-heating in the device. The latter is the explanation for the discrepancy between DC and pulsed IV characteristics seen in Figure 7.6. Due to the measurement window (t_{ON}) of only 1 μs the effects of device self-heating are negligible, resulting in no appreciable difference between pulsed IV characteristics of GaN

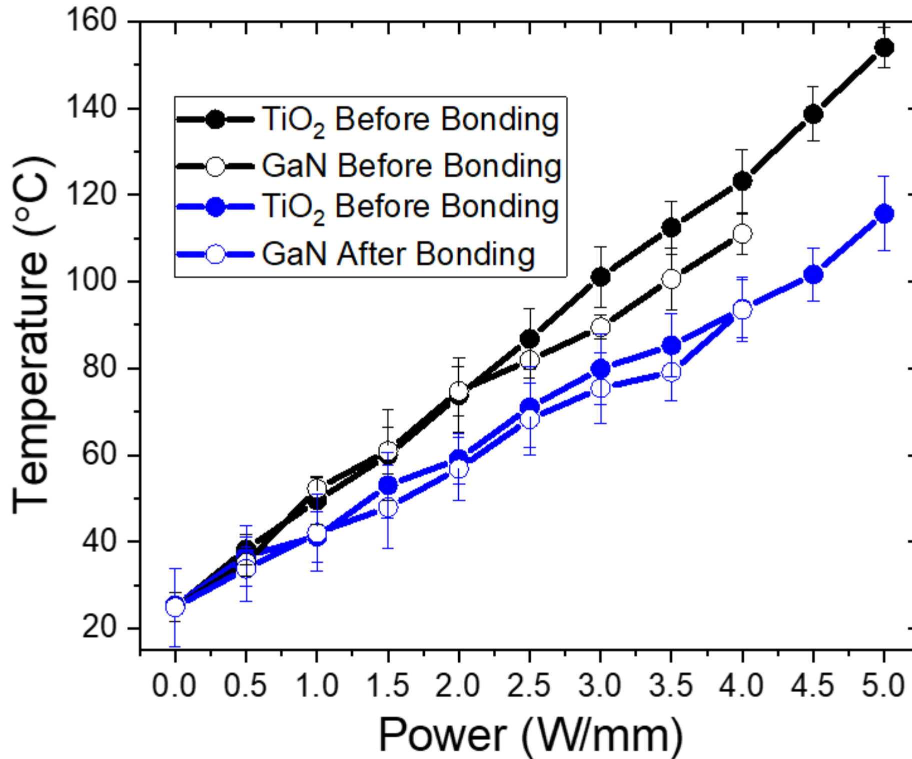

Figure 7.13: Temperatures measured using micro-Raman thermography method based on shifts in GaN E_2 and A_1 peaks (labelled T(GaN) to indicate average GaN temperature), and calculated from shift in the TiO_2 E_g mode (labelled T(TiO_2) to denote surface temperatures) for power dissipations up to 5 W/mm before and after bonding.

devices before and after bonding onto SiC substrate for measurements performed at quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [0 V, 0 V]. Stressing the devices at the quiescent bias point [$V_{D,Q}$, $V_{G,Q}$] = [40 V, -7 V], serves to investigate trapping effects in the drain-gate access region. The decrease in drain current at this bias point (shown in Fig. 7.6) suggest some minor trapping in this region, however there is little difference in current decreased between original GaN-on-Si HEMTs and bonded transistors indicating the source of trapping has been present before the bonding process. This result suggests bonding does not induce any further buffer trapping that would have an adverse effect on the device output characteristics. Both sets of devices show low Off-state current without any signs of punch-through, indicating good carrier confinement in the channel and absence of any parallel leakage paths before and after bonding.

Similar conclusions can be drawn from the dynamic R_{ON} measurements shown in Figure 7.7. Despite some minor differences in the R_{ON} across the entire measurement range, the dependence of On-resistance with applied off-state drain stress looks broadly similar in bonded devices as compare to the results from the original GaN-on-Si HEMTs. These results suggest bonding process has no significant negative influence on electrical performance of the devices.

Substrate ramp measurements shown in Figure 7.8 can be interpreted by comparing the

current response to the capacitive line (i.e. the line indicating an ideal case in which the entire epitaxy acts as a perfect dielectric). Any response below the line indicates negative charge storage in the buffer, while any response above the line suggests positive charge storage in the buffer. Substrate ramps measured for sets of devices initially follow the capacitive line for voltages $|V_{SUB}| < 15$ V, indicating leakage across each layer in the epitaxy is smaller than the displacement current $I_{DISS} = C_{TOT} \times V_{SUB}$, where C_{TOT} denotes the total capacitance of the epitaxial stack. As the substrate potential is increased the original devices before bonding show more rapid decrease in 2DEG current, indicating more significant negative charge storage in the buffer as compared to bonded devices. The decrease in current observed in this section of substrate ramp can be associated with charge redistribution across the C - doped GaN buffer and has been described in more detail in Chapter 4.

As the substrate bias reaches $|V_{SUB}| \approx 240$ V, the observed decrease in 2DEG current slows down. The change in gradient of normalised current at this point is very minor for HEMTs on Si substrate, however in case of bonded devices 2DEG conductivity almost plateaus for substrate voltages exceeding -300 V. This region correspond to band-to-band leakage across UID GaN channel and is discussed in more detail in previous chapters. The increase in positive charge storage in the buffer of bonded devices indicates the bonding process can have an effect on conduction via dislocations. Increased leakage across the UID GaN channel observed in this part of the substrate ramp results in better shielding of 2DEG current from the applied potential.

In general, bonded devices show higher 2DEG current throughout the entire forward sweep and as the substrate voltage reaches $|V_{SUB}| \approx 370$ V forward substrate ramp response crosses over the capacitive line indicated net positive charge storage in the buffer. The results suggest the bonding technique leads to overall higher positive charge concentration in the buffer, while it does not give rise to any effects adverse to the electrical performance of the buffer.

Bidirectional substrate ramp sweeps shown in Fig. 7.9 demonstrate little variation in the substrate ramp characteristics with the device active area for GaN HEMTs bonded to SiC substrates (similar observation was made for original devices on Si substrate). This result indicates no internal lateral leakage paths inside the epitaxy and therefore confirms the bonding process does not introduce 2DHGs or 2DEGs at heterointerface in the epitaxy, as the presence of lateral conduction path would result in significant difference in substrate ramp characteristics as demonstrate in [213]. Likewise, the measurements of vertical leakage current for original GaN-on-Si transistors and bonded devices (shown in Figure 7.10) suggest device transfer onto SiC substrate does not introduce any additional vertical leakage paths that would result in the reduction of breakdown voltage of the HEMTs.

In order to conduct a more comprehensively analysis of thermal performance of GaN HEMTs before and after bonding, the structures were simulated using Ansys FEA software (see Figure 7.14). Device geometry, epitaxy and measurement conditions were represent faithfully to replicate the experiment as accurately as posiible. The model includes 10 nm × 500 nm heater at the

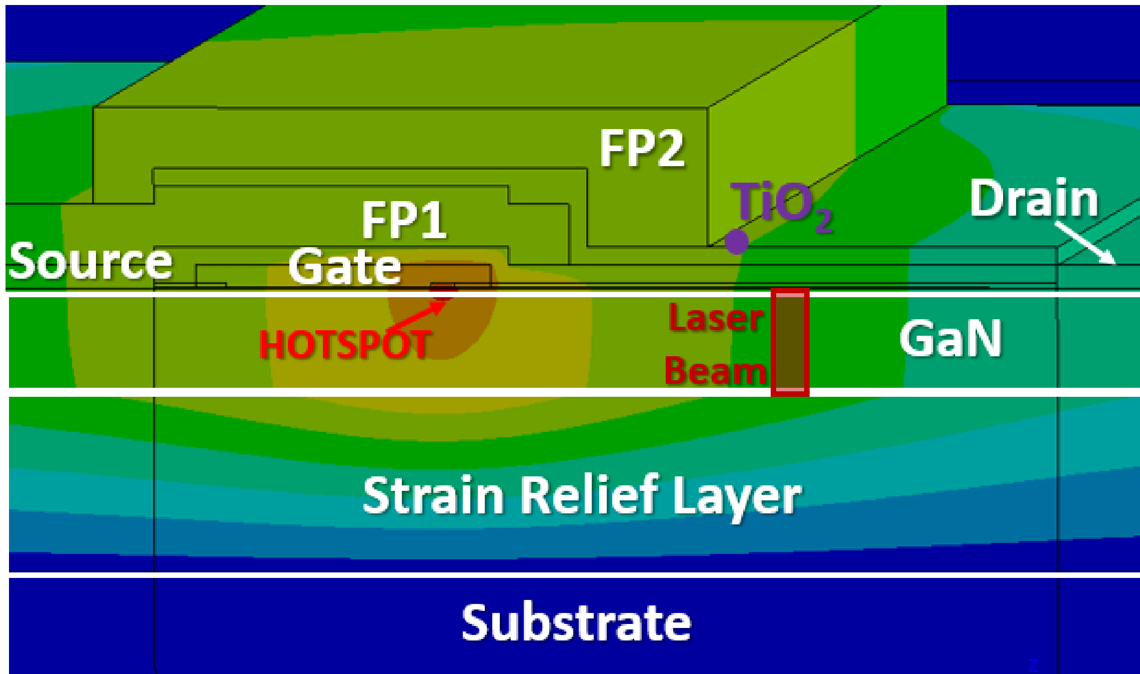

Figure 7.14: GaN HEMT structure simulated using Ansys FEA Software. The device geometry, epitaxial structure and measurement conditions were represented accurately including two source fieldplates (FP1 and FP2), the heater under the drain-side gate edge, TiO_2 nanoparticle and laser beam for averaged temperature measurement.

Table 7.2: Thermal Conductivity Values for Ansys Simulations

Material	Thermal Conductivity [W/mK]
GaN	$160 \times (298/T)^{1.4}$
4H-SiC	$360 \times (298/T)^{1.15}$
Si	$150 \times (298/T)^{1.3}$
SRL	5.2
AlGaN	14
Contacts	315

Thermal conductivity parameters used in the simulations of GaN HEMTs before and after bonding. Temperature dependence from [260] and [205].

drain-side gate edge to simulate hot spot present during device operation [190]. To simulate the micro-Raman thermogrpahy measurement, the temperature was averaged across a 500 nm wide rectangle extending across the entire depth of GaN channel and buffer. In addition, a particle with the dimensions 30 nm × 30 nm was placed on the device surface as indicated in Fig. 7.14. Thermal conductivities of all key layers used in Ansys simulation are summarised in Table 7.2.

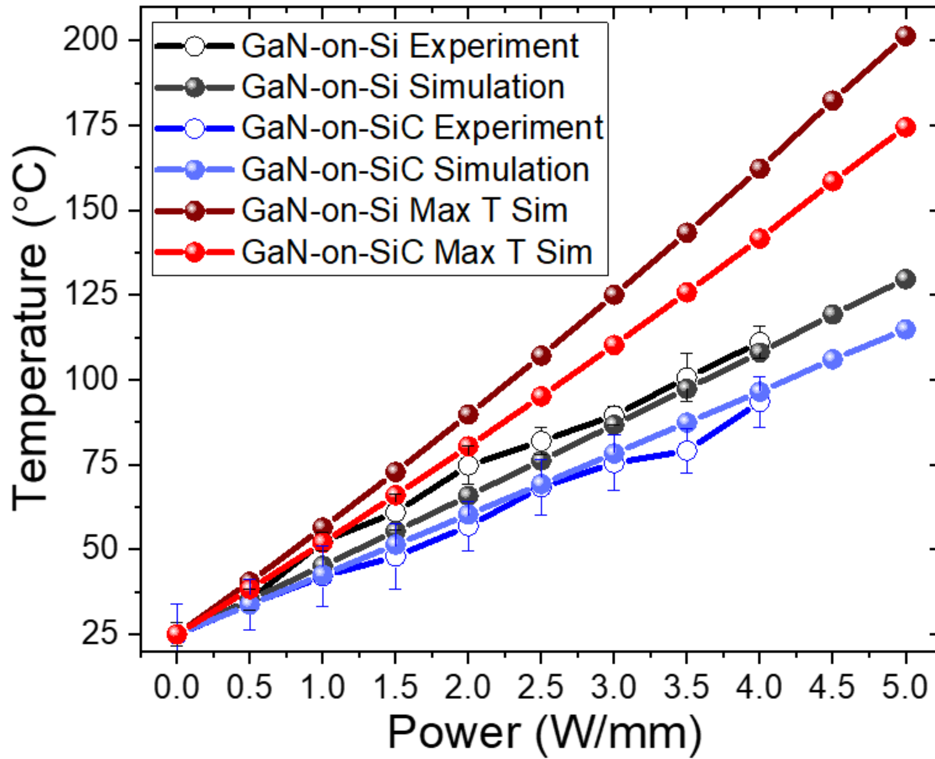

Figure 7.15: Average GaN temperature measurements measured experimentally and simulated in Ansys FEA software. Simulated peak device temperatures (Max T) before and after bonding onto 4H-SiC substrate shown for comparison.

Figure 7.15 shows a comparison between average GaN temperatures simulated in Ansys and the experimental results obtain from micro-Raman thermography, indicating good agreement between simulations and the experiment. The average thermal conductivity of strain relief layers has been extracted as 4.2 W/m·K by combining the experimental data from GaN-on-Si HEMTs with the simulations based on fixed thermal conductivities of other epitaxial layers. The results indicate GaN-on-Si HEMTs can reach maximum temperatures of 201.3°C at power dissipation of 5 W/mm. Removal of Si substrate and subsequent transfer of the heterostructure film onto 4H-SiC substrate results in temperature reduction of over 25°C, down to peak channel temperature of 174.4°C.

The bonding technique described in this chapter can further improve the thermal performance of GaN HEMTs if removal of Si substrate is followed by etching of the strain relief layers grown directly on top of it. By removing the thick section of the material with low thermal conductivity, the proximity of a substrate with high thermal conductivity can further reduce peak channel temperature resulting in prolonged device lifetime. So far, this technique has only been performed on samples with the diameter < 10 mm. For successful transfer of whole wafers, a number of processing steps would require further investigation and optimisation. Most notably, the etching rates of the substrate in radial direction require optimizations, as some non-uniformity has

been observed in the preparation of samples described in this chapter. Similarly, for successful removal of strain-relief layer the etching process requires a high level of control and uniformity in order to avoid local under-etching or accidental damage or complete removal of AlN nucleation layer. Finally, various aspects relating to structural integrity of transferred thin films need to be considered, as larger films are more susceptible to suffer mechanical damage throughout the bonding process.

7.5 Conclusions

This chapter describes a novel proof-of-concept low-temperature bonding technique of GaN-based power devices onto SiC substrate, with the main focus on electrical and thermal characterisation of the bonded devices in comparison with the original GaN-on-Si HEMTs. The process of device transfer onto the new bond substrate involves chemical etching of the original Si substrate, followed by bonding based on extremely thin water interlayer forming at the interface between the bottom of the AlGaN/GaN heterostructure thin film and the bond substrate. At elevated temperatures, the water reacts with AlN at the bottom of the heterostructure to form a thin (~ 30 nm) layer of solid aluminium hydroxide that provides a covanlent bond to the new substrate.

DC IV characterisation reveals drain current increase in bonded devices up to 20% resulting from reduction in self-heating as compared to the original GaN-on-Si HEMTs. The pulsed IV characterisation shows mild current collapse resulting from buffer trapping in the gate-drain access region, however the results also suggest that bonding does not introduce more trapping into the buffer. Similar conclusions can be drawn from dynamic R_{ON} measurements, as the dependence of On-resistance on applied off-state drain stress remains relatively unchanged after the bonding process. In addition, bidirectional substrate ramp sweeps indicate higher positive charge storage in the buffer after bonding, without indication of any adverse effects of the bonding process on the electrical characteristics of the buffer. The vertical leakage currents in bonded devices do not exceed that of the original transistors, suggesting breakdown voltage should not be compromised by device transfer onto SiC substrate.

Thermal analysis of GaN HEMTs was performed using a combination of micro-Raman thermography measurements of device surface and GaN layers, and thermal simulations performed in Ansys FEA software. The results suggest bonded devices show decrease in peak channel temperatures from 201.3°C to 174.4°C at power dissipation of 5 W/mm as compared to original GaN-on-Si HEMTs. Further significant improvement in thermal performance of the devices could be achieved by removal of strain relief layers prior to bonding.

The results show a variety of advantages that can be achieved using the bonding technique described in this chapter. However, there are many unanswered questions and thus possible avenues for future work. The main issues that would require further attention relate to removal of strain relief layer, scaling of the bonding process and heterointegration of different device

technologies on the same bond substrate.

Chapter 8

Summary and Conclusions

With the global energy demand growing rapidly and climate change becoming an increasingly important issue, the need for more efficient semiconductors is greater than ever. The push for materials capable of higher switching frequencies and greater power densities requires us to look beyond conventional Si electronics and towards wide bandgap semiconductors. GaN is a versatile material capable of achieving large breakdown voltages, while offering high electron mobilities in the form of 2DEG. Thus, GaN is an outstanding candidate to replace Si in many areas of RF and power electronics, enabling dramatic improvement in efficiency and significant reduction in module volume due to higher achievable power densities.

The main focus of this thesis is on electrical and thermal characterisation of GaN-based power and RF micro-devices. This was achieved by combination of electrical characterisation techniques (such as DC, pulsed IV and transient measurements), temperature measurements based on micro-Raman thermography and computational tools including TCAD and FEA simulators. This chapter summarises the key findings and outlines their implications for future work.

GaN buffers are doped with C to ensure adequate insulation for high power applications, however despite displaying outstanding blocking properties these buffers are also more susceptible to dynamic On-resistance and current collapse phenomena. The relation between C doping and current dispersion is still not well understood, limiting more widespread commercial application of GaN power HEMTs and diodes. Over the past years the impact of C compensation ratio and vertical leakage paths on the electrical characteristics of GaN buffers have been explored, but no direct link to dynamic R_{ON} has been established.

In this thesis, the role of carbon doping and dislocations in facilitating vertical charge transport processes in GaN buffer and channel layers is explored in the low-field regime (in devices rated up to 200 V). Bidirectional substrate ramp sweep measurements were performed on

a state-of-the-art GaN-on-Si expitaxy to identify voltage regions dominated by different vertical charge transport processes. The key vertical charge transport processes have been separated by performing substrate stress current transient measurements. The examination of temperature and fields dependence of these processes reveals the process responsible for charge redistribution across C - doped GaN buffer can be identified as variable range hopping in the bulk most likely via the defect band in the buffer. This process takes place at relatively low voltages and results in a formation of dipole, with negative charge accumulating at the UID GaN channel / C - doped buffer interface, while the positive charge is located towards the bottom of the GaN:C buffer. The negative charge at the top of the layer exerts back-gataing effect of the 2DEG, leading to reduction in the measured 2DEG current. This process is followed by band-to-band leakage across UID GaN channel, which can be attributed to 1D hopping along the dislocation cores. The dislocations provide an electrical connection between the 2DEG and otherwise floating C - doped buffer, mitigating the effects of stress potential on the 2DEG current. We also demonstrate the presence of a previously unobserved junction barrier between the dislocation cores and the 2DEG, resulting in a strong non-Ohmic behaviour of the band-to-band leakage process across the UID GaN channel. The model for 1D hopping conduction across the dislocations is demonstrated to be successfully implemented into a full transistor structure in a commercially available TCAD simulator. In spite of Ohmic nature of the simulated hopping, the results show good qualitative agreement with the measurements.

In the subsequent part of this work, the understanding of charge transport processes taking place in the GaN C - doped buffer and UID channel layers is applied to explore the temperature and field dependence of dynamic R_{ON} in a GaN-on-Si epitaxy. Recovery current transient and dynamic On-resistance measurements performed on the TLM structures over a wide temperature range demonstrate a direct link between the vertical charge transport processes and dynamic R_{ON} in the investigated structures. These results are compared and contrasted with the current recover transients and dynamic On-resistance measurements performed on lateral Schottky barrier diodes grown on the same wafer. Despite identical equivalent stress applied to these structures, the SBDs show more significant increase in R_{ON}, with more complex two-step recover transients. The experimental measurements are combined with the TCAD simulations to perform a comprehensive analysis of charge distribution in the buffer. The difference in temperature and field dependence of dynamic On-resistance between TLM structures and the Schottky barrier diodes can be explained in terms of different electric field distributions during stress: in case of TLMs the field is uniform across the entire device length and therefore dynamic R_{ON} will depend purely on vertical charge transport processes; in case of Schottky diodes, the field distribution is more complex resulting in uneven charge distribution at the interfaces across the device length. The two-step recovery current transients observed in diodes can therefore be explained by lateral and vertical charge redistribution occurring one after another during during the recovery phase. The results suggest it is not charge trapping, but predominately lateral and vertical charge

transport processes that affect the dynamic On-resistance in GaN buffers.

In the following part of the thesis, we demonstrate electrical and thermal analysis of early generation "buffer-free" GaN-on-SiC HEMTs (QuanFINE technology) developed by SweGaN AB, where the thick doped GaN buffer is absent and 250 nm UID GaN channel is grown directly on the AlN nucleation layer. This design is only possible due to application of a novel hot-wall MOCVD growth for the AlN nucleation layer deposition, resulting in excellent crystalline quality of this interlayer with defects and dislocation at the GaN/AlN interface significantly reduced and confined to a narrow region only ~10 nm wide. This unique transistor design enables reduction in raw materials required for growth by 90%, while shortening the growth time (and thus costs associated with running the reactor). In addition, omission of the thick buffer brings the high thermal conductivity SiC substrate closer to the main location of Joule heating during device operation and completely nullifies the issue of buffer trapping. The electrical and thermal performance of "buffer-free" devices are compared to conventional GaN-on-SiC HEMTs containing thick 2 μm Fe-doped buffer.

The electrical characterisation relies mostly on DC and pulsed IV measurements and involves comparison between the "buffer-free" and conventional GaN-on-SiC HEMTs with thick buffer. In contrast to conventional devices, the QuanFINE HEMTs show very little trapping present in the epitaxy, however the device exhibits carrier confinement issues resulting in observable punch-through and significant drain-induced barrier lowering manifested by significant stretch-out in the IdVg characteristics especially in the devices with short gate lengths (L_G = 150 nm). The experimental measurements are combined with computational simulations, indicating a reduction in the polarization charge across the AlN nucleation with the Fermi level pinned in the upper half of the band gap. This allows for electron flow around the depletion region in the off-state resulting in the stretch-out observed in the IdVg characteristics. The suppression of this effect can be achieved by increasing the gate lengths, with the longer gate lengths required for thicker GaN layer. Alternatively, to allow for high frequency operation of the device, the electron confinement issues in short gate length devices could be rectified by process optimisation aimed at increasing the polarization charge across the AlN nucleation layer or pinning of the Fermi level in the lower half of the bandgap.

Thermal analysis was based on micro-Raman thermography, suggesting very competitive thermal performance of "buffer-free" devices in comparison to conventional GaN-on-SiC HEMTs with thick buffer. The results indicate excellent quality thermal interface between the GaN channel and SiC substrate, however due to significant reduction in transverse thermal conductivity of GaN, most of the temperature is still dropped across the AlN nucleation layer. The experimental measurements are combined with Ansys FEA simulator to investigate the effects of GaN thickness and effective thermal boundary resistance between GaN and SiC on thermal performance of the devices. The analysis indicates the TBR_{eff} has a much more significant impact on devices with thin GaN layers than on conventional devices with thick GaN buffers.

Despite the proximity of the high thermal conductivity substrate, the thinner the device, the better thermal interface between GaN and the substrate required for effective heat diffusion. From the thermal perspective a very significant improvement in thermal performance of the "buffer-free" device can be achieved by increasing the GaN thickness from 250 nm to 350 nm. The combined thermal and electrical analysis of the "buffer-free" GaN HEMTs suggests ideal device design strongly depended on the intended device application.

In the final part of this thesis, the focus is shifted from novel devices to novel techniques for device transfer and bonding. This work contains a proof of concept, where power GaN-on-Si HEMTs are bonded onto a conductive SiC substrate after the original substrate is removed chemically. The bonding is achieved using a novel low-temperature adaptive technique that utilises extremely thin water layer between the AlN nucleation layer and target substrate to form a covalently bonded solid aluminium hydroxide layer between the transferred heterostructure thin film and the bond substrate. This technique can be applied to a wide range of III-nitride material systems and can reliably facilitate transfer and integration of different technologies on a single high performance substrate such as diamond. The motivation behind this work is to examine the effects of the bonding technique on electrical and thermal performance of the transferred devices.

The electrical characterisation involved comparison in IV characteristics, buffer trapping, vertical leakage and charge storage in the buffer between the original GaN-on-Si devices to their performance after bonding onto the SiC substrate. The DC IV characteristics show reduction in device self-heating after bonding, resulting from the presence of higher thermal conductivity substrate, while pulsed characterisation indicates no additional trapping induced during the bonding process. Likewise, the comparison of device On-resistance before and after bonding across a wide range of stress voltages shows very comparable device performance before and after bonding. Bidirectional substrate ramp sweeps reveal a consistent increase in positive charge storage in the buffer after bonding onto SiC substrate suggesting the bonding technique can affect charge transport via the dislocations, however the vertical leakage current remains unchanged before and after bonding. Thermal analysis involves micro-Raman thermography and the results are combined with Ansys 3D FEA simulations to assess temperature distribution of the investigated devices. The results indicate significant reduction in peak channel temperatures for bonded devices, while suggesting absence of any significant thermal boundary resulting from the bonding process. Overall, the electrical and thermal characteristics analysis of the bonded devices indicates no adverse effects of the bonding on the performance of the GaN transistors.

Based on the results presented in this thesis there are a few different avenues for the direction of future work. Firstly, Chapters 4 and 5 focus on analysing the impact of charge transport processes in GaN layers on dynamic R_{ON} and electrical performance of the GaN-on-Si power HEMTs rated up to 200 V. In case of power devices rated for 650 V, charge transport mechanisms in the strain relief layer start playing an important role. Understanding of the

effects of SRL on electrical performance of power device at could offer invaluable insight into dynamic R_{ON} phenomena at high voltages. In addition, the study of electrical performance of SRL could contribute the final missing element in creating an accurate lumped element model of the epitaxy to be implemented for device simulation in Spice and ADS simulation environments, which could greatly aid the process of GaN power device design.

An obvious continuation to the work presented in Chapter 6 on "buffer-free" GaN-on-SiC HEMTs could involve further exploration of electrical properties of the AlN nucleation layer, with the aim of improving carrier confinement in the channel. This could involve exploration of methods for pinning the Fermi level of the AlN nucleation layer in the bottom half of the bandgap and their impact on electrical characteristics of the device as well as on thermal properties of the interface between GaN channel and the SiC substrate. The QuanFINE technology presents a wide range of advantages over conventional devices, with the greatest incentive being expressed by the savings in raw materials and time required for device growth. For this reason, it is not surprising this technology is becoming increasingly popular among research groups worldwide.

Finally, in Chapter 7 a proof of concept for novel low-temperature bonding technique has been demonstrated. The results of this work indicate the substrate removal and subsequent bonding process have present no adverse effects to electrical or thermal performance of the transferred heteroepitaxial films. The outstanding questions regarding the bonding technique revolve around scaling and hetero-integration. The strength of the bonding technique presented in Chapter 7 lies in its simplicity and versatility. The ability to grow wafers on cheap substrates followed by reliable transfer and bonding onto of the III-nitride films onto final high performance substrates would allow to overcome current challenges relating to introduction of foreign materials between intended substrate and heteroepitaxial film during growth.

Appendix A

A.1 Publications

- F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball; *The Effects of Charge Transport Processes on Dynamic On- Resistance in GaN-on-Si Schottky Barrier Diodes*, IEEE Transactions on Electron Devices, Dec 2021, Under Review.
- F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball; *Low Field Vertical Charge Transport in the Channel and Buffer Layers of GaN-on-Si High Electron Mobility Transistors*, IEEE Electron Device Letters, Oct 2020, 12;41(12):1754-7.
- D. E. Field, F. Wach, J. W. Pomeroy, and M. Kuball; *Differences in SiC Wafer Thermal Conductivity from Face-to-Face Dependent on Polishing*, Proceedings of the International Conference on Compound Semiconductor Manufacturing Technology, 2022.

A.2 Presentations

- F. Wach, M. J. Uren, B. Bakeroot, M. Zhao, S. Decoutere and M. Kuball; *Low Field Vertical Charge Transport in AlGaN/GaN–on–Si High Electron Mobility Transistors*, UK Nitride Consortium, Jan. 2020.
- F. Wach, J. Zhu, M. J. Uren, S. Alam, D. J. Wallis, K-B. Lee, M. Kuball; *The Effects of Channel Donors on the Electrical Performance of GaN-on-Si High Electron Mobility Transistors* 44th Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe, May 2021.

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