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SPICE model for complementary resistive switching devices based on anti-serially connected quasi-static memdiodes

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ABSTRACT

This paper reports the use of the Quasi-static Memdiode Model (QMM) for simulating Complementary Resistive Switching (CRS) devices. CRS arises from the anti-serial connection of two memristors and it is used for generating low and high-resistance regions in the *I-V* characteristic with the aim of mitigating the sneak-path conduction problem in crossbar arrays. Here, the use of the QMM for CRS in the form of a six terminal subcircuit is explored. While two terminals of the subcircuit correspond to the conventional input and output pins of the CRS structure, the rest provide information about the voltage at the central node, the low-voltage conductance of each device, and the low-voltage conductance of the whole structure. Special attention is paid to the simulation of the so-called *table with legs* hysteresis loop (resistance at fixed bias vs. write voltage), which is often invoked in connection with devices that exhibit switching activity at the two interfaces of a single dielectric layer. Because of the internal potential drop distribution, the switching process takes place alternately at one side of the structure or the other giving rise to a *pseudo*-CRS behavior. The flexibility of the proposed approach is demonstrated through a series of fitting exercises that involve experimental data reported in the literature. The model script for the SPICE simulator is also provided.

1. Introduction

The anti-serial connection of two Resistive Switching (RS) devices or memristors leads to the so-called Complementary Resistive Switching (CRS) behavior. Such a functional structure has been proposed as a way of mitigating the sneak-path conduction problem in crossbar arrays used for information storage and neuromorphic computing [1–3]. Since the SET and RESET transitions of each device occur at opposite voltages (bipolar switching), the combined structure typically exhibits ON and OFF conducting windows in the *I-V* characteristic such as those illustrated in Fig. 1. This is the result of the alternate combination of the low (LRS) and high (HRS) resistive states of the individual devices induced by the application of a voltage sweep. Interestingly, the transmission windows (ON regions) can exhibit a wide variety of shapes (abrupt/progressive) and amplitudes (small/large) that not only are a consequence of the material used as the switching layer and the metal electrodes but also of the particular features of the generated filaments (oxygen vacancy- or metal ion-based pathways, electroforming voltage, lateral size, internal series resistance, etc.). Several CRS models can be found in the literature [4–9], and, basically, all of them rely on the anti-serial connection of two identical devices. The connection of dissimilar structures is rarely explored in the context of CRS. The most well-known CRS models together with the application of our Dynamic Memdiode Model (DMM) were benchmarked in [10]. In this work, instead of the DMM, we use the QMM, which is simpler and more robust but with reduced programming capability (this is not a limitation when sub-threshold dynamic programming is not an issue). Because of this lower complexity, the QMM is more tractable for representing CRS experimental curves in cases in which no information about the individual *I-V* curves or the system dynamics (time-dependence) is available. Again, following previous approaches [11–13], we model CRS using two anti-serially connected devices. The memdiode-based model considered for the simulations consists of a single subcircuit with 6 terminals or pins, which, in addition to the simulated *I-V* curves, provides the device low-voltage conductance curves (conductance loop measured at a very low fixed voltage). It is worth mentioning that a key issue for the accurate modeling of the CRS *I-V* characteristic is the realistic modeling of the devices that constitute the structure. For that reason, the memristor model considered needs to include all the crucial features required for the simulation of the individual curves such as the snapback (SB) and

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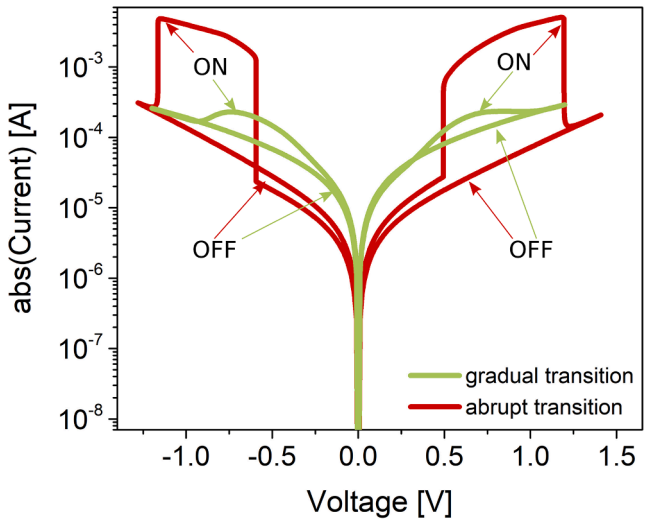

Fig. 1. Simulated I-V characteristics with gradual (green line) and abrupt (red line) ON-OFF transmission windows. The curves were simulated with the model script reported in this work.

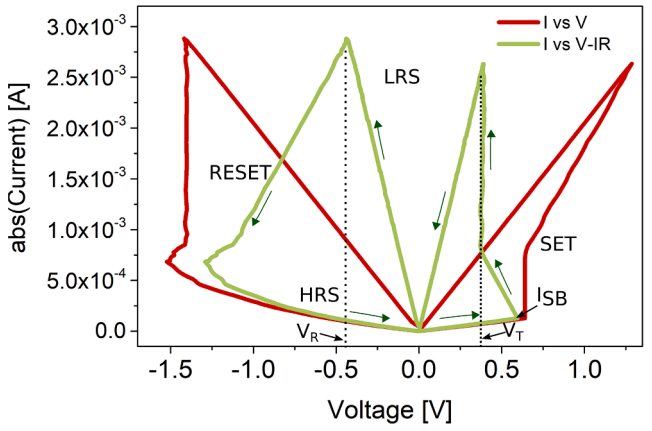

Fig. 2. Simulated I-V characteristics for a single memristor with (green line) and without (red line) SB and SF corrections (V-IR_i). The green arrows show the voltage sweep direction for the RS phenomenon. Notice that $V_R = -V_T$ for the corrected curve. I_{SB} denotes the triggering current for the SET process.

snapforward (SF) effects [14]. These effects correspond to the vanishing and formation of a gap or barrier along the filamentary pathway, respectively, and are essential ingredients for a correct representation of the device behavior as explained in Section 2. To illustrate how our model is able to cope with extreme situations such as those depicted in Fig. 1 as well as with intermediate cases, a number of experimental curves found in the literature were analyzed and simulated. One remarkable feature of our approach is that the proposed model can also be used to deconstruct the CRS experimental curve into its separate characteristics when, as already mentioned, the corresponding information is not available (not measured) and even when they cannot be measured (single dielectric structure). Although this issue is out of the scope of this paper, as reported in [10], the use of the central terminal or node in the CRS subcircuit provides a solution to this problem. It is also worth mentioning that simulations were carried out using the *LTSpice XVII* circuit simulator which can be downloaded for free from the webpage of Analog Devices [15].

2. Phenomenology of the hysteretic *I-V* characteristic

Fig. 2 illustrates a typical *I-V* characteristic for a RS device with SB and SF effects. The electroforming step is not shown here. The SB and SF effects can be understood as follows: after the completion of the filament formation process (SET) in a memristive structure, the voltage at the constriction suddenly drops (SB effect) and the current increases following the circuit load line dictated by the series resistance R_i (green solid line in Fig. 2). This resistance can be internal, external to the device, or both. Beyond this point, the filament laterally expands or accumulates defects at a constant voltage called the transition voltage V_T (vertical line in Fig. 2), which is a characteristic parameter of the insulating material and voltage ramp rate [14,16–19]. Once in LRS, the curve reaches the RESET point at negative bias and drops (SF effect) because of the filament dissolution. Again, the *I-V* curve follows the load line of the circuit. The red solid line in Fig. 2 corresponds to the same *I-V* characteristic but takes into account the additional potential drop occurring across the series resistance R_i. Notice that the SB effect is detected in this later representation as an abrupt current increase after the SET event. Depending on the magnitude of the SB and SF effects occurring in each memristive device, the SET and RESET voltages, the threshold voltage, and other factors, the CRS *I-V* curve that results from the combination of the two devices exhibits abrupt/digital (red line) or gradual/analog (green line) transitions as those illustrated in Fig. 1. Additionally, since we are referring to RS, the resistance or conductance of the devices depends on their previous history. Very often we are interested in the resistance or conductance of the devices measured at a particular bias, in general, a low bias, because this reflects the hysteretic nature of the devices in the linear regime and under a fixed voltage condition [20]. Subsequently, if needed, this value can be used to compute the read current of the device. However, in order to capture the whole SET-RESET transition, a bipolar voltage sweep is still required. To clarify this issue, let's consider some simulated results: Fig. 3 illustrates resistance–voltage (*R-V*) curves corresponding to the individual devices of a CRS structure (Fig. 3(a) and 3(b)) as well as to the *R-V* curve corresponding to the whole CRS structure (Fig. 3(c)). Since these curves are measured at a very low bias, they are independent of that precise bias because the device is in the linear regime. Notice that the series combination of the individual curves leads to the so-called *table with legs* hysteresis loop, which is a central topic of our paper. These kinds of curves are often observed in perovskite-based devices [21] but have also been observed in TaO_x- and HfO_x-based structures [20,22]. Importantly, in the case of a single dielectric layer, the *table with legs* is ascribed to the switching activity of both interfaces and not to the conventional connection of two independent devices. Physically, the conductance modulation has been attributed to different mechanisms such as tunneling or to modifications of the Schottky contacts with the electrodes [20,23], but this is out of the scope of this paper. Here, we focus the attention on the representation of the phenomenon for circuit simulation environments.

3. Brief description of the memdiode model

The Quasi-static Memdiode Model (QMM) is considered here for simulating two RS devices anti-serially connected forming a single CRS structure. The concept is illustrated in Fig. 4(a). The LTSpice CRS script consists of a subcircuit with six terminals: two terminals for the conventional *I-V* curve, one terminal for the central node of the structure, and the rest for the low-voltage conductances (individual and combined devices). The theoretical framework followed for modeling the structure is that proposed by Prof. Chua for memristive devices, namely two coupled equations for each device in the CRS structure: one for the electron flow through a filamentary-type conducting channel and a second equation representing the reversible movement of vacancies/ions within the dielectric layer caused by the application of the external electrical stimulus [11–13]. The *I-V* characteristic for each memdiode reads:

$$I(V) = I_0(\lambda)\sinh\{\alpha(\lambda)[V - (R_S(\lambda) + R_i)I]\} \quad (1)$$

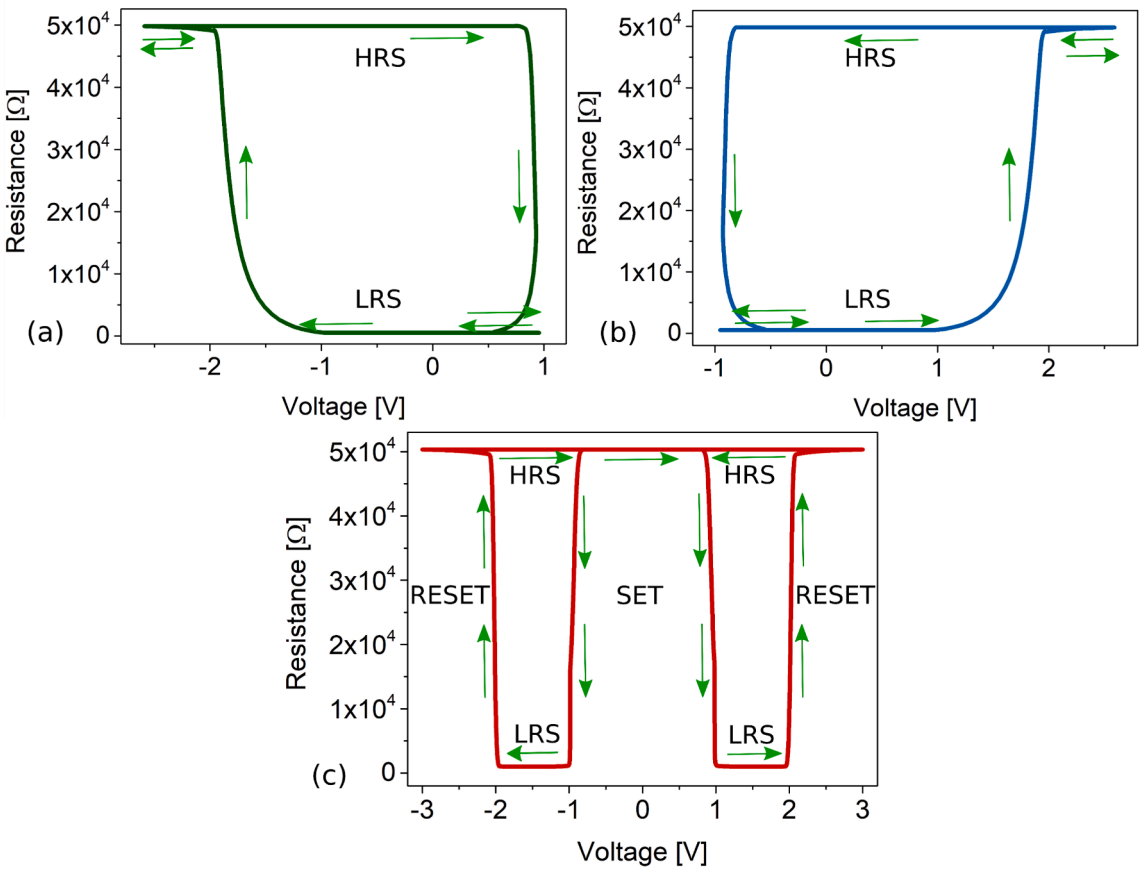

Fig. 3. Simulated R-V curves for each memristor in the CRS structure (a) and (b), and the curve for the corresponding CRS structure (c). The curves were simulated with the model script reported in this work (see APPENDIX, Figs. 11 and 12). The green arrows indicate the voltage sweep direction.

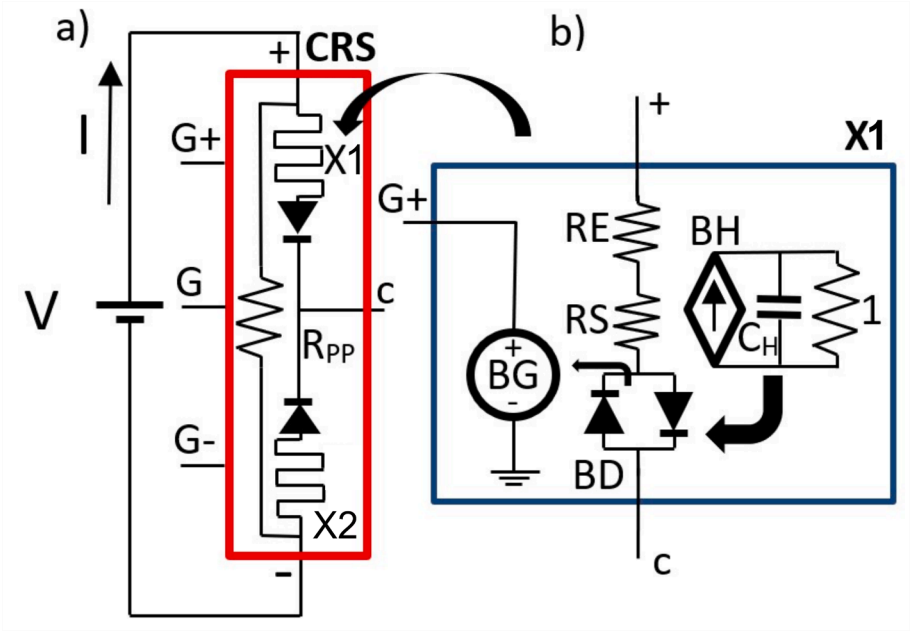

Fig. 4. Schematic circuit for (a) the CRS structure consisting of two memdiodes (X1 and X2) anti-serially connected. The CRS model consists of a six-port subcircuit: three for the I-V characteristics. Thanks to the accessible central terminal, the subcircuit allows representing the curves of the individual RS devices and the CRS device; three terminals are useful for obtaining the conductance of each device in the CRS structure, and the total conductance; (b) internal implementation of the QMM for the X1 memdiode. The memory circuit controls the conduction characteristics. The labels of the schematics (a) and (b), indicate the name of elements in the script shown in Fig. 11. RE and RS are the series resistances connected to the opposite-biased diodes that lead to the sinh dependence. BD corresponds to Eq.1 of the model. The current generator (BH) is driven by the voltage V_c (Eq. (2)) and it is used to store the memory state in the capacitor C_H. RPP is a parallel resistance required by the current generators.

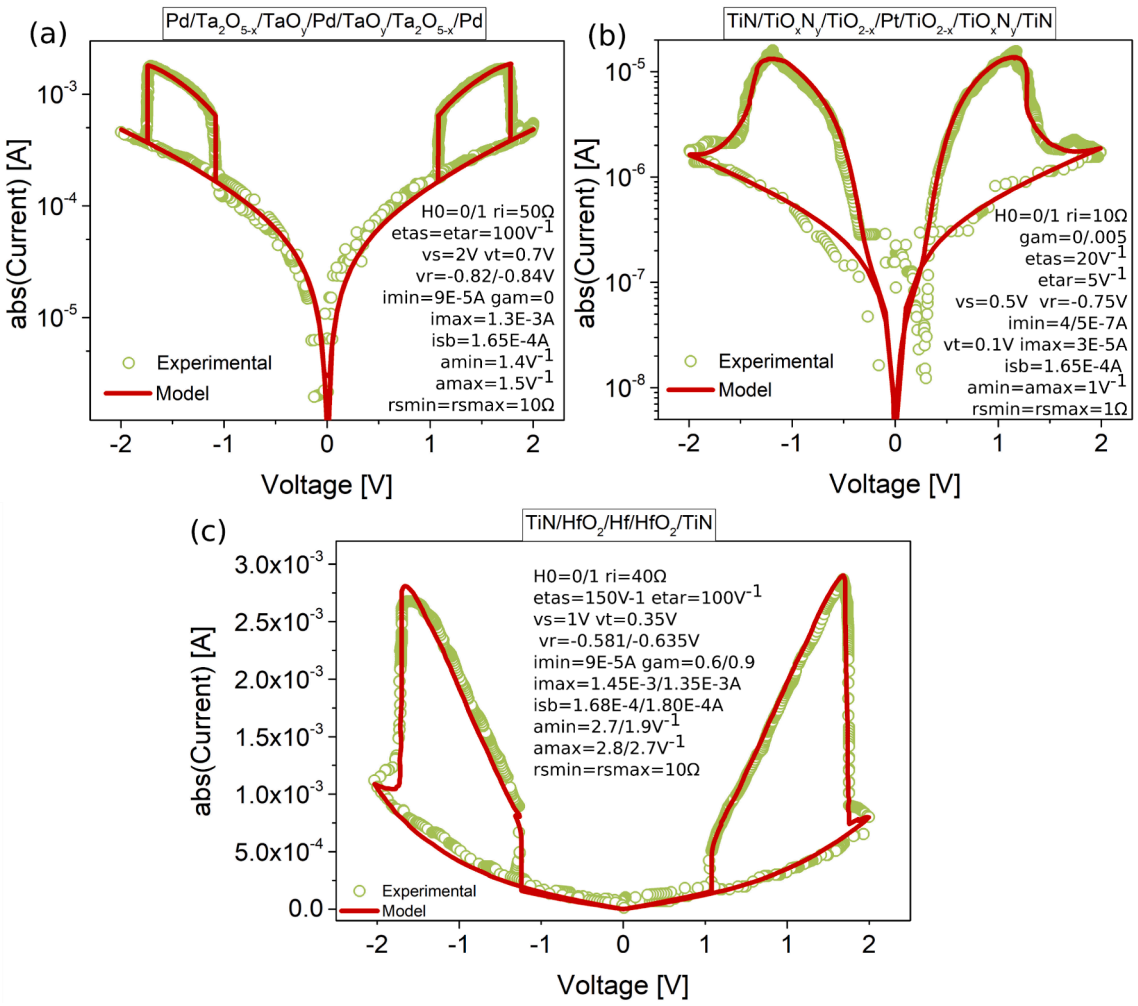

Fig. 5. Experimental and model results for different transition metal oxides as switching layers: (a) for a symmetric Tantalum oxide-based CRS structure [24]; (b) $TiN/TiO_xN_y/TiO_{2-x}/Pt$ memristors forming a CRS structure [25] and (c) two $Ti/HfO_2/Hf$-based structures anti-serially connected [14]. The insets show the parameter values considered for the simulations.

where $I_0(\lambda) = I_{min} + (I_{max} - I_{min})\lambda$ is the current amplitude factor. I_{min} (imin in the script) and I_{max} (imax in the script) are calibration parameters for the minimum and maximum currents, respectively. V is the voltage across the device terminals, $R_S(\lambda)$ (rs) a variable series resistance, R_i (ri) a fixed series resistance, and $\alpha(\lambda)$ a fitting parameter. For the sake of completeness, α (amin and amax) and R_S (rsmax and rsmin) can be described by relationships similar to that used for I_0. (1) resembles the *I-V* relationship for two opposite-biased diodes with shared series resistance (see Fig. 4(b)). Eq.(1) replaces the Lambert function and the Hermite-Padé approximation considered in [12]. The second equation relates the memory state $0 \leq \lambda \leq 1$ (H0 in the script) to the voltage drop across the constriction $V_C = V - R_i I$ through the recursive hysteresis operator [11]:

$$\lambda(V_C) = min\left\{R(V_C), max\left[\lambda(\overleftarrow{V_C}), S(V_C)\right]\right\} \quad (2)$$

where S and R are the so-called SET and RESET ridge functions (sigmoidal curves in this case), respectively, which physically represent the ion/vacancy movement (see the model script in the APPENDIX). Their behavioral expressions are $S(V_C) = \{1 + \exp[-\eta_S (V_C - \text{if}(I > I_{SB}, V_T, V_S))]\}^{-1}$ and $R(V_C) = \{1 + \exp[-\eta_R \lambda^{\gamma} (V_C - V_R)]\}^{-1}$, where η_S (etas) and η_R (etar) are transition rates and V_S (vs) and V_R (vr), the SET and RESET voltages, respectively. $\lambda\left(\overleftarrow{V_C}\right)$ is the memory state value a timestep before (hysteretic behavior). Equations (1) and (2) are implemented in *LTSpice* using an equivalent circuital approach with behavioral components and sources (see Fig. 4). A remarkable feature of the proposed model is that the SET event not only can be triggered by a SET voltage V_S but alternatively by a threshold current I_{SB} (isb) (see Fig. 2). This gives rise to the SB effect because of the completion of the filament. The model contains other parameters for the fine-tuning of the simulated curves. In particular, the γ (*gam*) parameter in the RESET ridge function (not considered before [12]) is used for modeling the low-current SF effect detected in many devices. These little but crucial details lead to the variety of behaviors observed in the experimental curves. In this regard, it is worth mentioning the connection of these parameters (I_{SB} and γ) with the possibility of generating digital or analog ON and OFF transitions in the CRS curves. The key issue behind the observation of abrupt ON transitions is a noticeable SB effect in the individual devices (triggered by I_{SB}). Similarly, abrupt OFF transitions are obtained by generating abrupt RESET transitions in the individual devices ($\gamma = 0$). The same considerations apply to the *table with legs R-V* curves as will be discussed in Section 5.

4. Experimental and simulated CRS *I-V* characteristics

In order to assess the versatility of the QMM for CRS devices, we first report some fitting results using experimental data found in the literature. A similar approach was followed in [10] but with a more complex

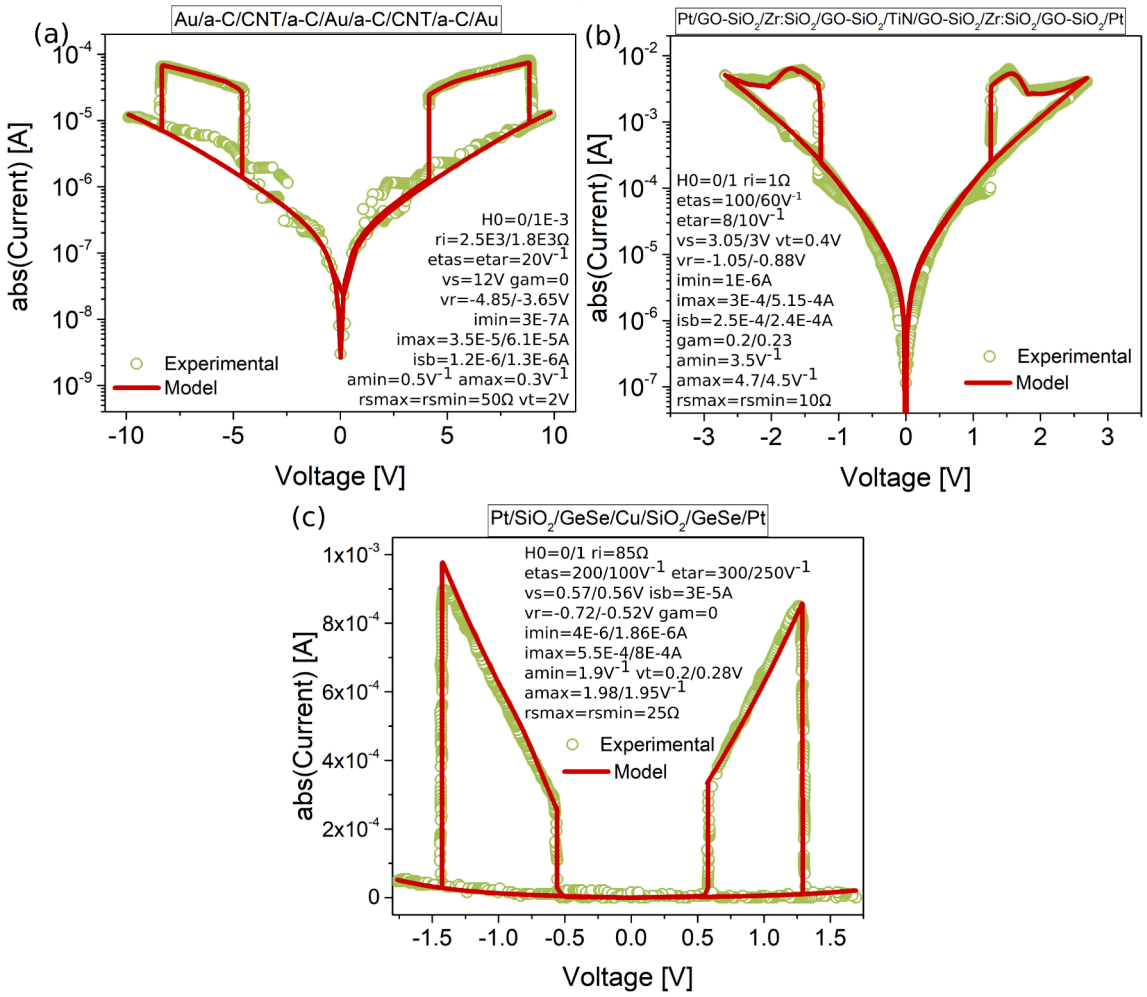

Fig. 6. Experimental and model results for different dielectric materials: (a) a-C(amorphous-Carbon)/ CNT-based memristors forming a CRS structure [26]; (b) for two-sided graphene oxide doped silicon oxide-based memristors forming a CRS structure [27] and (c) SiO_2/GeSe-based CRS structure [1]. Notice that the I-V characteristic is not symmetric. The insets show the parameter values considered for the simulations.

and less robust model, the DMM. For the sake of clarity, the model parameters are indicated in the inset of each figure. Fig. 5 illustrates experimental and simulation results for transition metal oxide-based structures: Fig. 5(a) shows the CRS behavior for two bilayer Pd/Ta_2O_{5-x}/TaO_y/Pd combined devices in log-linear axis [24]. The behavior is symmetric for both voltage polarities, the transitions HRS-LRS are abrupt (digital transmission windows) with good separation between the SET and RESET events; Fig. 5(b) corresponds to a combination of TiN/TiO_xN_y/TiO_{2-x}/Pt devices [25]. The structure exhibits analog transitions and a large transmission window; Fig. 5(c) illustrates the *I-V* curve for combined TiN/HfO_2/Hf devices [14]. In this plot, the SET and RESET transitions are abrupt and have associated SB and SF effects, respectively. Notice the small departures of the experimental curve at the end of the RESET transitions and how the model is able to capture the detail. Next, Fig. 6 illustrates *I-V* curves for CRS structures that do not contain a transition metal oxide as the switching layer: Fig. 6(a) shows results for the *I-V* curve of carbon nanotubes (CNT)-based devices [26]. The parameter values used in this simulation are very different from those considered in previous cases because the switching voltages are notably higher and the currents lower; Fig. 6(b) shows experimental and simulation results for graphene/Zr-based structures [27]. As reported by these authors, the two-sided graphene oxide (GO) structures exhibit an intrinsic current restriction ability and uniform switching (the model can also be applied in this case because of its behavioral nature). Notice the progressive RESET transitions achieved through the effective voltage reduction parameter *gam* in the RESET process; Fig. 6(c) illustrates fully digital CRS transitions for two Pt/SiO_2/GeSe/Cu devices [1]. Again, the general behavior is well captured by our model. It is worth mentioning that, though in all the cases we attempted to use model parameter values as close as possible to their corresponding observables, it was sometimes difficult to identify the optimum values. The reason is that the current behavior is affected by a combination of parameters and the only information available is the final CRS curve. For the sake of simplicity, we assumed initial states $\lambda(0) = 0$ and $\lambda(0) = 1$ for each memdiode. This is only important for the first *I-V* curve since, after this, the hysteretic loop enters into the stationary cycle.

5. Experimental and simulated *R-V* characteristics

Instead of the *I-V* characteristic, many papers on RS report the conductance or resistance of the device at a fixed bias as a function of the programming voltage (*G-V* or *R-V*). This is often referred to as the remnant conductance or resistance and for a given voltage it provides direct information on the read current of the structure. This is basically the current evolution measured at a fixed bias, usually a low voltage within the linear operating regime of the device. The same concept applies to the CRS case. Experimentally, the *G-V* or *R-V* curves are obtained by applying pulses of increasing magnitude and measuring the

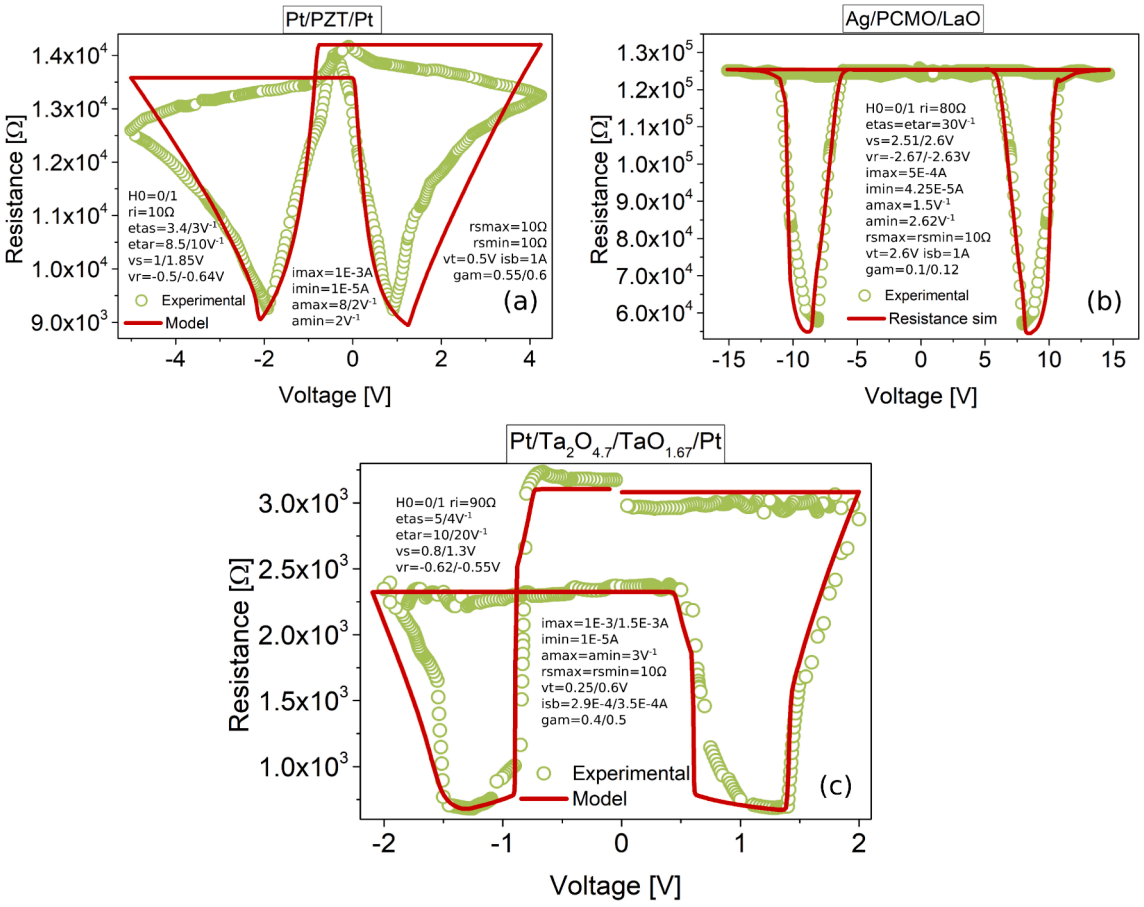

Fig. 7. Experimental and model results for different kinds of the table with legs experimental curves. (a) symmetrical triangular legs of hysteresis loop for Pt/PZT/Pt device [28], (b) symmetrical lengthened legs of hysteresis loop for Ag/PCMO/LaO device [29], and (c) asymmetrical hysteresis loop curve for $Pt/Ta_2O_{4.7}/TaO_{1.67}/Pt$ [23]. The insets show the parameter values considered for the simulations.

current at a low voltage in between the large pulses. This is not necessary in the case of simulations since the low voltage conductance of the device can be straightforwardly obtained from the model circuit (it is implicitly assumed that this operation does not affect the memory state of the device). Our model script provides this information through the terminals G^-, G^+, and G. While G^+ and G^- correspond to the conductances of each device in the CRS structure, G refers to its total conductance. In the proposed model, the conductances are calculated as follows: from (1), it is possible to obtain the low-voltage current flowing through each device (neglecting the series resistance effect) as:

$$I(V) \approx I_0(\lambda)\sinh[\alpha(\lambda)V] \tag{3}$$

so that the low-voltage conductance (*sinh(x)≈x*) reads:

$$G^{\pm} = I_0^{\pm}(\lambda)\alpha^{\pm}(\lambda) \tag{4}$$

Since the two memdiodes are series connected, we can calculate the total conductance as:

$$\frac{1}{G} = \frac{1}{G^+} + \frac{1}{G^-} \tag{5}$$

The *table with legs* (*R-V*) is then obtained from the *G-V* curve since $R = 1/G$. Fig. 7 exhibits a number of *R-V* curves for different RS devices reported in the literature. For instance, Fig. 7(a) shows the *R-V* curve for a Pt/PZT/Pt structure. The observed behavior is attributed to switching events in the Schottky-type interfaces which are assumed to be serially combined. Each interface is modulated by the ferroelectric polarization of the material [28]. The HRS regime is hard to fit because of the unavailable information on the individual *I-V* curves. Fig. 7(b) shows the *R-V* curve for a Ag/PCMO/LaO device [29]. Notice the good agreement between experiment and simulation. Even though the *legs* seem to be thin and sharp, the voltage span is from −15 V to 15 V. Finally, Fig. 7(c) shows the *R-V* characteristic for an asymmetric device ($Pt/Ta_2O_{4.7}/TaO_{1.67}/Pt$). The curve is obtained by applying after each write voltage pulse a low voltage reading pulse of 0.1 V. The obtained results indicate a high dependence on the maximum and minimum voltages applied to the device [23]. To simulate these curves, we have used the same methodology as in the case of the *I-V* characteristics. All the parameter values used to fit the curves are in the inset of each plot.

To conclude, simulation results corresponding to different values of the model parameters are illustrated. The attention is focused here on the *table with legs*. Figs. 8, 9, and 10 show the effects of modifying the model parameters around certain prescribed values. In all the cases, the curves correspond to the second hysteretic loop because the transient effects caused by the initial simulation conditions need to be eliminated. Fig. 8 shows the modification of the curves under small variations of the model parameters associated with the ON-OFF transitions for asymmetric CRS curves. Fig. 9 shows the effects of the same parameters for symmetric CRS devices. Finally, Fig. 10 shows the effects of some specific parameters on the *R-V* curves corresponding to symmetric CRS devices with narrow and long legs. These results are intended to be a guide for the potential user of our model.

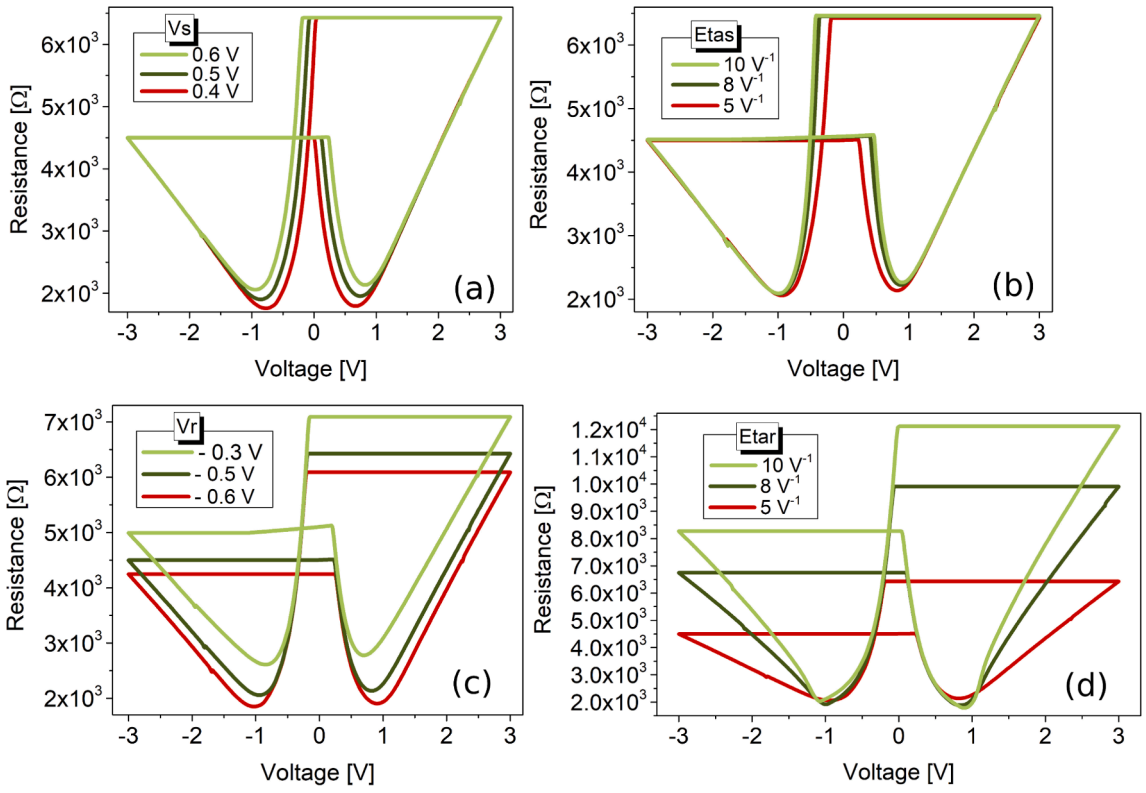

Fig. 8. Parameter values sweep for asymmetrical curves (kind (c) shown in Fig. 10): (a) and (b) show the SET process parameters, (c) and (d) show the RESET process parameter values.

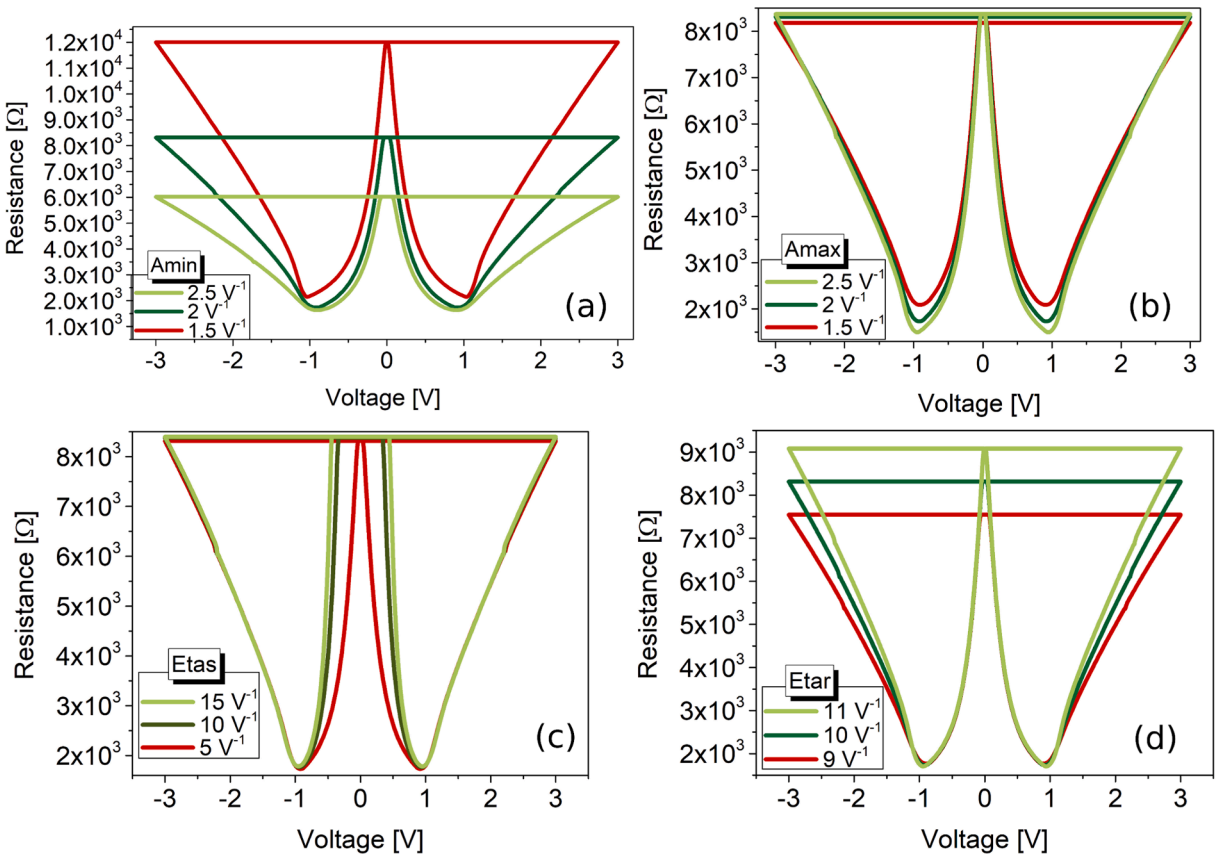

Fig. 9. Parameter values sweep for triangular legs (kind (a) shown in Fig. 10): (a) and (b) show the modification of the curve corresponding to changes in the slopes, (c) and (d) show changes corresponding to changes in the SET and RESET process parameter values, respectively.

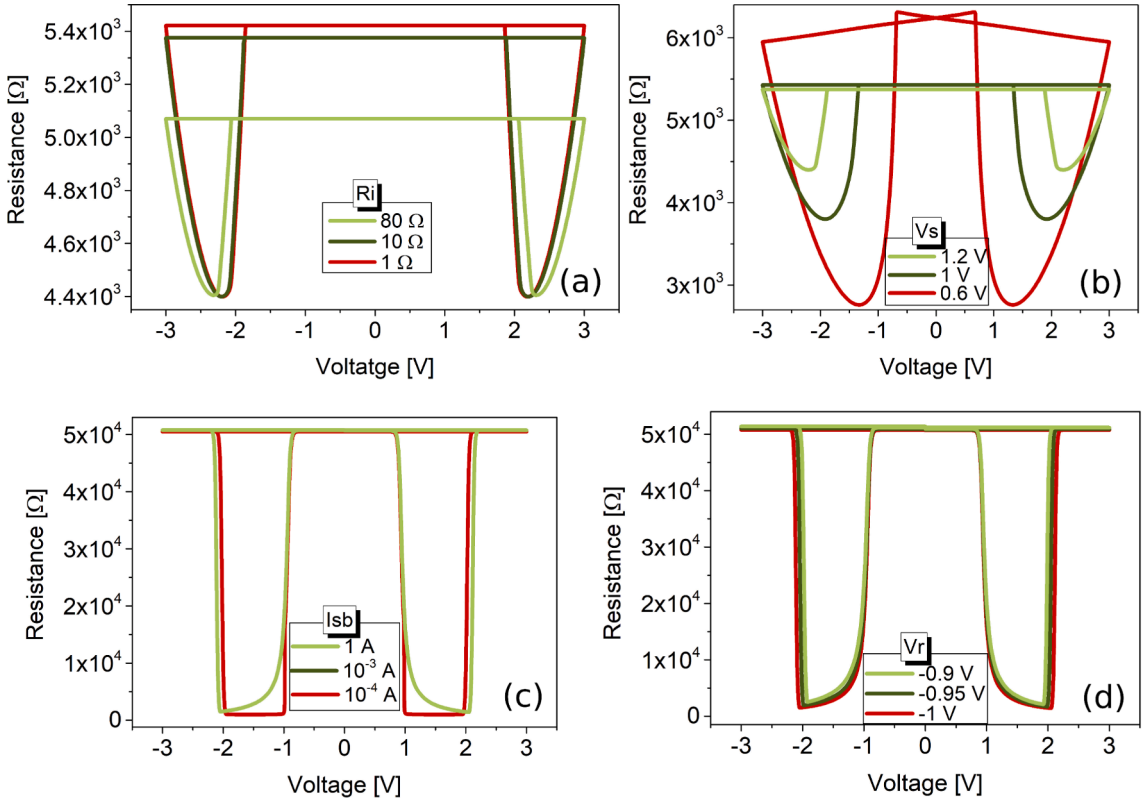

Fig. 10. Parameter values sweep of lengthened legs of the curve (kind (b) in Fig. 10): (a) shows the modification of the hysteresis loop varying the resistances, (b) and (c) show the modifications changing the SET process parameters, and (d) shows the modifications corresponding to changes in one of the RESET parameters.

6. Conclusions

Complementary resistive switching (CRS) has been proposed as a key element to control the crosstalk effects in memristor-based crossbar arrays. In this paper, we have reported and discussed a compact behavioral approach based on the quasi-static memdiode model (QMM). We showed that the proposed subcircuit is able to simulate a wide variety of experimental curves. The model for each individual device consists of two equations, one for the electron transport and a second equation for the memory state of the device. Crucial elements within this description are the snapback and snapforward effects. When both structures are combined, the CRS behavior emerges under the application of a voltage sweep. The concept can be extended to the case of the curve called *table with legs*, which is nothing but the resistance of the device measured at a fixed bias as a function of the writing signal. It was shown that the model is also able to represent these kinds of curves within the same framework and without the necessity of incorporating any other particular element.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix

The code shown in Fig. 11 for *LTSpice XVII* corresponds to two anti-serially connected memdiode structures. This results in the CRS behavior. The inset of Fig. 12 illustrates the circuit used to simulate all

```
.subckt CRS + c - G+ G G-
X1 + c G+ QMM H0=0 ri=10 etas=50 etar=50 vs=1 vr=-1 imax=1E-3
imin=1E-5
+ amax=2 amin=2 rsmax=10 rsmin=10 vt=0.5 isb=1e-4 gam=0.2
X2 - c G- QMM H0=1 ri=10 etas=50 etar=50 vs=1 vr=-1 imax=1E-3
imin=1E-5
+ amax=2 amin=2 rsmax=10 rsmin=10 vt=0.5 isb=1e-4 gam=0.2
RPP + - R=1E10
BG G 0 V=1/(1/V(G+)+1/V(G-))
.subckt QMM + - G
BH 0 H I=min(R(V(A,-)),max(S(V(A,-)),V(H))) Rpar=1
CH H 0 1E-3 ic={H0}
RE + A {ri}
RS A B R=K(rsmin,rsmax)
BD B - I=K(imin,imax)*sinh(K(amin,amax)*V(B,-)) Rpar=1E10
BG G 0 V=K(imin,imax)*K(amin,amax)
.func K(min,max)=min+(max-min)*V(H)
.func S(x)=1/(1+exp(-etas*(x-if(I(BD)>isb,vt,vs))))
.func R(x)=1/(1+exp(-etar*pow(V(H),gam)*(x-vr)))
.ends
.ends
```

Fig. 11. LTSPice script for the compact QMM used for simulating the CRS structures. The label CRS identifies the six-terminal subcircuit with 6 pins: +, c, and - are the three terminals of the device used to describe the I-V characteristics, G+, G-, and G are the terminals which describe the conductances measured at low voltages.

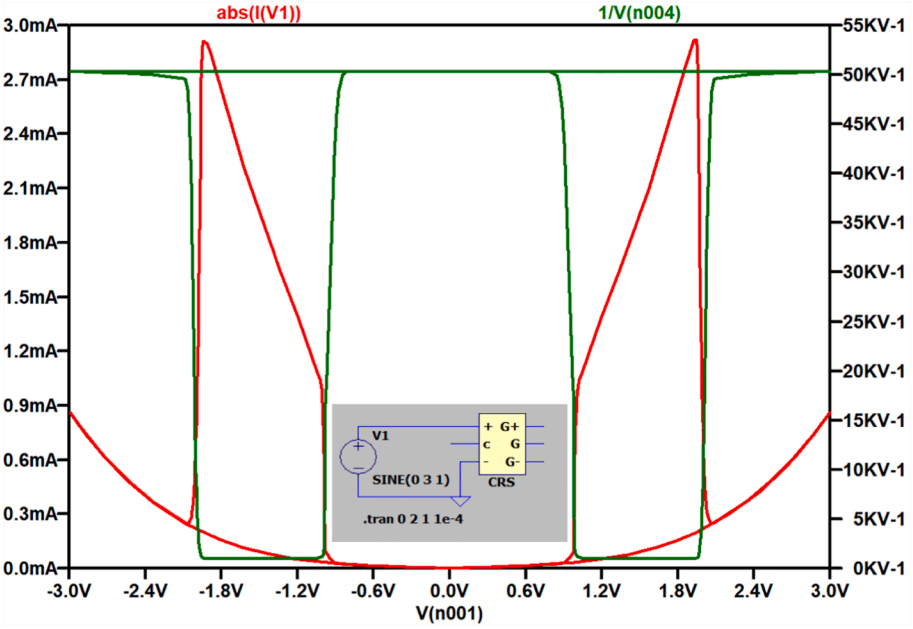

Fig. 12. CRS model curves obtained with the script shown in Fig. 11. The inset of the figure shows the schematic used for the simulation. The red line is the I-V characteristic and the green line is the hysteresis loop (R-V) curve.

the curves. The voltage source used for generating the simulated curves is a sinusoidal signal with a fixed frequency (frequency effects are not considered here). The script contains four sections: *i)* model parameters definition for each RS structure (X1 and X2) and the total conductance of the structure (*G*), *ii)* memory equation using the recursive operator, *iii) I-V* characteristic with series resistance effects, and *iv)* definition of the auxiliary functions. Fig. 12 shows the *I-V* and *R-V* curves for the CRS device (using pins + and *G*, respectively). Notice that the scale of the resistance is in KV^{-1}. This is a limitation of the software (output as a voltage source) and should be directly read as KΩ.

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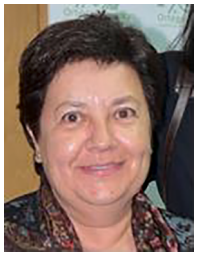

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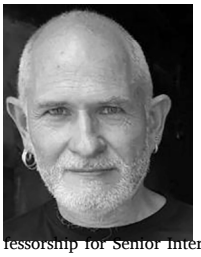

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