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Switching Modulation Strategies for Multilevel Inverter

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Abstract: There is always a need to create efficient and optimized converters to deliver the best possible results to achieve a better THD profile in the waveform output. One way is by controlling the switching of the power switches of the converters using appropriate modulation schemes. While numerous works have been done in proposing new switching modulation strategies for multilevel inverters, this work will compare multicarrier PWM and near-to-level control (NLC) modulation schemes. In this paper, multicarrier PWM variants, namely PD-PWM, POD-PWM, and APOD-PWM, are designed and simulated. Their voltage THD and spectrum performance are discussed when applied to single-phase 7, 9, and 11-level cascaded multilevel inverters. Then NLC modulation will be designed and applied to similar multilevel inverter circuits. It will be shown that the NLC exhibits some superior performances compared to PWM-based but with several drawbacks that can be optimized.

Keywords: multilevel inverter, THD, inverter, PWM, multicarrier, near to level control modulation

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1. INTRODUCTION

The energy utilities providers are looking for ways to ease and advance electricity generation. There are various ways to achieve that. One way is by harvesting energy from natural resources such as solar, wind, geothermal, solar heat, and tidal. These sources store abundant and raw energy that can be transformed into electricity. The idea of harvesting energy from these sources can be traced back centuries ago, but technology limits its development progress back then. However, due to the advancements in materials manufacturing and digital control processors, the momentum of natural sources such as solar (photovoltaic) as electrical energy sources is gaining in recent years.

In a typical photovoltaic system, the inverter takes the main responsibility to convert the solar panel's unregulated dc power to regulated ac power. Depending on the installation purposes, the inverter can be either grid-tied or off-grid type. The total harmonics distortion (THD) is used to measure the quality of the inverter voltage output. In general, the THD voltage of the output should not exceed 5% for a grid-tied inverter.

Two factors determine the THD value, namely the modulation strategies and the type of inverter circuits. To date, various switching modulation strategies can be found in the literature review [3, 4]. Primarily, it is based on pulse-width modulation (PWM). This type of modulation requires the power semiconductors to switch at a high-frequency value. It moves the output voltage harmonics to a high-order frequency value, making the filter design easier.

However, high-frequency switching will cause high electromagnetic interference (EMI) noises [1]. Moreover, the switching losses are considerably high. There are modulation strategies that operate in fundamental frequency, such as space vector modulation (SVM), selective harmonics elimination (SHE), and near-to-level control modulation (NLC). They are simple in implementation but contain low-order harmonics that are not easily removed.

A basic inverter circuit is constructed from two (half-bridge) and four power semiconductors (full-bridge or H-bridge). The simple, straightforward construction and low cost made it a direct choice for the industry. It can produce three-level voltage (+Vdc, 0, and -Vdc) output. However, the voltage across the power switches during the blocking state is as high as its dc source value. A high voltage rating must be used; hence cost increases for high voltage applications and limits its application out from high power applications.

Multilevel inverter (MLI) is a new breed of the inverter. The concept of the MLI is shown in Figure 1. Using multiple dc sources, it can generate multistep (also known as multilevel) output voltage. A lower THD value can be obtained through the use of MLI. The voltage stress across the power semiconductors is reduced significantly since more semiconductors are connected in series. Thus, the multilevel inverter is a direct choice for high-power applications.

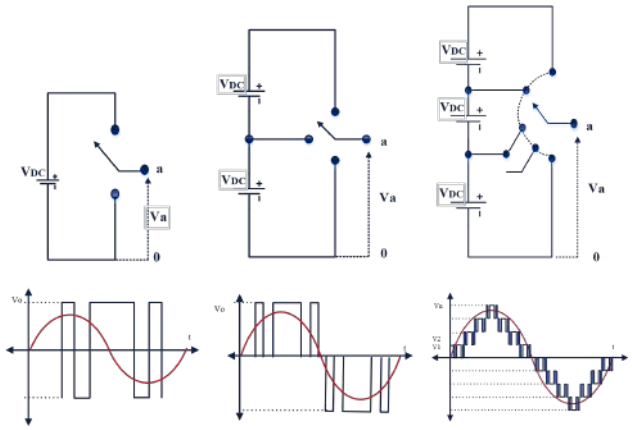


Figure 1. Examples of (a) 2-level inverter (b) 3-level inverter (c) n-level inverter

Three well-known MLIs, namely the neutral-point-clamped (NPC) MLI, cascaded-H-bridge (CHB) MLI topology, and flying-capacitor-clamped (FC) MLI, are widely used [1,2]. Due to its flexibility of control and larger structural modularity, the CHB MLI has received broader attention in practical use. Baker and Bannister originally pioneered CHB MLI's idea. In comparison to CHB MLI, Baker developed the NPC MLI in the year 1980. This particular topology of clamping the diodes is utilized for trimming the switch voltage with just a single dc source [3]. T. Meynard later put forward FC topology in 1992. The FC MLI resembles a similar design as NPC MLI but using capacitors rather than clamping diodes. The number of components increases significantly when the output voltage level increases for both NPC and FC MLIs. It will result in higher control complexity, reliability issue, and the foremost problem is the unequal charge balance across the NPC MLI capacitors [4-26]. Thus, NPC and FC MLIs are limited to three-level MLI only.

The inverter circuit and switching modulations strategies are the core of the inverter system. Modulation strategies are mainly used to control the semiconductor switching to generate an ac output voltage within the permissible THD value. It produces low THD by synthesizing multistep output voltage. On the other hand, a low THD value can also be achieved by using an MLI circuit. To date, there are plenty of MLI circuits and modulation strategies that can be found in the literature [5]. Most of the modulation strategies are PWM-based.

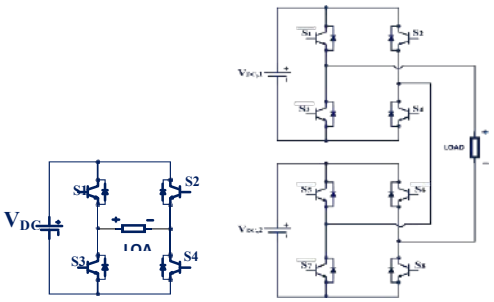
This paper presented the design and performance analysis of several PWM-based and NLC modulation switching strategies to a conventional CHB MLI circuit. For this work, 7, 9, and 11–level models of CHB MLIs are developed. The MLIs will be subjected to different PWM-based variants, namely APOD PWM, POD PWM, PD PWM, and the NLC modulation. Their performance for each MLI circuit is analyzed in terms of the THD, spectrum harmonics, and fundamental output voltage.

2. OVERVIEW OF CHB MLI

The concept of the CHB MLI topology is based on the H-bridge series connection. Each H-bridge unit is comprised of four semiconductors and one input dc source. Each unit has a separate input dc source to synthesize a staircase voltage waveform. Figure 2 shows a single-phase cascaded H-bridge inverter structure for 3-level and 5-level.

Table 1 shows all the possible switching states. To produce +Vdc at the output switches S1 and S4 are ON. Then, switches S2 and S3 are ON to produce –Vdc. To obtain zero voltage output, either switch S1 and S3 should be ON or S2 and S4. To avoid short-circuiting the circuit, the complementary switches, S1, S2, and S3, S4, should not be turned ON simultaneously.

The number of voltage output outputs depends on the total number of isolated dc sources; it is the sum of all levels generated by each cell. Output voltage levels are represented by 2N+1, where N is the number of dc sources.



(a) (b)

Figure 2. (a) Three-level CHB MLI, (b) Five-level CHB MLI Topology

Table 1. Switching states for Five-level CHB MLI

Switch States										
levels		S1	S2	S3	S4	S5	S6	S7	S8	V0
Positive levels	1	1	0	0	1	1	1	0	0	1Vdc
	2	1	0	0	1	1	0	0	1	2Vdc
Zero level	3	0	0	0	0	1	1	0	0	0
Negative levels	4	0	1	1	0	0	0	1	1	-1Vdc
	5	0	1	1	0	0	1	1	0	-2Vdc

3. OVERVIEW OF SWITCHING MODULATIONS

Most of the high switching modulation strategies are PWM-based. The pulses are generated by a comparison between the modulating signal with a carrier signal. In the inverter case, triangular is usually used as the carrier signal. High switching frequency methods generally perform more than two commutations over one period of the output voltages, producing staircase waveform. This technique is considered complex for MLI, and therefore its is only suitable for low-level MLIs. In this work, the PWM-based modulation strategies that are primarily discussed in the literature are presented.

Phase shift PWM is the most popular and commonly used modulation technique to improve the THD performance of CHB MLIs. The carrier-shifted signals are compared with the sinusoidal wave to generate pulses for the power switches, as shown in Figure 3. If the carrier signal is greater than the reference signal, then the power switch corresponding to that carrier signal is switched. The carrier signals' magnitude and frequency are the same for the multilevel inverter, but carriers are phase-shifted by180° (N-Level-1/2) to each other. For N-level MLI, (N-

1) carrier signals are required.

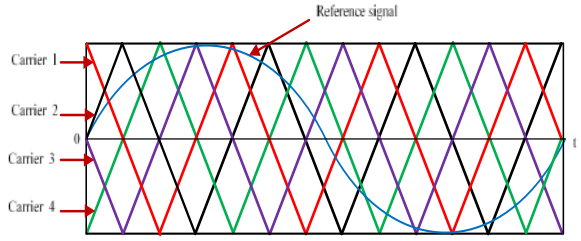


Figure 3. Phase shifted PWM

In level-shifted PWM, the amplitude of carrier signals is shifted, corresponding to output voltage levels. Disposition of carrier signals above and below the zero reference defines the level-shifted technique, which can be divided further into Phase Disposition (PD), Phase Opposition Disposition (POD), and Alternative Phase Opposition Disposition (APOD).

In Phase Disposition (PD) PWM, the carrier signals shifted above and below the zero references have the same magnitude and phase angle. This technique provides better harmonics performance in a higher modulation index compared to other disposition methods. This modulation technique is well suited for cascaded multilevel inverters. The voltage waveform of carrier signals f this technique is illustrated in Figure 4.

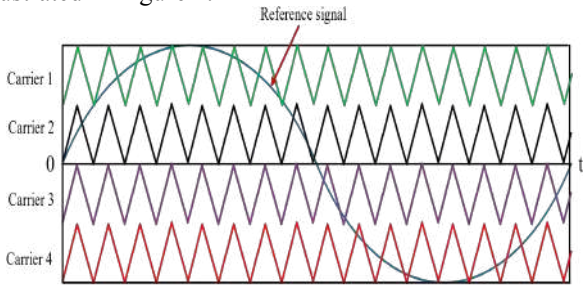


Figure 4. Phase disposition (PD) PWM

In Phase Opposition Disposition (POD) modulation technique, the carrier signals above zero reference are phase-shifted with those below the zero-reference voltage by 180 degrees. The voltage waveform of carrier signals of this technique is illustrated in Figure 5. This technique provides better harmonics performance in lower modulation index compared to phase disposition methods.

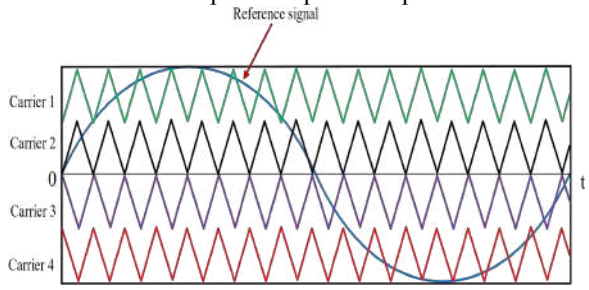


Figure 5. In phase opposition disposition (POD)

The third type of carrier disposition PWM is known as Alternative Phase Opposition Disposition (APOD). In this technique, each carrier signal is phase-shifted from its adjacent carrier signal by 180 degrees. Phase Opposition Disposition and Alternative Phase Opposition Disposition have the same results for the three-level inverter. The voltage waveform of carrier signals of this technique is illustrated in Figure 6.

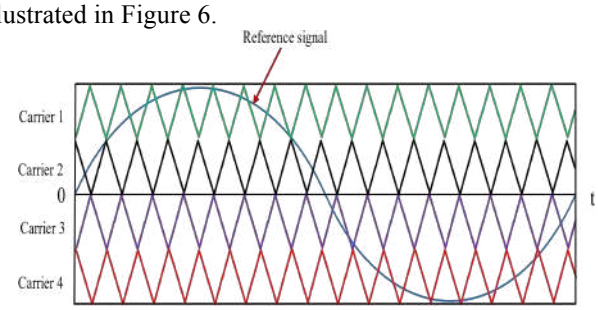


Figure 6. Alternative phase opposition disposition (APOD)

Fundamental switching frequency is generally described to be few multiples of fundamental switching frequency below 1 kHz. These switching modulation strategies' apparent advantage is low switching losses, making it the most preferred modulation strategy for high power application-based inverters. However, notable modulation strategies such as SVM and SHE demand high processing power for the implementation. The NLC, on the other hand, is a straightforward implementation. Discussions of both are widely found in the literature.

NLC method is called the round modulation method or can also be known as the half-integer method, which can be easily performed by round function (round {}) as seen in Figure 7. The nearest voltage level is produced in this technique when comparing sinusoidal voltage (V_{ref}) with the inverter output voltage to produce proper switching signals. The Nearest voltage level can be generated using the formula as in equation (1)[6].

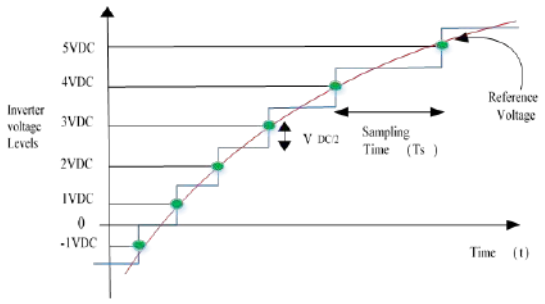
$$\text{Nearest voltage level} = V_{dc} \times \text{round}\,(V_{ref}/V_{dc}) \qquad (1)$$

The Vref is the reference voltage. Here, Vdc represents the voltage difference between the two levels. So, the round function is applied to this value to determine the closest value of an integer of Vdc. This method's main drawback is that it is not suitable for a low number of output voltage level inverters.

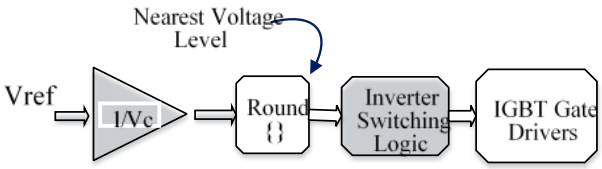
4. METHODOLOGY

Three types of level shift PWM, i.e., PD, POD, and APOD PWMs, are developed, simulated, and analyzed. For NLC, instead of comparing carriers, integers are compared with the sinusoidal to produce gating pulses. The performance analysis for different modulation strategies is conducted with 7,9 and 11-level CHB MLIs. All the CHB MLIs are developed using the Matlab-Simulink platform. Figures 8, 9, and 10 depict the model of the CHB MLI, respectively.

The dc source value for each H-bridge for all MLI circuits is equal to 100 V. The switching frequency carrier (switching frequency is set as 1 kHz, and the fundamental output frequency is 50 Hz. If the modulation index, m_i (equation 2), is set as unity, the maximum fundamental output voltage is 300 V, 400 V, and 500 V for 7, 9, and 11-level CHB MLI.



(a)



(b)

Figure 7. Nearest level method (a) waveform (b) control logic

$$m_i = \frac{A_m}{\frac{(N-1)}{2}A_C} = \frac{A_m}{MA_C} \quad (2)$$

Where A_m is the amplitude of the reference signal, A_c is the amplitude of carrier signal, and N is the number of dc sources.

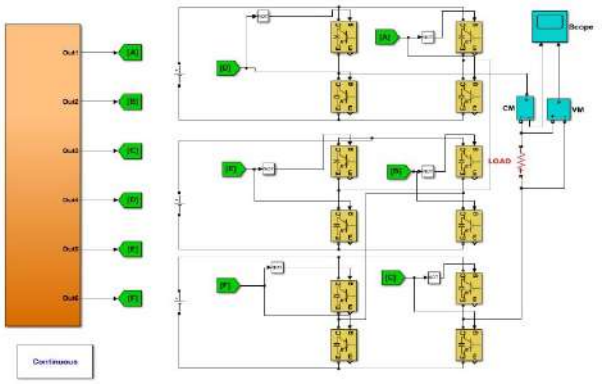


Figure 8. Circuit topology of seven-level CHB-MLI

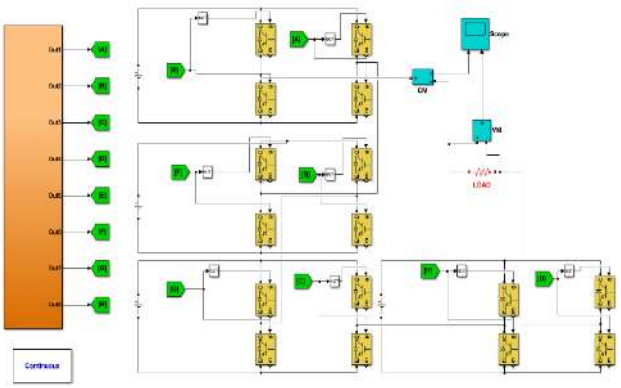


Figure 9. Circuit topology of nine-level CHB-MLI

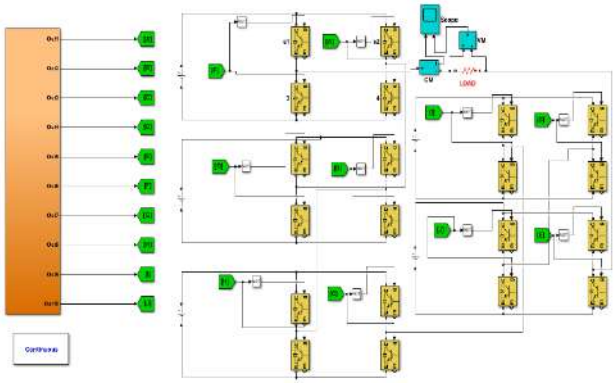


Figure 10. Circuit topology of eleven-level CHB-MLI

For NLC modulation, the circuit topology is the same as PWM. Unlike PWM-based, the NLC generates pulses based on the comparison between modulating signal with an integer. The NLC technique uses a round-off condition to know the nearest level with the formula given in equation (1).

$$Nearest\ voltage\ level = Vdc \times round(Vref/Vdc) \quad (2)$$

An example of how this equation works is shown below. Hence, if V_{ref} is chosen as 50V, 150V, and 250V for seven-level, the inverter will trigger each level's middle point. For the values of V_{ref} equal to 50V, 150V, 250V, 350V, the inverter will trigger at the middle point of each level for the nine-level inverter. If V_{ref} is equal to 50V, 150V, 250V, 350V, and 400V for an 11-level inverter, the inverter will trigger each level's middle point. The middle point is the 50% value of each voltage level and creates a trigger pulse for the switches.

It means is that the control circuit will not produce a trigger pulse for the switches unless more than a 50% value of the reference is reached because it rounds-off ≥ 50% value of Vref/Vdc to 100% of Vdc value of individual level and for ≤50%, it will give zero. This process is used at each voltage level of the modulation.

5. RESULTS AND DISCUSSION

Simulation results are obtained for 7-level, 9-level, and 11-level. First, simulations are conducted for single-phase CHB MLI using PWM modulations. The same circuits are then simulated using the NLC technique; however, NLC will be further analyzed and optimized using different reference and DC interference switching points. The block diagram to generate PWM switching is shown in Figure 11. The same block will be used to generate NLC modulation. The difference is that carrier signals will be replaced with integers that represent the dc voltage.

Figures 12 (a) and (b) show the output voltage waveform of PD-PWM and its harmonics spectrum for a 7-level MLI circuit, respectively. The THD_v measured is 17.86%. The output voltage and spectrum for 7-level NLC are shown in Figure 13(a) and (b), respectively. The THD_v is measured as 11.76.

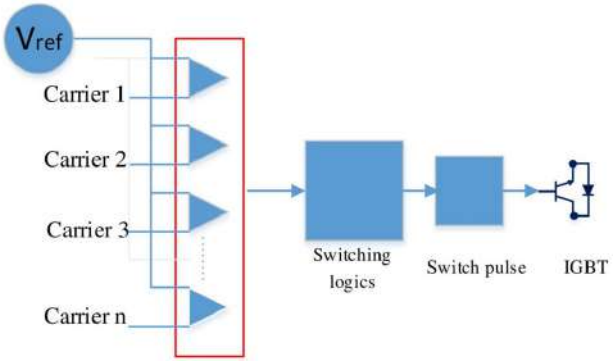
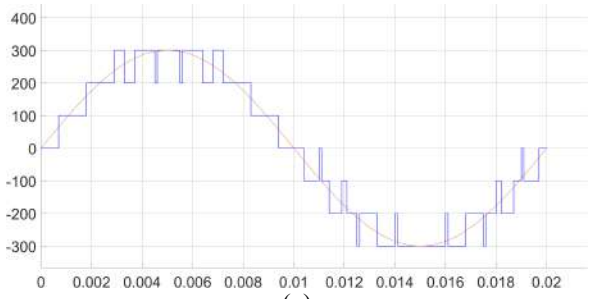
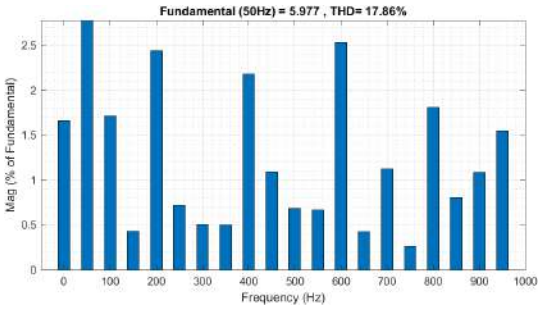


Figure 11. Block diagram for various techniques used in this work

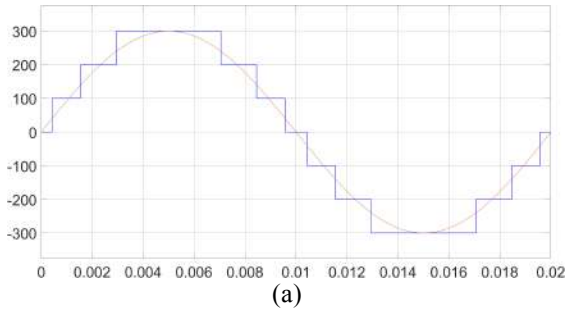


(a)

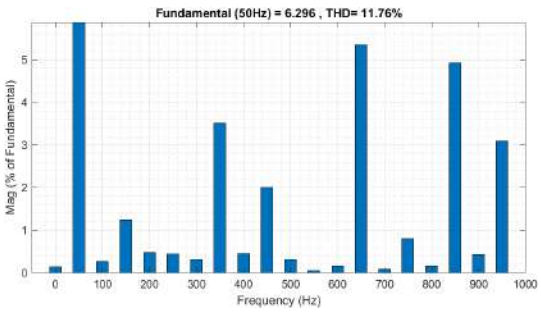


(b)

Figure 12. (a) Voltage output (b)Voltage THD; for 7-level PD-PWM



(a)



(b)

Figure 13. (a) Voltage output (b)Voltage THD; for 7-level NLC MLI

Table 2 shows the summary of the simulation. At a high modulation index, i.e., 1 in this case, PD-PWM shows better results, followed by APOD and POD. The POD gives better output at a lower modulation index. On the other hand, the NLC exhibits the best results than all PWM-based.

Table 2. Summary of simulation results

THD AND VOLTAGE AS PER LEVEL AND TYPES						
	7 LEVEL		9 LEVEL		11 LEVEL	
	THD%	Vo (at 300 Vin)	THD%	Vo (at 400 Vin)	THD%	Vo (at 500 Vin)
PD-PWM	17.86	294.9	13.70	400	10.58	498.1
POD-PWM	17.30	298.9	16.47	396.7	10.91	488.7
APOD-PWM	19.23	297.1	13.83	402.9	10.94	496.9
NLC	11.76	314.8	9.13	414.1	7.38	514.8

Further analysis of NLC modulation has been conducted. The objective is to search for the optimum performance of the NLC and parameters that affect the performance. The performance is measured on the fundamental magnitude voltage that NLC can generate and THD value measurement.

The literature shows that the triggering is determined by the variation in angles [27, 28]. However, this paper provides a different interpretation; unlike switching angle variation, the dc value at each level is chosen for switching. Hence, the dc level is divided into small sections; each represents 0.1Vdc. The value of the dc level is increased at a step of 0.1 from zero to unity value. The basis of this analysis is to detect the best output results as Total Harmonic Distortion for voltage (current being same as voltage), i.e., lowest is the best and vice versa.

It was best to check for single-phase 7, 9, and 11-level NLC at the intersection with 0.25Vdc, 0.5Vdc, and 0.75Vdc. It was observed that a lower than 0.5 would give better results in the THD value. Increasing values more than 0.5 will yield a higher fundamental voltage value and THD. However, the most optimized results were obtained at 0.4Vdc at each level, as seen in Figure 39.

All results for different points of switching are summarized in Table 3. The best values of %THD amongst them are highlighted in green.

Table 3. Summary of THD% at different points of switching in each level

THD% AT DIFFERENT POINTS OF SWITCHING IN EACH LEVEL						
	7 LEVEL		9 LEVEL		11 LEVEL	
	THD%	Vo (at 300 Vin)	THD%	Vo (at 400 Vin)	THD%	Vo (at 500 Vin)
0.25VDC	12.37	325.4	9.75	427.6	7.85	528.3
0.5VDC	12.23	306.1	9.34	406	7.57	504.9
0.75VDC	16.58	277.5	12.14	376.5	9.60	475.4
0.4VDC	11.76	314.8	9.13	414.1	7.38	514.8

6. CONCLUSION

This paper compares multicarrier PWM variants with near-to-level control (NLC) modulation for a cascaded multilevel inverter. It was shown that the NLC provides the lowest voltage THD compared to PWM modulation. However, the conventional NLC was not optimized. An in-depth study to correlate the THD, the fundamental voltage, and spectrum performance with the modulation synthesizing method was done. The use of per-level voltage interfered with triggering by the DC voltage's interfering value at each level with the rising sinusoidal reference was adopted. The optimized NLC is achieved when the voltage intersection is put at 0.4Vdc. The THD value is 7.38%, with the fundamental voltage is 3% higher than the DC input.

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