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Optimization of LLC resonant converters

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Optimization of LLC resonant converters

Trabalho de Projeto para a obtenção do grau de Mestre em Engenharia Eletrotécnica

Especialização em Automação e Comunicações em Sistemas de Energia

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ABSTRACT

This report comes under the Maters Degree in Electrical Engineering - Automation and Communications in Energy Systems Specialization Area, aiming an optimization of a 4.2 kW DC-DC converter to achieve maximum efficiency.

As the time passes there are more powerful motors, batteries and energy sources, and the delivery of the required energy needs to ensure maximum efficiency, but also, with higher power density having smaller but powerful devices.

This work consists on the optimization of the LLC converter continuing the work made previously by Mestre Maria Ruxandra Luca, in a partnership with the University of Oviedo in 2020.

At an early stage, the optimized design developed in [1] that already has a theoretical efficiency of 98.6%, will be used, comparing the simulated values using a real device model with the theorical ones, in order to see the differences and looking to where the converter could be improved. In a second phase, since the rectifier and the transformer are the components that produce the most losses, the hypothesis of using a mid-point transformer will be tested, in order to reduce the number of rectifiers by half, using also GaN HEMTs in order to lower those losses.

The project was carried out in partnership with the University of Oviedo, considered one of the best in Europe, and with the Instituto Superior de Engenharia de Coimbra.

Keywords: DC-DC resonant convert

LLC Convert Resonant

Power Density

Resonant Conversion

Resonant Frequency

Zero-voltage switching (ZVS)

Zero Current Switching (ZCS)

Resumo

Usualmente, na área da eletrónica de potência, tem que existir um trade-off entre densidade de potencia e o rendimento, por forma a desenhar dispositivos que sejam pequenos o suficiente, para ocupar o mínimo espaço, mas ao mesmo tempo altamente eficientes, por forma a maximizar a energia consumida em trabalho resultante, especialmente em veículos elétricos, onde existem várias etapas de conversão de energia. O presente trabalho visa estudar os conversores ressonantes e as suas topologias associadas, continuando o estudo realizado pela Mestre Maria Ruxandra Luca em parceria com a Universidade de Oviedo, tendo como principal objetivo a otimização de um conversor ressonante LLC de $4.2\ kW$ para carregamento de baterias.

Este tipo de conversor é mais vantajoso quando comparado com os conversores tradicionais, devido à utilização do conceito de ressonância e de técnicas *Soft Switching*, como o *Zero Current Switch (ZCS)* e *Zero Voltage Switch (ZVS)*. Estar em ressonância significa, ter um comportamento resistivo pelo facto da soma de todas as impedâncias do tanque de ressonante ser nula. Isto leva a que a corrente esteja em fase com a tensão, permitindo o mínimo de perdas, para uma situação em que o ganho do conversor é unitário. Porém, para alterar o valor da tensão da saída do conversor, este ganho tem que ser alterado (com a modulação de frequência), levando o conversor a trabalhar fora da sua zona de ressonância, com um desfasamento entre tensão e corrente, aumentando significativamente as perdas nos semicondutores comutadores.

O uso de técnicas *Soft Switching*, como o *Zero Current Switch (ZCS)* e *Zero Voltage Switch (ZVS),* permite a minimização de perdas de comutação quando o conversor trabalha fora de ressonância, utilizando mecanismos como a equalização da corrente no transformador (entre corrente magnetizante e corrente série) *e Dead-Time* para fazer com que as comutações sejam feitas quando a corrente e a tensão estão a zero. Devido á menor taxa de perdas nas comutações, o uso de frequências mais elevadas é possível, obtendo assim conversores com uma maior densidade de potência, mantendo uma operação com elevada eficiência.

Neste trabalho é apresentado um breve capítulo do estado da arte, em que diversos modos de conversão DC-DC são apresentados, comparando as suas vantagens e desvantagens, seguido de uma análise às arquiteturas e topologias mais utilizadas nos conversores ressonantes. Com o objetivo de aumentar a eficiência, são descritos os andares do conversor onde existem mais perdas, com as suas causas, e possíveis soluções como o uso de transístores de alta mobilidade de eletrões, (do Inglês *High Electron Mobility Transitors HEMT*) combinados com materiais *wide band-gap*, que permitem operar de forma mais eficiente quando comparados com semicondutores de silício, a utilização de *air-gap* distribuído, bobines entrelaçadas e o fio de *Litz*, para

minimizar as correntes de Eddy produzidas no transformador, e ainda a utilização de retificação síncrona em substituição aos díodos retificadores.

De seguida, num terceiro capítulo, é apresentada a configuração base do conversor LLC ressonante para o carregamento de baterias de iões de lítio, detalhando cada um dos blocos associados, acompanhado de uma análise teórica por forma a permitir compreender o funcionamento do conversor, quais os principais fatores mais importantes, e qual o impacto da frequência de comutação no comportamento do conversor. Neste capítulo é ainda apresentado o processo de desenho deste conversor discriminando quais os parâmetros iniciais necessários, com uma análise detalhadas das perdas associadas ao design base, finalizando com o estudo, das diferentes arquiteturas do conversor nos andares de conversão AC-DC e DC-AC, e da retificação síncrona com a utilização de HEMTs, na eficiência do conversor. Simulações serão então conduzidas posteriormente utilizando modelos reais dos componentes presentes no conversor, com o uso do *software* LTSpice, comparando de forma detalhada o design base, com os designs otimizados previamente obtidos, de forma a observar o impacto das alterações propostas.

Inicialmente foi previsto construir o conversor apresentado em [1] e o conversor otimizado mais eficiente, testá-los experimentalmente, mas devido à situação atual da pandemia Sars-Cov (Covid 19), o mesmo não foi possível, a tempo de entregar este trabalho, sendo este, um dos trabalhos futuros.

Este trabalho foi desenvolvido em parceria com a Universidad de Oviedo, com o grupo de investigação LEMUR na Escuela Politécnica de Ingeniería de Gijón, onde foram feitas as analises teóricas e simulações do conversor de ressonância LLC.

Table of Contents

List of Figures

List of Tables

SYMBOLOGY AND ABBREVIATIONS

A_e	Effective Cross-Sectional Area of the Core [m^2]
A_c	The cross-sectional area of the core [m^2]
b_w	Width of transformer turn [m]
B_m	Maximum flux density [T]
C	Capacitor [F]
Cap	Battery capacity [ah]
C_o	Output capacitance filter [F]
CC	Constant current
$CC-CV$	Constant current constant voltage
C_r	Resonant capacitor [F]
C_r	Junction capacitance [F]
Cte	Constant
CV	Constant voltage
c, x, y	Steinmetz coefficients
C_{DS}	Drain to Source Capacitance [F]
DT	Duty cycle [%]
t_{dT}	Dead Time [s]
E_{Sw_off}	HEMT switch-off energy [J]
ESR	Equivalent series resistance [Ω]
f	Frequency [Hz]
f_o	Resonant Frequency associated to L_r, and C_r [Hz]
fm	Frequency modulation
f_p	Resonant frequency associated to L_r, L_m, and C_r [Hz]
f_{sw}	Switching frequency [Hz]
H	Magnetic field [T]
I	Current [A]
I_{Ed}	Eddy currents loops [A]
I_f	Forward current [A]

I_o	Output current [A]
I_{oe}	Output equivalent current [A]
$I_{o_{nom}}$	Nominal battery current [A]
$I_{o_{max}}$	Maximum output current [A]
I_R	Insulation resistance [Ω]
K_h	Hysteresis constant
L	Inductance [H]
l_c	Length of the core [m]
l_{DS}	Power loop inductance [H]
L_{EX}	External source inductance [H]
I_w	Length of transformer individual turn [m]
L_{GATE}	Gate inductance [H]
L_k	Leakage inductance [H]
L_f	Output inductance filter [H]
L_r	Resonant inductance [H]
L_m	Magnetizing inductance [H]
L_n	Inductance ratio
M	Number of the winding interleaved multiples
MCC	Multistage constant current
M_g	Resonant tank gain
$M_{g_{max}}$	Maximum resonant tank gain
$M_{g_{min}}$	Minimum resonant tank gain
n	Transformer ratio
n_{periods}	Number of periods
η	Efficiency [%]
σ	Conductivity of the conductor material [$\Omega \cdot \text{m}$]
P	Power [W]
$P_{B_{max}}$	Maximum output power [W]
P_{core}	Core losses [W]
P_{cu}	Copper losses [W]
$P_{D_{Cond}}$	Diode Conduction losses [W]
$P_{D_{Sw}}$	Diode Switching losses [W]

P_{nom}	Charger nominal power [w]
P_{Sw}	Switching losses [W]
ρ_c	Resistivity of the core [Ω·m]
Q_e	Quality factor
Q_g	Total gate charge [C]
R	Resistance [Ω]
R_{AC}	Ac resistance [Ω]
R_d	Internal diode resistance [ω]
R_{DC}	Dc resistance [Ω]
$R_{DS_{on}}$	Drain to Source Resistance [Ω]
R_e	Equivalent output load [Ω]
R_G	Gate resistor [Ω]
$R_{L_{out}}$	Resistance output inductance filter [Ω]
R_o	Output load [Ω]
R_s	Series resistance [Ω]
δ_o	Skin depth [m]
TC	Transformer coupling [%]
t_j	Working temperature [°C]
T_P	Total Period [s]
T_{rr}	Reverse recovery time [s]
T_{ON}	Turn On Period [s]
μ_o	Magnetic permeability of free space
V	Voltage [V]
V_o	Output voltage [V]
$V_{B_{max}}$	Maximum battery voltage [V]
$V_{B_{nom}}$	Nominal battery voltage [V]
V_{BD}	HEMT reverse voltage drop [V]
V_{dc}	Nominal Charger input DC link [V]
$V_{dc_{max}}$	Maximum Charger input DC link [V]
$V_{dc_{min}}$	Minimum Charger input DC link [V]
V_{DD}	Driving voltage [V]
V_e	Core volume [m^3]

V_f	Diode voltage drop [v]
$V_{G(ON)}$	Turn on gate voltage [v]
$V_{G(OFF)}$	Turn off gate voltage [v]
V_{in_e}	Fundamental input voltage [v]
V_{o_e}	Fundamental output voltage [v]
V_{loss}	Voltage Drop Due to Power Losses[V]
V_{TH}	Threshold voltage drop of HEMT 2DEG [V]
ΔI	Battery current ripple
ΔV	Battery voltage ripple
$\sum x$	Sum of all section dimensions perpendicular to the section interfaces
$\sum x_{\Delta}$	Sum of all inter-section layer thickness

Measure Units from S.I.

A	**Ampère** – Unit of measure of electric current according to SI
C	**Coulomb** – Unit of measure of electric charge according to SI
F	**Farad** – Unit of measure of electric capacitance according to SI
H	**Henry** – Unit of measure of inductance according to SI
Hz	**Hertz** – Unit of measure of frequency according to SI
m	**Meter** – Unit of measure of length according to SI
rad	**Radian** – Unit of measure of angular degrees according to SI
s	**Second** – Unit of measure of time according to SI
V	**Volt** – Unit of measure of electric voltage according to SI
Ω	**Ohm** – Unit of measure of electric resistance according to SI
$\%$	**Percentage** – Unit of measure of percentage according to SI

LIST OF ACRONYMS

AC	Alternating Current
BMS	Battery Management System
DC	Direct Current
EV	Electric Vehicle
ESR	Equivalent Series Resistance
EMI	Electromagnetic Interference
FHA	First Harmonic Approximation
$HEMT$	High Electron Mobility Transistor
HEV	Hybrid Electric Vehicle
IPC	Instituto Politécnico de Coimbra
$ISEC$	Instituto Superior de Engenharia de Coimbra
$Li-Ion$	Lithium Ion
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RMS	Root Mean Square
SoH	State of Health
SoC	State of Charge
SR	Synchronous Rectifier
ZCS	Zero Voltage Switching
ZVS	Zero Current Switching

GLOSSARY

Duty Cycle, percentage of the total period which the signal is at high logic level, being low the rest of the period.

Ripple, AC component on an average value of a DC signal, due to an incomplete suppression of an AC component, generally obtained on AC to DC rectification.

Resonance, a phenomenon that occurs in an electronic circuit when the capacitive and inductive reactances cancel to each other, making an electronic circuit behaves like a resistive load.

ZVS, *Zero Voltage Switching* is a technique that allows the *Synchronous Rectifier* (SR) switch, when there is not a Voltage applied to the rectifier, leading to almost leading to almost no switching losses.

ZCS, *Zero Current Switching* is a technique that allows the Synchronous Rectifier (SR) switch, when there is not current crossing the rectifier, leading to almost leading to almost no switching losses.

Dead-time, the necessary time between the turn-off and turn-on of two switches either on primary side, or the secondary, guarantying that only one of the switches is conducting at the time**.**

CHAPTER 1. Introduction

Renewable energies are one of the main focuses in present days. Electric Vehicles (EV), and renewable energies are some of the solutions to reduce de emissions to the atmosphere, but with the growing demand for energy, power electronic devices need to ensure high reliability, high efficiency, in order to maximize the extracted energy, as well as higher power density $energy/cm^3$, which means obtaining more energy, maintaining constant the device size.

Nowadays car manufacturers are giving more attention to Electric Vehicles (EV) than to internal combustion engine (ICE) vehicles, as EV are considered one of the future vehicles [47]. They are entirely powered by batteries, providing energy to a converter, controlling the energy that goes to the electric motors (one or more, depending on the vehicle). The same motors can work as generators, and regenerative braking can be also used to charge the car batteries. However, they are not enough to hold long distance travels. To do that, the batteries need to be fully recharged using external charging points. Figure 1.1 presents a conventional battery charger, composed by two different systems. An AC-DC converter, converting the grid AC voltage to DC, (the charging station), and DC-DC converters responsible to regulate the charger output voltage, to the nominal battery levels charging the batteries until they reach hundred percent State-of-Charge (SoC).

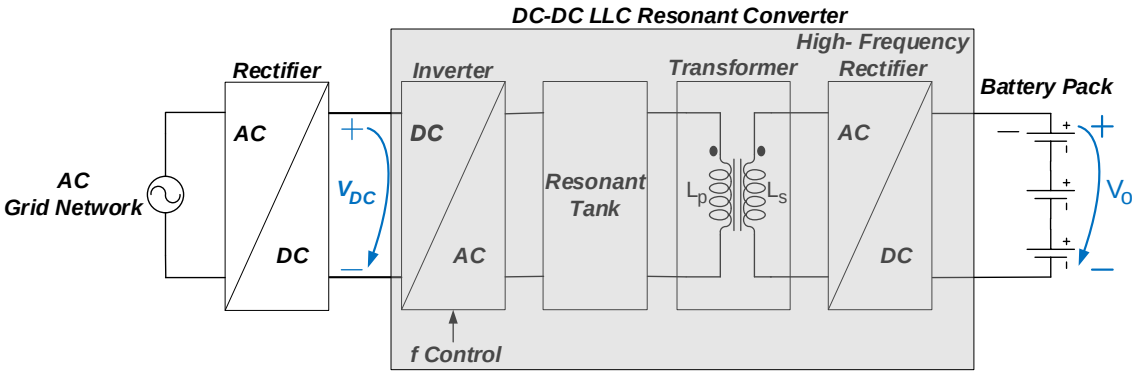


Figure 1.1 - General configuration of the battery charger

In order to regulate the output of the DC-DC converter, a control method is required. The most popular, are Pulse Width Modulation (PWM), and Pulse Frequency Modulation (PFM). PWM converters modulate the duration of the duty cycle (D_t) of the control signal, to regulate the output voltage. Those type of converters are popular due to their lower component number, their simplicity, and their improved efficiency when compared to the linear converters, as the lm317, being suitable to medium/high power levels. The main disadvantage of the non-resonant converter is the inefficient switching operation. Due to the hard-switching, high switching losses and electromagnetic interference (EMI) appear,

limiting the operating converter frequency, power density, and also the overall efficiency.

Knowing those issues, researchers focus their attention to the resonant converter. By working at resonance, (meaning that capacitive and inductive reactance cancel each other), the converter operates at *ZPA (Zero Phase Angle)*, behaving like a resistive load, with minimal the switching losses as the tank current is in phase with the input tank voltage. To control the output voltage on these converters, *PFM* is used instead *PWM*, allowing fewer switching commutations in the voltage range. The drawback, in this scenario, is the operation out of resonance that leads to high switching losses due to the drain current being out of phase when compared to the drain to source voltage (V_{DS}).

To solve this issue, researchers came across with *Soft-switching techniques*: *Zero Voltage Switching (ZVS)* and *Zero Current Switching (ZCS).* When the converter works out of resonance, those technics allow minimum switching losses by having the commutations made when the voltage or the current are zero, respectively, achieving higher stability, and higher efficiency under a wider range of operation.

The purpose of this work is to study the LLC resonant converter applied in a $4.2\ kW$ battery charger, and how could the efficiency be improved, continuing the study “Optimization of the Design of a Half-Bridge LLC Resonant Converter for Fast Charging of Storage in Electric Vehicles” developed by Master Maria Ruxandra Luca at the at the UNIVERSIDAD DE OVIEDO [1]. During this work, LTSpice softwares and Frenetic online software will be used, to analyze the converter losses at and out of resonance, and to improve the magnetic components present in the converter, comparing the base design of the converter made by [1], over the optimized designs .

1.1 – Objectives

The main objective of this work is to increase the LLC Resonant converter efficiency, in order to be used in a battery charger. Different architectures will be tested as well as new wide band-gap materials such as Gallium Nitride used in High Electron Mobility Transistors (forming GaN HEMT) for synchronous rectification, analyzing their operation and their impact in the efficiency of the converter, using the software LTSpice.

To achieve this, partial objectives were outlined:

- Analyze the different resonant converter topologies and architectures
- Operation of the transformer at high frequencies
- Study of GaN HEMTs

- Analysis of the LLC resonant converter
- Project and design of an LLC resonant converter
- Impact of the different converter architectures and synchronous rectification
- Simulation of the optimized designs comparing them with the base design from [1]

1.2 - Document Structure

This work will be divided into 5 chapters, being described as follows:

Chapter 1 - Introduction, makes a brief introduction about this work and what will be done, showing the objectives and the purpose of this work.

Chapter 2 - Resonant DC-DC converters, performance and application, presents the DC-DC conversion, several types of power converters available looking to their advantages and disadvantages, followed by a brief analysis of GaN HEMT devices over the common MOSFETs, the impact of high frequency in High Frequency Transformers, finalizing with the concepts that will be tested in the LLC converter to achieve higher efficiency

In **Chapter 3 – Analysis of the LLC Resonant Converter and its associated losses,** the LLC Resonant Converter will be evaluated, looking to its operation modes and the effect of frequency modulation in the converter. Next, the design process will be presented, producing the base design following the considerations made in [1] to obtain similar conversion, based on small changes on the topology and a fair comparison and losses will be calculated. To finalize this chapter, the proposed concepts will be analyzed, focusing on the loss analysis and equating them.

Chapter 4 – Efficiency Optimization of LLC Resonant Converter, simulations of the different topologies of the LLC resonant converter will be carried out in order, comparing them to see the most effective for this application.

The last chapter will be **Chapter 5- Conclusions, Contributions and Future Work**, presenting the conclusions obtained from this work, and identifying future work that may also improve the overall efficiency of the LLC resonant converter.

CHAPTER 2. Resonant DC-DC converters, performance and application

In this chapter, a brief comparison between the different DC-DC converters topologies will be made, looking at their power applications, and their main losses. Resonant converters will be studied, where among them, the LLC is the selected converter considering the application. Small changes in its architecture will be analyzed, as well the key points for loss analysis, and ways that could improve the overall efficiency. This implies, analyze the control methods applied to adjust the converter gain, the use of new wide band-gap semiconductors like Gallium Nitride High Electron Mobility Transistor, and the effects of high-frequency in power transformers. The chapter ends with the main aspects that must be considered, if this resonant converter is used for a battery charging application.

2.1. DC-DC converters

DC-DC converters are devices that are projected to change the amplitude of a supplied with a DC signal. Described in Table 2.1, DC-DC converters can be divided in three different groups: Linear, Hard-switch and Soft-switch (Figure 2.1), where each group may, or may not, allow galvanic insulation, separating the high voltage side from the low voltage [3].

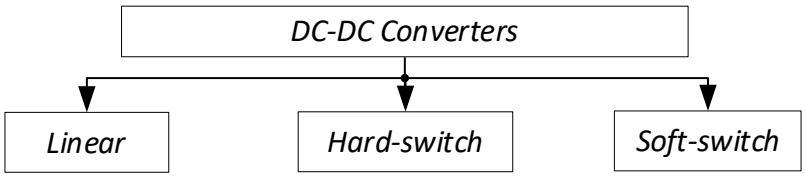


Figure 2.1 - Three basic converter configurations

Used in low power applications, the linear DC-DC converters are the simplest way to change the output voltage with low cost and low complexity, but are very inefficient due the high Joule loss. These type of converters are mainly used in circuits with low power and low current, where the mentioned losses can be considered insignificant. In applications that a better control of the output is required, Hard-switch converters can be used. Those, use the PWM technique applied to converter switches, varying the control signal duty cycle to control the gain, offering more precision than linear mode. Presenting a good operation for high-power applications, and simple circuit implementation, their disadvantage, is the hard-switching. When commutations happen, the converter power flow is interrupted, regarding the state of the circulating current or the voltage in that

node, resulting in high losses during the commutations, limiting the range of working frequencies, and power density. Resonant converts regulate the output voltage using PFM taking advantage of the resonant principle of operation, ZPA (Zero Phase Angle) operation minimizing switching losses. When operated out of resonance, the resonant current will be shifted causing switching losses, but when combined with using Soft-switching-techniques, Zero Voltage Switching (ZVS), and Zero Current Switching (ZCS), switching losses can be minimized since the commutations are made when the voltage or the current are near zero, leading to a higher efficiency in a wider operation range. This type of converters typically operate with high switching frequencies, allowing circuit miniaturization (higher power density), nonetheless, they are more complex and typically more expensive to build.

Table 2.1 - Comparison between the 3 groups of DC-DC converters [3]-[6]

	Linear Mode	**Hard Switch Mode**	**Soft Switch Mode**
Application in the Circuit	Simple	More complex	More complex
Power Applications	Low	Medium/High	Low/High
Number of Components	Low	Medium	High
Controller Driver	Not necessary	Necessary	Necessary
Galvanic Insulation	No	Possible	Possible
Output Ripple	High	Low/ Medium	High
Cost	Low	Medium	High
Efficiency	Low	Medium	High

2.2. Resonant Converters

Resonant converters are a type of DC-DC converter based in the principle of resonance to obtain high efficiency at nominal operation (resonance), and by using soft-switching, it is possible to minimize switching losses. These can have high efficiency under overload operation ($R_o < R_{nominal}$), as well at underload operation ($R_o > R_{nominal}$). By having the capability to work with higher frequencies due to the lower switching losses, the $power\ density/cm^3$ increases, allowing high power converters with smaller sizes [3].

Illustrated in Figure 2.2, DC-DC resonant converters can be divided into 3 blocks:

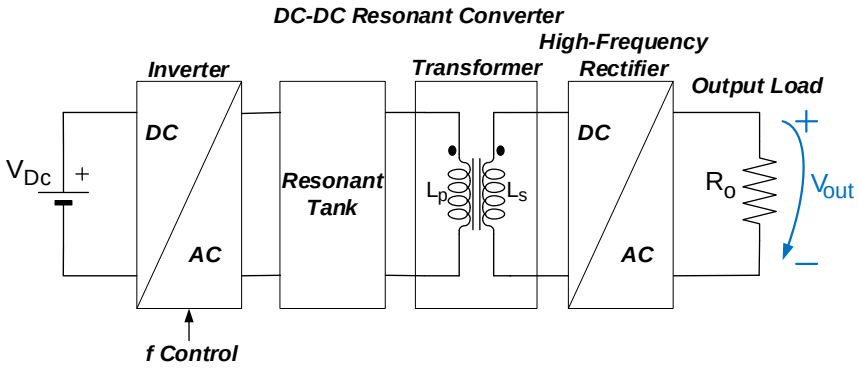
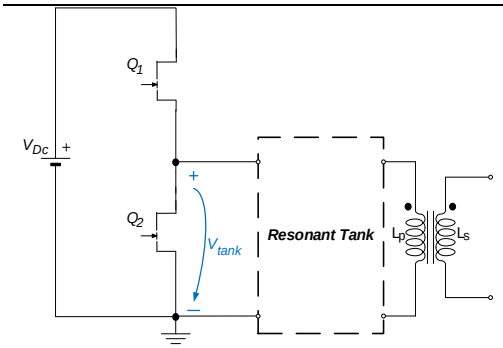
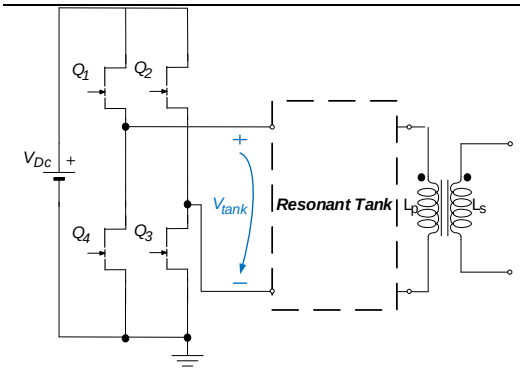


Figure 2.2- General configuration of insulated Resonant converters

- Inverter
  - This block contains the switches, operating at 50% duty cycle ($D.T$), with a certain dead time (d_t) between each other, responsible for producing the square wave that enters the Resonant tank.
- Resonant Tank
  - Composed by 2 or 3 passive components being capacitances or inductances, adjusting the gain of the filter depending on the frequency of the square wave that enters the tank.
- High-Frequency Rectifier
  - In the Rectifier Network the AC signal is converted to DC, using two or more asynchronous or synchronous rectifiers, along with passive components ensuring minimal ripple in the output.

Every block can have different topologies and architectures, resulting in a different behavior. Starting with the inverter block, mainly two architectures can be used, half-bridge and full-bridge. Table 2.2 lists the advantages and disadvantages of each [8] [9].

Table 2.2 – Different topologies for Inverter Block

Inverter Block Topologies	Advantages	Disadvantages
 **(a) Half-bridge DC-DC converter**	• Lower switch number • Simpler controllers for gate drivers • Suitable for lower power application	• Higher device and resonant tank RMS current • Switches with higher voltage rating
 **(b) Full-bridge DC-DC converter**	• Lower device and resonant tank RMS current • Lower conduction losses • Switches with lower voltage rating • Suitable for high power application	• Increased complexity for gate drivers • Require more switches • Higher cost when compared to Half bridge

Regardless the inverter architecture, either full-bridge or a half-bridge, the main feature of the converter is the resonant tank. Having two or more passive components, the most common resonant tank topologies are presented in Figure 2.3

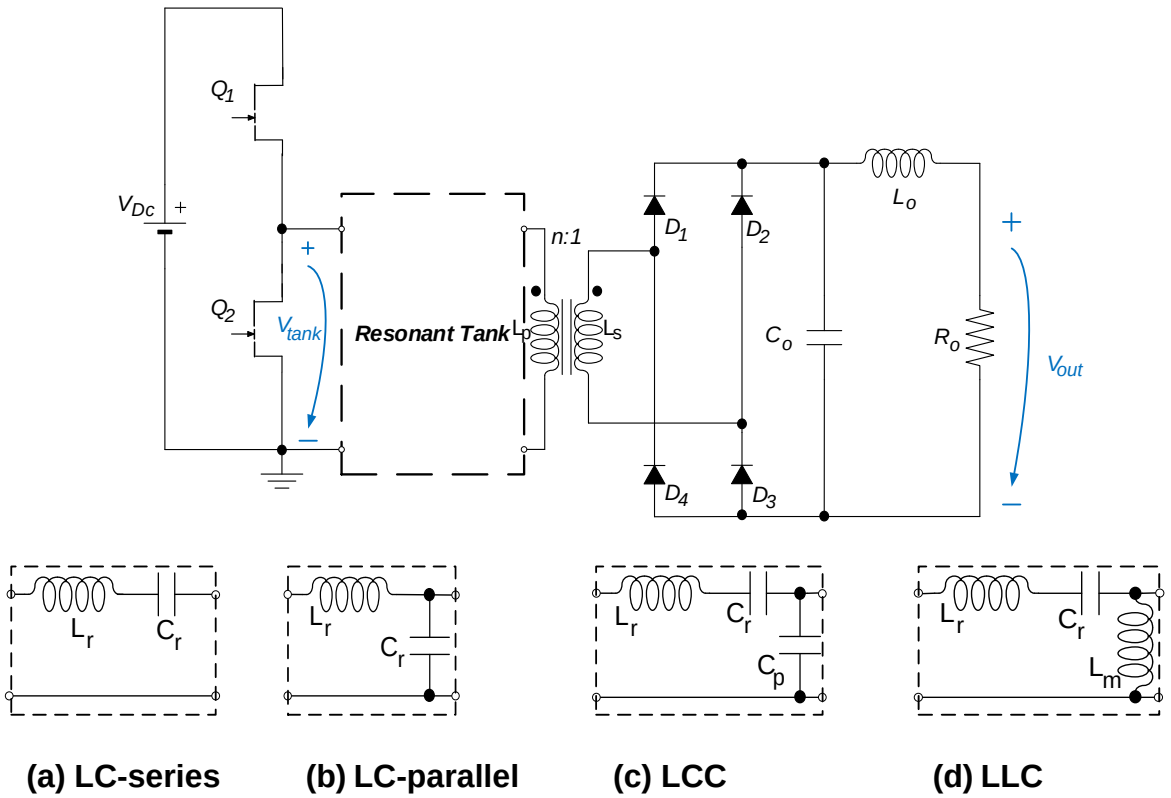


Figure 2.3 – Different resonant tank topologies applied to the half-bridge converter, with full-bridge rectification: (a) series resonant converter (SRC), b) parallel resonant converter (PRC), (c) LCC resonant converter, (d) LLC resonant converter

The LC-series have a series inductance (L_r) and a series capacitance (C_r) in series creating a high impedance tank, perfect for no load operation ($R \approx \infty$), (due the zero current in the resonant tank). The main problem with this topology, is operating with low output loads ($R \approx 0$), where due to the resonant tank dynamics, the voltage gain, cannot be higher than one. The LC-parallel solves the LC-series voltage gain problem, but as the resonant tank have in parallel the series capacitance C_r, at no load operation, there will be a high consumed energy in the resonant tank, resulting in in a negative impact to the. The LCC topology allows both low resonant tank impedance and voltage regulation at $R \approx 0$, but the integration of galvanic insulation between the input and the output of the converter, adds more components this topology. Even though the galvanic insulation is not critical for the converter operation, in terms of safety, it presents higher risks to humans, due to the lack of protection against the high voltage discharges if some of the component gets damaged. The LLC have the capability to use galvanic insulation, by replacing the magnetizing inductance (L_m) with the primary winding, as well the integration of the series inductance (L_r), with the leakage inductance (L_k) of the transformer. Doing this, less component (or smaller ones) will be present in the circuit, increasing the power density of the converter, and high efficiency either at overload operation ($R \rightarrow 0$ short-circuit), or at no load operation ($R \rightarrow \infty$, open-circuit), making this converter the best

candidate to be used in a battery charger. A study conducted in [7] details the different resonant tank topologies, where Table 2.3 shows the main aspects of each topology.

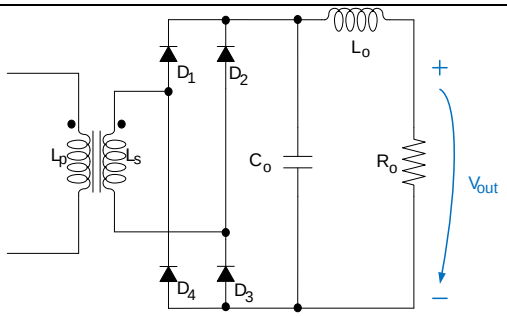
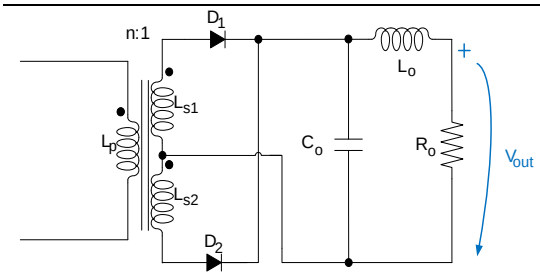
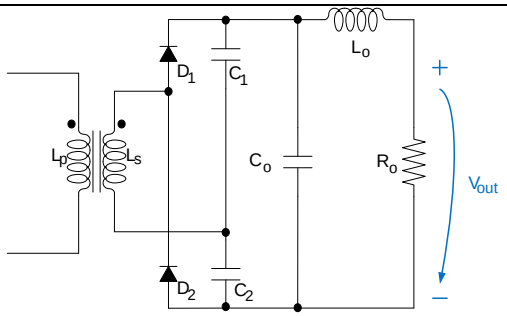
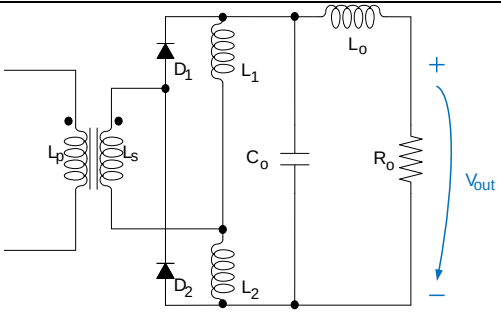
Table 2.3 - Comparison between the 4 types of resonant converters [7]

	LC SERIES	**LC PARALLEL**	**LCC**	**LLC**
Voltage gain (M_g)	$M_g \leq 1$	$M_g \geq 1$	$0 \geq M_g \geq 1$	$0 \geq M_g \geq 1$
ZVS	Possible	Possible	Possible	Possible
ZCS	No	No	Possible	Possible
Output regulation with load variation	Can´t regulate voltage with a lower ohmic load	Possible	Possible	Possible
Input impedance with no load	Very High	Very Low	High	High
Magnetic components integrated in transformer core	No	No	No	Possible
Losses at non-resonant operation	High switching losses	High switching losses, increasing as input voltage increase	High switching losses	Theoretically 0 switching losses, due to ZVS and ZCS

In order to stabilize the output voltage that comes from the resonant tank, and converting the AC component into DC, a High-Frequency Rectification block is needed. The most famous architectures for this block are the full-bridge converter, and the center-tapped.

The Full-bridge architecture consists of a single secondary winding attached to four diodes, conducting two diagonal diodes at the same time depending on the polarity of the applied transformer voltage, converting the negative semi cycles into positive ones. The output filter elements stabilize the voltage and the current turning it, into DC. The Center-tapped architecture uses the same concept but with a transformer with two equal secondary windings, having each winding connected to a rectifying element. Several options for the High-Frequency Rectifier block were investigated in [8] and [9], where Table 2.4 lists the advantages and disadvantages of each topology.

Table 2.4 – Different architectures for High-Frequency Rectifier Block

High-Frequency Rectifier Architectures	Advantages	Disadvantages
 **(a) Full-bridge output rectification**	• Simpler transformer assembly • Diodes with lower voltage rating • Suitable for high voltage/ low current output applications	• High Conduction losses • Added inductor increases the loss and complexity • Blocking voltage of diodes increased
 **(b) Center-tapped output rectification**	• Lower conduction losses • Only two diodes needed • Suitable for low voltage/ high current output applications	• Complex implementation due to multiple output windings • Diodes with higher voltage rating
 **(c) Voltage-doubler rectification**	• Suitable for high voltage output applications	• For high current output, the capacitors will be bulky for the demand output voltage ripple.
 **(d) Current-doubler rectification**	• Suitable for high output current applications	• Two added inductors resulting in higher power loss and complexity

This work will focus in the four most used architectures:

- Full-bridge LLC resonant converter with full-bridge rectification
- Half-bridge LLC resonant converter with full-bridge rectification
- Full-bridge LLC resonant converter with center-tapped rectification
- Half-bridge LLC resonant converter with center-tapped rectification

comparing their losses and the efficiency, when used in a $4.2\ kW$ battery charger.

2.3. Control Methods

As mentioned before different control methods can be used in DC-DC converters, among them:

- Pulse Width Modulation (PWM)
- Pulse Frequency Modulation (PFM)

The PWM control method is used in a great variety of applications. By modulating the pulse width, retaining the same frequency, the average value of the signal will vary, increasing or lowering the time that the switches are conducting. DC-DC converters that use these control method, usually have a lower cost and their application in circuit is simpler. Their problem is the relatively low efficiency at underload operation ($R > R_{nominal}$). Using PMW, when the output voltage needs to be lower, the pulse width will be shorter, but as the frequency remains constant, the switching cycles will be the same as when it is operated to obtain a high output voltage, lowering the efficiency at low outputs. In the case of PFM, if a lower output voltage is required, a lower frequency will be applied to the switches (maintaining the duty cycle constant), lowering the average value of the control signal that will lower the output voltage. The main difference when compared to PWM is that by reducing the frequency, there will be less switching cycles, obtaining higher efficiency when compared to PWM.

In order to exemplify, two similar DC-DC converters will be compared, where one uses PWM and the other PFM. Knowing that in every cycle there is a turn-on and a turn-off switching, and the number of periods is directly connected to the switching frequency, and the switching losses can be expressed as:

$$Switch_{Loss_{\text{periods}}} = Switch_{ON\,Loss} + Switch_{OFF\,Loss} \tag{2.1}$$

$$f_{sw} = n_{\text{periods}} \tag{2.2}$$

$$Total\ Switching\ Losses = n_{\text{periods}} \cdot Switch_{Loss_{\text{periods}}} \tag{2.3}$$

In order to the PWM converter lower the output voltage, the pulse width needs to shrink, keeping the switching frequency constant, while, in the PFM converter, the switching frequency needs to be reduced, maintaining the duty cycle (DT) at 50% rate. Knowing this, to get a lower output voltage in PWM and PFM the follow equations were obtained:

$$Vo_{PWM} \searrow \rightarrow DT \searrow \rightarrow Total\ Switching\ Losses \approx constant \quad (2.4)$$

$$Vo_{PFM} \searrow \rightarrow fsw \searrow \rightarrow Total\ Switching\ Losses \searrow \quad (2.5)$$

Figure 2.4 represents the efficiency curves as a function of the load current, for PWM and PFM control techniques. Both have similar efficiency at nominal operation, achieving a similar peak efficiency, but at lower load currents (meaning lower voltages maintaining the same load), PFM presents a wider operating range maintaining high the efficiency, validating (2.4) and (2.5)

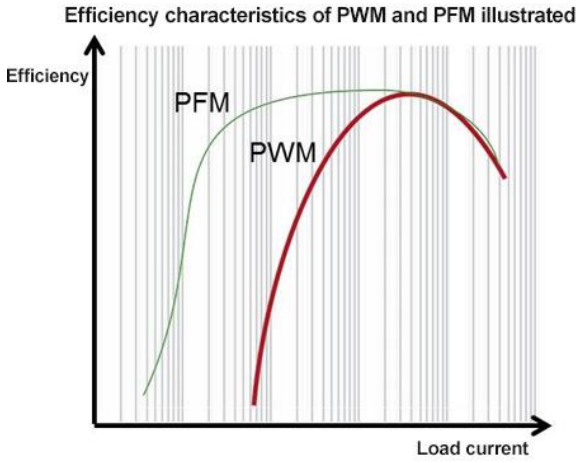
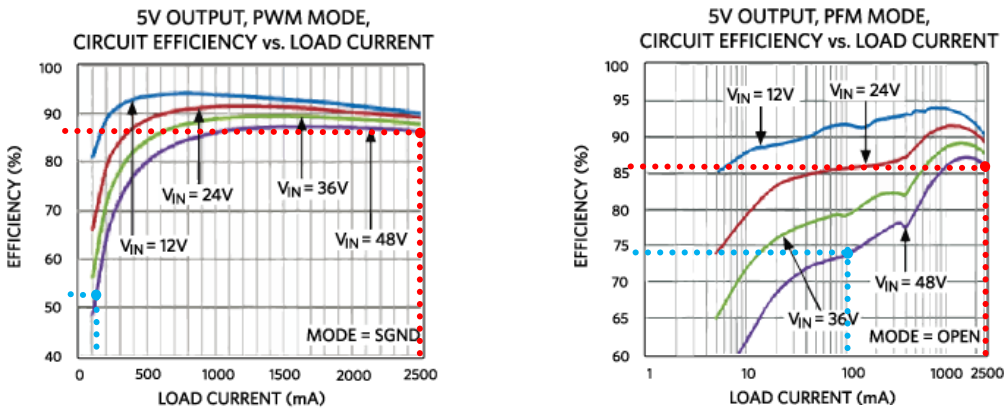


Figure 2.4- Efficiency over the load current of switching technics [4]

An experiment was conducted in [5] (represented in Figure 2.4), comparing two 120 W step down converters, one using PWM as a control method (Figure 2.5 (a)), and the other utilizing PFM (Figure 2.5 (b)).



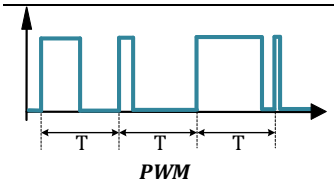
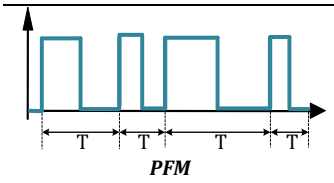
(a) (b)

Figure 2.5 PWM (a) and PFM(b) efficiency curves for the MAX17503 step-down converter [11].

At nominal operation ($V_{in} = 48\ V\ and\ Load_{current} = 2500\ mA$, marked with red doted lines) both converters show similar efficiencies around 88%, but at lower current loads like $Load_{current} = 100\ mA$ with an input voltage of $V_{in} = 48\ V$ (marked with blue doted lines), PWM obtained an efficiency lower than 50 %, while, for the same condition, PFM obtained an approximate efficiency of 74 %, representing an high improvement just by using a different control technique.

To summarize, Table 2.5 shows the key aspects of each control method, where PMW control, is simpler, have a low cost, work at high power levels, but having lower output voltages the efficiency will drop. PFM, have similar peak efficiency when compared to the PFM, but at lower output voltage, less commutations will happen, widening the efficiency, in the output voltage range. Nonetheless, PFM is more complex to use, requires a higher component number and usually have a higher cost.

Table 2.5- Switching mode technics [10]

	Frequency	Pulse Width	EMI	Switching losses	Driver	Cost
	Fixed	Variable	Predictable	High at low output voltages	Simple	Low
	Variable	Fixed	Hard to predict, due the variable frequency	Low	Complex	High

2.4. LLC Resonant Converter Optimization

Known for their soft-switching techniques, LLC resonant converters are capable to achieve high efficiency over the voltage gain range, with reduced switching losses, allowing higher operating frequencies, and minimization of the converter size. Those, gained renewed attention over the years, leading researchers to find new ways that could extract the full potential from this converter.

Even though high frequencies lead to converter minimization, extra stress will be applied to the inverter switches, the transformer, and the rectifying elements at the output, being the most critical points of the system [12] (Figure 2.6). To overcome that, new materials and techniques were tested, in order to have the full advantage of using high frequencies, without making a high trade-off with efficiency.

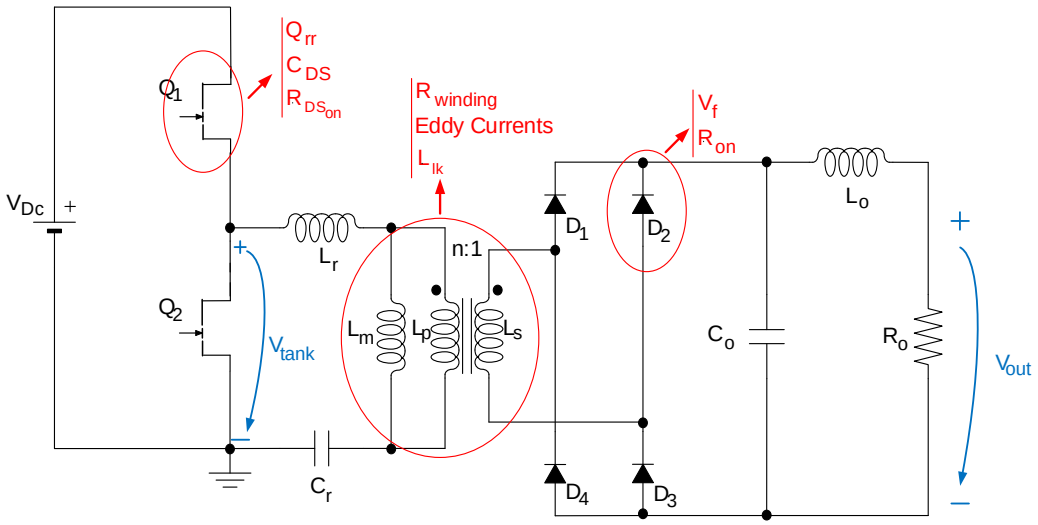


Figure 2.6 – Loss model power components in the LLC resonant converter, where Qrr is the reverse recovery charge, C_DS the switch drain to source capacitance, R_DS_ on the drain to source resistance at on state, L,lk the leakage inductance, Vf the diode voltage drop, and R,on the diode resistance when conducting

Replacing the Silicon devices with Gallium Nitride High Electron Mobility Transistors (GaN HEMT), allow an operation at higher frequency and higher power levels, with improved efficiency due to their better internal characteristics [13]. Also, to improve transformer, being one of the components that produce more losses in the converter, distributed air gapped core, interleaved windings, and *Litzendraht (Litz)* windings, allows a minimization of eddy currents, improving the overall efficiency of the converter.

2.4.1. Switch Selection

For many years Silicon (Si) was the base for the semiconductors. This semiconductor material is an abundant element in the world becoming very affordable for the productors to construct semiconductor devices. With the evolution of power electronics requiring lower conduction and switching losses, high voltage and the capability to hold high temperatures, silicon based semiconductors, reached their theorical limit, forcing researchers to find newer alternatives to keep the improvement in semiconductors area. [14]. Wide band-gap materials (WBG) such as Silicon Carbide (SiC) and Gallium Nitride (GaN), are two newer materials, that allow “a better performance in terms of higher blocking voltage capabilities, faster-switching speeds, high-temperature operation, and lower on-state resistance (Figure 2.7) [15].

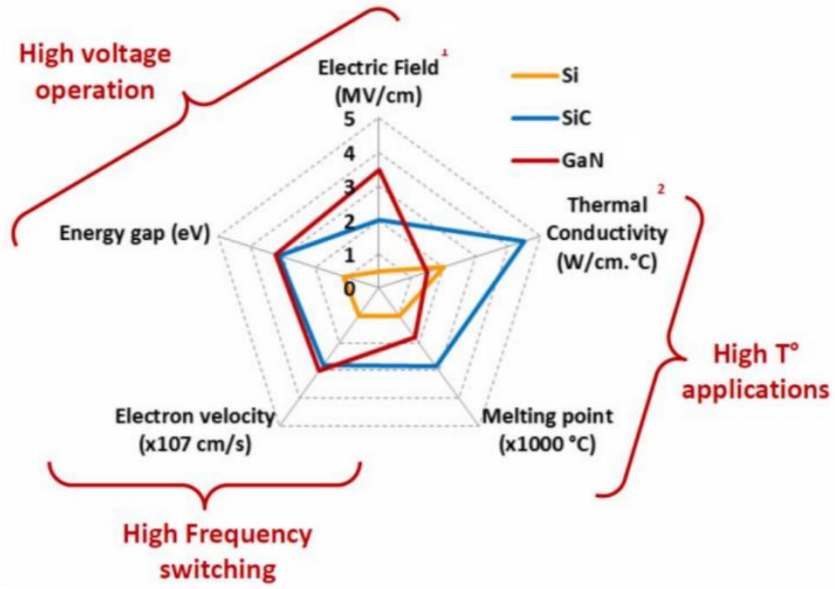


Figure 2.7- Key characteristics of GaN vs Silicon Carbide (SiC) vs Si [16]

GaN HEMTS have some similarities to Si MOSFETs when their structures is compared. Both use the same pads nomenclature (Gate, Drain and source), have parasitic capacitances between the different substates, and behaves like a Switch when a control signal is applied to the Gate. The fundamental advantage of Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) over their competitors, is the lower gate charge (Q_G), allowing lower dead-times, lower resistance $R_{DS_{on}}$ improving the conduction losses, and lower drain to source capacitance C_{DS} (sometimes called C_{oss}) permitting the operation at higher switching frequencies. In [15] three similar $15\,kW$ buck converters where constructed, using Si, SiC and GaN semiconductors, and the final consusion was that “GaN has higher efficiency due to its lower conduction, switching losses and the absence of the reverse recovery losses”, considering that “GaN can be used for high efficiency application such as Evs applications”.

GaN HEMTs have one main difference when compared to the regular MOSFETS, and that is the lack of the body-diode. MOSFET devices are mainly composed by p-type substrate, that is used to the body, two $n+$ type regions, for the drain and source, and an oxide layer on gate to induce an n channel into the p-type substrate, allowing the conduction between Source to Drain (Figure 2.8). Usually, MOSFETs have the body connected to the source to improve the device stability and performance [17], [18] as “leaving the body floating does complicate device behavior due to hysteretic, e.g., switching-history dependent, fluctuations in body charge” [19].

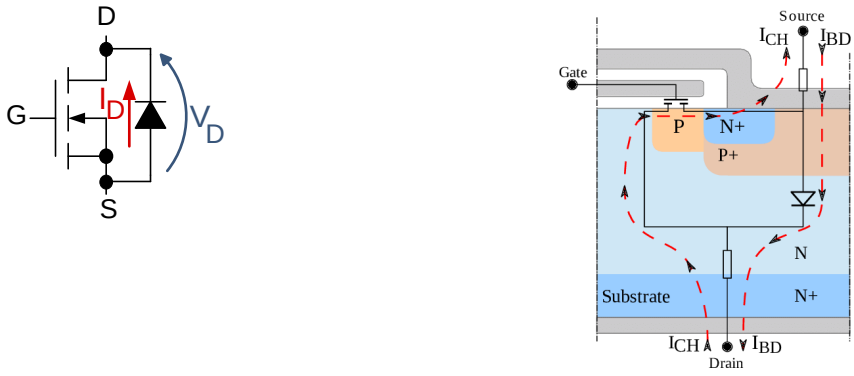


Figure 2.8 – a) Power MOSFET pinout diagram with body diode current I_D and body diode voltage V_D; b) Cross section of a power MOSFET, showing the IBD (body diode) and ICH (channel) current paths [20]

By connecting the Body with Source path, a pn junction will be formed, creating the parasitic diode called body-diode, that generates considerable loss during reverse recovery [21] [22]. When a diode switch from forward conduction to reverse conduction (Figure 2.9) the current I_D will decrease reaching a negative value called I_{RM} (maximum reverse current), and the diode forward voltage V_f ($t_1 - t_3$) is maintained. Reaching I_{RM}, current will increase until it reaches $0\,A$, resulting in a voltage oscillate until it reaches the reverse voltage, being this point where the diode is considered completely off.

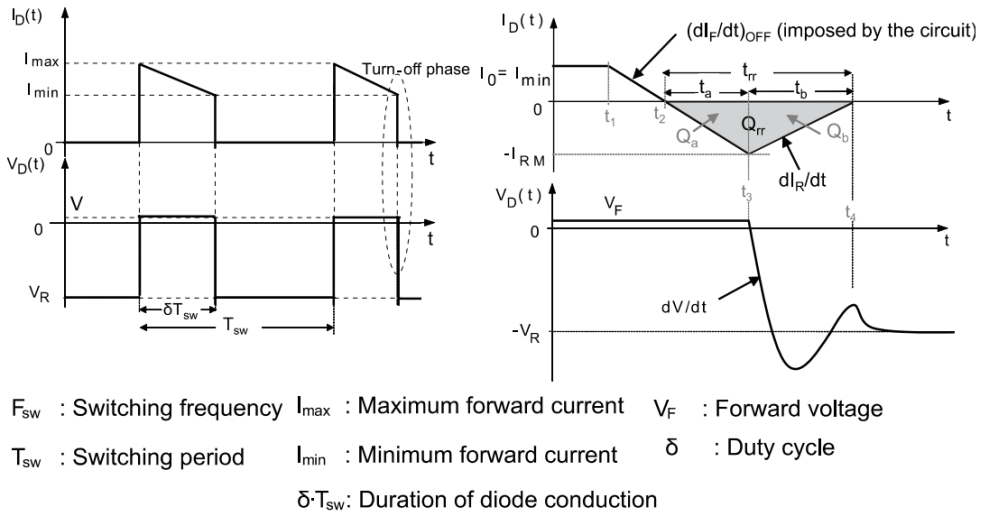


Figure 2.9 – Current and voltage waveforms of a diode during turn-off phase, adapted from [22]

T_{rr}, can be defined as the reverse recovery time, being it the sum of t_a(the time that current takes, when it reaches $0\ A$ for the first time until it reaches I_{RM}), with t_b(the time that current takes, from I_{RM} untill it reaches $0\ A$ for the second time), and the diode turn off power loss that could be expressed as [22]:

$$.P_{d_{Sw\_off}} = \int^{T_{rr}} v_d(t) \cdot i_d(t)\, dt \cdot f_{sw} \tag{2.6}$$

GaN HEMT devices do not have a body-diode, meaning no reverse recovery, but still have the capability to reverse conduct. Without detailing its chemical structure, enhancement mode GaN HEMTs (being the most similar ones when compared to Si MOSFETs, as they are normally off devices) have a two-dimensional electron gas channel (2DEG) forming a channel between the GaN layer and the AlGaN (Figure 2.10). When fluorine atoms are implanted into the AlGaN layer, it is possible to hold some negative charges depleting the 2DEG

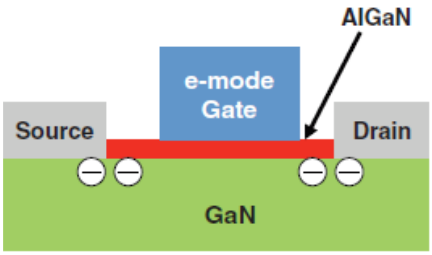


Figure 2.10 – Structure of an e-mode GaN HEMT [23]

When the GaN E-HEMT is forward conducting with a positive V_{GS}, it performs like a typical MOSFET, with better switching performance, but when $V_{GS} \leq 0\ V$, 2DEG starts to conduct. Detailed in Figure 2.11, when a reverse voltage is applied to an HEMT or a MOSFET, it will reverse conduct (with the gate at off-state) if V_{DS} is higher in module, than the body diode voltage V_D that in case of MOSFET is approximately 0.8 V. The main downside of GaN E-HEMT not having a body diode, is their higher reverse voltage drop V_{VD}, being it defined as:

$$V_{VD} = I_{SD} \cdot R_{DS_{ON}} + V_{TH} + V_{GS(OFF)} \quad (2.7)$$

where I_{SD} is source to drain current, $R_{DS_{ON}}$ the drain-to-source, V_{TH} the threshold voltage drop of 2DEG, being approximately $1.3\,V$, and $V_{GS(OFF)}$ the negative voltage applied to gate-source [24]. Having higher V_{VD} leads to higher reverse conduction losses, being those easily fixed by lowering the dead time [25]

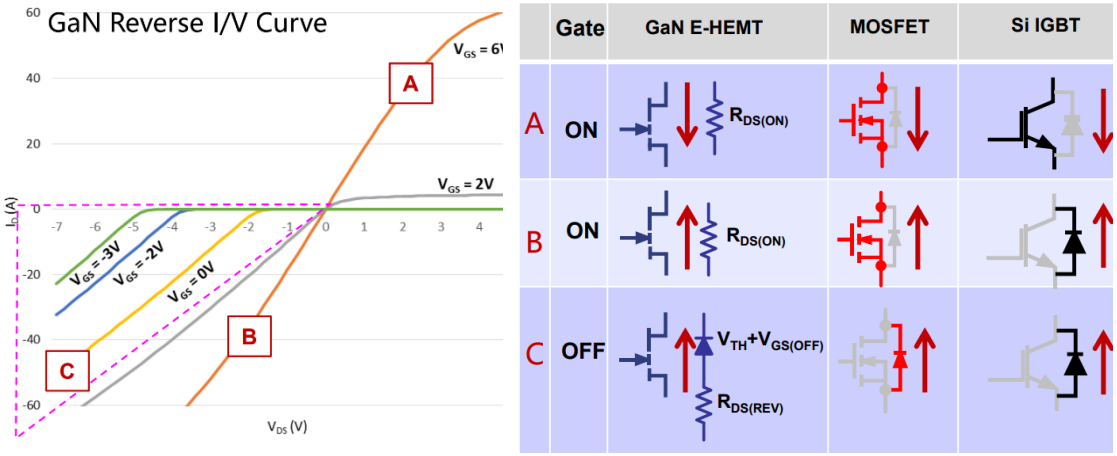


Figure 2.11 Operation modes of GaN E-HEMT depending on gate and current condition [26]

2.4.2. Magnetic Components Performance

Resonant converters are composed by one or more magnetic components, being them inductances and a transformer. By using the magnetic field it is possible to provide filtering, and transfer energy from one winding to other winding. Modern DC-DC converters use high frequency to reduce the size of the passive components and improve the power density, but higher losses in the magnetic components will appear, due the higher effect of eddy currents, becoming a significant problem [27]-[29]. In the LLC converter, several magnetic losses can be analyzed, being them separated in winding losses and cores losses.

1) Winding Losses

In a transformer, when several turns from the same winding are overlapped, a concentrated magnetic flux will be generated, concentrating the magnetomotive force (MMF) in one spot near the last turn of primary winding, and the first of the secondary winding. Due to this this high concentration, some of the flux will leak from the core to the air, winding layers, and insulators, being known as leakage flux, causing an imperfect coupling.

The leakage flux can be represented as a leakage inductance L_k (equated in (2.8)), storing some of magnetic flux [30].

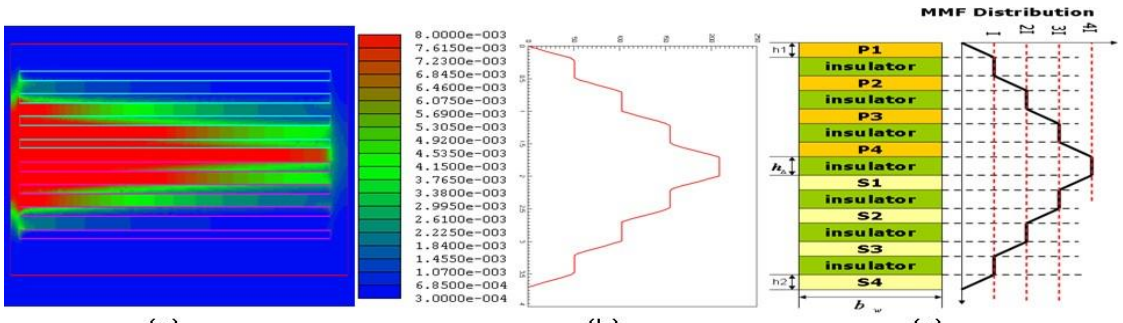
$$L_k = \mu_o \cdot \frac{I_w}{b_w} \cdot \frac{N^2}{M^2} \cdot \left[\frac{\sum x}{3} + \sum x_\Delta\right] \tag{2.8}$$

where μ_o is the magnetic permeability of free space equal to $\mu_o = 4 \cdot \pi \cdot 10^{-7}\ \mathrm{H/m}$; I_w is the length of each turn; b_w is the width of each turn; M implies the number of the winding interleaved multiples; $\sum x$ is the sum of all section dimensions perpendicular to the section interfaces; $\sum x_\Delta$ is the sum of all inter-section layer thickness

Even though leakage inductance can play the role of series inductance in the resonant converter reducing the number of physical components [8], a reduction in the efficiency would be obtained, when the energy stored in the leakage inductance is dissipates through the switches [31]. Leakage inductance can be influenced by 4 main parameters:

- Winding distribution
- Permeability of the copper and the insulator
- Length and width of conductor
- Transformer core geometry

To overcome this, researchers tried new winding configurations. Analysis made in [8] and [30] shows several proposed windings, (represented in Figure 2.12, Figure 2.13 and Figure 2.14) where primary and secondary windings have different interleaved configurations, dividing the windings into segments, wounding alternately each layer or each winding, until all the layers are completely stacked in the core. Different windings result in different energy distribution patterns with less concentrated flux spots, reducing leakage, and thermal energy made from the excessive flux. According to [30] P-S-P-S winding arrangement, had 17.5 times lower leakage inductance ($14.3\ nH$) when compared to the non-interleaved structure ($252.2\ nH$), and was obtained less proximity effect, and a lower AC winding resistance. [32]



(a) (b) (c)

Figure 2.12 – Non-interleaved structure (a) Energy distribution in FEA 2D simulation (b) Magnetic field strength distribution in FEA simulation (c) Analytical MMF distribution [30]

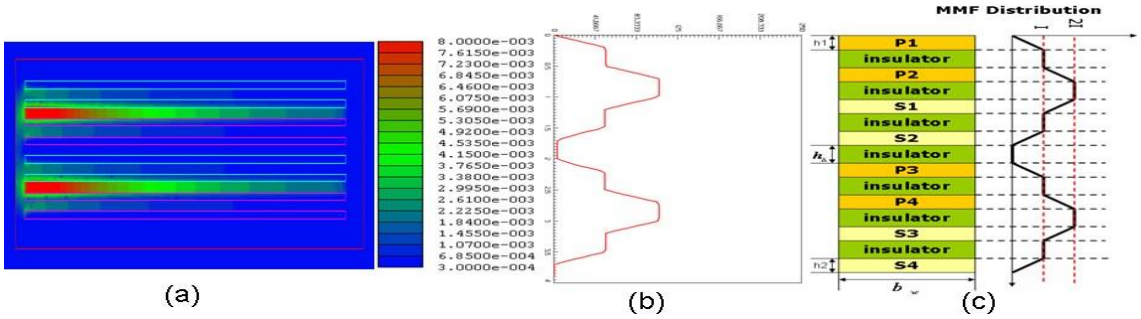


Figure 2.13 – P-P-S-S-P-P-S-S structure (a) Energy distribution in FEA 2D simulation (b) Magnetic field strength distribution in FEA simulation (c) Analytical MMF distribution [30]

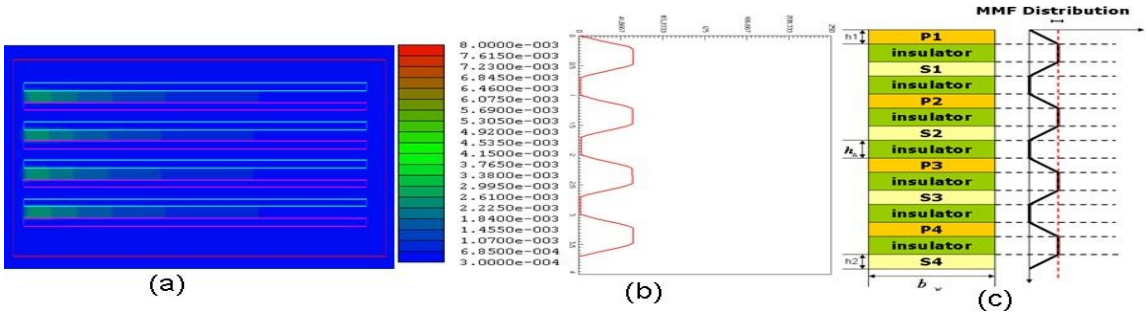


Figure 2.14 – P-S-P-S-P-S-P-S structure (a) Energy distribution in FEA 2D simulation (b) Magnetic field strength distribution in FEA simulation (c) Analytical MMF distribution [30]

One of the major causes of power loss in windings are skin effect and the proximity effect [27]-[29]. When AC current (I) flows through an electrical conductor, a magnetic field (H) will be generated around itself, inducing eddy currents loops (I_{Ed}). Shown in Figure 2.15, the eddy currents placed in the center of the conductor, have a opposite direction of the main current, slowing the current flow, while in the outside, both currents have the same direction as the current reinforcing the current flow.

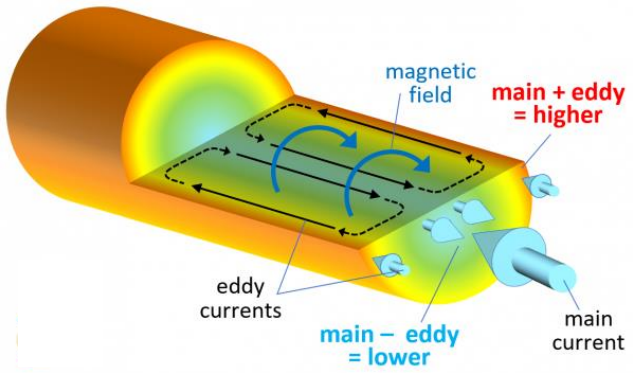


Figure 2.15 – Eddy current inside a round conductor and Skin effect [33]

Called skin effect, this phenomenon causes lower current density inside the conductor, reducing the useful area of the conductor (Skin depth δ_o), resulting in a increment of the AC resistance R_{AC}

Using (2.9) the skin depth can be obtained,[34]

$$\delta_o = \frac{1}{\sqrt{\pi \cdot f_{sw} \cdot \mu_o \cdot \sigma}} \tag{2.9}$$

where σ is the conductivity of the conductor material.

It is known that, when an alternating current flows through one conductor, a magnetic field around itself will be created, inducing eddy currents into the adjacent conductor. When two nearby conductors carry current in the same direction, the magnetic field from conductor 1 will induce eddy currents into conductor 2 (and vice-versa), concentrating current density in the farthest area of the conductor (Figure 2.16). This effect it is called proximity effect, and happens in the windings of transformers and inductors

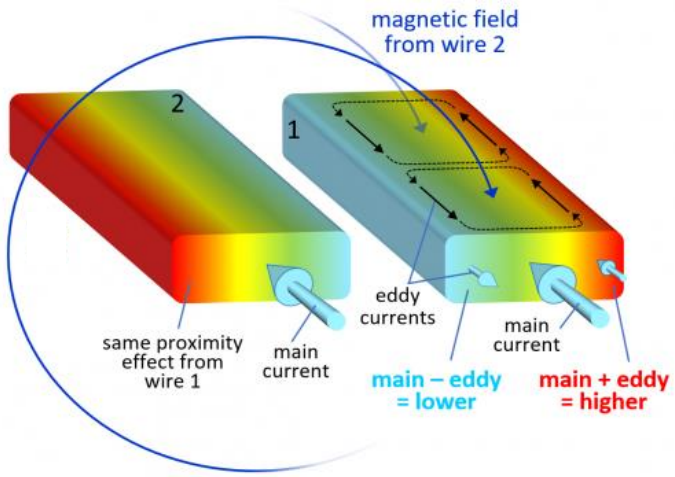


Figure 2.16 – Proximity effect of two adjacent square conductors copper foils carrying currents in same direction [33]

By replacing the solid wires with stranded Litz wire, it is possible to mitigate the skin and proximity effect. This type of wire is made by twisting several insulated tinner wires within each others, making one single strand, reducing the skin depth, minimizing the eddy currents, lowering R_{AC} resulting in less coper losses, even though the twisted strand becomes longer than with higher DC resistance R_{DC}, than a solid straight wire

2) Core Losses

In addition to the losses in the transformer winding, the used magnetic core material, has also a considerable influence. Caused by the B field, that magnetize and demagnetize the core, there are constant changes in module and direction of the magnetic flow lines, generate friction of the molecules in the core and joule losses are created. According to Steinmetz equation (2.10), the losses produced by the core, are directly connected to the frequency

$$P_{core} = K_h \cdot f_{sw} \cdot A_c \cdot l_c \cdot (B_m)^{1.6} \quad (2.10)$$

where, K_h is a Hysteresis constant (4.44 for a sine voltage), A_c the cross-sectional area of the core, l_c the length of the core, and B_m the maximum flux density [35].

The core of the transformer acts like a direct path of magnetic flux from the primary to the secondary windings. Considering a battery with a load $R_o = 0\,\Omega$, (short circuited), current will tend to be infinite saturating the conducting wires with excess of current. To control this current, a resistance in series with the output load can limit the current, allowing the conducting wires handle the amount of current that flows through it. The same effect happens to the transformer core, where the winding act as a power supply, the core as the current path, and the air gap being the resistance that will control the maximum flux, preventing it to reach saturation [36]. The general rule of air gapped transformer is to have twice gap size between the core and the windings (which leads to higher transformer volumes) [37] in order to limit the impact of the fringing flux in the closest areas, generally the windings, Figure 2.17. Eddy currents will be induced within the winding turns close to the air gap, increasing the R_{AC}, and creating thermal hotspots in the transformer.

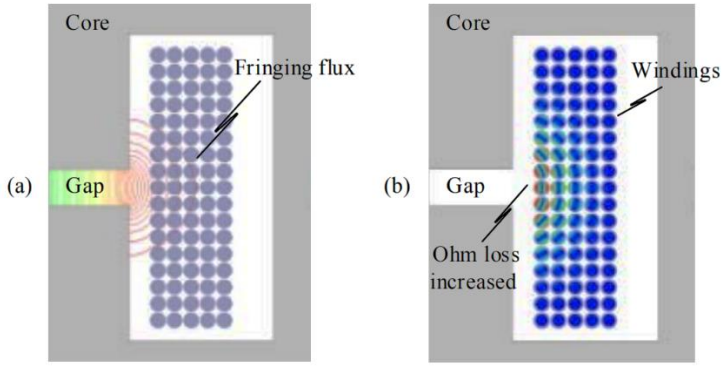


Figure 2.17- Fringing field and winding loss in conductors near the air gap: (a) magnetic flux around the air gap; (b) ohm loss distribution in the windings [8]

To mitigate this effect, two different solutions can be used, considering some changes in the transformer air gap:

- Powder Gap Core
- Quasi Distributed Air Gap Core

•Powder Gap Core

Conventional transformer uses an air gap, to prevent saturation, by adding a reluctance (which have a low permeability), however fringing flux will be produced near the gap. To control that, [42] compared two similar cores, one using a single airgap, and the other using a center leg made from nanocrystalline iron core with $KoolM\mu$ sendust, forcing the flux to stay inside the core material. Every particle of $KoolM\mu$ sendust is chemically insulated creating a small air gap between every particle making a distributed air gap [43]. As final result, the powder Gap Core obtained a fringing effect at the air gap multiple times lower when compared to the air gap transformer, at similar operation ranges, claiming the author that the hotspots are eliminated when this design is used.

•Quasi Distributed Air Gap Core

Like the windings structure, having a concentrated magnetic flux spot, result in lower skin depth, that increases the AC resistance, and total losses. By having reduced uniformly distributed air gaps (keeping the total gap width for the same inductance), the fringing field will be uniformly distributed with a lower intensity (illustrated in Figure 2.18), in every air gap spot, decreasing the induced eddy currents, R_{AC} and joule losses [38].

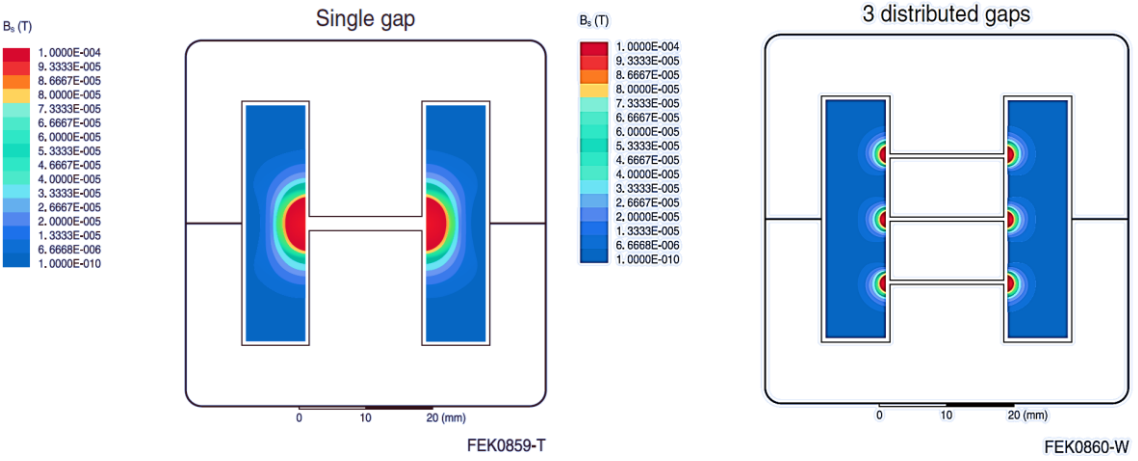


Figure 2.18- Hot spot comparison in the winding area between cores with single air gap and 3 evenly distributed air gaps [8]

Studies made in [38]-[40], compare single air gap vs multiple air gaps, concluding that distributed air gap, can reduce the fringing field up to 70 % as well a reduced heat generation, but according to [37] there will be an uneven flux density distribution, limiting the power density of the magnetic components [41].

2.5. LLC Resonant Converter for lithium-ion battery charger

Lithium-Ion batteries have been considered the best choice for mobile applications like Cameras, Laptops, Electric-Vehicles, due to their high capacity and low volume [45]. When the lithium-ion battery pack discharges (meaning that the chemistry in the neutralized [46]) an external voltage supply its needed, to make the negative electrode attract the lithium ions until the chemistry is neutralized again and the cell fully charged [47]. To do this charging process, different processes can be used. From the simple noncontrolled supplies charging at a constant current, to more complex, using converters that control the applied voltage and current to ensure a safety, a efficient charge and a long battery life.

LLC resonant converters are known for their lower switching losses, high power density and high efficiency converter, amount other characteristics [48], being used over the years in DC-DC conversion. The present work, will continue the study made in [1], using the LLC resonant converter as a DC-DC charging circuit for a $4.2\ kW$ battery charger, shown in Figure 2.19.

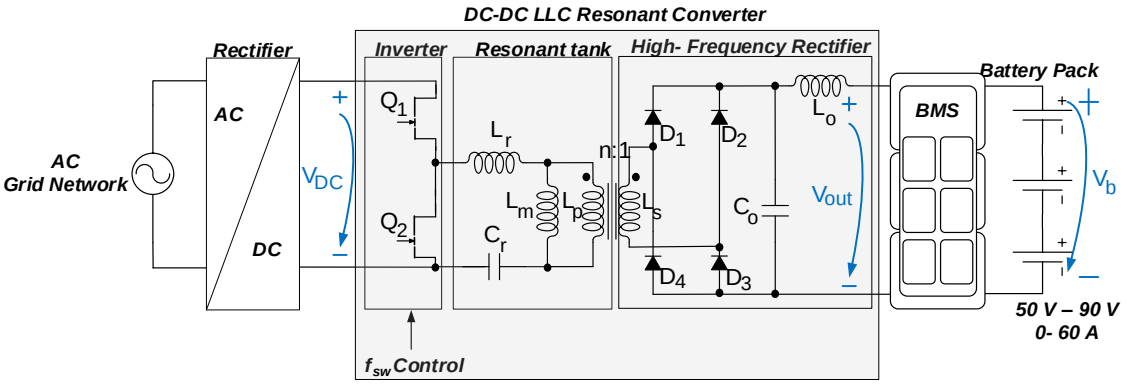


Figure 2.19 – Battery charger base structure using resonant converter.

The charging process is mainly composed by three stages. The charging station, being it a AC-DC converter, that converts the grid AC voltage to DC, followed by DC-DC converter, and the Battery Management System, to supply a controlled charge to the battery pack. BMS is not a mandatory device, as the Lithium-Ion battery could be charged using the Constant-Current/Constant-Voltage (CC-CV) charging, but this method apply a constant current and the constant voltage, to the whole battery pack making some of the cells “susceptible to certain risks such as overheating, over-voltage, deep discharge, over-current

and pressure or mechanical stress" [49], damaging the battery pack (Figure 2.20).

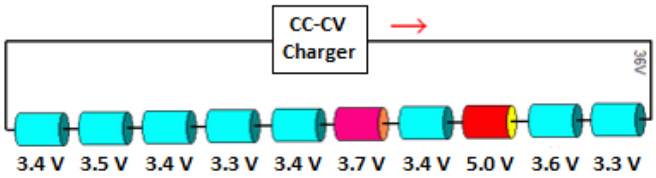


Figure 2.20- Charging using CCCV, resulting in overcharged cells [50]

By analyzing each group of cells (Figure 2.21), when one of the groups presents high temperature, overvoltage or any imbalance that may exist, the charge to the defective cell group will be stopped, being it restored when the defective group is stable again. As the BMS constantly monitors the battery ensuring safety and protection to the cells, and a longer battery life, some other parameters can be added. Safety controls, alarms, and the State of Function in the form of State of Charge (SoC) and State of Health (SoH) are some of them.

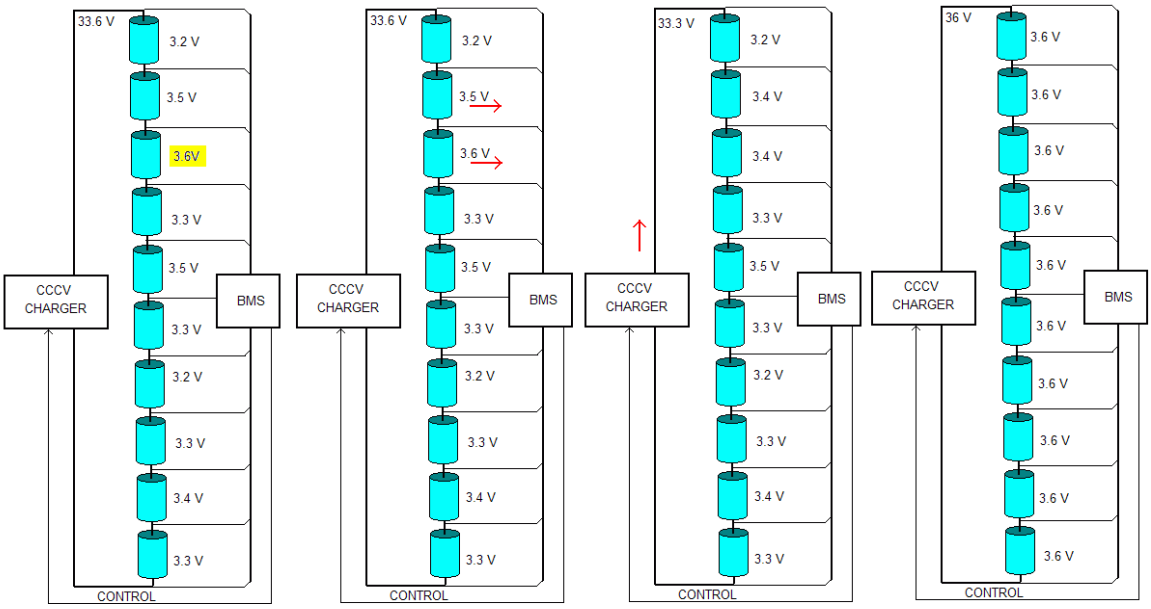


Figure 2.21- Charging with a BMS controlling the charger [50]

According to [50] a regulated charger is not mandatory, as long the BMS controls the charging process, meaning that the converter could be projected to work at the maximum efficiency zone letting the BMS handle the charge. But, by doing this extra stress would be applied to the BMS, causing high current spikes to the battery, if the BMS is not fast enough to control the charging current that is provided to the Lithium-Ion cells.

This work will mainly focus in the LLC converter, modeling the charging station as a DC supply voltage (V_{DC}) with an input voltage of 600V DC, and the BMS and the battery pack as an equivalent resistive output load R_o obtained by $R_o = \frac{V_{b_{nominal}}}{I_{b_{nominal}}}$ assuming the BMS as a perfect model without losses associated in

it. The key aspect of the work will be the performance enhancement of the converter taking in account the previously detailed point.

CHAPTER 3. Analysis of the LLC Resonant Converter and associated losses

In this chapter the LLC resonant converter will be present, analyzing the principle of operation and the design of a $4.2\ kW$ lithium-ion battery charger using the LLC resonant converter (suitable for higher power applications). To finalize this chapter an estimated efficiency of the base design will be calculated using analytical equations to calculate the losses of the different blocks of the converter.

3.1. LLC Resonant Converter for battery charging

Considering the constant-current / constant voltage (CC-CV) charging method, along the BMS to control the charge of the individual group of cells, the initial current will be at maximum value, increasing the battery voltage from the minimum to the near the maximum voltage, and then, this maximum voltage will be maintained, untill current reaches $0\ A$, letting the battery reach its maximum capacity.

Table 3.1 shows the main specifications considered for the LLC resonant converter, as well the characteristics of the battery bank.

Table 3.1 – LLC Resonant Converter and Battery Specifications

Description	Specification
Main Converter parameters	$590\ V_{DC} \leq V_{DC} \leq 600\ V_{DC}\ ;\ f_{sw} = 107488\ Hz$
Battery bank	$52.5\ V_{DC} \leq V_{out} \leq 82.5\ V_{DC}\ ;\ 0\ A \leq I_o \leq 60\ A;$

To improve the converter efficiency at CC-CV charging (Figure 3.1), in the inverter stage, full-bridge architecture will be tested, as well the center-tapped output rectification, with the main goal of lower circulating currents, decreasing the losses made by semiconductors, and the resonant tank elements. Being the switches in [1] already GaN HEMTs, a search for newer and more efficient devices will be made, replacing them with newer ones with have better internal parameters, Q_{rr}, C_{oss}, $R_{DS_{on}}$ in order to obtain lower switching losses, when the converter does not work at resonance, as well, reduced conduction losses at forward and reverse conduction. The transformer will be designed using the online tool named “Frenetic” optimizing the transformer. This tool “combines real analysis with trained AI models to deliver the most accurate predictions for temperature, leakage and RAC properties, among others” [44], offering the best prediction of the transformer, under the different operational points, and the

possibility to design the magnetic components with the best efficiency and power density. Knowing that the diodes have a voltage drop when are forward conducting (V_f) synchronous rectification (or active rectification) will be tested, using new wide band-gap semiconductors. The main goal of using synchronous rectification is to reduce the conduction losses present the high-frequency rectification block. The converter is projected to have either low output voltage with high currents, and high output voltage and low output current. The previous concepts will be tested, in order to see, the design that performer better in the total charge of the lithium battery pack

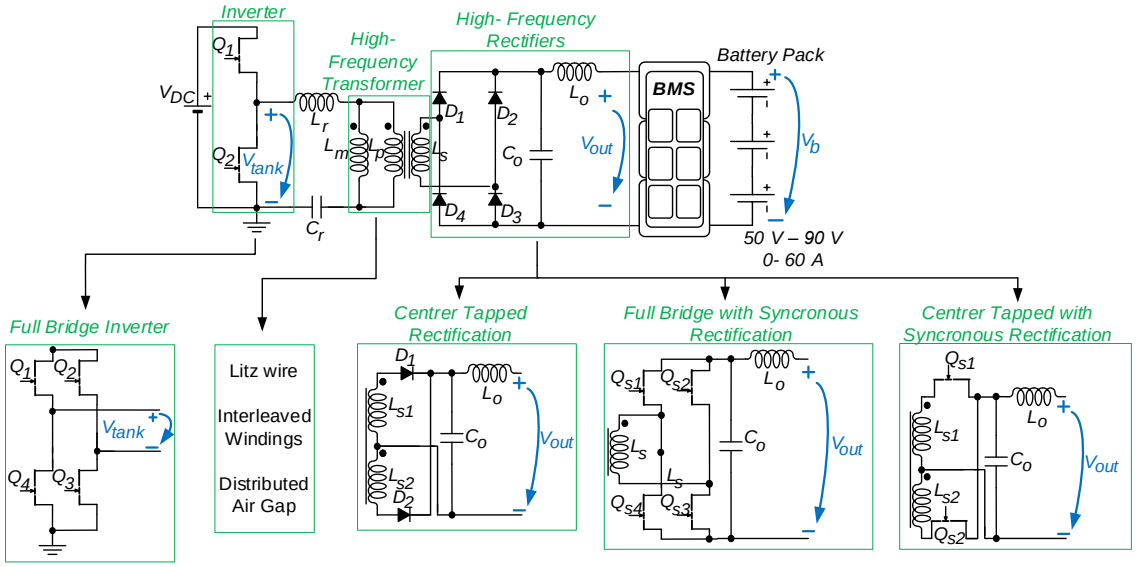


Figure 3.1 – Analyzed power blocks of LLC resonant converter for optimization improvement

3.2. LLC resonant Converter Topology

Represented in Figure 3.2, and previous analyzed in section 2.2 the LLC Resonant converter can be divided in 3 main blocks: Inverter, Resonant Tank and High Frequency Rectification.

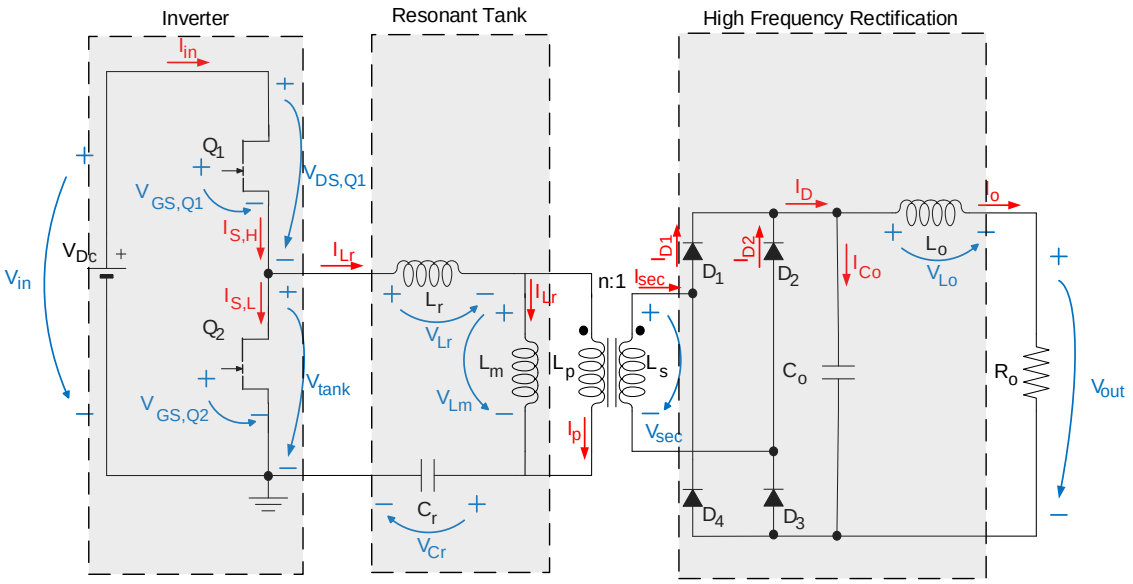


Figure 3.2- General configuration of insulated Resonant converters

Fed by the DC voltage supply V_{DC}, the Inverter block produce a square voltage wave (V_{tank}) using two E-GaN HEMT (being later called just HEMT for simplicity reasons) $Q1$ and $Q2$, with an operation rate of 50% each. The V_{tank} will be applied to the resonant tank (composed by series inductance L_r, magnetizing inductance L_m and series capacitance C_r), inducing a current in the transformer secondary side supplying the output load (R_o). Depending on the output load condition, two extreme operation modes can be reached.

When $R_o = 0\Omega$ (short-circuited), the output voltage of the transformer will be constant, clamping the primary side voltage. This leads to a resonance frequency, f_o (equated in (3.1)) that considers the series inductance L_r, and the series capacitance C_r. This frequency is the one that is normally attributed to a resonant converter, having the output voltage equal or less than input voltage.

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}} \tag{3.1}$$

The other mode is when, $R_o = \infty\ \Omega$ (open circuit), where L_r will be in series with L_m resulting a resonance frequency f_p (3.2) that consider all the three passive components L_r, C_r, and L_m, resulting in a output voltage that is higher than input voltage [53] [54].

$$f_p = \frac{1}{2 \cdot \pi \cdot \sqrt{(L_r + L_m) \cdot C_r}} \quad (3.2)$$

By modulating the frequency in the resonant tank square wave (V_{tank}), the harmonic filtration will be changed, as well the voltage gain (Figure 3.3 a)), leading to three possible operation regions: [55]

- Under Resonance (Capacitive region ($f_{sw} < f_o$))
- At Resonance (Resistive region ($f_{sw} = f_o$))
- Above Resonance (Inductive region ($f_{sw} > f_o$))

When the converter operates in capacitive region (Figure 3.3 b)) the series current I_{Lr} will be delayed, when compared to square wave V_{tank}, forcing Q1 HEMT reverse conducting, (increasing conduction losses). As I_{Lr} reaches I_{Lm} before the ending of switching period, load current will reach zero earlier, obtaining zero current switching (ZCS). Higher gain can be obtained by operating in this mode, increasing the output voltage

At Resistive region (also called resonance, illustrated in Figure 3.3 c)), the sum of passive components impedance will be null, having the series current I_{lr}, in phase with V_{tank}, (Zero Phase Angle (ZPA)) leading to a current that is almost sinusoidal at the output with a complete power delivery, and maximum efficiency.

Operating in inductive region (Figure 3.3 d)), I_{Lr} will be shifted over V_{tank}, and the current will not be totally delivered to the output, due the interruption to the start of the new cycle. Higher switch-off losses will be obtained as well hard commutation from the high frequency rectifiers.

The main difference between Capacitive and Inductive regions, is that in Inductive region, the current I_{Q1} will start negative, but will naturally evolve to zero, having a general controlled operation, while at capacitive region the current I_{Q1} starts positive, and will tend to minus infinite, making the switching off uncontrollable, being this the reason that its preferable the converter operate at resonant, or over resonance.

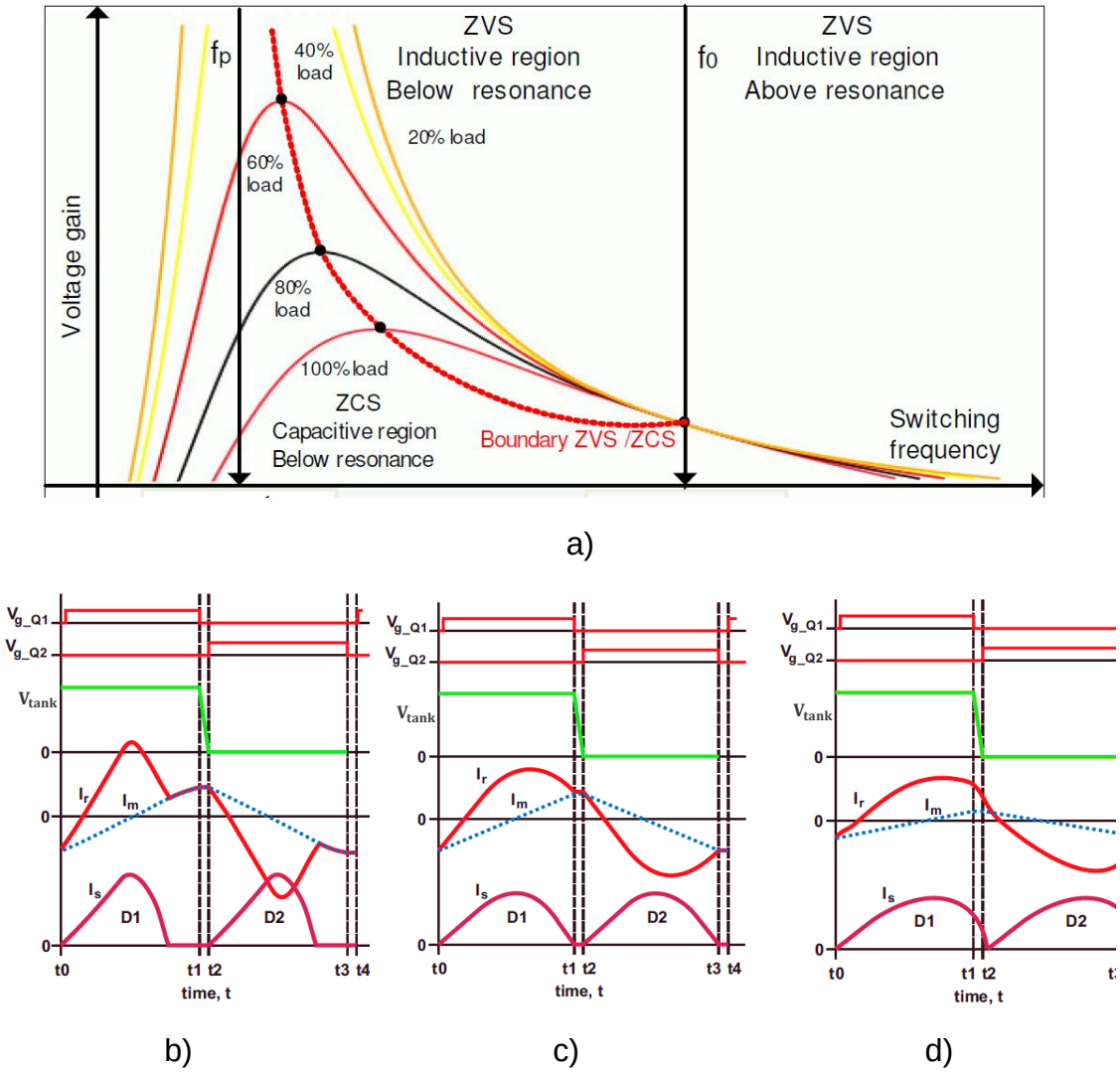


Figure 3.3 – a) Typical gain curves of LLC resonant converter for various loads, adapted from [45];Typical operation wave forms in: b) Capacitive operation; c) Resonant operation; d) Inductive operation, adapted from [56]

Receiving the AC current from the transformer secondary winding, the output diodes will convert the negative semi-cycles of the current, to positive, being it stabilized to DC with the LC filter (output capacitor C_o, and output inductance L_o) .

3.2.1. Operational principles of LLC Resonant Converter

Depending in the operation region, the LLC Resonant Converter, have several stages of power delivery. These converters, mainly operates in inductive regions, between $f_p > f_{sw} < f_o$, and $f_{sw} > f_o$, resulting in up to six stages of power delivery in one period, while if $f_{sw} = fo$ the mode 3 and 6 disappear [75] [76]. Figure 3.4, illustrates the several stages, as well the waveforms, considering previous normal operation.

Mode 1 ($t_a \leq t < t_b$): The first cycle begins with both switches turned off, at the dead-time zone, to allow the parasitic capacitance C_{DS} from Q_2 discharge from the previous cycle. Due the presence of negative energy, the "body diode" from $Q1$ switch will be forward- biased, making Q_1 reverse conducting until t_b.

Mode 2 ($t_b \leq t < t_c$): At t_b, switch $Q1$ is turned on, transferring I_{Lr} from the body diode to the switch, and gradually increasing I_{Lm}, transferring energy to the secondary side of the transformer. As $D1$ and $D3$ are forward-biased, they will conduct charging the capacitor C_o while the load is supplied with current I_o.

Mode 3 ($t_c \leq t < t_d$): When I_{Lm} equalizes I_{Lr}, the transformer will stop the energy transfer to the secondary side, interrupting the current that flows through D_1 and D_3. As the output capacitor C_o was charged by the previous modes, and diodes are reverse-biased, C_o will discharge only to the output load R_o.

Mode 4 ($t_d \leq t < t_e$): Like mode 1, the C_{DS} of switch $Q1$ will discharge using the positive energy present in the resonant Tank. Also, the "body diode" from $Q2$ switch will be forward- biased, making $Q2$ to reverse conduct until it reaches t_e.

Mode 5 ($t_e \leq t < t_f$): At t_e the Switch $Q2$ is at on state, restarting the energy transfer to the transformer secondary winging, making D_4 and D_2 direct-biased supplying the load with I_o.

Mode 6 ($t_f \leq t < t_g$): At t_f, I_{Lm} will be equalized to I_{Lr}, clamping the transferred energy from the transformer. Without current circulation through the secondary, C_o will discharge to the output load.

Due the presence of the parasitic output capacitance C_{DS},(discharging when on to off commutation happen), the dead time t_{dt} is required to prevent both switches conduct at the same time. By not having it, high current spikes would be obtained damaging the switching devices. If designed it is too high, the "body-diode" will have longer conduction times, negatively affecting the efficiency of the converter.

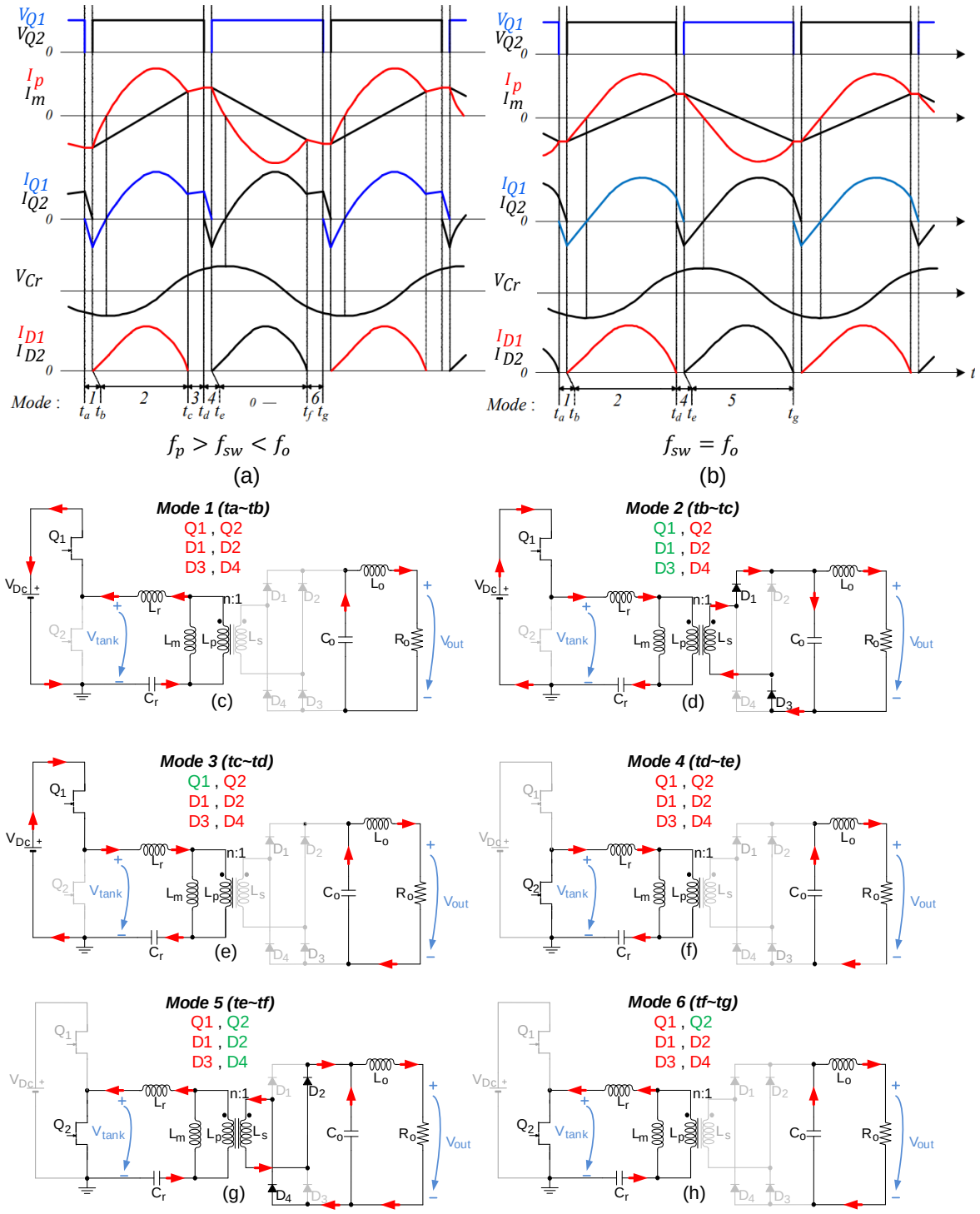


Figure 3.4 – Operation modes resonant tank; a) Mode 1 [t1~t2]; b) Mode 2 [t2~t3]; c) Mode 3 [t3~t4]; d) Mode 4 [t4~t5] and e) Typical waveforms of LLC resonant converters at resonant operation

3.2.2. Fundamental Harmonic Approximation Analysis

The resonant tank, define the behavior of the converter, but the calculation of the resonant component can be complex, making the design of the converter

a difficult task. By considering that the power transfer from the source to the load is mainly achieved by the fourier fundamental components of the currents and voltages, R. Steigerwald designed a simplified method using First Harmonic Approximation (FHA) (represented in Figure 3.5) that allows a faster design and evaluation of resonant power converters described in [55] [57].

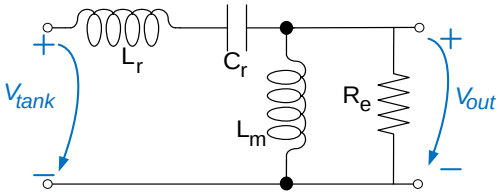


Figure 3.5 – Simplified LLC Resonant Converter under Fundamental Harmonics Appropriation

V_{tank} represents the square wave voltage that enters the resonant tank, and R_e the equivalent load (modeling the output rectification and R_o) equated in (3.3) [53]

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot R_o \tag{3.3}$$

where n represents the transformer ratio and R_o the output load (defined as $R_o = V_o/I_o$)

Three major factors dictate the converter normalized gain (M_G), and the gain bandwith:

- Quality factor Q_e
- Inductance ratio L_n
- Normalized Frequency f_n

$$M_G = \left| \frac{L_n \cdot f_n^2}{[(L_n + 1) \cdot f_n^2 - 1] + j[(f_n^2 - 1) \cdot f_n \cdot Q_e \cdot L_n]} \right| \tag{3.4}$$

Defined in (3.5) the quality factor describes, how fast the gain (from the resonant tank) drops when the switching frequency (f_{sw}) deviates from the resonant frequency (f_o).

$$Q_e = \frac{\sqrt{L_r / C_r}}{R_e} \tag{3.5}$$

The normalized frequency f_n , defined as $f_n = f_{sw}/f_o$, (where f_{sw} is the switching frequency and f_o the tank resonance frequency), dictates the relation between the switching frequency f_{sw} and resonant frequency demonstrating how far the operating frequency is from the main resonance frequency f_o. Having $f_n =$

1, is the same as $f_{sw} = f_o$, meaning resonance operation. Inductance ratio L_n (where $L_n = L_m/L_r$) describe the distance between the two resonant frequencies (f_o and f_p) and the gain bandwith. To illustrate the effect of the L_n, Figure 3.6 shows some gain plots for different L_n values, over the normalized frequency f_n. The lower the L_n value is, the higher the gain will be, with narrower range of the frequency modulation. This allows a more flexible control and regulation, being valuable in applications with wide input voltage range, however for the same resonant frequency, smaller magnetizing inductance L_m will be obtained causing, increased circulating energy and conduction losses.

Low L_n value:

➔Higher boost gain

➔Narrower frequency range

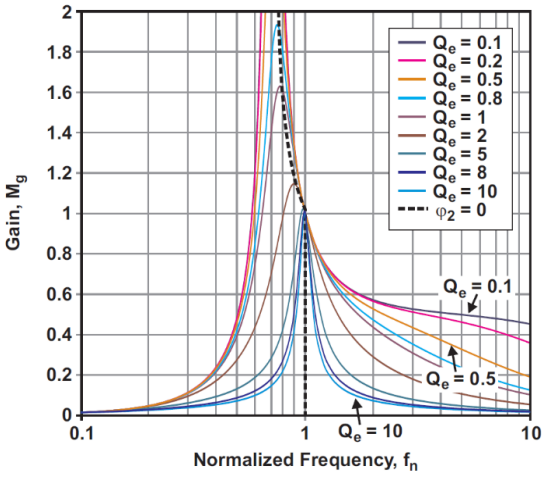
➔More flexible regulation

High L_n value:

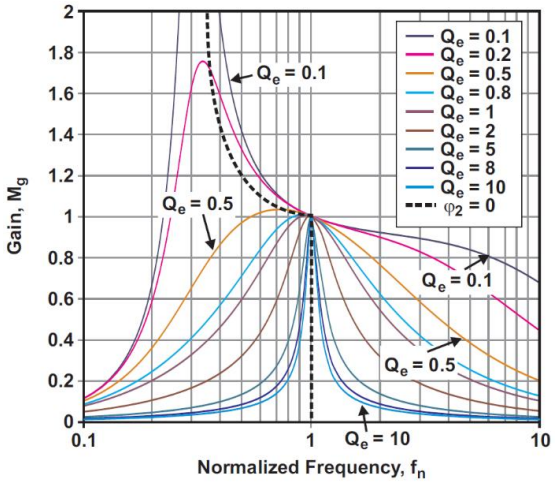
➔Higher magnetizing inductance

➔Lower magnetizing circulating current

➔Higher efficiency



a. $L_n = 1$.



c. $L_n = 10$.

Figure 3.6 – Gain plots with different Ln values keeping the same resonant tank

3.3. Design Steps of the LLC Converter

The most important step to get the converter working at best efficiency, is the design of it. Using the FHA approximation to determine the resonant tank parameters, three basic requirements must be known: nominal input and output voltage and current, line and load regulation and operating frequency.

Step 1- Transformer turn ratio

Considering all the necessary parameters, the first element to be calculated is the transformer turns ration n, where this will be the base set the converter gains. At resonance, gain will be unitary, and the output nominal voltage will be set by transformer ratio n, minus the overall losses on the converter (3.6) [1]:

$$n = \sqrt{k} \cdot M_g \cdot \frac{(V_{dc}/2)}{V_{o_{nom}} + V_f} \tag{3.6}$$

where k is the transformer coupling factor, M_g the gain of the resonant tank, which will be 1 (as the converter is designed assuming resonance), V_{Dc}, the converter input voltage, $V_{o_{nom}}$ the output nominal voltage and V_f is the voltage drop from the output rectifier diodes.

Step 2- Converter Minimum and Maximum gain

Assuming the input and output voltage variation, the minimum and maximum gain can be obtained using (3.7) and (3.8):

$$M_{g_{min}} = \frac{n \cdot (V_{o_{min}} + V_f)}{(V_{DC_{max}}/2)} \tag{3.7}$$

$$M_{g_{max}} = \frac{n \cdot (V_{o_{max}} + V_f + V_{loss})}{(V_{DC_{min}}/2)} \tag{3.8}$$

where V_{loss} is the assumed voltage drop due to power losses in the circuit.

Step 3- Inductance ratio and Quality factor

L_n, and Q_e are important factors and choosing them, can be a challenging. Usually as initial design, L_n, is fixed, (between 3-5 according to [58]), then Q_e is selected guaranteeing the minimum and maximum gains (exemplified in Figure 3.7, where Q_e needs to be 1.6). After the base design is made, L_n and Q_e can be iterared in order to achieve the maximum efficiency out of the converter

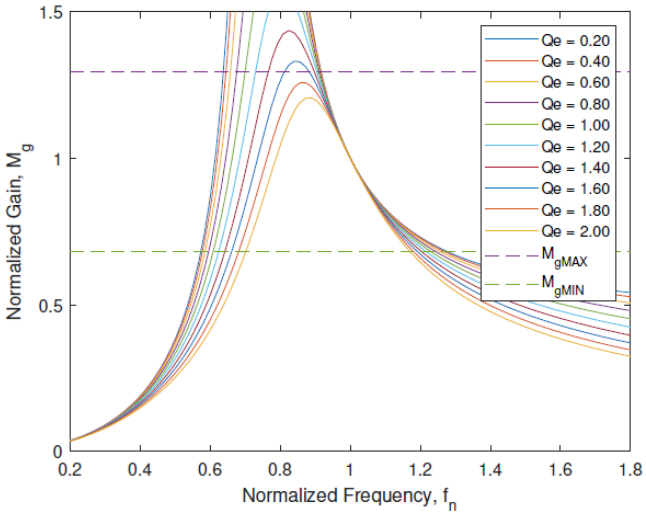


Figure 3.7- Quality Factor Curves over the Normalized Frequency [1]

Step 4- Determine the minimum and maximum frequency

After selected the quality factor curve with the previous calculated minimum and maximum gains, their associated frequencies can be calculated using (3.9) and (3.10)

$$f_{sw_{min}} = M_{g_{min}} \cdot f_{SW} \tag{3.9}$$

$$f_{sw_{max}} = M_{g_{max}} \cdot f_{SW} \tag{3.10}$$

Step 5- Resonant Tank Parameters

Knowing the turns ratio n, and the output load R_o (defined as $R_o = V_o/I_o$) the equivalent output load can be calculated (3.11), and with that calculate the resonant elements (3.12), (3.13) and (3.14)

$$R_e = \frac{8 \cdot n^2}{\pi^2} \cdot R_o \tag{3.11}$$

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_{sw} \cdot R_e} \tag{3.12}$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_{sw})^2 \cdot C_r} \tag{3.13}$$

$$L_m = L_n \cdot L_r \tag{3.14}$$

Step 4- Output Rectification Filters

The Output Filter elements are used in the converter output to stabilize the output voltage and output current, so the ripple does not exceed the maximum preset values at the beginning of the project. Filtering capacitance (C_o) and inductance (L_o) can be calculated by the following equations:

$$C_o \geq \frac{I_o}{8 \cdot f_{sw} \cdot V_o \cdot \frac{\Delta V_o}{100}} \tag{3.15}$$

$$L_o \geq \frac{V_o \cdot \Delta V_o}{I_o \cdot \Delta I_o \cdot 2 \cdot \pi \cdot f_{sw}} \tag{3.16}$$

where ΔV_o is the output voltage ripple.

Step 5- Dead-time of Inverter Switchs

Having all the converter parameters calculated, the required last step is the calculation of the minimum dead-time between the two control signals used in the inverter switches. To calculate the dead-time (t_{dt}), the following equation can be used:

$$t_{dt} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m \tag{3.17}$$

Table 3.2- Calculated LLC resonant converter parameters

Description	Specification
Nominal input and output voltage	$V_{DC_{nom}} = 600\ V_{DC}$ $V_{o_{nom}} = 76.5\ V_{DC}$
Resonant frequencies	$f_o = 107488\ Hz$ $f_p = 84978{,}3\ Hz$
Resonant tank characteristics	$Q_e = 1.6$ $L_n = 0.83$ $L_r = 41.149\ \mu H$ $C_r = 53.279\ nF$ $L_m = 34.154\ \mu H$
Transformer parameters	$n = 3.9032$
Output filter	$C_o = 105.1\ \mu F$ $L_o = 334.225\ nH$
Dead-Time	$t_{dt} \geq 13.8677 ns$

3.4. Design Losses overview of LLC Resonant Converter

Every component present in the circuit introduces losses to the system. In this subchapter the losses corresponding to the GaN HEMTs, the resonant elements, the high-frequency transformer, and the rectifying elements will be equated. Those equation allow us to obtain an approximated efficiency, when the converter operates near resonance.

3.4.1. GaN HEMT

The Inverter block is the first block of the converter, composed by two HEMT devices with four types of associated losses:

- Forward conduction losses ($P_{H_{Fw}}$)
- Reverse conduction losses ($P_{H_{Rs}}$)
- Switching losses ($P_{H_{Sw}}$)
- Driving losses ($P_{H_{Dr}}$)

1) Forward conduction losses

Forward conduction losses can be seen as the dissipated power in the forward conduction, described as:

$$P_{Fw,c} = {I_{DS_{rms}}}^2 \cdot R_{DS_{ON}} \tag{3.18}$$

$$I_{DS_{rms}} = \frac{I_{DS} \cdot \sqrt{DT}}{\sqrt{2}} \tag{3.19}$$

where, I_{DS} is the drain to source current (described as $I_{DS} = \frac{I_o \cdot \sqrt{2}}{n}$), $R_{DS_{ON}}$ the internal drain-source resistance and DT the Duty Cycle of the control signal applied to the HEMT. $R_{DS_{ON}}$ is directly connected to the working temperature of the HEMT, and will be as high as the temperature increase, (demonstrated in Figure 3.8). For calculation purposes, this value can be obtained, considering an operation at ambient temperature (25ºC).

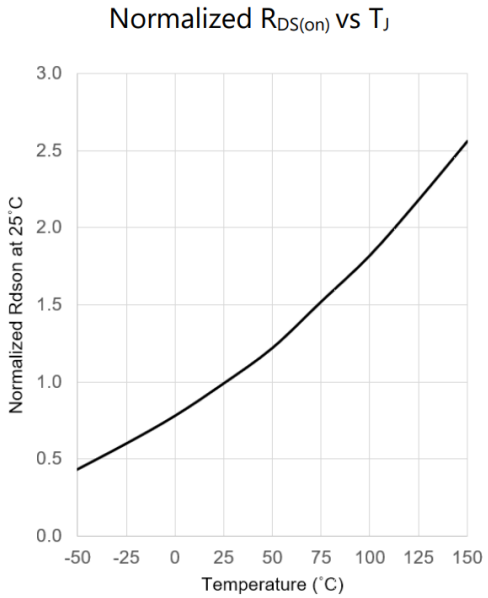


Figure 3.8- Relationship between RDS(ON) of GS66516T and temperature [59]

2) Reverse conduction losses

As mentioned before, GaN HEMTs do not have a body diode, but they still reverse conducting when:

$$V_{SD} > V_{GS(th)} - V_{GS(off)} \tag{3.20}$$

where V_{SD} is the Source to Drain voltage, $V_{GS(off)}$ the gate voltage, in off-state, and $V_{GS(th)}$ the threshold voltage typically around $1.3\ V$ at $V_{GS} = 0\ V$ [60].

When that happen, losses are made by the internal resistance, and by the threshold voltage. The reverse conduction losses can be described with the follow equation:

$$P_{H_{Rs}} = ((2 \cdot \left(V_{GS(th)} + I_{DS} \cdot\ R_{DS_{(ON)}}\right) \cdot I_{DS} \cdot\ t_{dt}) + {I_{DS}}^2 \cdot\ R_{DS_{(ON)}} \cdot T_{ON}) \cdot f_{sw} \tag{3.21}$$

where I_{DS} is the current that flows from drain to source, t_{dt} the time in seconds of the Dead-time, T_{ON} the turn-on-time, and f_{sw} the operating frequency.

3) Switching losses

Switching losses can be complex to calculate due to the lack of an accurate models, that allows an approximated calculation, since GaN devices are a recent technology with different properties when compared to the Silicon devices. Even though the design of the converter is considered to work at resonance for simplicity, the same does not happen in a real scenario, where the converter will operate in inductive region. This will produce switching losses and reverse conduction losses. Thankfully, ZVS technic minimize the turn-on losses, remaining only the turn off-losses, that happen, when the drain voltage overlaps with the source current of the HEMT, Figure 3.9).Using the model from GaN Systems in LTSpice software, it is possible to simulate the drain-to-source voltage and the drain current that flows thought the HEMT, integrate the product of both, and with that, obtain the turn-off losses of the produced by the HEMT (3.22).

$$E_{Sw\_off} = \int v(t) \cdot i(t)\, dt$$
$$P = \frac{E}{t} \qquad t = \frac{1}{f} \iff P = E \cdot f \tag{3.22}$$
$$P_{Sw} = \int v(t) \cdot i(t)\, dt \cdot f_{sw}$$

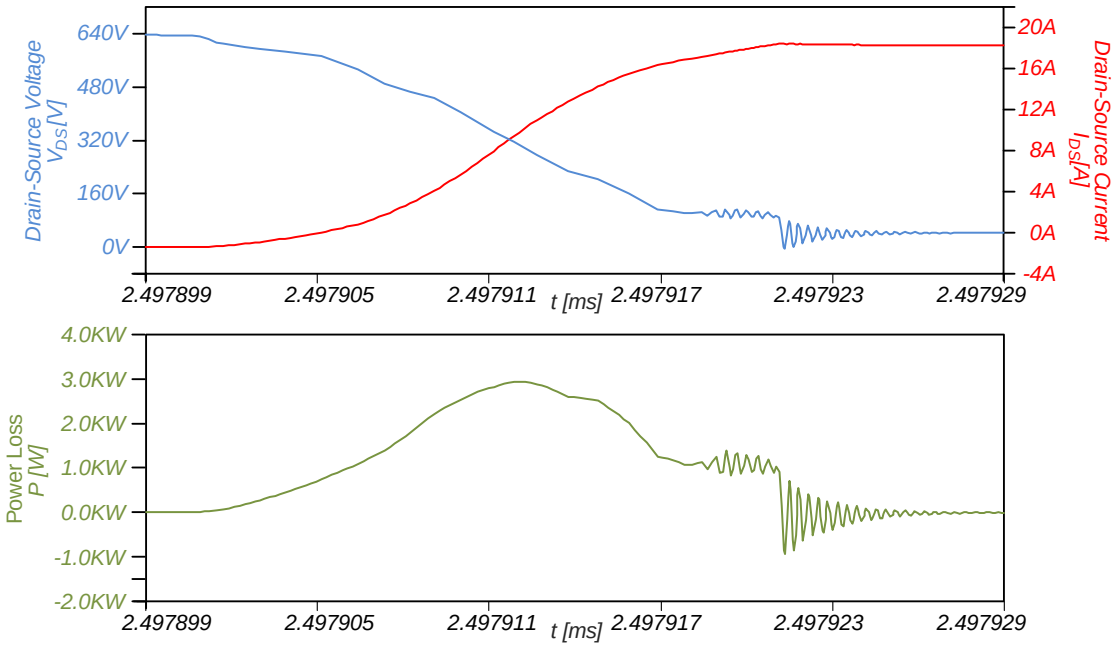


Figure 3.9- Switch-off waveforms of GaN HEMT under simulation

4) Driving losses

Due to the internal capacitances in the gate path of the switch (Figure 3.10) and the constant on and off commutations, the gate path will charge and discharger through the gate to source capacitance, and gate to drain capacitance of the HEMT, generating driving losses.

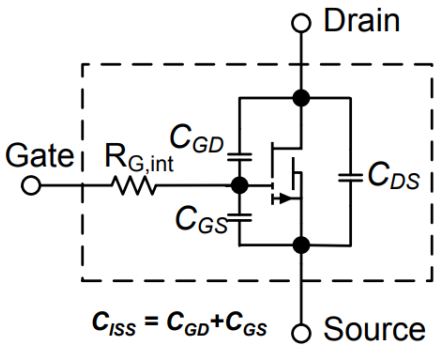


Figure 3.10- Internal HEMT parameters, adapted from [26]

To calculate them, (3.23) can be used, where, Q_g is the total gate charge, and V_{GS} the driving voltage.

$$P_{Dr} = Q_g \cdot V_{GS} \cdot f_{sw} \tag{3.23}$$

3.4.2. Resonant elements and High-Frequency Transformer

The resonant tank and the output filter are composed by passive components being those, inductances, capacitances, and the transformer.

1) Inductance losses

Inductances have mainly two types of losses, cooper, and core losses. Knowing the RMS current that flows through the inductance, and its AC resistance, copper losses can be easily obtained with (3.24):

$$P_{cu_L} = R_{AC_L} \cdot {I_{L_{rms}}}^2 \tag{3.24}$$

Core losses are more complex to calculate. Composed by Eddy currents losses, and leakage losses, to many variables must be known (where some of them are not given by the manufacturer and must be measured) in order to precisely calculate the losses produced by them. Steinmetz equation (3.25) gives an approximation loss value, depending only in the switching frequency f_{sw}, the maximum magnetic flux, and the core specification [61] [62].

$$P_H = c \cdot f_{sw}^x \cdot (B_{ac|HF})^y \cdot V_e \tag{3.25}$$

being c, x, y are the Steinmetz coefficients, and V_e the volume of the core in m^3.

Combining copper loss, with the core loss, total inductance loss is obtained as $P_{L_{total}} = P_{cu_L} + P_{core_L}$.

2) Capacitance losses

Ideally a capacitor is considered "insulator" to DC current, due the presence of the air gap between the two electrodes, conducting only, when AC current is applied to it. In a real capacitor there is an internal Insulation Resistance R_{IR}, with high ohmic value. When a DC current is applied to the capacitor, knowing that current does not flow through the pure capacitor, R_{IR} will limit the current flow, and the heat losses made by R_s are negligible. But when an AC current is applied, higher current flows through C and R_s will produce a considerable amount of joule losses.

Transforming IR and R_s into a single series resistance ESR, an equivalent model is obtained (Figure 3.11) [63].

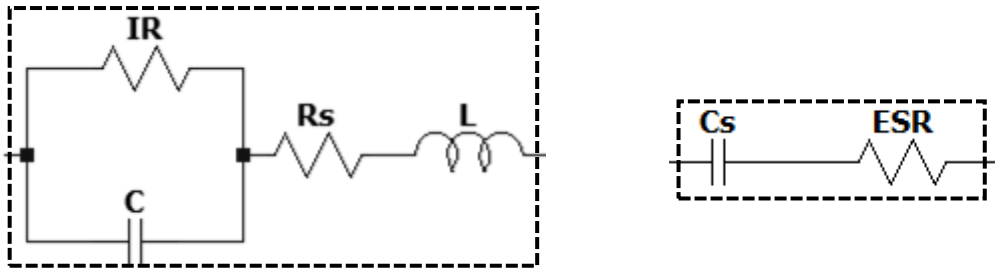


Figure 3.11 – a) Circuit diagram of real capacitor; b) Equivalent capacitor diagram for high frequencies, adapted from [63]

To calculate the power losses, only ESR resistance is considered, resulting the following equation:

$$P_{C_r} = ESR \cdot {I_{RMS}}^2 \tag{3.26}$$

3) Transformer losses

Like inductances, in transformer there is core losses (majority composed by Hysteresis Losses and Eddy Current losses) and the windings losses. In every AC cycle, there will be forward and reverse current applied to the primary winding, magnetizing, and demagnetizing the core, retaining some of the magnetization from the original signal. When an opposite field is applied, it must counteract the field that stored in the core, producing heat. This property of retaining some magnetization, and the lack of ability to return to the original condition, have the name of hysteresis losses and can be calculated using (3.27).

$$P_H = K_h \cdot f_{sw} \cdot A_c \cdot l_c \cdot (B_m)^{1.6} \quad (3.27)$$

where, K_h is a Hysteresis constant (4.44 for a sine wave voltage), A_c the cross-sectional area of the core, l_c the length of the core, and B_m the maximum flux density [35]. According to Faradays law, a variable magnetic flux in a closed loop will induce a voltage in that loop, causing a current circulation. This happen to the transformer core, and as there will be current circulating through it, losses will be produced in form of heat. Those losses are known as Eddy Current Losses and can be described by:

$$P_E = \frac{A_c \cdot (B_m)^2 \cdot f_{sw}}{\rho_c} \quad (3.28)$$

where, ρ_c is the resistivity of the core [35].

When an AC voltage is applied to the primary winding, a magnetic field is created, using the core to link the secondary winding, inducing a voltage. This primary magnetic flux created by the current flowing through the primary winding will not be totally linked to the secondary winding, as there will be leakage flux, contributing for energy losses in the transformer.

$$P_L = \frac{L_{leakage} \cdot {I_{pk}}^2}{2} \quad (3.29)$$

Those losses are usually very small when compared to the mentioned ones, being neglected, obtaining a total estimated core loss described as:

$$P_c = P_H + P_E = K_h \cdot f \cdot A_c \cdot l_c \cdot (B_m)^{1.6} + \frac{A_c \cdot (B_m)^2 \cdot f_{sw}}{\rho_c} \quad (3.30)$$

As there will be induced voltage to the windings, there will be Eddy currents that will counteract the useful current, as seen in Figure 2.15 , lowering the effective area of the conductor, increasing the AC resistance (R_{AC}) of the windings, and the losses produced by them.

Those winding losses can be calculated by:

$$P_{cu} = P_{cu_{prim}} + P_{cu_{sec}} = \left(R_{AC_{prim}} \cdot {I_p}^2\right) + \left(R_{AC_{sec}} \cdot {I_s}^2\right) \quad (3.31)$$

3.4.3. Schottky Diode Losses

At the output of the resonant tank a full-bridge rectifier is used, being composed by four output Schottky diodes, having them two types of losses:

- Conduction losses ($P_{D_{Cond}}$)
- Switching losses ($P_{D_{Sw}}$)

1) Conduction losses

Like the HEMT conduction losses, Schottky diode losses are made by the internal resistance of the component. In the case of the diodes, there is also losses made by the internal voltage drop (V_f), being the total conduction losses described as:

$$P_{D_{Cond}} = {I_f}_{rms}^{2} \cdot R_d + V_f \cdot {I_f}_{Avg} \tag{3.32}$$

where the ${I_f}_{rms}$ is the RMS value of the forward current that (calculated with equation 3.19), R_d is the internal diode resistance, and ${I_f}_{Avg}$ the average value of the forward current which can be calculated with:

$$ {I_f}_{Avg} = \frac{2 \cdot I_{max}}{\pi} \cdot DT \tag{3.33}$$

$$ I_{max} = n \cdot I_{oe} \cdot \sqrt{2} \tag{3.34}$$

2) Switching losses

Switching losses are referred to the power dissipation during the turn-on and turn-off commutations, being calculated with (3.35)

$$P_{D_{Sw}} = \left(\frac{1}{2} \cdot C_{jr} \cdot {V_R}^2 \cdot f\right) + (\frac{1}{6} \cdot I_{RR} \cdot V_R \cdot t_b \cdot f_{sw}) \tag{3.35}$$

where, C_{jr} is the Junction Capacitance, V_R the reverse voltage applied to the diode, I_{RR}, the reverse recovery current, and t_b the time duration that the body diode takes to pass from the reverse current to zero.

Normally, reverse recovery losses are also considered, but in Schottky diodes, the reverse recovering time is approximately zero [64], simplifying (3.35), obtaining:

$$P_{D_{Sw}} = \frac{1}{2} \cdot C_{jr} \cdot {V_R}^2 \cdot f_{sw} \tag{3.36}$$

3.4.4. Summary

Appendix 1 have in detail loss calculation, using standard components for the converter, with similar characteristic when compared the projected ones. Those losses were calculated assuming resonance operation, where reverse conduction and switching losses produced by the switches in inverter block will not be considered. Using (3.37), an approximated efficiency of 97.73% was obtained, with total losses equal to $P_{Total_{Losses}} = 79.3\,W$ for the base design.

Looking to Figure 3.12, Schottky diodes, make 45% of the losses, followed by the transformer. Series inductance and inverter switches, also have considerably high loss. Changing the inverter topology can lead to lower a current, producing lower losses in the primary of the converter.

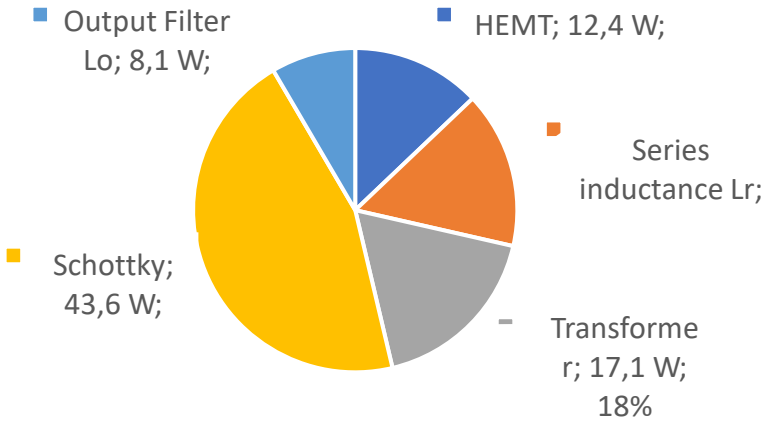


Figure 3.12 - Detailed power losses of the Half-bridge LLC Resonant converter base design at resonance

$$\eta = \frac{P_o}{P_o + P_{Total_{Losses}}} \tag{3.37}$$

3.5. Proposed Concepts and devices for Efficiency Optimization

In order to achieve a higher efficiency from the LLC resonant converter, some converter architectures and concepts were presented in section 2.4. (Represented in Figure 3.13). To understand their impact in the converter, this subsection, will analyze the impact of the full-bridge and half bridge in primary side of the converter, as well the full-bridge and center-tapped architectures for the secondary, finalizing with impact of synchronous rectification when Schottky diodes are replaced with them.

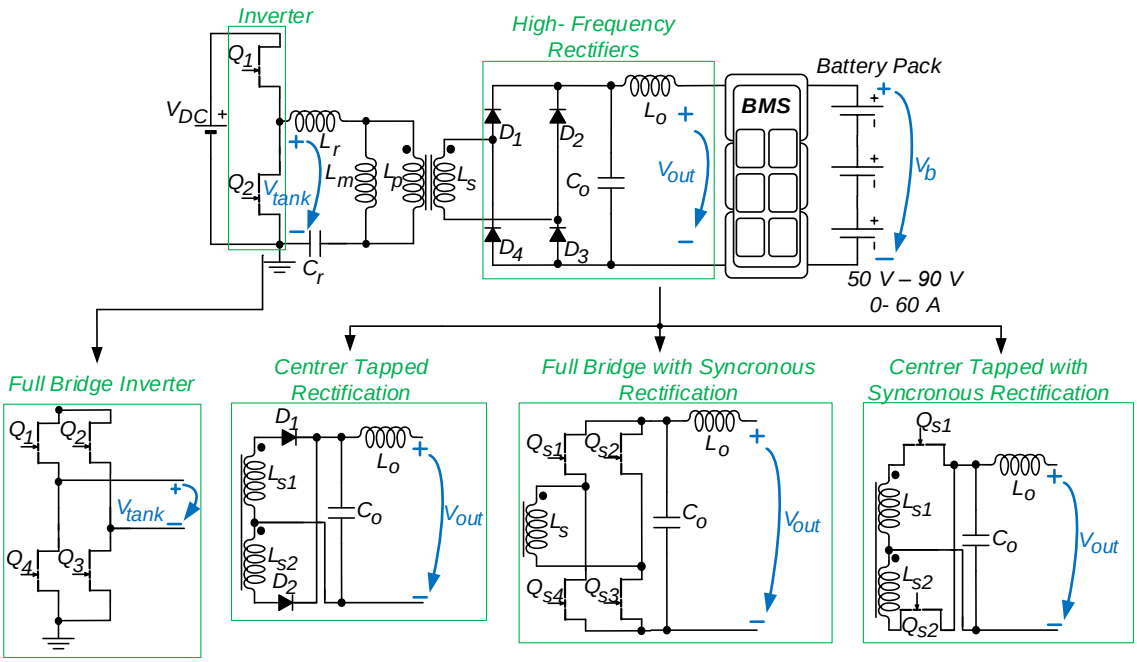


Figure 3.13 – Analyzed power blocks of LLC resonant converter for optimization improvement

3.5.1. Impact of different LLC resonant converter Architectures

Inverter block and High Frequency Rectification block of the LLC Resonant Converter can use different architectures to achieve DC-AC and AC-DC conversion. Starting with the Inverter block (DC-AC), two possible architectures can be used:

- Half-bridge
- Full-bridge

Half-bridge primary side architecture (resumed in Table 3.3 - Comparison Between Inverter Block Architectures assuming the same conditions [66]Table 3.3) allows half the switches, and half the required drivers to control them, reducing the converter size. The square wave voltage V_{tank} produced by them, will vary between $+V_{dc}$ and $0\,V$, resulting in a transformer voltage between $-V_{dc}/2$ and $+V_{dc}/2$. As there is half the voltage applied to the transformer, there will be twice the current to meet the same power level (when compared to the full-bridge). Even though the transformer turns ratio is lower (giving a primary winding with lower resistance), due to the higher current that circulate through the inverter and the resonant tank, increased conduction losses will appear.

The full-bridge architecture, produce a square V_{tank} that varies between $+V_{dc}$ and $-V_{dc}$, resulting in conduction losses that are four times lower ($P = R \cdot I^2$), using the same devices as the Half bridge. The downside, is the transformer with twice the primary winding turns, and twice the switches, increasing the size of the and complexity of the converter.

An experimental study made in [65], replaced the half-bridge with the full-bridge inverter to see the impact in the efficiency. By keeping the same devices and parameters, winding losses decreased approximately 24% and the total conduction losses produced by the switches decrease 33. The selection of the Inverter block architecture of the LLC resonant converter should match the converter power level, where, for a low power converter, the half-bridge architectures is more advantageous (as the double $R_{DS_{on}}$, result in higher losses, than half the circulating current), and for high power levels the full-bridge architecture.

Table 3.3 - Comparison Between Inverter Block Architectures assuming the same conditions [66]

	Switch number	Transformer turns ratio	Circulating Current	Conduction losses	Power density
Half-bridge	2	n	$2 \cdot I$	Higher	Higher
Full-bridge	4	$2 \cdot n$	I	Lower	Lower

Like the Inverter block, the High Frequency Rectifying block, have different architectures. Some of them are the center-tapped architecture and full-bridge architecture. The center-tapped architecture consist in two equal secondary windings, each, attached to a rectifying element. These will block the negative semi cycles, having in their output only positive ones, being later stabilized to DC with the output capacitance and inductance filters. This architecture allows a lower device number, lower circulating currents in the windings and the Schottky diodes. The major drawbacks, is the use of diodes with double the voltage rating (when compared to the full-bridge), and two secondary windings, that may increase the transformer size. The full-bridge architecture only need one secondary winding, being it attached to four diodes (forming a Graetz bridge), but depending in the used devices, conduction losses may increase. Tested in [65], 50% lower total conduction losses were obtained using center-tapped architecture (due to half the rectifiers diodes conducting at the same time), while the losses made in the secondary windings, remained constant, as only one of the windings conduct at the time. According to [65], the center-tapped architecture is more appropriated to high output current applications, while the full-bridge is advantageous to high output voltage applications.

Table 3.4 - Comparison Between High Frequency Rectifier Architectures assuming the same conditions [66]

	Rectifier Number	Required Secondary Winding	Rectifier Voltage Rating	Conduction losses	Power density
Half-bridge	2	$2 \cdot W_s$	$2 \cdot V_{rating}$	Lower	Lower
Full-bridge	4	W_s	V_{rating}	Higher	Higher

Demonstrated in the previous analysis the architecture that should perform better in this work, is the full-bridge Inverter along with the center-tapped rectification, due to the high power of the converter, and the high output current.

3.5.2. Impact of Output Synchronous Rectification in LLC Resonant converter

Schottky diodes are used in AC-DC converters to block the negative semi cycles allowing only positive voltage to be stabilized by filters. These diodes are simple to apply in circuit, have automatic switching depending in current direction (if forward or reverse), and have a relatively low cost when compared to other solutions. However, the internal voltage drop V_f produced by the pn junction, makes higher conduction. Synchronous rectification or active rectification, consist in the replacement of the diodes with active switches like MOSFETs or HEMT devices (Figure 3.14).

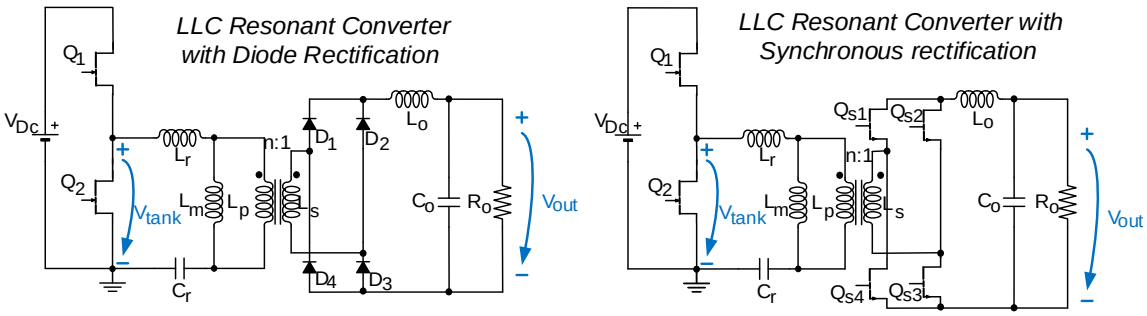


Figure 3.14 LLC Resonant Converter with Diode Rectification (left) or Synchronous rectification using HEMTs (right)

Those switching devices have parasitic components, where one of them is the “body-diode”, that allows reverse conduction, even if gate signal is at off-state. When current flows through switch devices there are three possible scenarios:

- Forward conduction with Gate ON
- Reverse conduction With Gate ON

- Reverse conduction with Gate OFF

When Gate is at on-state, current will flow either forward or reverse trough the switch, but when its off, current still have the ability to reverse conduct through the body-diode. Having gate path either at on or off-state, reverse conduction will always be present [26]. The main difference is where the current flows, and the loss production in both cases. With gate path at on-state, conduction losses can be described with (3.18), considering only the drain-to-source resistance $R_{ds_{on}}$, while when the body diode is conducting there will be losses from the fixed diode voltage drop V_f and his internal resistance R_d (3.32), where depending in the diode characteristics may result in higher conduction losses. In synchronous rectification, the switch is reversed, keeping the "body diode" in the same direction as the rectifier diode in passive rectification, controlling the gate, to have the switch conducting when the body diode is conducting, reducing the conduction losses [26].

$$P_{P_{HEMT}conduction_{loss}} = {I_{DS}}_{RMS}^{2} \cdot R_{DS(ON)} \tag{3.18}$$

$$P_{diode_{conduction_{loss}}} = {I_f}_{RMS}^{2} \cdot R_d + {V_f}_d \cdot {I_f}_{Avg} \tag{3.32}$$

Gate control can be a complex task specially on this type of converters. Depending on V_{tank} frequency, the converter changes it is behavior, shifting of delaying the output current I_o, when compared to V_{tank} (represented in Figure 3.15), requiring a turn-on (T_a) and turn-off (T_b) compensation time, being it positive or negative, depending in the operating region. Turning-on the switch too early or turning if off too late, and severe reverse conduction will appear, where both rectification branches, may short within each other. Having an late turn-on or early turn-off, reduce the time that the switchs is conducting, increasing conduction losses, harming the converters efficiency [69], but it is safer to be used, as the risk of short both rectification branches is much lower. To control the switches several technics can be used. [70] and [71] describes some of them, as self-driven, current sense, and others, comparing their complexity, their cost and how it impacts the stability of the converter, as well the efficiency. Studies made in [70]-[74], replaced the passive rectifiers with synchronous devices, and considerably lower conduction losses (from 1% to 1000% less) were obtained, improving the converter efficiency, even that the complexity and the cost of the circuit, increase.

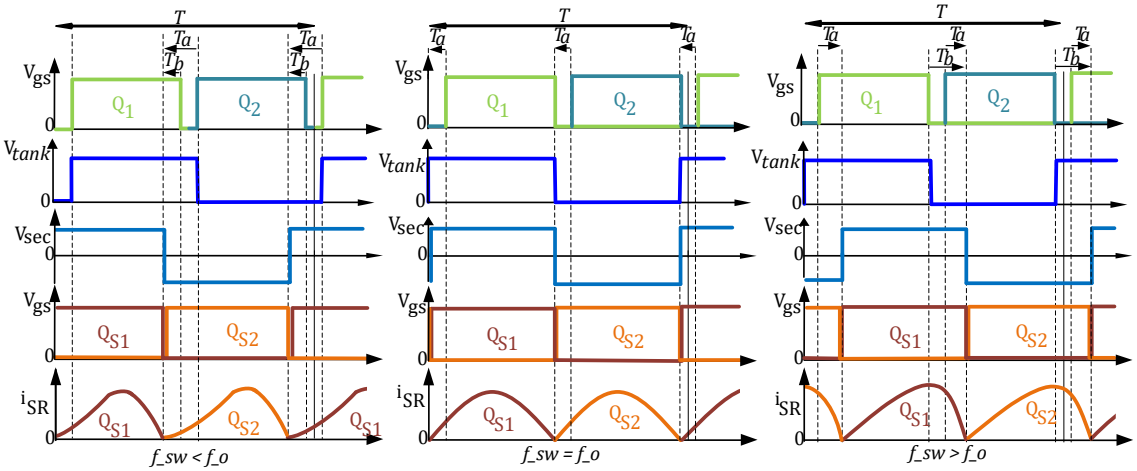


Figure 3.15 SR Switch on-time, depending on the LLC resonant converter operating region.

This work will only focus on the replacement of the diodes with SR, without entering much in detail in synchronous rectification drivers. The control of the switches was automatic, using a function in LTSpice, turning it on when the switch body diode current is higher than $3\ A$, to prevent false turn-on, and voltage ringing in the switches.

CHAPTER 4. Efficiency Optimization of the LLC Resonant Converter

From the previous chapters the LLC resonant converter was presented, as well their principal characteristics. Considering the proposed concepts to optimize the efficiency of the converter, in this chapter, eight designs will be tested (Figure 4.1) using different converter architectures, as well active rectification in the high frequency rectification block, studying their losses, comparing them with the base design, that was developed in [1]. Two different tests were conducted, analyzing the losses made in the converter, and see their impact:

- Detailed losses operating at different regions, modulating the switching frequency to see the behavior of the converter, keeping the same load
- Output constant-current and constant-voltage, adjusting the equivalent load to simulate the constant-current/constant-voltage charging method.

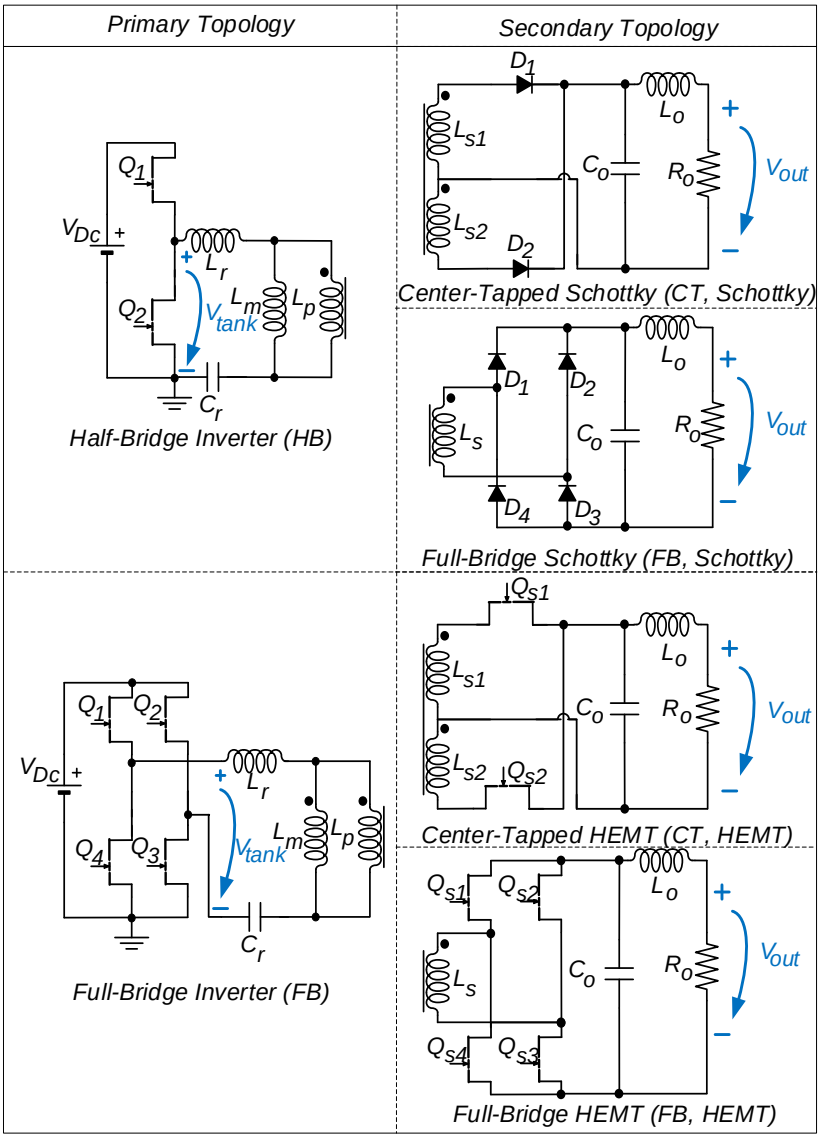


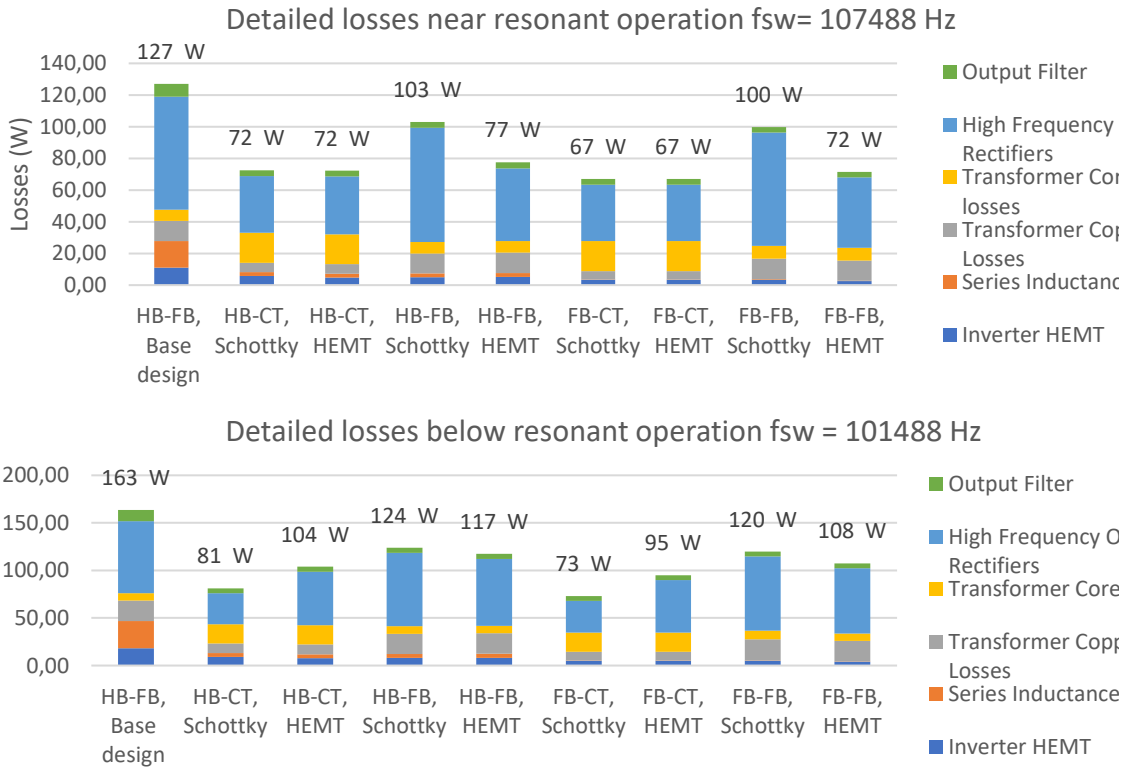
Figure 4.1 Proposed LLC resonant Converter Designs

4.1. Detailed losses operating at different regions

During this work, some concepts were proposed, to improve the global efficiency of the LLC resonant converter. Using real component model in LTSpice, combined with Frenetic, a detailed loss production was obtained, being them, illustrated in Figure 4.2. In the newer proposed designs, updated components with better characteristics, were used, being them listed in Appendix A. By comparing the HB-FB base design with the with the same topology using updated components, an improvement of approximately 23% was obtained, just by replacing them older components with better ones. Using the center-tapped rectification instead of full-bridge, the total rectification losses was reduced in half as well the transformer winding losses, but transformer core losses increase.

Changing the operation mode of the converter, to operate under resonance, V_o and I_o increase as expected, while operating above resonance, V_o and I_o will be reduced (considering a constant load). For those operation modes distinct designs presented higher efficiency, where the deciding factor was the output current. Operating with higher output currents and the center-tapped configuration stands out, due the lower number of rectifying elements and the lower circulating current. Also, the active rectification HEMT, presented a worse performance, than the Schottky diode. The reason to this, is the difference between the devices internal resistance, where the HEMT have an $R_{DS_{(ON)}} = 0.01\ \Omega$ and the Schottky diode $R_d = 0.0015\ \Omega$, almost 7 times lower.

When the converter is operated above resonance, the scenario is different. Due the higher transformer core losses in the center-tapped topology, the converter that operates with higher efficiency, is the full-bridge, even when using more rectifying elements. In this application, and in all the developed designs, the full-bridge inverter presented a better performance when compared to the half-bridge, by the lower primary current. This leads to lower losses made by the inverter switches, series inductance, and the primary winding.



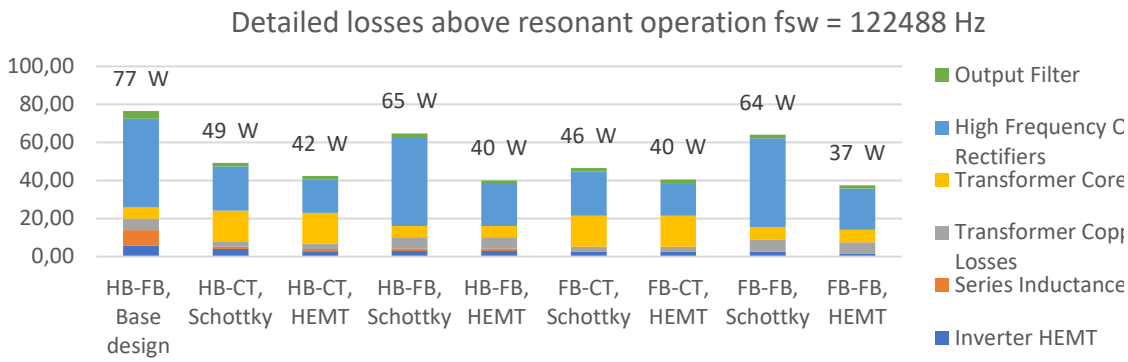


Figure 4.2- Detailed Losses of the LLC Resonant Converter, below resonance, at resonance and above resonance

To select the converter that presents the best performance for the battery charging application, the presented simulations are not enough, as the load was constant. The best methodology to compare the designs, is to simulate the charge of the battery, combining an operation at low-voltage/high current, and high-voltage/low-current, adjusting the battery equivalent load (given by $R_o = V_o/I_o$), and the frequency, to regulate V_o and I_o simulating the CC-CV charging method as illustrated in Figure 4.3.

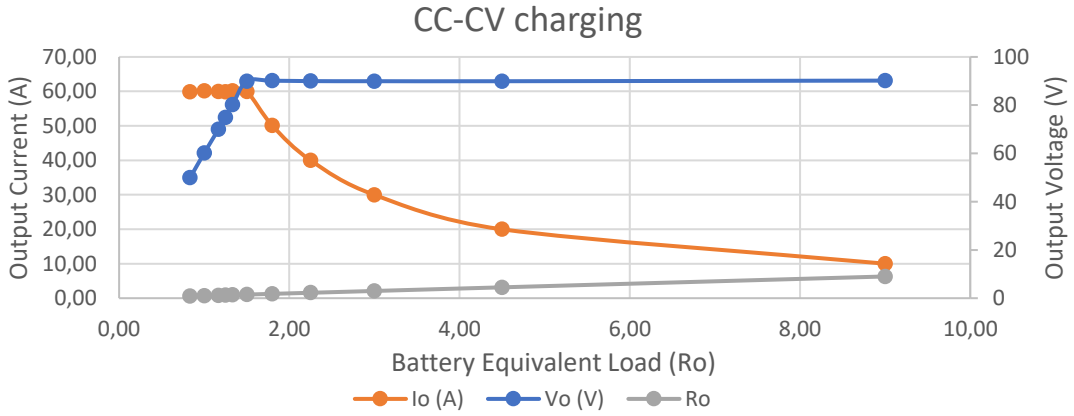


Figure 4.3- Constant-Current Constant-Voltage, along with the equivalent battery load

4.2. Output constant current and output constant voltage

To analyze different points in the charging spectrum, two tests were conducted. The first test was made by clamping the output current at its maximum value, adjusting the frequency until V_o reaches the nominal value. This simulates the constant-current charge of the battery, as well the operation of the converter with high output currents at different output voltage points, in order to see how the output voltage impacts the converter efficiency. The second test was similar, but instead, the output voltage was camped to the maximum voltage, slightly adjusting the frequency and the load, to obtain diverse current points and

simulate the constant-voltage charging, as well the impact of the current in the converter efficiency. Both tests were joined into one, having all the points represented in Figure 4.4, simulating the CC-CV charge applied to a discharged battery.

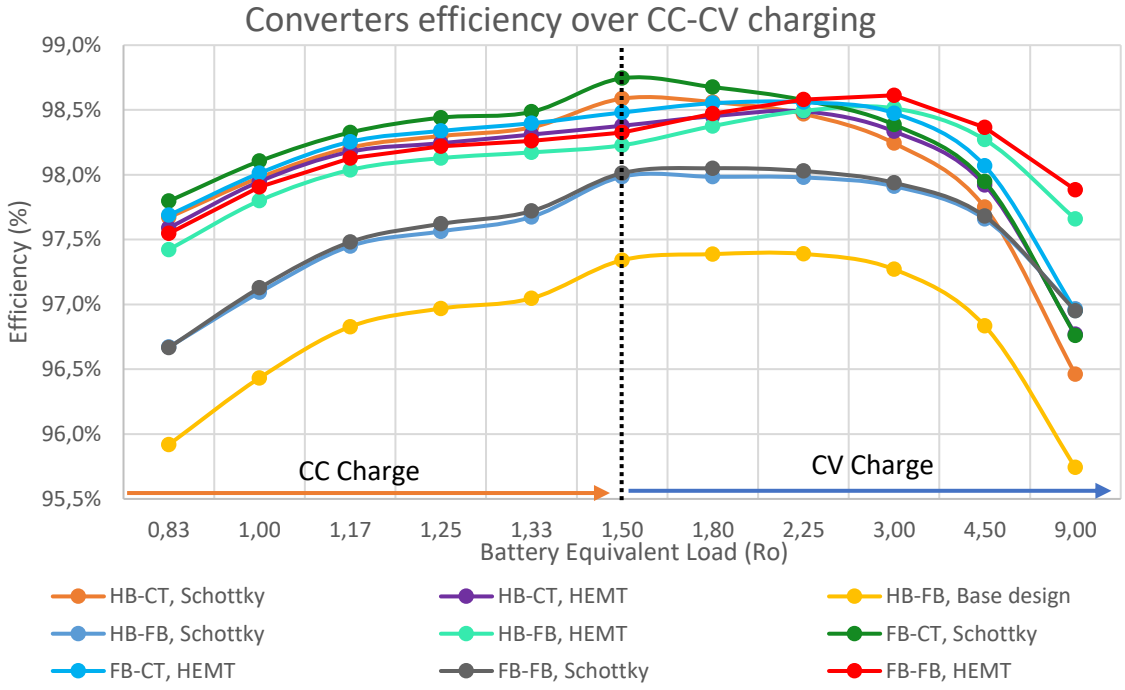


Figure 4.4- Different LLC Resonant Converter designs operating under CC-CV charging method

Starting with the base design, the maximum obtained efficiency was 97,39%, making this design, the one with the worse performance, when compared to all the other designs. According to the conducted simulations, at CC charging, the design that uses full-bridge inverter/center-tapped with Schottky diodes, presents the highest efficiency (98,74%), but when the CV charging starts, the efficiency progressively drops reaching a minimum of 96,95% at $I_o = 10\,A$. Using synchronous rectification, the efficiency is slightly lower at CC charging, but increases when operates in CV. Looking at full-bridge/full bridge using active rectification, when it operates at CC charging, the efficiency is slightly lower, than the previous mentioned design, but when the CV charging starts, this design presents the best efficiency, obtaining a peak efficiency of 98,61%. As there is a lot of efficiency variations in the CC-CV charging process, the results presented in Figure 4.4 were integrated, calculating the total area under the efficiency curves, being it represented in Figure 4.5 . By integrating the results an easier analysis of all the designs over the complete CC-CV charging can be made, where the design that presents the higher area, is the design that present higher efficiency, for full battery charging.

Analyzing Figure 4.5, the first detail that can be seen is significative improvement of all the presented designs over the base design. By comparing

passive with active rectification, it is possible to see that the active rectification improves the total efficiency of every converter topology. For this application, the design that presents the highest integrated efficiency is the full-bridge inverter with the full-bridge synchronous rectification, being this design, the best one to make a CC-CV charge.

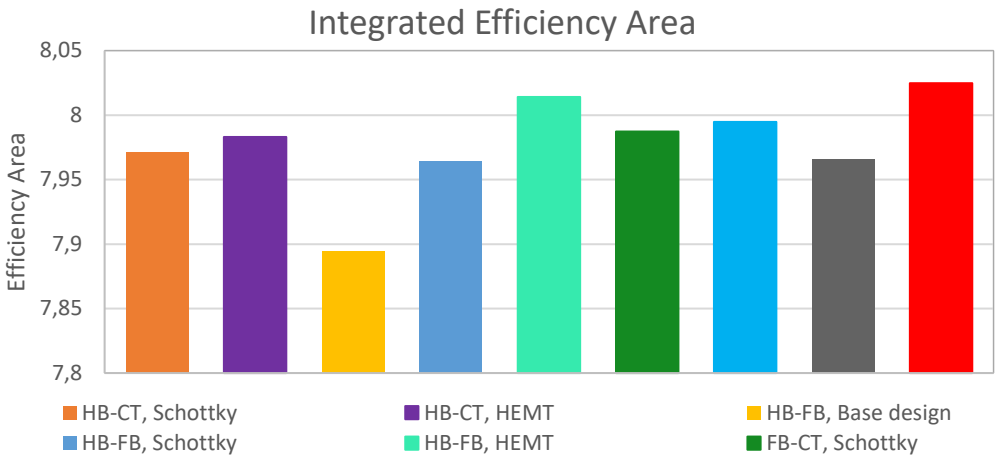


Figure 4.5- Integrated Efficiencies of the different LLC resonant converter designs

CHAPTER 5. Conclusions, Contributions and Future Work

The main goal of improving the LLC converter optimized in [1] was achieved, obtaining all the proposed designs higher efficiency than the base design. Depending on the application, different designs perform better than others. Looking at the CC charge, the design that stands out is the full-bridge/center-tapped using Schottky diodes reaching a peak efficiency of 97.84%, but by looking to the integrated efficiencies three other designs presented better performance. For this specific application, being it a lithium battery charge, the design with the best performance was the full-bridge/full-bridge using synchronous rectification, reaching a peak efficiency of 98,61%, and less $38\,W$ at that point when compared to the base design.

5.1. Conclusions

This project studied the LLC resonant converter and its principle of operation, with the main goal of improving the efficiency when the CC-CV method is used. By maintaining the converter characteristics presented in [1], different converter topologies were studied and designed, combining the output rectification with synchronous rectification using new wide band-gap semiconductors with improved characteristics. Even though experimental tests were not possible due to the COVID-19 pandemic, complicating the access to the university, real component models were used in the LTSpice simulation, along with Frenetic to obtain the core and winding losses at different operation point, being all the harmonics considered to the power loss. Choosing the topology that suits better one application can be challenging. Converter operation region, output load, and output current are some of the factors that changes the converter architecture with the best performance. As seen before, the same converter can operate with higher efficiency at higher output voltage and low current, but may not be the best for high output currents. At the moment, the liming factors that highly affect the efficiency are the relatively high $R_{DS_{ON}}$ of the semiconductors and the High frequency transformer, producing the majority of the losses in the converter.

5.2. Future work

To further improve this work, some changes can be made. Starting with the synchronous rectifier controller, the SR turn-on time was set automatically when the circulating current reached 3A. A fully autonomous controller can improve the efficiency of the rectification stage, automatically adjusting the duty cycle of the synchronous rectifiers, looking to the circulating current and voltage

in the rectifier. Continuing with the switch devices, searching for better semiconductors, with lower $R_{DS_{ON}}$ and Q_g, also would reduce rectification losses as well the losses produced in the Inverter block, allowing lower dead-times, reducing the time that the inverter switches are in reverse conduction. For the transformer, an extended search for better core materials must be made, testing the matrix windings to reduce copper losses, integrating it with center-tapped architecture lowering the number of the rectifying elements. To conclude, the converter will be constructed, comparing the experimental data to the simulation, seeing how close the LTSpice models are to the real experiments, analyzing how the converter behaves in a real scenario.

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Attachments

Index

1. Appendix A - LLC Resonance Converter Design

In this thesis, the optimized values from [1] will be used, and in order to be able to determine adequately all the elements of the resonance tank, some specifications must be known.

SYMBOL	QUANTITY	VALUE
V_{dc}	Input Voltage	$600\ V_{dc}$
$V_{B_{min}}$	Minimum Battery Voltage	$52.5\ V_{dc}$
$V_{B_{nom}}$	Nominal Battery Voltage	$75.6\ V_{dc}$
$V_{B_{max}}$	Maximum Battery Voltage	$88.2\ V_{dc}$
I_o	Maximum Output Current	$60\ A$
$P_{B_{max}}$	Maximum Output Power	$5.2\ kW$
Cap	Battery Capacity	$55\ Ah\ (at\ 1C)$

Table A.1- Battery Parameters

SYMBOL	QUANTITY	VALUE
f_s	Switching Frequency	$107.488\ kHz$
P_{nom}	Charger Nominal Power	$4.2\ kW$
$V_{dc_{min}}$	Minimum Charger input DC link	$590\ V_{dc}$
V_{dc}	Nominal Charger input DC link	$600\ V_{dc}$
$V_{dc_{max}}$	Maximum Charger input DC link	$610\ V_{dc}$
ΔI	Battery Current Ripple	$\leq 5.5A$
ΔV	Battery Voltage Ripple	$\leq 0.5V$
V_{f_d}	Forward voltage of output rectifier Diodes	$0.75V$
V_{f_m}	Forward voltage of output rectifier HEMTs	$\approx 0\ V$

Table A.2- Parameters to consider for the LLC resonant converter

1.1. Half Bridge Inverter

Step 1- Determine the transformer transformation ratio

$$n = \sqrt{k} \cdot M_g \cdot \frac{(V_{dc}/2)}{V_{o_{nom}} + V_f} \tag{3.6}$$

In this work two possibilities approaches were looked, use diodes, or HEMTs in the output rectification, having in the case of diodes a V_f of

approximately 0.75V, and in the case of HEMTs, approximately 0V, and the transformer coupling equal to 0.99.

$$n_{exacto_{diodos}} = \sqrt{0.99} \cdot 1 \cdot \frac{600/_2}{75.6 + 0.75} \leftrightarrow n_{exacto_{diodos}} = 3.90958$$

$$n_{exacto_{HEMT's}} = \sqrt{0.99} \cdot 1 \cdot \frac{600/_2}{75.6 + 0} \leftrightarrow n_{exacto_{HEMT's}} = 3.94836$$

By obtaining the transformation ratio, the minimum and maximum gain of the converter can be obtained, by the following equations:

Step 2- Determine the minimum and maximum gain

$$M_{g_{min}} = \frac{n \cdot (V_{B_{min}} + V_f)}{V_{DC_{max}}/_2} \quad (3.7)$$

$$M_{g_{max}} = \frac{n \cdot (V_{B_{max}} + V_f)}{V_{DC_{min}}/_2} \quad (3.8)$$

$$M_{g_{min_{diodos}}} = \frac{3.90958 \cdot (52.5 + 0.75)}{610/_2} \leftrightarrow M_{g_{min_{diodos}}} = 0.682575$$

$$M_{g_{max_{diodos}}} = \frac{3.90958 \cdot (88.2 + 0.75)}{590/_2} \leftrightarrow M_{g_{max_{diodos}}} = 1.17884$$

$$M_{g_{min_{HEMT's}}} = \frac{3.94836 \cdot (52.5 + 0)}{610/_2} \leftrightarrow M_{g_{min_{HEMT's}}} = 0.679636$$

$$M_{g_{max_{HEMT's}}} = \frac{3.94836 \cdot (88.2 + 0)}{590/_2} \leftrightarrow M_{g_{max_{HEMT's}}} = 1.18049$$

Step 3- Selection of the inductance ratio L_n an the quality facto Q_e

L_n, and Q_e are important factors and choosing them, can be a challenging task. Usually as initial design, L_n, is fixed, (between 3-5 according to [58]), then Q_e is selected guaranteeing the minimum and maximum gains (exemplified in Figure 3.7, where Q_e needs to be 1.6), iterating later L_n, and Q_e, to achieve the maximum efficiency out of the converter

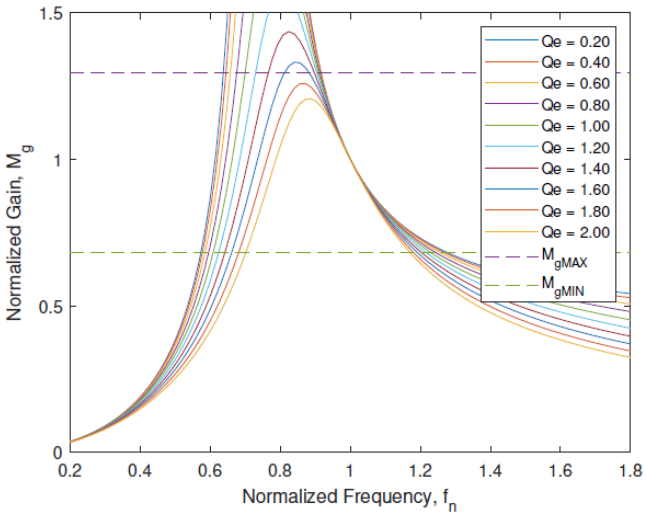

Figure 5.1- Quality Factor Curves over the Normalized Frequency [1]

Step 4- Determine the minimum and maximum gain

$$f_{sw_{min}} = M_{g_{min}} \cdot f_{sw} \quad (3.9)$$

$$f_{sw_{max}} = M_{g_{max}} \cdot f_{sw} \quad (3.10)$$

$$f_{sw_{min_{diodos}}} = 0.682575 \cdot 107488 \leftrightarrow f_{sw_{min_{diodos}}} = 73.3685\ kHz$$

$$f_{sw_{max_{diodos}}} = 1.17884 \cdot 107488 \leftrightarrow f_{sw_{max_{diodos}}} = 126.711\ kHz$$

$$f_{sw_{min_{HEMT's}}} = 0.679636 \cdot 107488 \leftrightarrow f_{sw_{min_{HEMT's}}} 73.0527\ kHz$$

$$f_{sw_{max_{HEMT's}}} = 1.18049 \cdot 107488 \leftrightarrow f_{sw_{max_{HEMT's}}} = 126.889\ kHz$$

Step 5- Determine the resonant elements using the FHA simplification model

$$R_e = \frac{8n^2}{\pi^2} \cdot \frac{V_o}{I_o} \quad (3.11)$$

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_{sw} \cdot R_e} \quad (3.12)$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_{sw})^2 \cdot C_r} \quad (3.13)$$

$$L_m = L_n \cdot L_r \quad (3.14)$$

$$R_{e_{diodos}} = \frac{8 \cdot 3.90958^2}{\pi^2} \cdot \frac{75.6}{55} \leftrightarrow R_{e_{diodos}} = 17.0298\ \Omega$$

$$C_{r_{diodos}} = \frac{1}{2 \cdot \pi \cdot 1.6 \cdot 107488 \cdot 17.0298} \leftrightarrow C_{r_{diodos}} = 54.34\ nF$$

$$L_{r_{diodos}} = \frac{1}{(2 \cdot \pi \cdot 107488)^2 \cdot 54.34 \cdot 10^{-9}} \leftrightarrow L_{r_{diodos}} = 40.344997uH$$

$$L_{m_{diodos}} = 0.83 \cdot 40 \cdot 10^{-6} \leftrightarrow L_{m_{diodos}} = 33.486uH$$

$$R_{e_{HEMT's}} = \frac{8 \cdot 3.94836^2}{\pi^2} \cdot \frac{75.6}{55} \leftrightarrow R_{e_{HEMT's}} = 17{,}3693\ \Omega$$

$$C_{r_{HEMT's}} = \frac{1}{2 \cdot \pi \cdot 1.6 \cdot 107488 \cdot 17{,}3693} \leftrightarrow C_{r_{HEMT's}} = 53.279\ nF$$

$$L_{r_{HEMT's}} = \frac{1}{(2 \cdot \pi \cdot 107488)^2 \cdot 38{,}1792 \cdot 10^{-9}} \leftrightarrow L_{r_{HEMT's}} = 41.149uH$$

$$L_{m_{HEMT's}} = 0.83 \cdot 29 \cdot 10^{-6} \leftrightarrow L_{m_{HEMT's}} = 34.15396uH$$

Step 6- Check the design values, ensuring that they follow the initial specification

Mosfets Dead-Time:

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m \quad (3.14)$$

$$t_{dead_{Diode}} \geq 3.90958 \cdot 1 \cdot 10^{-9} \cdot 107488 \cdot 33 \cdot 10^{-6} \leftrightarrow t_{dead_{Diode}} \geq 13.8677\ nS$$

$$t_{dead_{HEMT's}} \geq 3.94836 \cdot 236 \cdot 10^{-12} \cdot 107488 \cdot 34 \cdot 10^{-6} \leftrightarrow t_{dead_{HEMT's}} \geq 3.4054\ \text{nS}$$

Series resonance frequency:

$$F_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}} \quad \text{(A.1)}$$

$$F_{o\,diodos} = \frac{1}{2 \cdot \pi \cdot \sqrt{40 \cdot 10^{-6} \cdot 54.34 \cdot 10^{-9}}} \leftrightarrow F_{o\,diodos} = 107952\ Hz$$

$$F_{o\,HEMT's} = \frac{1}{2 \cdot \pi \cdot \sqrt{41 \cdot 10^{-6} \cdot 53.279 \cdot 10^{-9}}} \leftrightarrow F_{o\,HEMT's} = 107684\ Hz$$

Inductance ratio:

$$L_n = \frac{L_m}{L_r} \quad \text{(A.2)}$$

$$L_{n\,diodos} = \frac{33 \cdot 10^{-6}}{40 \cdot 10^{-6}} \leftrightarrow L_{n\,diodos} = 0.85$$

$$L_{n\,HEMT's} = \frac{34 \cdot 10^{-6}}{41 \cdot 10^{-6}} \leftrightarrow L_{n\,HEMT's} = 0.829$$

Quality factor at full load

$$Q_e = \frac{1}{R_e} \cdot \sqrt{\frac{L_r}{C_r}} \quad \text{(A.3)}$$

$$Q_{e\,diodos} = \frac{1}{17.0298} \cdot \sqrt{\frac{40 \cdot 10^{-6}}{54.34 \cdot 10^{-9}}} \leftrightarrow Q_{e\,diodos} = 1.59316$$

$$Q_{e\,HEMT's} = \frac{1}{17{,}3693} \cdot \sqrt{\frac{41 \cdot 10^{-6}}{53.279 \cdot 10^{-9}}} \leftrightarrow Q_{e\,HEMT's} = 1.5971$$

Quality factor at 110% overload

$$Q_e = \frac{1}{1.1 \cdot R_e} \cdot \sqrt{\frac{L_r}{C_r}} \quad (A.4)$$

$$Q_{e_{diodos_{overload}}} = \frac{1}{17.0298 \cdot 1.1} \cdot \sqrt{\frac{40 \cdot 10^{-6}}{54.34 \cdot 10^{-9}}} \leftrightarrow Q_{e_{diodos_{overload}}} = 1.44833$$

$$Q_{e_{HEMT's_{overload}}} = \frac{1}{1.1 \cdot 17{,}3693} \cdot \sqrt{\frac{29 \cdot 10^{-6}}{38{,}1792 \cdot 10^{-9}}} \leftrightarrow Q_{e_{HEMT's_{overload}}} = 1.45191$$

Step 7- Design the output filter elements

$$C_o \geq \frac{I_o}{8 \cdot f_{sw} \cdot V_o \cdot \frac{\Delta V_o}{100}} \quad (3.15)$$

$$L_o \geq \frac{V_o \cdot \Delta V_o}{I_o \cdot \Delta I_o \cdot 2 \cdot \pi \cdot F_{sw}} \quad (3.16)$$

$$C_{o_{Diodes}} \geq \frac{55}{8 \cdot 107952 \cdot 75.6 \cdot \frac{0.5}{100}} \leftrightarrow C_{o_{Diodes}} \geq 168uF$$

$$L_{o_{Diodes}} \geq \frac{75.5 \cdot 0.5}{55 \cdot 5.5 \cdot 2 \cdot \pi \cdot 107952} \leftrightarrow L_{o_{Diodes}} \geq 184.228nH$$

$$C_{o_{HEMT}} \geq \frac{55}{8 \cdot 107684 \cdot 75.6 \cdot \frac{0.5}{100}} \leftrightarrow C_{0_{HEMT}} \geq 169uF$$

$$L_{o_{HEMT}} \geq \frac{75.5 \cdot 0.5}{55 \cdot 5.5 \cdot 2 \cdot \pi \cdot 107684} \leftrightarrow L_{0_{HEMT}} \geq 184.687nH$$

1.2. Full Bridge Inverter

Step 1- Determine the transformer transformation ratio

$$n = \sqrt{k} \cdot M_g \cdot \frac{V_{dc}}{V_{o_{nom}} + V_f} \quad \text{(A.5)}$$

In this work two possibilities approaches were looked, use diodes, or HEMTs in the output rectification, having in the case of diodes a V_f of approximately 0.75V, and in the case of HEMTs, approximately 0V, and the transformer coupling equal to 0.99.

$$n_{exacto_{diodos}} = \sqrt{0.99} \cdot 1 \cdot \frac{600}{75.6 + 0.75} \leftrightarrow n_{exacto_{diodos}} = 7.81915$$

$$n_{exacto_{HEMT's}} = \sqrt{0.99} \cdot 1 \cdot \frac{600}{75.6 + 0} \leftrightarrow n_{exacto_{HEMT's}} = 7.8967$$

By obtaining the transformation ratio, the minimum and maximum gain of the converter can be obtained, by the following equations:

Step 2- Determine the minimum and maximum gain

$$M_{g_{min}} = \frac{n \cdot (V_{B_{min}} + V_f)}{V_{DC_{max}}} \quad \text{(A.6)}$$

$$M_{g_{max}} = \frac{n \cdot (V_{B_{max}} + V_f)}{V_{DC_{min}}} \quad \text{(A.7)}$$

$$M_{g_{min_{diodos}}} = \frac{7.81915 \cdot (52.5 + 0.75)}{610} \leftrightarrow M_{g_{min_{diodos}}} = 0.682574$$

$$M_{g_{max_{diodos}}} = \frac{7.81915 \cdot (88.2 + 0.75)}{590} \leftrightarrow M_{g_{max_{diodos}}} = 1.17884$$

$$M_{g_{min_{HEMT's}}} = \frac{7.8967 \cdot (52.5 + 0)}{610} \leftrightarrow M_{g_{min_{HEMT's}}} = 0.679636$$

$$M_{g_{max_{HEMT's}}} = \frac{7.8967 \cdot (88.2 + 0)}{590} \leftrightarrow M_{g_{max_{HEMT's}}} = 1.18049$$

Step 3- Selection of the inductance ratio L_n an the quality facto Q_e

L_n, and Q_e are important factors and choosing them, can be a challenging task. Usually as initial design, L_n, is fixed, (between 3-5 according to [58]), then Q_e is selected guaranteeing the minimum and maximum gains (exemplified in Figure 3.7, where Q_e needs to be 1.6), iterating later L_n, and Q_e, to achieve the maximum efficiency out of the converter

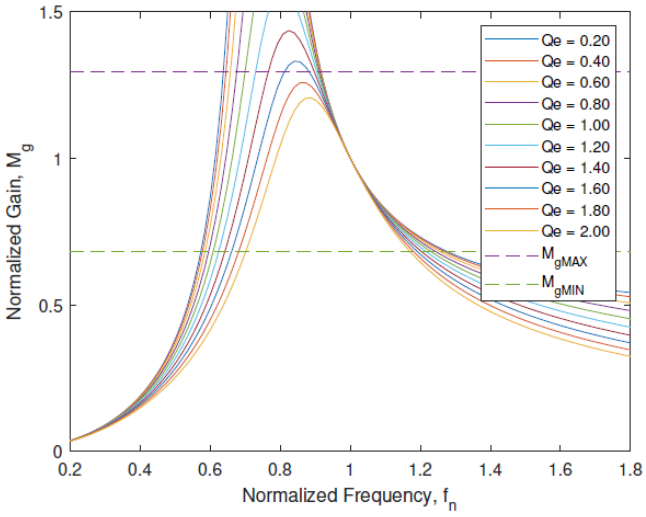

Figure 5.2- Quality Factor Curves over the Normalized Frequency [1]

Step 4- Determine the minimum and maximum gain

$$f_{sw_{min}} = M_{g_{min}} \cdot f_{sw} \quad (3.9)$$

$$f_{sw_{max}} = M_{g_{max}} \cdot f_{sw} \quad (3.10)$$

$$f_{sw_{min_{diodos}}} = 0.682574 \cdot 107488 \leftrightarrow f_{sw_{min_{diodos}}} = 73.3685\ kHz$$

$$f_{sw_{max_{diodos}}} = 1.17884 \cdot 107488 \leftrightarrow f_{sw_{max_{diodos}}} = 126.711\ kHz$$

$$f_{sw_{min_{HEMT's}}} = 0.679636 \cdot 107488 \leftrightarrow f_{sw_{min_{HEMT's}}} 73.0527\ kHz$$

$$f_{sw_{max_{HEMT's}}} = 1.18049 \cdot 107488 \leftrightarrow f_{sw_{max_{HEMT's}}} = 126.889\ kHz$$

Step 5- Determine the resonant elements using the FHA simplification model

$$R_e = \frac{8n^2}{\pi^2} \cdot \frac{V_o}{I_o} \quad (3.11)$$

$$C_r = \frac{1}{2 \cdot \pi \cdot Q_e \cdot f_{sw} \cdot R_e} \quad (3.12)$$

$$L_r = \frac{1}{(2 \cdot \pi \cdot f_{sw})^2 \cdot C_r} \quad (3.13)$$

$$L_m = L_n \cdot L_r \quad (3.14)$$

$$R_{e_{diodos}} = \frac{8 \cdot 7.81915^2}{\pi^2} \cdot \frac{75.6}{55} \leftrightarrow R_{e_{diodos}} = 68.119\ \Omega$$

$$C_{r_{diodos}} = \frac{1}{2 \cdot \pi \cdot 1.6 \cdot 107488 \cdot 68.119} \leftrightarrow C_{r_{diodos}} = 13.5853\ nF$$

$$L_{r_{diodos}} = \frac{1}{(2 \cdot \pi \cdot 107488)^2 \cdot 13.5853 \cdot 10^{-9}} \leftrightarrow L_{r_{diodos}} = 161.3795\ uH$$

$$L_{m_{diodos}} = 0.83 \cdot 161.3795 \cdot 10^{-6} \leftrightarrow L_{m_{diodos}} = 133.94499\ uH$$

$$R_{e_{HEMT's}} = \frac{8 \cdot 7.8967^2}{\pi^2} \cdot \frac{75.6}{55} \leftrightarrow R_{e_{HEMT's}} = 69.4769\ \Omega$$

$$C_{r_{HEMT's}} = \frac{1}{2 \cdot \pi \cdot 1.6 \cdot 107488 \cdot 69.4769} \leftrightarrow C_{r_{HEMT's}} = 13.3199\ nF$$

$$L_{r_{HEMT's}} = \frac{1}{(2 \cdot \pi \cdot 107488)^2 \cdot 13.3199 \cdot 10^{-9}} \leftrightarrow L_{r_{HEMT's}} = 164.5966\ uH$$

$$L_{m_{HEMT's}} = 0.83 \cdot 164.5966 \cdot 10^{-6} \leftrightarrow L_{m_{HEMT's}} = 136.615\ uH$$

Step 6- Check the design values, ensuring that they follow the initial specification

Mosfets Dead-Time:

$$t_{dead} \geq n \cdot C_{eq} \cdot f_{sw} \cdot L_m \quad (3.14)$$

$$t_{dead_{Diode}} \geq 7.81915 \cdot 1 \cdot 10^{-9} \cdot 107488 \cdot 133.94499 \cdot 10^{-6} \leftrightarrow t_{dead_{Diode}} \geq 112.581\ nS$$

$$t_{dead_{HEMT's}} \geq 7.8967 \cdot 236 \cdot 10^{-12} \cdot 107488 \cdot 136.615 \cdot 10^{-6} \leftrightarrow t_{dead_{HEMT's}} \geq 27.366 \text{ nS}$$

Series resonance frequency:

$$f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L_r \cdot C_r}} \quad \text{(A.1)}$$

$$f_{o_{diodos}} = \frac{1}{2 \cdot \pi \cdot \sqrt{161.3795 \cdot 10^{-6} \cdot 13.5853 \cdot 10^{-9}}} \leftrightarrow F_{o_{diodos}} = 107488.33\ Hz$$

$$f_{o_{HEMT's}} = \frac{1}{2 \cdot \pi \cdot \sqrt{164.5966 \cdot 10^{-6} \cdot 13.3199 \cdot 10^{-9}}} \leftrightarrow F_{o_{HEMT's}} = 107487.81\ Hz$$

Inductance ratio:

$$L_n = \frac{L_m}{L_r} \quad \text{(A.2)}$$

$$L_{n_{diodos}} = \frac{133.94499 \cdot 10^{-6}}{161.3795 \cdot 10^{-6}} \leftrightarrow L_{n_{diodos}} = 0.83$$

$$L_{n_{HEMT's}} = \frac{136.615 \cdot 10^{-6}}{164.5966 \cdot 10^{-6}} \leftrightarrow L_{n_{HEMT's}} = 0.83$$

Quality factor at full load

$$Q_e = \frac{1}{R_e} \cdot \sqrt{\frac{L_r}{C_r}} \quad \text{(A.3)}$$

$$Q_{e_{diodos}} = \frac{1}{68.119} \cdot \sqrt{\frac{161.3795 \cdot 10^{-6}}{13.5853 \cdot 10^{-9}}} \leftrightarrow Q_{e_{diodos}} = 1.6$$

$$Q_{e_{HEMT's}} = \frac{1}{69.4769} \cdot \sqrt{\frac{164.5966 \cdot 10^{-6}}{13.3199 \cdot 10^{-9}}} \leftrightarrow Q_{e_{HEMT's}} = 1.6$$

Quality factor at 110% overload

$$Q_e = \frac{1}{1.1 \cdot R_e} \cdot \sqrt{\frac{L_r}{C_r}} \quad \text{(A.4)}$$

$$Q_{e_{diodos_{overload}}} = \frac{1}{1.1 \cdot 68.119} \cdot \sqrt{\frac{161.3795 \cdot 10^{-6}}{13.5853 \cdot 10^{-9}}} \leftrightarrow Q_{e_{diodos_{overload}}} = 1.4545$$

$$Q_{e_{HEMT's_{overload}}} = \frac{1}{1.1 \cdot 69.4769} \cdot \sqrt{\frac{164.5966 \cdot 10^{-6}}{13.3199 \cdot 10^{-9}}} \leftrightarrow Q_{e_{HEMT's_{overload}}} = 1.4545$$

Step 7- Design the output filter elements

$$C_o \geq \frac{I_o}{8 \cdot f_{sw} \cdot V_o \cdot \frac{\Delta V_o}{100}} \quad \text{(3.15)}$$

$$L_o \geq \frac{V_o \cdot \Delta V_o}{I_o \cdot \Delta I_o \cdot 2 \cdot \pi \cdot F_{sw}} \quad \text{(A.16)}$$

$$C_o \geq \frac{55}{8 \cdot 107488 \cdot 75.6 \cdot \frac{0.5}{100}} \leftrightarrow C_{o_{Diodes}} \geq 169.21uF$$

$$L_o \geq \frac{75.5 \cdot 0.5}{55 \cdot 5.5 \cdot 2 \cdot \pi \cdot 107488} \leftrightarrow L_{o_{Diodes}} \geq 184.779nH$$

2. LLC Resonant Converter Loss Calculation

Losses are present in every system and to obtain an approximated efficiency, those must be known. This appendix will present, a detailed loss calculation of the half-bridge converter, as well the full-bridge, presenting in the final of each converter design a table with all the components used, as well the calculated losses in every block.

2.1. LLC Resonant Converter half-bridge

Mentioned in the beginning, the main objective of this work is the optimization of the converter presented in [1]. The component used in it will be presented Table A. 2.1. Table A. 2.2 presents the calculated losses for the half-bridge resonant converter

Table A. 2.1 LLC converter component list with associated details to loss calculation

Component name	Design	Description	Details
Inverter Switches	Base	GS66516T	$R_{DS_{(ON)}} = 0.025\,\Omega$ $Q_g = 5.8\,nC$
	Optimized	GS-065-150-1-D	$R_{DS_{(ON)}} = 0.01\,\Omega\ Q_g = N.A$
Series inductance	Base	Custom	$L = 40.35\,\mu H\ R_{L_r} = 40.052\,m\Omega$
	Optimized	HA55L-3623400LF	$L = 40\,\mu H\ R_{L_r} = 5.7\,m\Omega$
Series Capacitance	Base	Not mentioned	$C = 54.34\,nF\ ESR = N.A$
	Optimized	B85121A2503B250	$C = 50\,nF\ ESR = N.A$
High Frequency Transformer		Frenetic Half-bridge Full-bridge Design	$P_{cu} = 9.55\,W\ \ P_{core} = 7.55\,W$
		Frenetic Half-bridge Full-bridge Design	$P_{cu} = 9.55\,W\ \ P_{core} = 7.55\,W$
High Frequency Rectifying Element		STPS160H100TV	$R_d = 0.0015\,\Omega\ V_f = 0.68\,V\ C_{jr} = 1\,nC$
		GS-065-150-1-D	$R_{DS_{(ON)}} = 0.01\,\Omega\ Q_g = N.A$
		GS61008T	$R_{DS_{(ON)}} = 0.007\,\Omega$ $Q_g = 238\,pC$
Output Filter Capacitance	Base	Not mentioned	$C = 180\,uF\ ESR = N.A$
	Optimized	861011483007	$C = 180\,uF\ ESR = N.A$
Output Filter Inductance	Base	Custom	$L = 170\,nH\ R_{L_o} = 2.688\,m\Omega$
	Optimized	PA4344.471ANLT	$L = 170\,nH\ R_{L_o} = 0.7\,m\Omega$

2.1.1. Inverter Block

1) Conduction losses

$$I_{DS} = \frac{I_o \cdot \sqrt{2}}{n}$$

$$I_{DS_{rms}} = \frac{I_{DS} \cdot \sqrt{DT}}{\sqrt{2}} \quad (4.4)$$

$$P_{H_{Fw}} = {I_{DS_{rms}}}^2 \cdot R_{DS_{(ON)}} \quad (4.3)$$

$$I_{DS} = \frac{55 \cdot \sqrt{2}}{3.90958} = 19.8952A$$

$$I_{DS_{rms}} = \frac{19.8952 \cdot \sqrt{0.5}}{\sqrt{2}} = 9.9476\ A$$

$$P_{H_{Fw}} = (9.9476^2 \cdot 0.025) = 2.47387\ W$$

2) Driving losses

$$P_{H_{Dr}} = Q_g \cdot V_{GS} \cdot f_{sw}$$

$$P_{H_{Dr}} = 5.8 \cdot 10^{-9} \cdot 6 \cdot 107488 = 3.74058mW$$

Summing both conduction and switching losses, and knowing that in one period both switches conduct, the total inverter losses will be equal to $P_{HEMT's} = 4.9552\ W$

2.1.2. Resonant tank

1) Series inductance L_r

- Cooper losses

$$I_{oe,p} = \frac{I_0 \cdot \pi}{2 \cdot \sqrt{2} \cdot n} \quad (4.7)$$

$$I_m = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_{B_{nom}}}{2 \cdot \pi \cdot f_{sw} \cdot L_m} \quad (4.8)$$

$$I_{L_r} = \sqrt{{I_m}^2 + {I_{oe,p}}^2} \tag{4.9}$$

$$P_{cu_{L_r}} = R_{L_r} \cdot {I_{L_r}}^2 \tag{4.10}$$

$$I_{oe,p} = \frac{55 \cdot \pi}{2 \cdot \sqrt{2} \cdot 3.90958} = 15.6256\ A$$

$$I_m = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{3.90958 \cdot 75.6}{2 \cdot \pi \cdot 107488 \cdot 33.486 \cdot 10^{-6}} = 11.7664\ A$$

$$I_{L_r} = \sqrt{11.7664^2 + 15.6256^2} = 19.5604\ A$$

$$P_{cu_{L_r}} = 0.040052 \cdot 19.4228^2 = 15.1094\ W$$

Core losses

$$B_{ac|HF} = \frac{L \cdot I_{ac|HF}}{A_e \cdot n}$$

$$P_{core} = c \cdot f^x \cdot (B_{ac|HF})^y \cdot V_e$$

Looking at [1], core material or Steinmetz coefficients, are not available, leading us to considerer only copper losses, resulting in :

$$P_{L_r\,total} = 15.1094\ W$$

2) Series Capacitance C_r

$$P_{C_r} = ESR \cdot {I_{rms}}^2 \tag{4.14}$$

Due to the lack of information about C_r losses can not be calculated.

3) Transformer

As the design of the transformer was made using the optimization tool the losses made by it are already calculated obtaining the following data:

- Cooper losses, $P_{cu} = 9.55\ W$
- Core losses, $P_{core} = 7.55\ W$

Resulting in a total of $P_{transformer} = 17.1\ W$

2.1.3. High-frequency rectification network

Full bridge configuration allows devices with half the nominal voltage, and because of that it is possible to use devices with lower $R_{DS_{on}}$. In this case, the schottky diodes will be kept the same, as a better component was not found.

1) Conduction losses

$$P_{D_{Cond}} = {I_f}_{rms}^{\,2} \cdot R_d + V_{f\,d} \cdot I_{f\,Avg} \tag{4.16}$$

$$I_{max} = n \cdot I_{oe,p} \cdot \sqrt{2}$$

$$I_{f\,Avg} = \frac{2 \cdot I_{max}}{\pi} \cdot DT \tag{4.17}$$

$$I_{f\,RMS} = I_{max} \cdot \sqrt{\frac{DT}{2}} \tag{4.18}$$

$$I_{max} = 3.90958 \cdot 15.6256 \cdot \sqrt{2} = 86.3936\ A$$

$$I_{f\,Avg} = \frac{2 \cdot 86.3936}{\pi} \cdot 0.5 = 27.4999\ A \tag{4.17}$$

$$I_{f\,RMS} = 86.3936 \cdot \sqrt{\frac{0.5}{2}} = 43.1968\ A \tag{4.18}$$

$$P_{D_{Cond}} = 43.1968^2 \cdot 0.0015 + 0.68 \cdot 27.4999 = 21.4989\ W \tag{4.16}$$

2) Switching losses

$$P_{D_{Sw}} = \frac{1}{2} \cdot C_{jr} \cdot {V_R}^2 \cdot f_{sw} \tag{3.42}$$

$$P_{D_{Sw}} = \frac{1}{2} \cdot 1 \cdot 10^{-9} \cdot 75.6^2 \cdot 107488 = 307.166\ mW$$

Summing both conduction and switching losses and knowing that, in the full-bridge configuration, two diodes simultaneously conduct, the total rectification losses will be equal to $P_{Total_{diode_{loss}}} = 43.6121 \ \ W$

2.1.4. Output Filter

1) Output filtering inductance L_o

- Cooper losses

$$P_{cu_{L_o}} = R_{L_o} \cdot I_o^2 \tag{4.10}$$

$$P_{cu_{L_o}} = 0.002688 \cdot 55^2 = 8.1312 \ W \tag{4.10}$$

- Core losses

$$B_{ac|HF} = \frac{L \cdot I_{ac|HF}}{A_e \cdot n}$$

$$P_{core} = c \cdot f^x \cdot (B_{ac|HF})^y \ \cdot V_e$$

Looking at [1], core material or Steinmetz coefficients, are not available, leading us to considerer only copper losses, resulting in :

$$P_{L_{o_{total}}} = 8.1312 \ \ W$$

2) Output filtering Capacitance C_o

$$P_{C_r} = ESR \cdot {I_{Co}}^2 \tag{4.14}$$

For this application, the Electrolytic Capacitor 861011483007, was chosen, but in the manufacturer datasheet, there is not the ESR, disallowing the loss calculation in this component.

Table A. 2.2 - Detailed analytical losses from the half-bridge converter design

Converter description	Inverter Switches (W)	Series inductance (W)	Transformer (W)	Rectifying elements (W)	Filter inductance (W)	Total (W)
HF-CT Base	4,9552	15,109	24,07	43,6121	8,1312	95,878

HF-CT Schottky	1,979	2,1809	24,07	21,8061	2,1175	52,153
HF-CT HEMT	1,9404	2,1322	24,07	18,6598	2,1175	48,92
HF-FB Schottky	1,979	2,1809	17,1	43,6121	2,1175	66,989
HF-FB HEMT	1,9404	2,1322	17,1	26,14	2,1175	49,43

2.2. Full-Bridge LLC resonant Converter

From the previous design, the required components were selected being described in Table A. 2.3, and Table A. 2.4 presents all the analytical calculated losses.

Table A. 2.3 - LLC converter component list with associated details to loss calculation

Component name	Description	Details
Inverter Switches	GS-065-150-1-D	$R_{DS_{(ON)}} = 0.01\ \Omega\ Q_g = N.A$
Series inductance	ECS-HCMPI-0503Q-R16M	$L = 160\ \mu H\ R_{L_r} = 2.33\ m\Omega$
Series Capacitance	SFJNL2K00103MX1	$C = 10\ nF\ ESR = N.A$
High Frequency Transformer	Frenetic Half-bridge center-tapped Design	$P_{cu} = 4.11\ W\ \ P_{core} = 19.02\ W$
	Frenetic Half-bridge Full-bridge Design	$P_{cu} = 9.81\ W\ \ P_{core} = 8.43\ W$
High Frequency Rectifier Diode	STPS160H100TV	$R_d = 0.0015\ \Omega\ V_f = 0.68\ V$ $C_{jr} = 1\ nC$
	GS-065-150-1-D	$R_{DS_{(ON)}} = 0.01\ \Omega\ Q_g = N.A$
	GS61008T	$R_{DS_{(ON)}} = 0.007\ \Omega\ Q_g = 238\ pC$
Output Filter Capacitance	861011483007	$C = 180\ uF\ ESR = N.A$
Output Filter Inductance	PA4344.471ANLT	$L = 170\ nH\ R_{L_o} = 0.7\ m\Omega$

2.2.1. Inverter Block

1) Conduction losses

$$I_{DS} = \frac{I_o \cdot \sqrt{2}}{n}$$

$$I_{DS_{rms}} = \frac{I_{DS} \cdot \sqrt{DT}}{\sqrt{2}} \quad (4.4)$$

$$P_{H_{Fw}} = {I_{DS_{rms}}}^2 \cdot R_{DS_{(ON)}} \quad (4.3)$$

$$I_{DS} = \frac{55 \cdot \sqrt{2}}{7.81915} = 9.9476A$$

$$I_{DS_{rms}} = \frac{9.9476 \cdot \sqrt{0.5}}{\sqrt{2}} = 4.9738\ A$$

$$P_{H_{Fw}} = (4.9738^2 \cdot 0.01) = 247.387\ mW$$

1) Driving losses

$$P_{H_{Dr}} = Q_g \cdot V_{GS} \cdot f_{sw}$$

The datasheet of the component does not provide the gate charge, and because of that, driving losses ca not be calculated. As the full bridge topology uses two switches at the same time the total inverter losses will be $P_{H_{Fw}} = 0.494774$

2.2.2. Resonant tank

1) Series inductance L_r

- Cooper losses

$$I_{oe,p} = \frac{I_0 \cdot \pi}{2 \cdot \sqrt{2} \cdot n} \quad (4.7)$$

$$I_m = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{n \cdot V_{B_{nom}}}{2 \cdot \pi \cdot f_{sw} \cdot L_m} \quad (4.8)$$

$$I_{L_r} = \sqrt{{I_m}^2 + {I_{oe,p}}^2} \quad (4.9)$$

$$P_{cu_{L_r}} = R_{L_r} \cdot {I_{L_r}}^2 \quad (4.10)$$

$$I_{oe,p} = \frac{55 \cdot \pi}{2 \cdot \sqrt{2} \cdot 7.81915} = 7.81282\ A$$

$$I_m = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{7.81915 \cdot 75.6}{2 \cdot \pi \cdot 107488 \cdot 133.94499 \cdot 10^{-6}} = 5.88315\ A$$

$$I_{L_r} = \sqrt{5.88315^2 + 7.81282^2} = 9.78016\ A$$

$$P_{cu_{L_r}} = 0.00233 \cdot 9.78016^2 = 222.868\ mW$$

- *Core losses*

$$B_{ac|HF} = \frac{L \cdot I_{ac|HF}}{A_e \cdot n}$$

$$P_{core} = c \cdot f^x \cdot (B_{ac|HF})^y \cdot V_e$$

To calculate core losses, Steinmetz coefficients $c,\ x$ and y of the core material are required. Looking at manufacturer datasheet, the core material or Steinmetz coefficients, are not available, leading us to considerer only copper losses, resulting in :

$$P_{L_{r\,total}} = 222.868\ mW$$

2) Series Capacitance C_r

$$P_{C_r} = ESR \cdot {I_{RMS}}^2 \tag{4.14}$$

For this application, the polypropylene Feedthrough Capacitor SFJNL2K00103MX1, was chosen, but in the manufacturer, there is not the ESR, disallowing the loss calculation in this component

4) Transformer

As the design of the transformer was made using the optimization tool the losses made by it are already calculated obtaining the following:

- Cooper losses, $P_{cu} = 4.11\ W$
- Core losses, $P_{core} = 19.02\ W$

Resulting in a total of $P_{transformer} = 23.13\ W$

2.2.3. High-frequency rectification network

Full bridge configuration allows devices with half the nominal voltage, and because of that it is possible to use devices with lower $R_{DS_{on}}$. In this case,

the schottky diodes will be kept the same, as a better component was not found, but in the synchronous rectification, the GS61008T will replace the GS-065-150-1-D

1) Conduction losses

$$P_{D_{Cond}} = {I_f}_{RMS}^{\,2} \cdot R_d + V_{f\,d} \cdot {I_f}_{Avg} \tag{4.16}$$

$$I_{max} = n \cdot I_{oe,p} \cdot \sqrt{2}$$

$${I_f}_{Avg} = \frac{2 \cdot I_{max}}{\pi} \cdot DT \tag{4.17}$$

$${I_f}_{RMS} = I_{max} \cdot \sqrt{\frac{DT}{2}} \tag{4.18}$$

$$I_{max} = 7.81915 \cdot 7.81282 \cdot \sqrt{2} = 86.3938\ A$$

$${I_f}_{Avg} = \frac{2 \cdot 86.3938}{\pi} \cdot 0.5 = 27.5\ A \tag{4.17}$$

$${I_f}_{RMS} = 86.3938 \cdot \sqrt{\frac{0.5}{2}} = 43.1969\ A \tag{4.18}$$

$$P_{D_{Cond}} = 43.1969^2 \cdot 0.0015 + 0.68 \cdot 27.5 = 21.5\ W \tag{4.16}$$

1) Switching losses

$$P_{D_{Sw}} = \frac{1}{2} \cdot C_{jr} \cdot {V_R}^2 \cdot f_{sw} \tag{3.42}$$

$$P_{D_{Sw}} = \frac{1}{2} \cdot 1 \cdot 10^{-9} \cdot 75.6^2 \cdot 107488 = 307.166\ mW$$

Summing both conduction and switching losses and knowing that, in the center-tapped configuration, only one of the diodes conduct at the time, the total rectification losses will be equal to $P_{Total_{diode_{loss}}} = 21.8078\ \ W$.

2.2.4. Output Filter

1) Output filtering inductance L_o

- Cooper losses

$$P_{cu_{L_o}} = R_{L_o} \cdot I_o^2 \quad (4.10)$$

$$P_{cu_{L_o}} = 0.0007 \cdot 55^2 = 2.1175\ W \quad (4.10)$$

- *Core losses*

$$B_{ac|HF} = \frac{L \cdot I_{ac|HF}}{A_e \cdot n}$$

$$P_{core} = c \cdot f^x \cdot (B_{ac|HF})^y \cdot V_e$$

To calculate core losses, Steinmetz coefficients $c,\ x$ and y of the core material are required. Looking at manufacturer datasheet, the core material or Steinmetz coefficients, are not available, leading us to considerer only copper losses, , resulting in :

$$P_{L_o\,total} = 2.1175\ W$$

1) Output filtering Capacitance C_o

$$P_{C_r} = ESR \cdot {I_{Co}}^2 \quad (4.14)$$

For this application, the Electrolytic Capacitor 861011483007, was chosen, but in the manufacturer datasheet, there is not the ESR, disallowing the loss calculation in this component.

Table A. 2.4 - Detailed analytical losses from the half-bridge converter design

Converter description	Inverter Switches (W)	Series inductance (W)	Transformer (W)	Rectifying elements (W)	Filter inductance (W)	Total (W)
FB-CT Schottky	0,4948	0,2287	23,13	21,8061	2,1175	47,777
FB-CT HEMT	0,4803	0,2179	23,13	18,6598	2,1175	44,605
FB-FB Schottky	0,4948	0,2287	18,24	43,6121	2,1175	64,693
FB-FB HEMT	0,4803	0,2179	18,24	26,14	2,1175	47,196