Optimized Modulation and Thermal Management for Modular Power Converters

Dissertation

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«What we know is a drop, what we don't know is an ocean.»
Isaac Newton

Acknowledgement

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Deutsche Kurzfassung der Arbeit

Der Übergang zu einer dezentralen Stromerzeugung mit erneuerbaren Energien ist mit großen Herausforderungen verbunden. Modulare Stromrichter spielen eine zentrale Rolle zur Bewältigung dieser, nicht nur zur Netzintegration, sondern auch für flexible Netzservices, zur hocheffizienten Leistungsübertragung und zur sicheren Speicherintegration. Diese Ziele sind zentral, um in Zukunft unabhängig von fossilen und nuklearen Kraftwerken zu werden.

Auch wenn die Kosten für erneuerbare Energien aus Wind oder Fotovoltaik bereits wettbewerbsfähig ggü. konventionellen Lösungen sind, sind ein flexiblerer Betrieb und weitere Kostensenkungen für eine schnelle globale Transformation zu nachhaltigen Energiesystemen erforderlich. Die Optimierung modularer Stromrichter kann als ein idealer Weg gesehen werden, diese ehrgeizigen Ziele zu erreichen, und steht im Mittelpunkt dieser Arbeit.

Parallele Neutral-Point-Clamped (NPC) Stromrichter werden als vielversprechende Lösung zum Anschluss hoher Leistungen über Transformatoren ans Stromnetz vorgestellt. Demgegenüber wird der MMC (engl.: Modular Multilevel Converter) als bevorzugte Lösung zum direkten Anschluss ans Mittel- (MS) und Hochspannungsnetz (HS) angesehen. Beide Lösungen werden für hohe Wirkungsgrade und ein ökonomisches Design untersucht. Zudem ist ein detaillierter Vergleich für den MMC mit Halb- und Vollbrücken durchgeführt.

Einer der Hauptvorteile modularer Stromrichter zur optimierten Modulation liegt in der Mehrstufigkeit, die eine Vielzahl an redundanten Schaltzuständen birgt. Zum einen wird die verzahnte (engl.: interleaved) Modulation für parallele NPC-Stromrichter untersucht, um Kreisströme bei geringen Schaltfrequenzen stark zu reduzieren. Zum anderen wird eine fundamentale Schaltfrequenz für beide MMC-Konfigurationen erzielt, bei Wirkungsgraden von über 99 % in MS- und HS-Systemen. Dank des hohen Wirkungsgrads und der exzellenten Leistungsqualität ist der MMC die bevorzugte Wahl zur Wandlung hoher Leistungen.

Der MMC verfügt gewöhnlich über eine hohe Anzahl von Submodulen (SM), verknüpft mit sehr vielen Leistungshalbleitern und Kondensatoren. Für deren optimierte Auslegung und Nutzung wird ein allgemeines thermisches Management für beide SM-Topologien vorgestellt, beruhend auf Echtzeitschätzungen aus verfügbaren Sensordaten. Es werden verschiedene Algorithmen zur Mehrzieloptimierung vorgestellt, die von der hohen Zahl redundanter Schaltzustände profitieren, ohne Leistung und Wirkungsgrad zu verringern. Die thermische Belastung wird für Leistungshalbleiter und Kondensatoren erfolgreich reguliert und eröffnet hohes Potenzial zum wirtschaftlichen Design. Auch wird eine hohe Überlastfähigkeit erreicht, und die Lebensdauer der Halbleiter wird etwa verdoppelt, z.B. für längere Wartungsintervalle.

Für die thermische Bewertung und Zyklierung wird ein universeller Teststand entwickelt und vorgestellt, der den Fokus auf jedes einzelne SM des MMC legt. Er wird beispielhaft für die Emulation einer HS-Anwendung verwendet, bei der eine genaue Prüfung und Überwachung des Systems aus praktischer und wirtschaftlicher Sicht nicht sinnvoll ist. Mithilfe des Versuchsstandes werden Hotspots und thermische Zyklen der realen Anwendung identifiziert und können über das Design und durch thermisches Management optimiert werden.

English Summary

The transition to a more and more decentralized power generation based on renewable energy generation is accompanied by high challenges. Modular power converters play a central role in facing these challenges, not only for grid integration but also to provide flexible services, highly efficient power transmission and safe storage integration. These goals are the key elements in becoming independent from fossil and nuclear power plants in near future.

Even if the costs for renewable energy power plants like wind or photovoltaic systems are already competitive to conventional solutions, more flexible operation and further reduction in costs are required for faster global transformation towards sustainable energy systems. The further optimization of modular power converters can be seen as an ideal way to achieve these ambitious goals. It is therefore chosen as the focus of this work.

Parallel neutral-point clamped (NPC) inverters are presented as the most promising solution for connecting high powers to the electrical grid by classical transformers. In contrast to this, the modular multilevel converter (MMC) is identified as the most suitable solution for direct connection to the medium voltage (MV) and high voltage (HV) grid. Both solutions are investigated for high efficiencies and an economical design. A detailed comparison for the MMC is provided as well, for the equipment of chopper-cells and bridge-cells.

One of the main benefits of modular converters for optimized modulation is found in their multilevel waveform generation, providing a high number of redundant switching states. On the one hand, interleaved modulation is investigated for parallel NPC inverters, strongly reducing circulating currents at limited switching frequencies. On the other hand, even fundamental switching operation is achieved for both MMC configurations, obtaining efficiencies of above 99 % in MV and HV applications. Due to its high efficiency and its high power quality the MMC is identified as the preferred choice for high power conversion.

The MMC usually provides a high number of submodules (SM), being linked to a huge number of power devices and capacitors. For their optimized design and utilization, a generalized thermal management is presented in this work for both SM topologies, taking into account real-time estimations based on available sensor data. Different algorithms for multi-objective optimization are introduced by profiting from the huge number of redundant switching states without deteriorating the system performance and efficiency. The thermal stress is effectively regulated for both the power devices and the capacitors, revealing a high potential for a more economical design. Furthermore, high overload capability is achieved and the semiconductor lifetimes are approximately doubled for extended maintenance intervals.

For thermal evaluation and cycling a universal experimental bench is developed and introduced, putting the focus on each single SM of the MMC. It is used exemplary for the emulation of an HV application where accurate testing and monitoring of the full system would be reasonable from neither practical nor economical point of view. By means of the presented experimental bench hotspot temperatures and thermal cycles from the real application are identified and can be optimized by design decisions and thermal management approaches.

Used symbols and abbreviations

General symbols

General symbols

$v(t)$, v	Instantaneous value
V	Root mean square (rms) value
$\hat{v}$	Sinusoidal amplitude
$\bar{v}$	Mean vale

Superscripts

$*$	Reference value
3rd	Applied third harmonic injection
100 Hz	Related to a specific frequency, here 100 Hz
55 %	Relative value, here 55 %
dead_time	Deadtime taken into account
LV	Low voltage
MV	Medium voltage

Subscripts

a	Phase a
arm	Arm related
b	Phase b
BC	Bridge-cell related
c	Phase c
cap	Capacitor related
C	Case related
CC	Chopper-cell related
coupl	Coupled
dc	DC-link related
D	Diode related
exc	Grid excitation
H	Heatsink related
jc	Junction to case
lim	Limitation
max	Maximum value
min	Minimum value

n	Lower arm
nom	Nominal
off	Turn off
on	Turn on
p	Upper arm
prim	Primary side related
φ	Phase shift between grid voltage and current
rat	Rating
sc	Short-circuit
sec	Secondary side related
sm	Submodule related
T	IGBT related
th	Thermal
total	In total
trafo	Transformer related
人	Star configuration

Special symbols

0	Related to specific test conditions (reference)
A	Area
a_1, a_2, a_3	Fitting parameters for semiconductor lifetime model
av	Averaged
α	Weighting factor
C	Capacitance
C_m	Cummulated damage
C_{th}	Thermal capacitance
c	Cost function
$\vec{D}$	Electric flux density
d	Duty cycle
d_s	Distance
ΔT_j	Magnitude of a thermal cycle (junction)
$\vec{E}$	Electric field strength
E_a	Activation energy
E_{cap}	Total stored energy in capacitors
ε_0	Vacuum permittivity
ε_r	Relative permittivity
f_c	PWM carrier frequency
f_m	Current frequency
f_g	Grid frequency
f_s	Sampling frequency

ϕ	Electric potential
i_{cap}	Capacitor current
i_{circ}	Circulating current
i_{conv}	Converter current
i_{dc}	DC-side current
i_{diff}	Differential current
i_{f}	Diode current
i_{g}	Grid current
i_{n}	Lower arm current
i_{p}	Upper arm current
k	Sampling step
K_{B}	Boltzmann's constant ($K_{\mathrm{B}} = 1.380649 \cdot 10^{23} J \cdot K^{-1}$)
L_{arm}	Arm inductance
L_{cable}	Cable inductance
L_{conv}	Converter filter inductance
L_{esl}	Equivalent series inductance
L_{f}	Expected lifetime
L_{filter}	Equivalent filter inductance
L_g	Grid inductance
L_{line}	Line filter inductance
m	Modulation index
N	Number of submodules per arm
N_{f}	Number of thermal cycles to failure
n_{i}	Number of thermal cycles in the stress range i
N_{i}	Number of thermal cycles to failure in the stress range i
n_{v}	Voltage stress exponent (capacitors)
$n_{\mathrm{off,N}}$	Number of bypassed full-bridge submodules (state 1)
$n_{\mathrm{off,P}}$	Number of bypassed full-bridge submodules (state 2)
n_{on}	Number of inserted half-bridge submodules
$n_{\mathrm{on,N}}$	Number of inserted full-bridge submodules (negative voltage)
$n_{\mathrm{on,P}}$	Number of inserted full-bridge submodules (positive voltage)
n_{off}	Number of bypassed half-bridge submodules
N_{p}	Number of turns in primary winding
N_{s}	Number of turns in secondary winding
P_{g}	Active power to the grid
P_{l}	Power losses
$P_{\mathrm{l,con}}$	Conduction power losses
$P_{\mathrm{l,sw}}$	Switching power losses
Q_{cap}	Capacitor charge
Q_{g}	Reactive power exchange with the grid
Q_{rr}	Reverse recovery charge
R_{arm}	Arm resistor
R_{esr}	Equivalent series resistance

r_f	Differential diode resistance
R_p	Insulation resistance
R_{th}	Thermal resistance
S_g	Apparent power to the grid
t	time
T	Temperature
T_a	Ambient temperature
T_c	Case temperature
T_j	Junction temperature
T_R	Transformer turns ratio
t_{rr}	Diode blocking delay time
u	Short-circuit voltage
v_{cap}	Capacitor voltage
v_{ce}	Collector-emitter voltage
v_{cm}	Common-mode voltage
v_{conv}	Converter voltage
V_{dc}	DC-link voltage
v_{diff}	Differential voltage
v_f	Diode voltage
v_{f0}	Diode forward voltage
v_g	Grid voltage / transformer voltage
$v_{L,arm}$	Voltage drop across arm inductances
$v_{L,conv}$	Voltage drop across converter filter inductance
$v_{L,line}$	Voltage drop across line filter inductance
$v_{L,trafo}$	Voltage drop across transformer inductance
v_{mod}	Voltage reserve for modulation/control
v_n	Lower arm voltage
v_p	Upper arm voltage
v_{phase}	Phase voltage
V_R	Diode breakdown voltage
v_{req}	Required converter voltage
v_{phase}	Phase voltage
v_{sm}	Terminal voltage at the SM
Z_g	Grid impedance
Ψ_g	Grid impedance angle

Abbreviations

AC	Alternating Current
APOD	Alternative Opposition Disposition
BC	Bridge-Cell (full-bridge)
CC	Chopper-Cell (half-bridge)
CHB	Cascaded H-Bridge Converter
CVB	Capacitor Voltage Balancing
DBC	Direct Bound Copper
DC	Direct Current
DFIG	Double-Fed Induction Generator
DUT	Device-Under Test
ESR	Equivalent Series Resistor
ESL	Equivalent Series Inductance (L)
FACT	Flexible AC Transmission Systems
FC	Flying Capacitor
FPGA	Field Programmable Gate Array
HV	High Voltage
HVDC	High Voltage Direct Current
IGBT	Insulated-Gate Bipolar Transistor
IGTC	Integrated Gate-Commutated Thyristors
IR	Infrared
LV	Low Voltage
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MV	Medium Voltage
MVDC	Medium Voltage Direct Current
MMC	Modular Multilevel Converter
MPPF	Metalized Polypropylene Film
NLM	Nearest Level Modulation
NPC	Neutral Point Clamped
PET	Polyethylene Terephtalate
PD	Phase Disposition
PK	Press-Pack
POD	Phase Opposition Disposition
PP	Polypropylene
PS	Phase-Shifted
PWM	Pulse-Width Modulation
PV	Photovoltaic
RMS	Root Mean Square
SG	Synchronous Generator
ST	Smart Transformer
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion

1 Introduction

This chapter shows the motivation for using modular power converters in high-power applications and defines the research proposals of the thesis. It also provides the structure of the thesis and the publications related to the different sections.

At the UN Climate Change Conference in Paris in 2015, 197 countries agreed for the first time on a global climate agreement to limit the global warming below $2\,°C$. Achieving the defined climate targets demands high efforts from economical and technical point of view around the globe. The wide integration of renewable energy systems for a decarbonization of the energy production is accompanied by high challenges. The inertia of big rotating masses from classical large-scale power plants needs to be compensated. However, the power generation from renewable energy systems is linked to high fluctuating powers. Furthermore, high generated energies need to be transmitted from renewable energy sources (e.g. offshore wind farms) to the high-power consumers (e.g. factories). All these points are linked to important challenges for both the energy management and the grid infrastructure. Existing solutions like disconnecting renewable energy systems from the grid for safety reasons are not further reasonable from economical and ecological point of view to compensate high production and low consumption, as it is common practice.

High power solutions are required for replacing conventional fossil and nuclear plants towards a more and more decentralized distribution grid by renewable energy systems. High power solutions need to be provided not only for the grid integration of renewable energy systems but also to enable flexible and high-efficient transmission solutions. Furthermore, more energy storage capability needs to be integrated into the distribution grid e.g. based on batteries or sector coupling (e.g. hydrogen) for an improved load management, for potential island mode operation and for providing black start capability in case of unforeseen network outages. Furthermore, flexible grid services are from high importance regarding the maximization of the grid capacity for renewable energy systems in existing grids, also taking into account the network structure and properties.

1.1 Motivation

The motivations for using modular power converters and for high-power applications are provided in this section, to face the aforementioned challenges, highlighting their importance and potential for suitable integration of more and more renewable energy generation.

1.1.1 Modular Power Converters

Modular power converters play a central role for the successful transition to a more and more decentralized distribution grid based on renewable energy systems. They provide flexible and highly efficient solutions for proper grid integration, for high efficiency power transmission solutions, for storage integration and for flexible grid support.

Modular power converters especially profit from high power capabilities based on standard semiconductor components. Furthermore, modular building blocks provide highly redundant systems. On the one hand, such modular building blocks can be connected in series to increase the voltage ratings. On the other hand, also parallel connection is possible to increase the current ratings. Accordingly, modular power converters can be flexibly scaled within very wide power ranges for different grid voltage levels depending on the target application. For instance, based on the modular multilevel converter (MMC or M2C) power ranges into the GW range become possible by cascading hundreds of semiconductor devices for direct connection to the high voltage (HV) grid.

The modular and redundant structure of modular power topologies is also linked to possible fault tolerant operation and to fulfilling grid codes in fault ride through conditions. Furthermore, the system availability can be increased which is particularly important for reliable and economical operation of huge renewable energy systems. Beyond that, multilevel waveform generation and a high number of redundant switching states provide a high potential for high-efficient modulation techniques, for minimized filter effort and for regulation of the thermal stress by advanced thermal management approaches.

1.1.2 High-Power Applications

High-power applications are essential to replace classical big power plants for energy generation. Modular power converters already enable competitive renewable solutions and safe integration of huge renewable energy systems, e.g. based on wind or photovoltaic systems. The high potential of wind power generation is shown exemplary in Fig. 1.1. The installed power capacity has been doubled from 2013 to 2021 in Europe and offshore applications are becoming more and more relevant due to high energy generation and limited areas for onshore wind parks. In 2030 it is expected that the energy production from onshore and offshore applications is already shared.

Huge powers need to be transmitted from offshore wind farms to the mainland. For this purpose, direct current (DC) transmission systems are preferred to limit the power losses and cabling effort, being particularly crucial for maritime applications and also for transmitting very high powers over longer distances. Converter stations up into the GW range are required. In general, the development is going more and more towards higher voltages to limit rated currents, power losses and cabling effort.

The integration of high-power static synchronous compensator (STATCOM) applications is desired as well for flexible grid support to ensure a stable and effective use of available grid capacities. Ancillary services can be optimized by using the knowledge of the grid behavior and the grid characteristics. By proper grid analysis, the integration of renewable energy systems can be strongly improved.
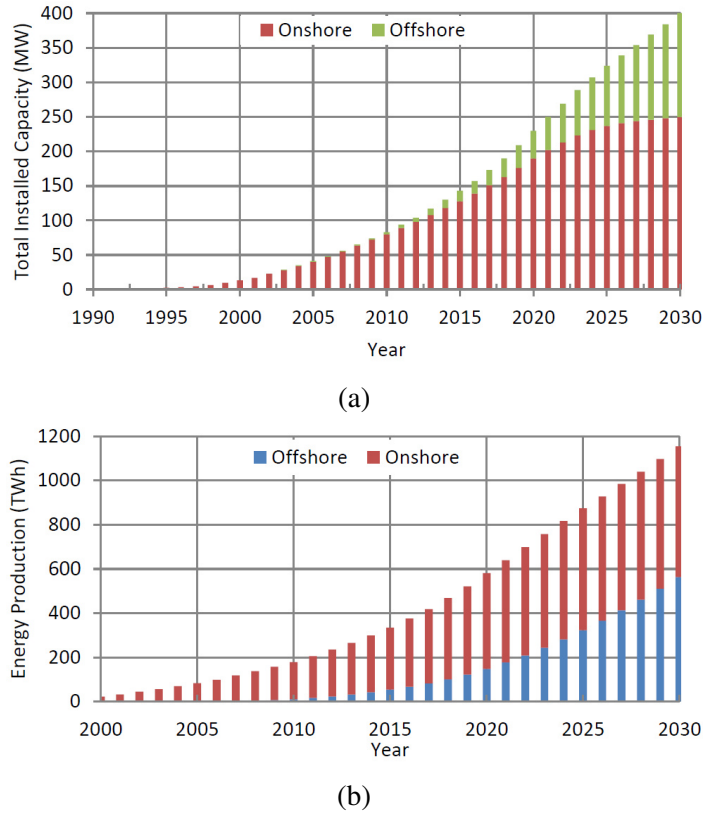
(a)

(b)

Figure 1.1: Wind energy installation and production in the European Union, projected until 2030: (a) Installed power capacity. (b) Energy production. [1]

1.2 Research Proposal

The aim of this thesis is to investigate the modulation and the thermal management for modular power converters for a wide range of high-power applications. Suitable power electronics solutions are analyzed and selected for connection to the medium voltage (MV) and HV grid. The converter performance is optimized in several study cases by improved modulation techniques. Furthermore, for an economical design and increased reliability, a generalized thermal management is developed and implemented for cascaded power converters.

Target 1: Investigation of high-power applications for improved grid integration of renewable energy systems

The first research objective is the investigation and selection of suitable high-power applications for decentralized grids which are based on renewable energy sources. A grid impedance analyzer for the MV grid is developed to determine its main characteristics for improved integration of renewable energy systems and flexible AC transmission systems (FACT). STATCOM applications are investigated for flexible grid support, providing advanced features like overload and active power filtering capability. DC transmission solutions are analyzed for a flexible and efficient transport of high-power generations, e.g. from onshore and offshore wind farms. Suitable modular power electronics solutions are investigated. It is distinguished between parallel converters for grid connection by classical step-up transformers and cascaded converters for direct connection the MV and HV grid. An experimental bench

is developed to enable electrical and thermal evaluation of modular building blocks with the goal to even emulate and validate the behavior of HV systems.

Target 2: Analysis and optimization of parallel converters in high-power applications

The second research objective is to analyze and optimize the operation of parallel power inverters. Multilevel modulation and interleaved modulation are investigated to enable small switching frequencies at a low filter effort. Parallel neutral-point clamped (NPC) inverters with a common DC link are considered as a study case where circulating currents are derived and analyzed. Suitable modulation techniques are investigated to reduce the common-mode voltages and the circulating currents between the parallel inverters. For the applications of a wind power plant and of a MV grid analyzer the potential of interleaved modulation for harmonic cancellation is demonstrated for a wide frequency range. The main research findings are validated by experimental measurements.

Target 3: Analysis and optimization of cascaded topologies in high-power applications

The third research objective is the analysis and optimization of the MMC, being equipped with cascaded chopper-cells (CC) or bridge-cells (BC). Low switching frequency modulation techniques are investigated and compared for both topologies to maximize the efficiency of the system at an economical converter design. Thermal management approaches are developed for the MMC with very high numbers of semiconductor devices and capacitor storages to achieve a cost-effective design, overload capability and extended component lifetimes. It also includes the analysis and the accurate thermal modeling of each single component by real-time condition monitoring based on available system information. Thermal management approaches are developed for both the MMC with CCs and BCs with the goal to not affect the overall performance and efficiency of the system.

1.3 Structure of the Thesis

The presented work is divided into seven chapters as illustrated in Fig. 1.2. In Chapter 2 power electronics solutions for different high-power applications are introduced, including suitable power inverter topologies as well as related technologies for semiconductor devices and capacitor storages for safe and reliable operation. In Chapter 3 suitable multilevel modulation techniques and interleaved operation are analyzed and optimized for the NPC and for the MMC, respectively. In Chapter 4 parallel LV NPC inverters are considered and optimized by the modulation for wind power applications and for a grid impedance analyzer. In Chapter 5 the MMC is optimized by modulation for direct connection to the MV and HV grid, also providing a detailed comparison for the application of CCs and BCs. Chapter 6 introduces a thermal management for the MMC with both SM topologies and an experimental bench for practical evaluation to enable an economical design, overload condition and long component lifetimes just by software implementation. Chapter 7 provides the summary and the conclusions of this work, followed by promising aspects for future research.

In addition to selected oscilloscope and infrared (IR) images, experimental results from three laboratory setups are processed in MATLAB for improved illustration and analysis, being highlighted with gray backgrounds in this work. The laboratory setups of parallel NPC inverters and the experimental bench are located at the Chair of Power Electronics of the Christian-Albrechts-Universität zu Kiel. The MMC prototype has been provided by the Department of Energy of the Aalborg University, Denmark also by supporting with the recording of measurements.

1.4 List of Publications

The scientific papers and one patent associated to this work are listed in this section.

Journal Publications

[J1] **F. Hahn**, M. Andresen, G. Buticchi and M. Liserre, "Thermal Analysis and Balancing for Modular Multilevel Converters in HVDC Applications," in IEEE Transactions on Power Electronics, vol. 33, no. 3, pp. 1985-1996, March 2018, doi: 10.1109/TPEL.2017.2691012.

[J2] Z. Zou, **F. Hahn**, G. Buticchi, S. Günter and M. Liserre, "Interleaved Operation of Two Neutral-Point-Clamped Inverters With Reduced Circulating Current," in IEEE Transactions on Power Electronics, vol. 33, no. 12, pp. 10122-10134, Dec. 2018, doi: 10.1109/T-PEL.2018.2800402.

[J3] A. Lashab, D. Sera, **F. Hahn**, L. Camurca, M. Liserre and J. M. Guerrero, "A Reduced Power Switches Count Multilevel Converter-Based Photovoltaic System With Integrated Energy Storage," in IEEE Transactions on Industrial Electronics, vol. 68, no. 9, pp. 8231-8240, Sept. 2021, doi: 10.1109/TIE.2020.3009594.

[J4] A. Lashab, D. Sera, **F. Hahn**, L. Camurca, Y. Terriche, M. Liserre and J. Guerrero, "Cascaded Multilevel PV Inverter With Improved Harmonic Performance During Power Imbalance Between Power Cells," in IEEE Transactions on Industry Applications, vol. 56, no. 3, pp. 2788-2798, May-June 2020, doi: 10.1109/TIA.2020.2978164.

[J5] A. Marquez, J. Leon, **F. Hahn**, R. Gómez-Merchán, G. Buticchi, S. Vazquez, C. Gerada, M. Liserre and L. G. Franquelo, "Power Devices Aging Equalization of Interleaved DC-DC Boost Converters via Power Routing," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, vol. 1, no. 1, pp. 91-101, July 2020, doi: 10.1109/JESTIE.2020.2999598.

[J6] S. Hansen, **F. Hahn**, H. Krueger, F. Hoffmann, M. Andresen, R. Adelung and M. Liserre, "Reliability of Silicon Battery Technology and Power Electronics Based Energy Conversion," in IEEE Power Electronics Magazine, vol. 8, no. 2, pp. 60-69, June 2021, doi: 10.1109/MPEL.2021.3075756.
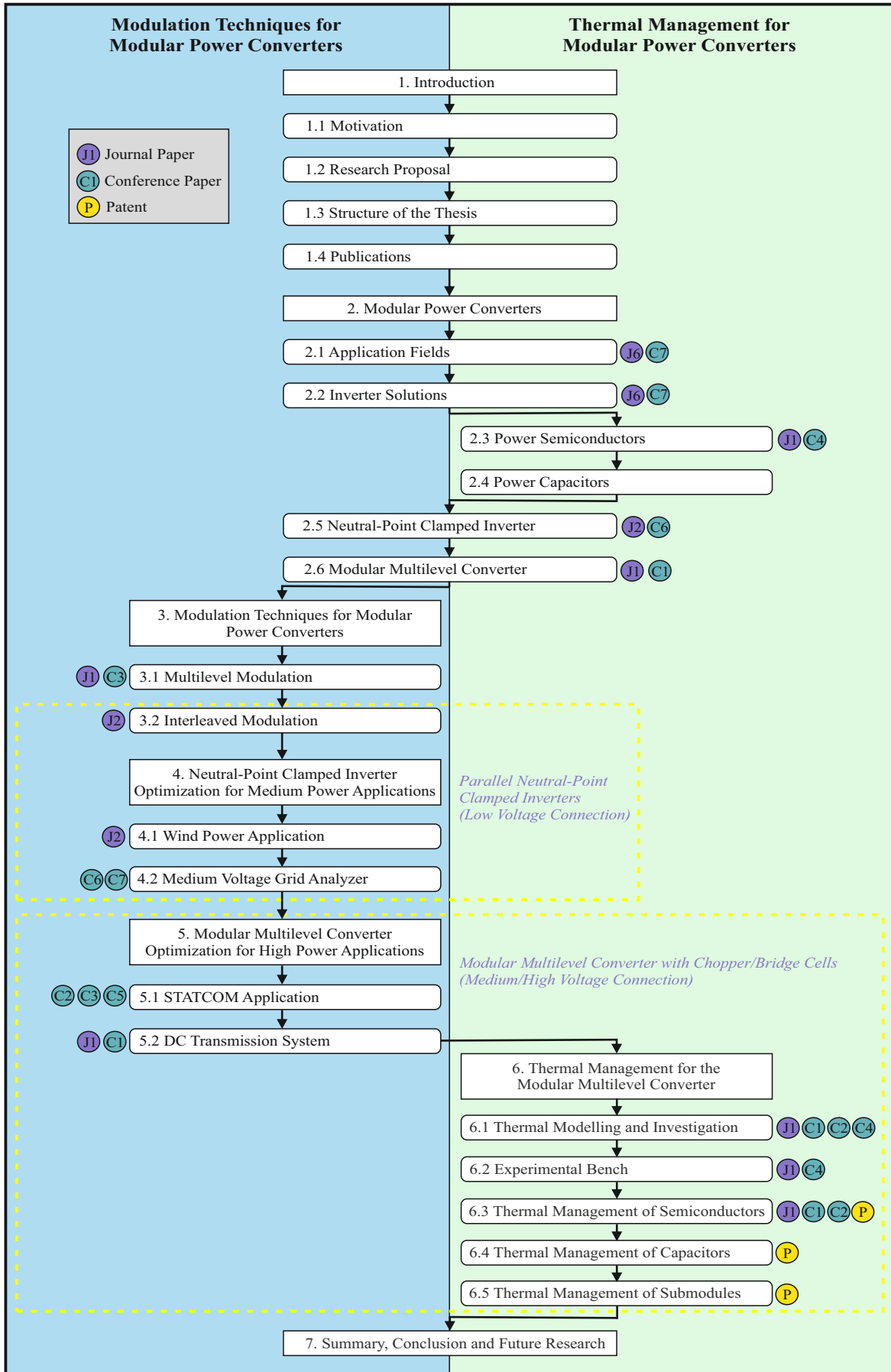
Figure 1.2: Structure of the thesis and related publications.

Conference Publications

[C1] **F. Hahn**, G. Buticchi and M. Liserre, "Active thermal balancing for modular multilevel converters in HVDC applications," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1-10.

[C2] **F. Hahn**, M. Andresen and M. Liserre, "Enhanced Current Capability for Modular Multilevel Converters by a Combined Sorting Algorithm for Capacitor Voltages and Semiconductor Losses," 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019, pp. 3071-3077.

[C3] **F. Hahn**, R. Teodorescu, G. Buticchi, M. Liserre and C. Lascu, "Impact of Modulation Methods on the Trade-Off between Investment and Operation Costs of a Medium-Voltage MMC-based STATCOM," 2018 IEEE Energy Conversion Congress and Exposition (ECCE), 2018, pp. 2924-2930.

[C4] **F. Hahn**, M. Andresen, G. Buticchi and M. Liserre, "Mission Profile Based Reliability Evaluation of Building Blocks for Modular Power Converters," PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2017, pp. 1-7.

[C5] **F. Hahn**, L. Camurca and M. Liserre, "Investigation of Modular Multilevel Converters for E-STATCOM Applications," 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), 2020, pp. 1028-1032.

[C6] **F. Hahn**, G. Buticchi, R. Teodorescu, F. W. Fuchs and M. Liserre, "Optimal Design of a Medium-Voltage Grid Analyzer," 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), 2019, pp. 1-9.

[C7] **F. Hahn**, S. Brüske, B. Benkendorff, G. Buticchi, F. W. Fuchs and M. Liserre, "Wide frequency range medium-voltage grid impedance analysis by current injection of a multi-MW power converter," 2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1-10.

Patent

[P] M. Andresen, **F. Hahn**, M. Langwasser, M. Liserre, "Energy Storage and Semiconductor related Selection of Cells in Modular Multilevel Power Converters and Computer Program," European Patent EP 3780376A1, 2019 Aug 13 (in application).
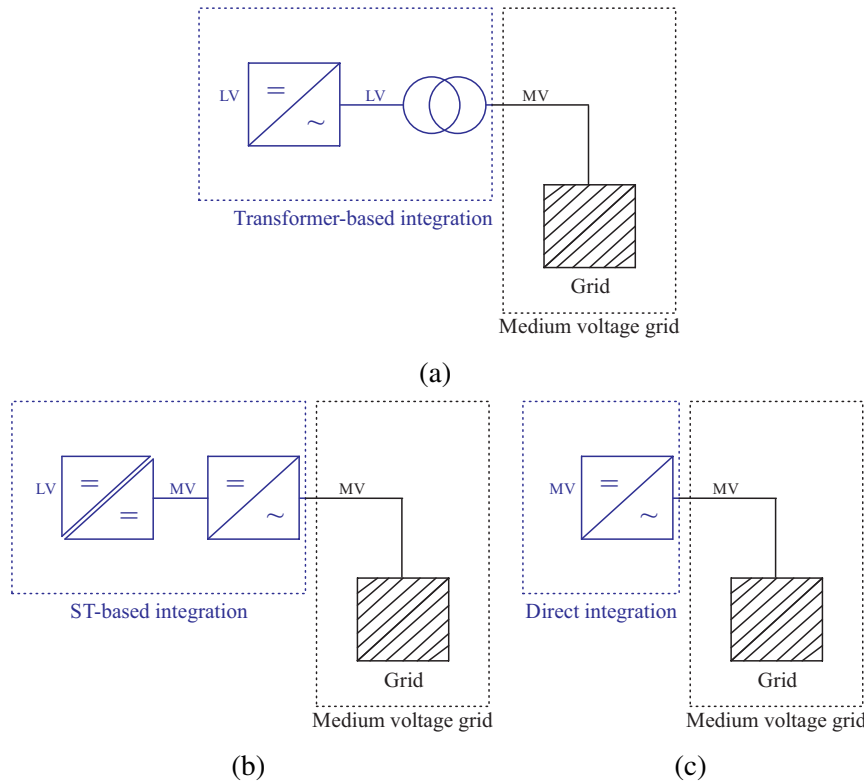
Figure 2.1: MV grid connection by: (a) Classical 50 Hz transformer. (b) Smart transformer. (c) Transformerless connection.

2 Power Electronics Solutions for High-Power Applications

For suitable grid integration of high-power applications, the targeted voltage level is of high importance. Power electronics solutions can be easily adopted to the LV grid if the power rating of the system is limited. However, for higher powers the connection to the MV grid is required. Traditionally, the required voltage levels will be set by low frequency step-up transformers, as depicted in Fig. 2.1a. However, also ST architectures can be applied, instead according to Fig. 2.1b, where boost capability and galvanic isolation are provided by a medium frequency transformer inside the DC-DC conversion stage. In addition, one modular multilevel inverter topology is characteristic in ST architectures, interfacing the DC-DC stage with the MV grid. The ST particularly benefits from its DC and AC (alternating current) connectivity on LV and MV level, high modularity and limited size. In case that MVDC connection is already available or realizable by cascaded power sources, the boost conversion stage can be potentially eliminated as seen in Fig. 2.1c.

From a power electronics point of view the main motivation for direct connection to higher voltage levels can be seen in the reduction of currents and related chip area and losses as well as cabling issues [2]. For integration of higher powers, the connection to the 20 kV MV grid is very well established. If classical transformers are applied, e.g. for simplified inverter connection and operation on LV level, the voltage and current can be adjusted according to the number of primary and secondary transformer windings N_p and N_s of the transformer according to (2.1).
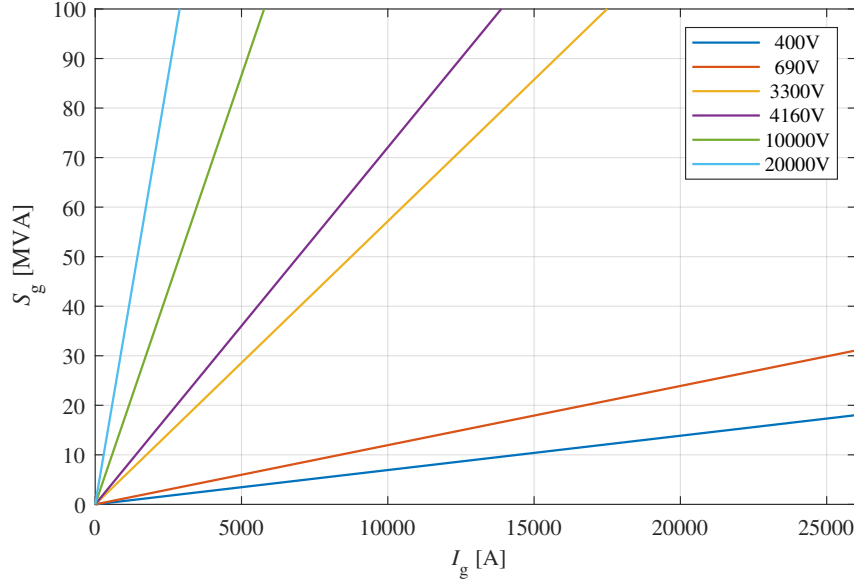
Figure 2.2: Nominal power rating depending on the voltage and current levels.

$$T_{\mathrm{R}} = \frac{N_{\mathrm{prim}}}{N_{\mathrm{sec}}} = \frac{V_{\mathrm{prim}}}{V_{\mathrm{sec}}} = \frac{I_{\mathrm{sec}}}{I_{\mathrm{prim}}} = \frac{V_{\mathrm{g}}^{\mathrm{LV}}}{V_{\mathrm{g}}^{\mathrm{MV}}} = \frac{I_{\mathrm{g}}^{\mathrm{MV}}}{I_{\mathrm{g}}^{\mathrm{LV}}} \tag{2.1}$$

The primary and secondary voltages and currents are directly linked by the turns ratio T_{R} according to (2.2). The required current ratings are depending on the power injection as illustrated in Fig. 2.2 for several voltage levels. It becomes obvious that the currents become huge for connection on LV level, e.g. corresponding to more than 25000 A for 30 MVA power injection at 690 V. For the handling of such high currents, parallel connection of power modules or of power inverters becomes inevitable. Instead, the currents can be reduced below 1000 A by direct connection to the 20 kV MV grid, however linked to higher complexity and higher safety measures. The power ratings can be even further scaled up at reasonable current levels by connecting to the HV grid, enabling power ratings from hundreds of MWs even into the GW range.

$$S_{\mathrm{g}} = \sqrt{3} V_{\mathrm{g},\Delta}^{\mathrm{MV}} \cdot I_{\mathrm{g}}^{\mathrm{MV}} = \sqrt{3} V_{\mathrm{g},\Delta}^{\mathrm{LV}} \cdot I_{\mathrm{g}}^{\mathrm{LV}} \tag{2.2}$$

2.1 Application Fields

High-power converters can be seen as the key element for flexible and cost effective integration of renewable energy systems, for grid service supply and within the electromotive sector, as indicated in Fig. 2.3. High-power converters are able to exchange both active and reactive power between connected sources and loads. Beside the exchange of active power,
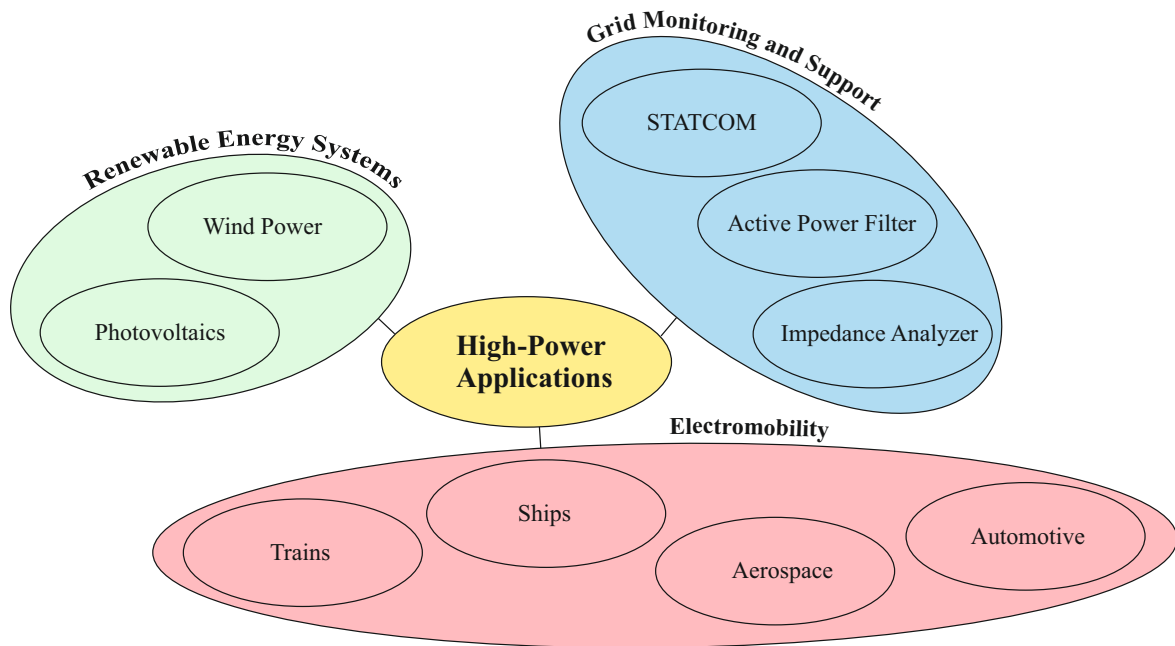
Figure 2.3: Common high-power application fields.

the reactive power supply has become more and more important for a stable operation of the grid. Nowadays, renewable energy systems like wind and solar are already able to provide reactive power for flexible grid stabilization. Particularly for weak grids flexible systems like STATCOM applications are one important solution to provide ancillary services to the electric grid for stable operation. Ancillary services like reactive power supply as well as active power filtering can be optimized by taking into account the time dependent grid characteristics. For this purpose, grid analyzers can be used, being able to detect important information like the frequency dependent grid impedance during grid operation.

Modular power converters are able to provide not only active power but also reactive power for grid support as an additional feature. Beyond that, own high-power STATCOM applications can be realized based on modular power converters for supporting weak power grids. With the knowledge of time dependent power grid characteristics, the grid services can be optimized. For this purpose, the harmonics and grid impedance characteristics can be detected by a grid analyzer. The application and the potential of wind power systems, STATCOM applications as well as grid analyzers are described, respectively.

2.1.1 Wind Power Generation

The installation of wind power plants has grown a lot in recent time [2]. In parallel, also the wind generators and power electronics systems are reaching higher and higher powers as shown in Fig. 2.4 [2], [3]. Within decades the maximum power ratings of wind generators have been multiplied, achieving rotor diameters of 220 m and maximum powers of up to 14 MW in offshore applications [4]. In very few years, even powers up to 16 MW become possible by rotor diameters of 242 m.
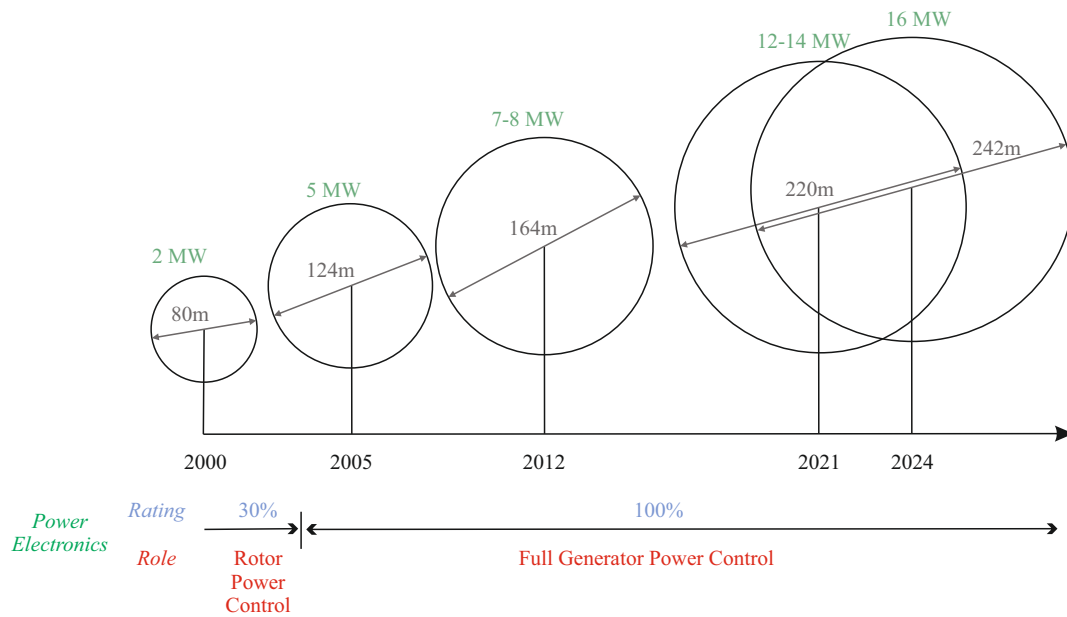
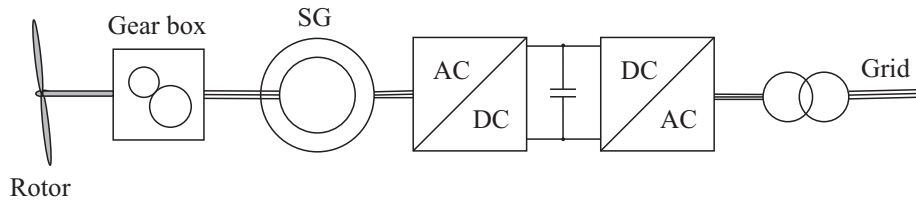Figure 2.4: Development of wind turbines and power electronics [2].

Figure 2.5: Wind generator for high powers: SG with stator connected back-to-back inverter (full scale).

With the help of power electronics inverters, it has become possible to control the rotational speed of wind generators for high efficiencies and to stay connected during grid disturbances and grid faults, supporting the grid by flexible power control in accordance with available grid codes [2], [5]. The most important generator types can be seen in induction generators and synchronous generators (SG), where the double-fed induction generator (DFIG) and the stator connected SG (rotor excited or with permanent magnets) are most established [2]. For the DFIG the back-to-back inverter is connected to the rotor, typically rated with 30 % of the nominal power. Different to this, the back-to-back inverter of the SG needs to be designed for the full nominal power [2], [6]. For the DFIG the rotational speed is limited and sensitive slip rings are required for connection to the rotor [2], [6]. However, the DFIG is very cost effective and therefore attractive up to limited power ranges (e.g. 5 MW) [2]. Instead, full-scale back-to-back inverters provide flexible full power support and high power quality also during grid faults and disturbances [2], [6], [7]. In combination with SG very high efficiencies become possible, making it very attractive for higher power ratings (e.g. more than 5 MW) in onshore and offshore applications [2], [6]. The basic structure is depicted in Fig. 2.5.
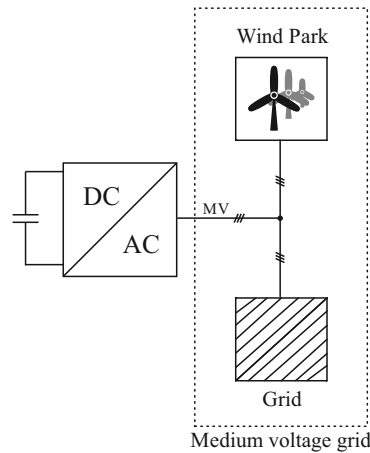
Figure 2.6: MV STATCOM integration.

2.1.2 STATCOM Applications

The integration of high-power renewable energy sources is linked to high challenges for safe and stable operation of the distribution grid. The power generation from wind generators and PV cells is fluctuating a lot and it is only predictable up to a certain degree. On the other hand, more and more flexible power consumption, e.g. from fast charging stations, are challenging for an effective grid management. An imbalance of power generation and load consumption can cause variations in voltage and frequency and can be a risk for the grid stability [8]. Therefore, usually strict grid codes are defined for high power plants to ensure a safe and stable generation [8].

For instance, nowadays conventional wind energy systems are able to flexibly control active and reactive power also during low voltage ride through conditions. Fluctuations or even dips of the grid voltage are typically regulated by reactive power supply. STATCOM applications are specially designed for high and flexible reactive power supply to maintain the grid voltage [9] and can be applied in addition to renewable energy systems for supporting the grid. This is particularly beneficial for weaker grids where already small changes can lead to undesired conditions. As an additional feature active power filtering can be applied to compensate undesired current and voltage harmonics within the grid [10], [11].

2.1.3 Grid Impedance Analyzer

The main goal of grid impedance analyzers is the determination of the grid impedance depending on the frequency, also varying with the time due to changing conditions. Different to LV grids [12], [13], [14], measurements and analysis for MV grids are very scarce [15], [16]. However, the effectiveness of grid services, e.g. from STATCOM applications, can be enhanced a lot by proper knowledge and analysis of the grid characteristics. The reactive power supply can be perfectly adapted to the exact impedance for effective voltage stabilization. Furthermore, active power filtering can be optimized by taking into account the
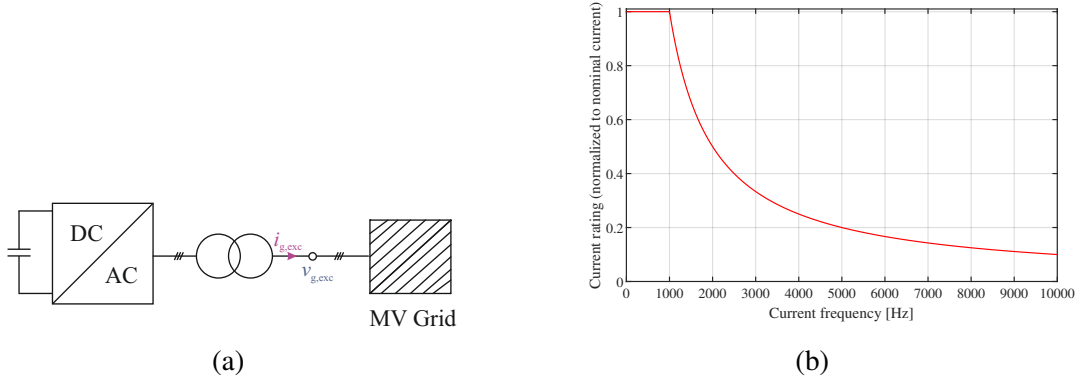
Figure 2.7: MV grid analyzer connected by step up transformer: (a) Basic scheme. (b) Current rating profile.

available online measurements. In addition to this, resonance damping can be achieved by knowing the resonances of the grid for stable operation.

The basic principle of the MV grid analyzer is indicated in Fig. 2.7a. By the injection of monofrequent currents $I_{g,exc}(f)$, an excitation of the grid voltage $V_{g,exc}(f_m)$ is achieved. The relation between achieved voltage excitation and required current injection provides the frequency-dependent grid impedance $Z_g(f_m)$. Beside the determination of the grid impedance, the system is able to provide reactive power supply and active power filtering for grid voltage stabilization and harmonic cancellation. The system is fed directly from the MV grid.

With the goal of a proper signal to noise ratio, a grid voltage excitation of 1 % is aimed in a frequency range between 100 Hz and 10 kHz. The required nominal current for proper excitation of the grid depends on the minimum occurring grid impedance and can be expressed as follows:

$$I_{g,exc,max} = \frac{V_{g,exc,\lambda}}{Z_{g,sc}} = \frac{0.01 \frac{V_{g,\Delta}}{\sqrt{3}}}{Z_{g,sc}} \tag{2.3}$$

Assuming a simple ohmic-inductive behavior of the grid the resistive and inductive part can be expressed based on the grid angle Ψ according to (4.10) and (4.11).

$$R_{g,sc} = Z_{g,sc} \cdot \cos\left(\Psi_g\right) \tag{2.4}$$

$$L_{g,sc} = \frac{Z_{g,sc} \cdot \sin\left(\Psi_g\right)}{2\pi f_g} \tag{2.5}$$

2.1.4 DC Power Transmission

For optimal use of available power generation from renewable energy systems the grid infrastructure and its capacity is of high importance. High powers need to be transferred from re-
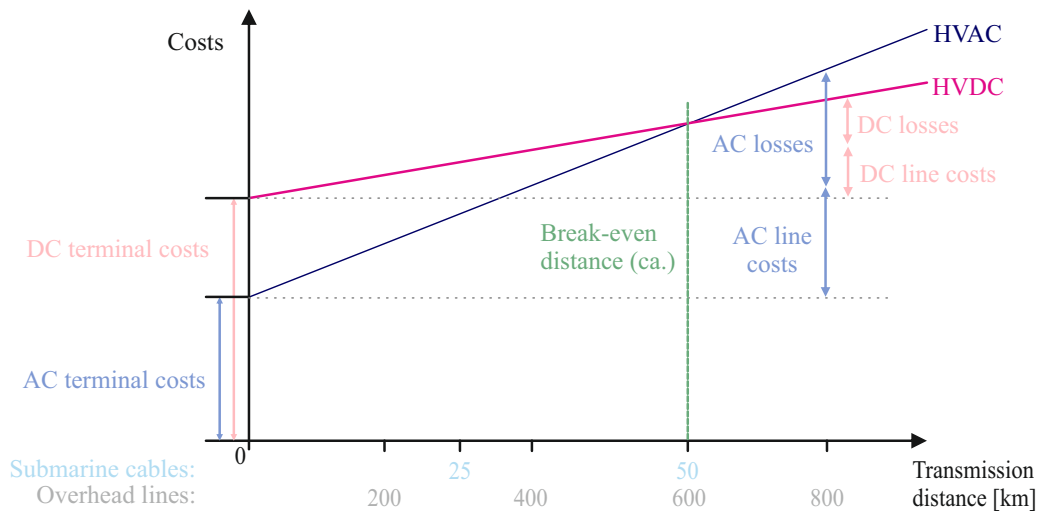
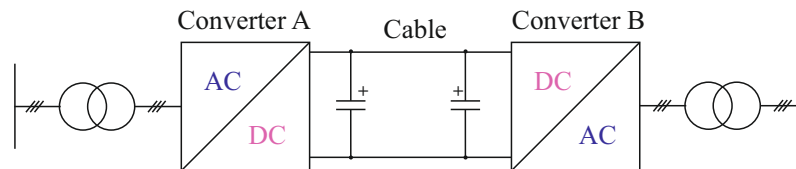Figure 2.8: Cost comparison for HVDC and HVAC transmission systems [19].

Figure 2.9: Basic scheme for DC power transmission systems based on voltage-sourced converters.

newable energy generation (e.g. offshore wind farms) to the largest consumers (e.g. energy-intensive industry). For this purpose, in often cases long distances need to be covered. Traditionally, the power transmission is realized by AC technology. However, meanwhile, the transmission by DC technology has become very important, profiting from higher efficiencies and smaller wire cross section [17] for instance. Particularly, for offshore applications HVDC transmission has become the preferred choice since capacitive effects in the underwater cables can be avoided [18]. However, also for overhead lines the HVDC technology has become very attractive, especially for transmission of very high powers and at longer distances.

In Figure 2.8 the costs for power transmission by HVDC and HVAC are compared [19]. For HVDC transmission the costs of the converter stations are relatively high since very complex and expensive power electronics converters are required. Instead, for HVAC technology the transmission lines become very cost-intensive at longer distances. The break-even distance is obtained at around 600 km from where the investment costs for DC transmission are lower due to the reduced effort for the transmission lines.

In Figure 2.9 the basic scheme for a DC transmission system is depicted. Traditionally, thyristor based solutions have been used to handle very high powers at high voltage level. However, meanwhile the MMC is very well established for HVDC applications and also very promising for MVDC transmission at limited voltages. By cascading dozens or even hundreds of standard IGBT modules medium and high voltages can be blocked.
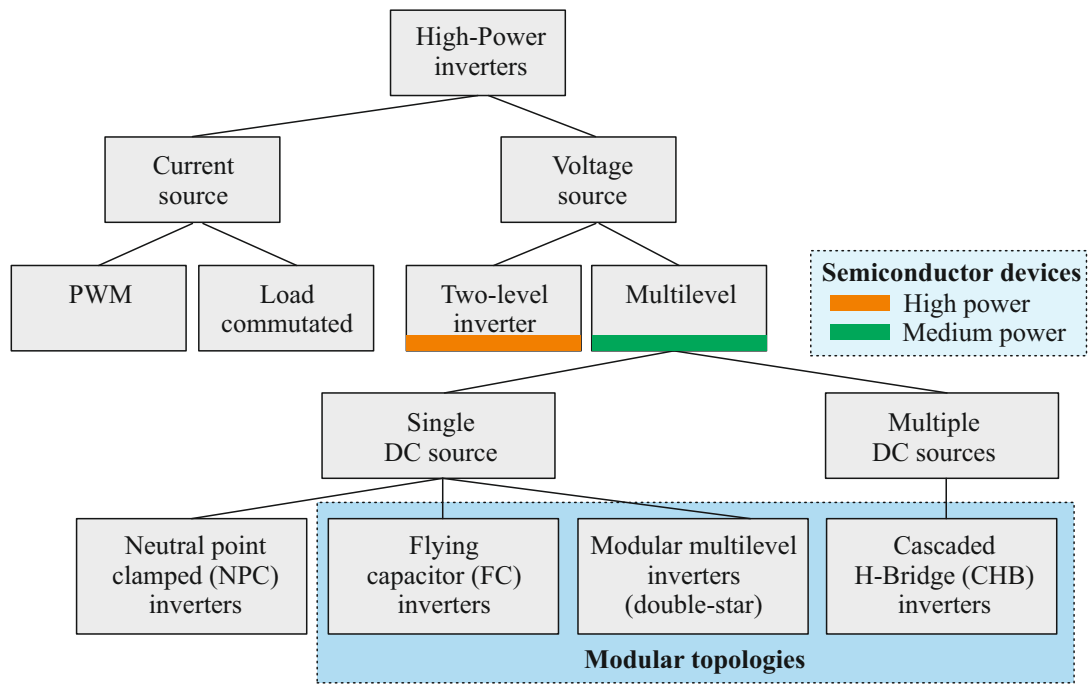
Figure 2.10: High-power inverter classification [22], [23], [24], [25].

2.2 Inverter Solutions

Nowadays a high variety of solutions is available to fulfill the associated power capabilities. Central inverter requirements are related to the efficiency, power quality, reliability, volume, complexity and costs. Additional features as high redundancy can be provided by modular topologies for high safety and high availability in case of component failures and fault conditions. With the help of modular power converters, the system power ratings can be flexibly adopted for the target applications.

2.2.1 Inverter Classification

The most important high-power inverter topologies are classified in Fig. 2.10. They can be divided into current source inverters, pulse width modulated (PWM) or load commutated, and voltage source converters (transistor-based). Voltage source converters are commonly applied up to very high power ranges due to the flexible switching operation and grid support by flexible control of active and reactive powers [20], [21].

Among the voltage source inverters, it can be distinguished between the well-established two-level inverter and between more advanced multilevel inverter topologies. The multilevel inverters can be classified into neutral point clamped (NPC) inverters, flying capacitor (FC) inverters, cascaded H-bridge (CHB) inverters and the MMC. CHB inverters are connected to multiple direct current (DC) sources, which can be distributed equally and unequally, depending on the application. Different to this, the other multilevel inverter families are linked to one single DC source as also known from the classical two-level inverter.

FC and CHB inverters as well as the MMC are not only taking benefit from its multilevel waveform generation but also from a highly modular structure with high redundancies. This enables fault tolerant capabilities, high availability and limited maintenance costs, linked to low operation points.

The well-established two-level inverter benefits from low number of switching device components and limited complexity from both hardware and software side. However, it is strongly limited in the power rating due to limited voltage capability of standard semiconductor devices. New semiconductor technologies based on SiC technology with blocking capabilities of 10 kV or 20 kV have the potential to move these boundaries [26]. However, for direct connection to the 10 kV or 20 kV MV grid even higher blocking voltages would be required.

Instead, the connection to lower voltage levels is linked to large currents and very high conduction losses for high-power applications. Not only the conduction losses but also the switching losses are very high since high switching frequencies are required for two-level pulse-width modulation with limited harmonic content. In addition to the low efficiency the high harmonic distortion is one the main drawbacks of the two-level inverter technology, since big passive filters are required. Beyond that, high voltage transients put stress on all important components (semiconductor devices, storage capacitors and filters). Even if only one semiconductor device is failing the system cannot operate anymore due to missing redundancies.

2.2.2 Multilevel Inverters

Multilevel inverter technology can overcome the limitations of classical two-level inverters and can provide multilevel waveform generation. One basic principle of multilevel voltage generation is illustrated in Fig. 2.11. For the classical two-level inverters only the positive and negative DC-link voltage, $+V_{dc}$ and $-V_{dc}$, can be applied at the output terminal. Different to this, in multilevel inverter topologies the DC-link voltage will be splitted among several cascaded capacitor units [27]. For instance, in three-level inverter topologies the DC-link voltage is shared among two capacitor units. One midpoint is generated and can be used for three-level voltage generation ($+V_{dc}$, 0, $-V_{dc}$). For multiple numbers of voltage levels the DC-link voltage can be splitted among n capacitor units, corresponding to $n+1$ voltage levels. For the inverter operation it is important to keep the capacitor voltages within proper limits by suitable switching algorithms and can be seen as one of the main challenges in multilevel inverter topologies [28].

The applied capacitor voltages are crucial for the voltage design of the capacitors and of the semiconductor devices. Compared to the two-level inverter topology, the capacitor voltages as well as the required semiconductor voltage ratings (blocking capabilities) are halved for conventional three-level inverter topologies. Accordingly, the inverter voltage rating can be doubled if the same semiconductor voltage class will be applied in classical three-level inverters. This multilevel waveform generation can be extended for multilevel inverters with
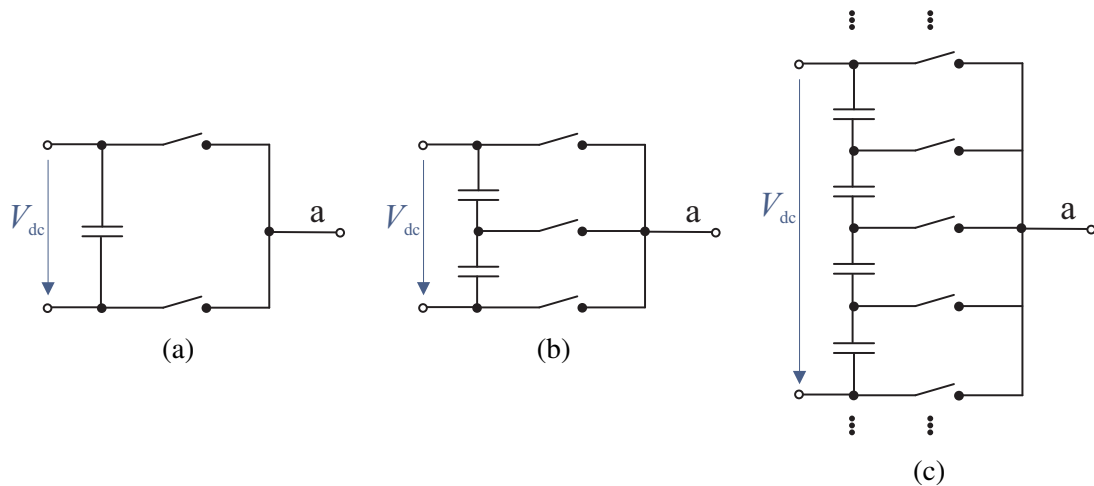
Figure 2.11: One leg: (a) Two-level inverter. (b) Three-level inverter. (c) Conventional multilevel inverter [27].

n capacitor units where the DC-link voltage can be selected n times higher than in two-level applications. Therefore, even MV and HV connection for high and ultra-high powers can be realized by cascading dozens or hundreds of capacitor units and standard semiconductor devices such as in STATCOM applications or high-voltage direct current (HVDC) applications [22], [29], [30], [31]. Instead, if the voltage level is defined to be constant, the voltage rating of semiconductor devices can be reduced by multilevel topologies, linked to lower device switching losses and smoother voltage transients in the system [22], [32], [33], [34], [35] .

Beside the high power capability and scalability with standard components, the multilevel voltage generation can be seen as the most important advantage in multilevel applications [33]. With multilevel voltage generation the harmonic distortion can be strongly reduced and excellent voltage and current waveform qualities become possible [33], [34], [35]. This allows very low number of switching commutations, linked to very high efficiencies, particularly crucial in high-power applications [33], [34], [35]. The inherent dynamic performance is very high and filters can be designed very small and economically [36].

Multilevel inverters are already well established in the industry and have become very attractive for high-power applications [22], [37], [38]. However, there is not only a high demand in high-power three-phase applications, but also for lower powers (e.g. down to 1 kW) and in single phase-applications, e.g. for photovoltaic (PV) [27]. Apart from the capacitor voltage balancing (CVB), the main practical challenges can be seen in the additional number of switching devices and gate drivers, linked to a more complex design and control, especially for high number of voltage levels [25], [27], [39], [40].

The age of multilevel inverters started with CHB and FC inverters, patented in 1971 [41], [42]. The classical three-level NPC topology has been introduced in 1981 [43], [44]. From the 1990s the different inverter families have been achieved higher relevance for medium voltage (MV) applications with high power ratings [45], [46]. The MMC has been introduced later in 2003 [47] and has become the preferred solution in HV applications up into the GW range.

2.2.3 Comparison and Selection

The proper choice of inverters is highly dependent from the target application and the definition of the voltage level. Smaller renewable energy systems (e.g. PV panels) are usually connected to the low voltage (LV) grid as long as the power rating is limited. However, bigger powers need to be connected to the MV grid for safe and reliable grid operation, classically to the 20 kV grid. The connection to the MV grid is possible by direct connection of MV inverters or with the help of step-up transformers.

For direct MV connection, the same power can be transferred with significantly lower inverter currents, also limiting the cross area of cables and transmission losses. Direct MV connection is particularly important in hybrid grids and in advanced architectures like the Smart Transformer (ST), with highly flexible structure and control [48], [49]. The number of required semiconductor devices in multilevel inverters can be limited by selecting switching devices with very high blocking capability up to 6.5 kV. However, the costs for semiconductor devices with high blocking capability are very high, increasing exponentially with the voltage [50]. Furthermore, the efficiency is very limited and very high voltage transients need to be managed despite of big required filters. Therefore, standard three-level multilevel topologies like the three-level NPC are only established up to lower MV levels [36], [39], [51]. Thus, for the use of cost-effective standard switching devices and for achieving high waveform qualities and very high efficiencies, an extended number of voltage levels is required in MV high-power applications.

In general, FC inverters are getting more and more attention for higher number of voltage levels [27]. However, the challenges for proper voltage balancing are increasing a lot [52]. Furthermore, large capacitors would be required for connection to the MV grid [52]. The high costs and the high complexity for the extension to a high number of voltage levels make this topology unattractive for 20 kV MV applications. Also the NPC inverter can be extended to a higher number of voltage levels, however, for the price of additional clamping diodes, linked to additional conduction and switching losses due to reverse recovery currents and much more challenging voltage balancing [27], [53], [54]. Therefore, also the application of high-level NPC inverters is not suitable for 20 kV MV applications.

Different to this, the MMC is very well suited for high numbers of voltage levels with standard semiconductor devices due to modular scalability by limited number of components and very high efficiencies [22]. The single-star MMC is well established for PV parks with several DC sources and in the Smart Transformer architecture [55], [56]. Instead, the double-star MMC provides a common DC-link, being very attractive in conventional hybrid grids and for DC transmission systems. The excellent waveform generation enables very low switching frequencies, very high efficiencies and the elimination of additional filters. Meanwhile the double-star MMC has become the preferred choice in high-voltage applications and high-power motor drives [57], [58], also becoming more and more relevant in MV applications like STATCOM applications [59], energy storage systems and shipboard systems. Thus, the double-star MMC can be seen as the preferred solution for direct connection to the

MV grid and will be further investigated in terms of design, control and modulation. Practical challenges can be seen in the high complexity and high safety requirements for MV operation.

From an industry perspective, there always needs to be found a compromise between number of voltage levels, complexity and safety requirements, also explaining the high practical importance of NPC and FC inverter topologies even for high-power applications [27]. With the use of step-up transformers, LV inverter topologies can be used for safe and simplified connection to the MV grid. Nevertheless, the application of multilevel inverters can be advantageous for increasing the voltage capability even at LV level as well as for improved waveform qualities for low switching losses and low filter effort. Classical two-level inverters require very high switching frequencies, deteriorating the efficiency, especially in combination with semiconductor devices with high voltage ratings. Therefore, also from efficiency point of view, it is more reasonable to increase the number of voltage level instead of using conventional switching devices with higher blocking capability to achieve higher power capabilities.

The best compromise for three-level inverter topologies in terms of voltage capability, number of components, simplicity and efficiency can be seen in the classical NPC inverter and in the classical FC inverter. However, the flying capacitors are linked to high expenses and the balancing linked to relatively high switching frequencies [22], [60]. The three-level NPC inverter is very well established due to limited costs and high power densities, and therefore selected to be as the preferred choice for connection to the MV grid by classical step-up transformers.

2.3 Power Semiconductor Devices

Power semiconductor devices are essential for the realization of high-power inverter solutions. The proper selection and integration are linked to different important requirements, such as voltage blocking capability, current rating, power loss behavior, cooling capability and reliability.

2.3.1 Power Diodes

The structure of a simple diode corresponds to a pn junction. Diodes are not switchable and can be operated in reverse and in forward direction. Figure 2.1 shows the characteristic curve of a diode. The diode current i_F is plotted in dependence from the applied voltage u_F, where the forward voltage is defined by U_{F0}, and the reverse voltage by U_R.

The behavior of a diode can be linearized with the help of a tangent, related to the differential on-resistance r_F. Based on the linearization the conduction losses of a diode can be approximated as follows:
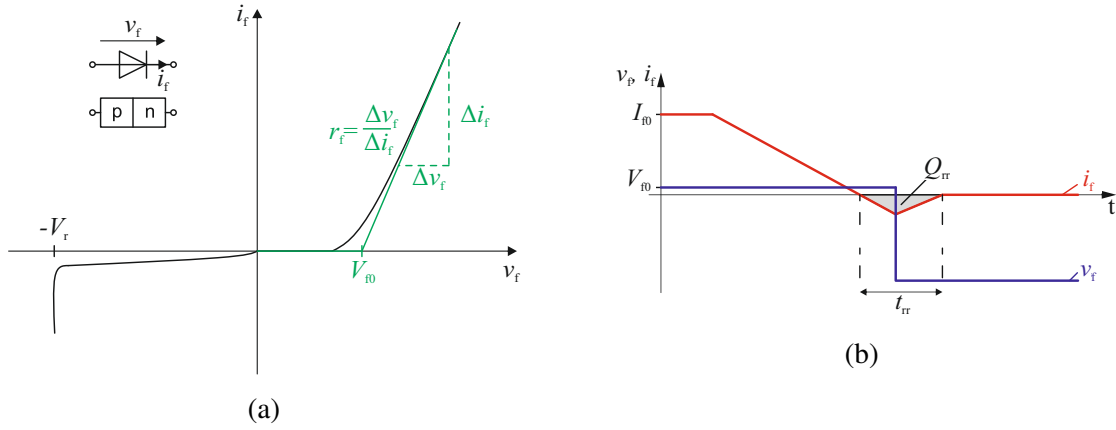
Figure 2.12: Diode behavior (simplified, not to scale): (a) Characteristics. (b) Reverse recovery effect.

$$P_{\text{con,D}} = V_{\text{f0}} \cdot \bar{i}_{\text{f}} + r_{\text{f}} \cdot I_{\text{f}}^2 \tag{2.6}$$

If the diode will be turned off, there will occur a blocking delay time t_{rr} until the charge carriers have flowed back out of the center region. This charge is called the reverse delay charge Q_{rr}. The recovery process is illustrated in Fig. 2.12b.

The reverse delay charge corresponds to the integral of the reverse current peak over the reverse delay time, marked in gray. Since during the reverse time the reverse voltage is already applied to the diode, high losses are the result. The losses during the switch-on process, on the other hand, are generally negligible since a diode only conducts the current when the voltage across it has dropped [61].

During inverter operation diodes act as free-wheeling diodes. This means that the phase current, e.g. with an inductive load, does not change abruptly when a transistor is switched off. Instead, the phase current is conducted by free-wheeling diodes.

In order to increase the reverse voltage of a diode for high-power applications, a conductive intermediate layer will be inserted between the p- and n-region, also referred as a pin diode [62]. This non-doped or only lightly doped intermediate layer reduces the field strength between anode and cathode and thus enables higher blocking voltages. In forward mode, the intermediate region is flooded with charge carriers and recombination can occur [63].

2.3.2 Power Switching Devices

Power switching devices are essential for multilevel AC voltage generation. The most important power module semiconductor technologies are silicon (Si) insulated gate bipolar transistors (IGBT), Si integrated gate-commutated thyristors (IGCT) and silicon carbide (SiC) MOSFETs [64]. The benefits and drawbacks of the most important solutions are summarized and compared in Table 2.1 [65].

Table 2.1: Power modules for high-power applications, comparison [2], [65].

	IGBT module	IGBT PK	IGCT PK	SiC MOSFET module
Power density	Low	High	High	Low
Reliability	Moderate	High	High	Unknown
Cost	Moderate	High	High	High
Failure mode	Open circuit	Short circuit	Short circuit	Open circuit
Easy maintenance	+	-	-	+
Snubber requirement	-	-	+	-
Thermal resistance	Large	Small	Small	Moderate
Gate driver	Moderate	Moderate	Large	Small

Wire-bonded IGBT modules profit from simple gate driver circuits, low costs as well as easy mounting and maintenance [65]. Wire-bonded IGBT modules are linked to a relatively long history and they are well established in practical applications [65]. However, the connection of internal chips by bond-wires and soldering is also linked to limitation in terms of power density, cooling capability and reliability [66], [67].

Press-pack (PK) packaging allows better connection of internal chips by direct PK contacts [66]. In this way, the power density and cooling capability can be increased and parasitic effects minimized [66], [68], [69]. Furthermore, the inherent short-circuit failure mode allows safe operation without the need of a bypass circuit [70]. Also the reliability can be potentially increased by PK packaging. However, the pressure of the external clamping as well as thermo-mechanical stress in the different materials are linked to internal stress and can lead to an increase in collector-emitter voltage and junction temperatures, cracking and finally to premature wear out failures [71] [72], [73]. Due to lack of experience, the evaluation of different aging mechanisms for PK IGBTs is still under investigation. Accurate and validated lifetime models, considering all important degradation factors, are still missing [71]. Further studies need to be done, also taking into account the analysis of fast transients [71]. Nevertheless, PK IGBT modules have a high potential especially for the MMC in medium and high voltage applications [74]. First high-power PK products are already on the market, being applied in very first HVDC projects [75]. In future, PK IGBTs can become a very important solution also for reduced power levels, especially when further experiences have been collected, also for manufacturing processes to limit the costs.

PK IGCT modules particularly profits by very low conduction losses, particularly advantageous in high current applications. However, the complexity and costs of the gate units are very high and big snubber circuits required, linked to additional losses [76], [77]. However, IGCTs are linked to very high power ratings, being relevant for HVDC applications. For connection to LV levels or to the MV grid with adequate number of levels, the available power ratings are too overdimensioned.

The development of WBG devices, e.g. based on SiC, is also progressing in fast steps where adopted MOSFET technology can have future potential in high-power applications, especially due to a high voltage blocking capabilities, low on-state resistances and very low

Table 2.2: Common power modules which integrate multilevel topologies [27].

Topology	Manufacturer	Voltage rating [V]	Current rating [A]
NPC	Infineon	650, 1200	30 to 400
NPC	Semikron	650, 1200	20 to 600
NPC	Vincotech	1200, 1500	30 to 1800
T-type	Fuji Electric	600, 900, 1200	50 to 600
T-type	Infineon	650, 1200	15 to 600
T-type	Semikron	650, 1200	50 to 600
T-type	Vincotech	650, 1200	25 to 1800
ANPC	Vincotech	1200, 1500	150, 300, 600
FC	Vincotech	1200	200

switching energies. Taking these advantages allows to limit the number of cascaded semi-conductor devices as well as the harmonic content in high-power applications. Also for three-level applications the use of fast switching WBG devices can be advantageous due to limited number of voltage levels. In general, challenges for SiC MOSFETs can still be seen in the proper integration, very high voltage transients, high operating temperatures and the reliable application. Nowadays suitable solutions at reasonable costs are still missing for providing competitive solutions. Nevertheless, solutions with high voltage blocking capabilities at reasonable costs might become very interesting in foreseeable future.

For future promising solutions like PK IGBT and IGCT as well as SiC MOSFET modules further research, development and optimization need to be done for wide and competitive applicability. Due to high practical relevance, high availability and reasonable costs the focus of this work is related to well-established standard wire-bonded IGBT modules. Blocking voltages of 1200 V and 1700 V are considered, providing an adequate voltage range for three-level LV inverters and multilevel MV inverters. Also for NPC and FC topologies a wide range of semiconductor devices is available rather for 1200 V blocking capability which can still operate on LV level, listed in Table 2.2.

2.3.3 IGBT Modules

The basic structure of an IGBT module is depicted in Fig. 2.13, consisting of IGBT and diode chips, direct-bond-copper (DBC) substrate, solder and a copper baseplate [78]. The DBC is usually composed by one ceramic and two metalized copper films. The DBC substrate is soldered onto the baseplate and the IGBT and diode chips solder from the other side. Additionally, aluminum bond wires are used for further interconnections, also between the power chips [78]. The housing is commonly done by a plastic case, enclosed with insulating Si gel [78]. For high-power application a water cooling is advantageous compared to conventional heatsink or air-cooling systems due to better cooling capability.
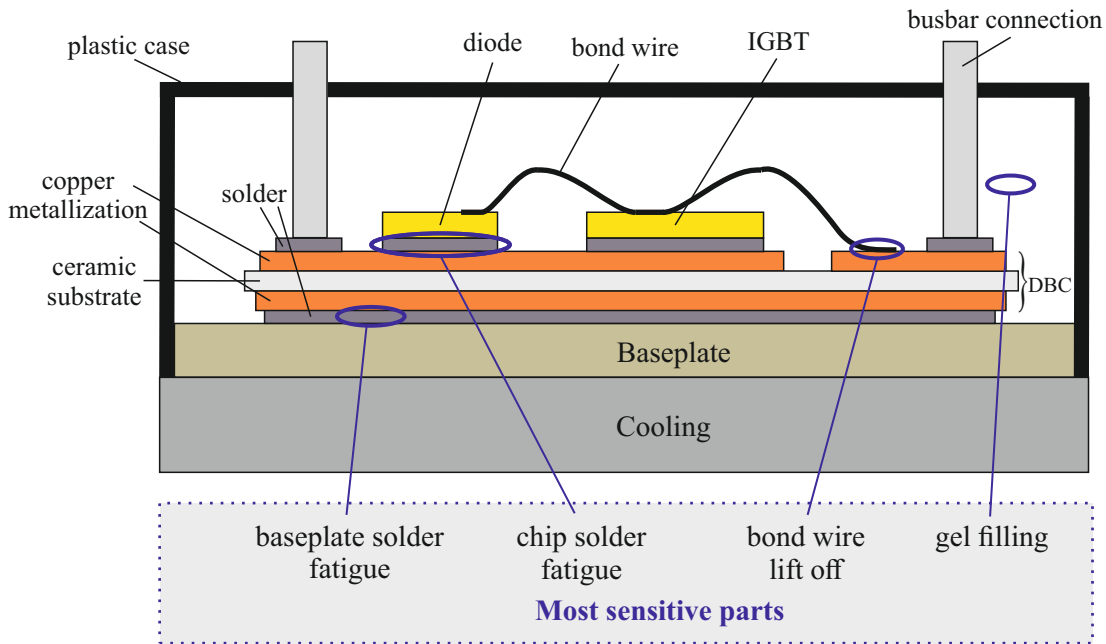
Figure 2.13: Basic structure of an IGBT module and most sensitive parts [78], [79].

2.3.4 Reliability

The power semiconductors devices are the components with the highest failure rate in power electronics conversion systems, reported with 31 %, almost 60 % of them due to thermal stress [80], [81]. Thermal stress can be seen as the most important degradation factor for power semiconductor devices due to different materials and thermal expansion factors inside the power modules. The inhomogeneous thermal expansion leads to mechanical stress between the layers and at the connection points. Besides, also the maximum temperature should be limited for safe and reliably operation. The most important stress parameters can be identified by the average junction temperature and the thermal cycles [82]. The locations of common failures, also highlighted in Fig. 2.13, are related to the baseplate solder, the soldering of the chips, the bond wires and also the insulating gel [83].

Each semiconductor's efficiency and lifetime are affected by its junction temperature. The junction temperature itself is mainly affected by the power losses, the geometries (e.g. compactness) and the applied cooling. Failure mechanisms of semiconductor devices are mainly driven by the junction temperature [84]. The number of expected power cycles to failure can be approximated by (2.7) in dependence from the junction temperature T_{j} and its thermal cycle ΔT_{j} [85].

$$N_{\mathrm{f}} = a_1 \cdot (\Delta T_{\mathrm{j}})^{-a_2} \cdot \exp^{\frac{a_3}{\overline{T}_{\mathrm{j,av}}}} \tag{2.7}$$

The constants a_1, a_2 and a_3 need to be fitted by cycling tests in an empirical way, since available physical models are not able to properly predict the failure mechanisms in a real application. Accordingly, extensive and long cycling tests are required for a high number of semiconductor devices to approximate the lifetime expectation of a certain semiconductor
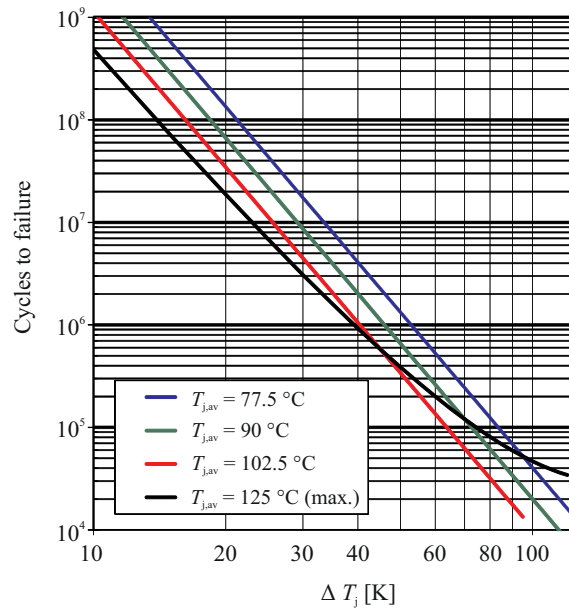
Figure 2.14: Number of power cycles to failure for a standard IGBT module from Semikron [87].

device [86]. Results from cycling tests for a standard IGBT module from Semikron are interpolated in Fig. 2.14 [87]. It can be seen that the lifetimes are not significantly affected by small variations of the average junction temperatures. Instead, already small variations in the thermal cycling amplitudes have a significant impact on the semiconductor lifetimes.

The presented lifetime model is limited to a specific junction temperature and a specific thermal cycle of the semiconductor device. For taking into account a real mission profile, the miner rule is applied for linear damage accumulation according to (2.8).

$$C_{\mathrm{m}} = \sum_{i=0}^{\infty} \frac{n_{\mathrm{i}}}{N_{\mathrm{i}}} \leq 1 \qquad (2.8)$$

N_{i} describes the number of cycles to failure for a specific stress level i and n_{i} the detected cycles for the corresponding stress level. The semiconductor is expected to fail after having reached an accumulated damage C_{m} of 1. The lifetime can be approximated by the ratio of the applied time interval and the accumulated lifetime for IGBTs and for diodes, as well.

For very accurate lifetime modeling of different IGBT modules, very time-consuming and cost-intensive cycling tests would be required, as well. This effort would be only reasonable for manufacturer of semiconductor devices or of power converters with simplified access to statistical failure rates. Instead, the fitted lifetime model for a standard IGBT module from Semikron can be also applied for similar module structures, since the degradation processes and the failure mechanisms are very similar. Even if the absolute values need to be interpreted very carefully, the available lifetime model can reveal clear trends, e.g. to compare and evaluate different control approaches.
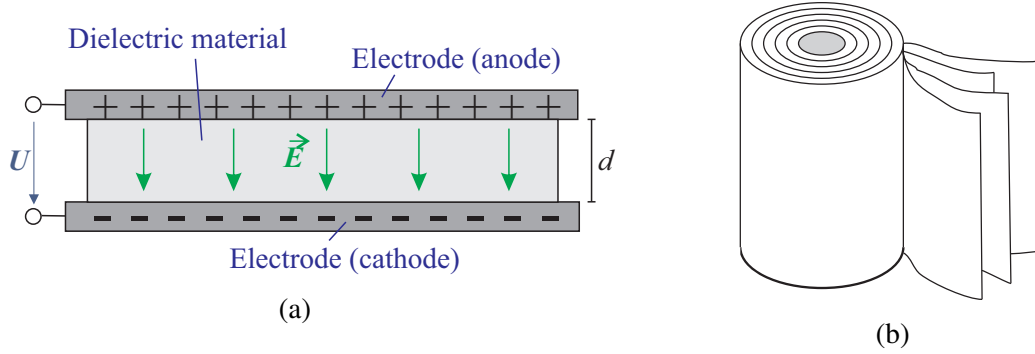
Figure 2.15: Power capacitor: (a) Parallel-plate capacitor. (b) Cylindrical geometry.

2.4 Power Capacitors

2.4.1 Basic Principles

Apart from the power semiconductor devices, the power capacitors are one of the key components in high-power applications. The proper design of capacitor storage banks is highly important to limit system costs and dimensions while maintaining high safety, reliability and long service life [88]. The main functions of DC-link power capacitors lie in buffering instantaneous power imbalances between DC and AC side and in smoothing the voltages [88]. Particularly in the MMC very high powers need to be buffered due to high oscillating powers in each phase, driven by the ac-side grid current and DC-side circulating currents [89]. For classical LV inverters as the NPC inverter the power oscillations in the capacitor banks are limited in balanced three-phase systems, mainly driven by PWM harmonics [90]. Also the behavior in unbalanced grid conditions need to be taken into account [91]. The most important types for high-power applications are aluminum electrolyte capacitors and metalized film capacitors [88].

In a classical parallel-plate capacitor, depicted in Fig. 2.15a, two thin conducting plates are separated from each other by a thin dielectric material (separator) and can be rolled into cylindrical form, as illustrated in Fig. 2.15b, for optimized use of available volume. The energy is stored in an electric field, its strength $\vec{E}$ is linked to the applied voltage V and the distance d between the plate according to (2.9).

$$V_{\mathrm{ab}} = \phi_{\mathrm{a}} - \phi_{\mathrm{b}} = \int_{s=0}^{d} \vec{E} \, d\vec{s} \tag{2.9}$$

The capacitance of capacitors is a measure of how much energy can be stored. It can be described by the ratio between the stored electric charge Q_{cap} on the plates and the applied voltage V_{cap}:

$$C = \frac{Q_{\mathrm{cap}}}{V_{\mathrm{cap}}} \tag{2.10}$$
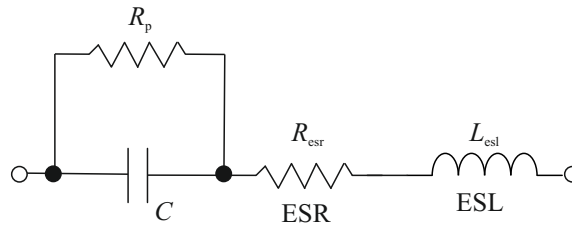
Figure 2.16: Equivalent circuit for capacitors.

The capacitance strongly depends on the geometry and the dielectric of the capacitor. For a classical parallel-plate capacitor the capacitance can be approximated as follows:

$$C = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{A}{d_s} \tag{2.11}$$

The plate area and the distance in between are described by A and d, respectively. ε_0 describes the vacuum permittivity and ε_r the relative permittivity of the dielectric material. It becomes obvious, apart from the geometry, the characteristics of the capacitor mainly depend on the dielectric and its permittivity. The higher the permittivity, the more energy can be saved between the capacitor plates, linked to a high electric flux density $\vec{D}$.

$$\vec{D} = \varepsilon_0 \cdot \varepsilon_r \cdot \vec{E} \tag{2.12}$$

On the one hand, the surface area should be selected properly to achieve high capacitances. On the other hand, the dielectric should be designed very thin, however sufficient to withstand rated electric field strengths. Beside the applied voltage, the capacitance decides about the amount of energy being stored in one capacitor according to:

$$E_{cap} = \frac{1}{2} \cdot C \cdot v_{cap}^2 \tag{2.13}$$

2.4.2 Modeling

Independent from the capacitor type, the electrical behavior can be represented by a simplified equivalent circuit according to Fig. 2.16 [88]. The widely used model is based on ideal components where C represents the storage capacitance, R_{esr} the equivalent series resistor and L_{esl} the equivalent series inductance [88]. The insulation is represented by the resistance R_p [88]. Further characteristics can be modeled by extended circuits, e.g. the dielectric losses and the the dielectric absorption [92]. Also frequency dependencies and the skin effect can be taken into account [93]. The circuit parameters can vary depending on the applied voltages and frequencies as well as the operating temperature and load profiles [88]. In addition, manufacturing tolerances and aging affects have an impact on the parameters and can cause parameter variations among the capacitors.
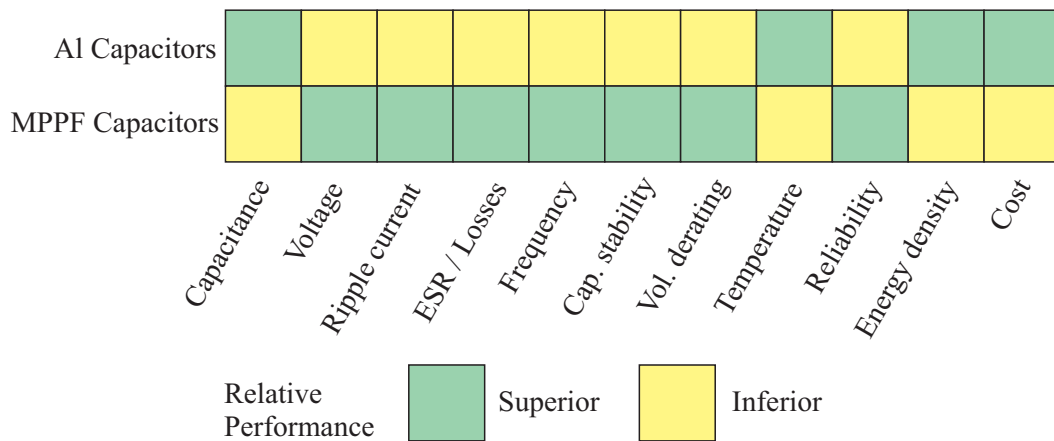
Figure 2.17: Relative performance between aluminum electrolyte capacitors and MPPF capacitors [88].

2.4.3 Capacitor Types

Aluminum electrolyte capacitors are well established in high-power applications. The electrodes are based on aluminum (Al) foils as conducting metal. The anode is covered by a very thin aluminum oxide (Al_2O_3) layer as dielectric. Aluminum oxide benefits from a very high permittivity and high electric field withstand capability. Liquid electrolyte is being inserted by a separator paper between the anode and cathode foils, effectively closing all available volume and pores. The cathode serves as electric contact to the electrolyte, the energy is being stored in the electric field between the anode and the electrolyte.

In metalized film capacitors ultra thin plastic films serve as the dielectric. Most common materials in industry are polypropylene (PP) and polyethylene terephtalate (PET) [94]. The advantages of PET lie in a higher dielectric constant, better mechanical resistance and a slightly higher operation range [94]. Compared to this, the PP benefits from much lower ESR linked to a much higher ripple current capability and absorbs less moisture [94], [95]. The metalized electrodes (usually zinc or aluminum) are applied on the surface of the dielectric plastic film in very thin layers [94], [96].

Beside aluminum electrolyte capacitors and metalized polypropylene film (MPPF) capacitors, high capacitance multi-layer ceramic capacitors are applicable, where ceramic materials serve as dielectric [97]. Despite of outstanding dielectric permittivity and high temperature capability, ceramic capacitors are from limited relevance due to low field strength, limited power densities and very high costs [88]. Although further developments are in progress, nowadays electrolyte capacitors and film capacitors can be seen as the state of the art in high-power applications. The performance of both types is summarized in Fig. 2.17 [88].

The main advantages of electrolyte capacitors can be seen in the high energy densities, achieved by high dielectric permittivity. Accordingly, capacitor banks can be designed smaller which is particularly beneficial [98]. Not only the footprint but also the costs of high-power inverters can be significantly reduced by electrolyte capacitors. However, the electrolyte capacitors suffer from a high ESR, significantly limiting the power and ripple
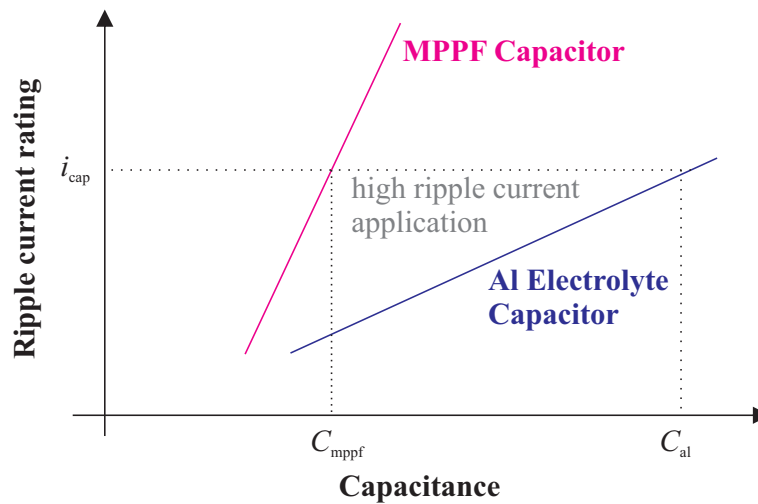
Figure 2.18: Ripple current rating vs. capacitance for MPPF and for aluminum electrolyte power capacitors [88].

current capability, as indicated in Fig. 2.18. By parallel connection of capacitor units, the ESR can be reduced, however with the expense of deteriorated performance in terms of system costs and energy density. In addition, the lifetime of electrolyte capacitors is limited due to stronger wear out by evaporation of electrolyte [88].

Instead, MPPF capacitors benefit from high nominal voltages (up to 1500 V, without the need of several series-connected capacitors to fulfill the voltage requirements in high-power applications. Furthermore, the ESR and corresponding losses are very low, corresponding to a high power and high ripple current capability. MPPF capacitors show a very stable frequency behavior at low temperature density [99]. The reliability is very high at slow capacitance degradation and high voltage impulse strength [100]. Their inherent self-healing capability makes it particularly interesting for high-power applications with high demand of availability and limited accessibility. However, MPPF capacitors are relatively expensive, requires moderate operating temperatures and a higher volume, increasing the footprint of the system [88].

In classical LV high-power applications like wind energy systems, aluminum capacitors are well established due to low costs and high power density [101]. Several studies have been done for different converter topologies, modulation techniques and grid conditions [102], [103], [104], [105], [106]. MPPF capacitors already have high relevance for ac-side grid filters due to high voltage capability, parameter stability and longer lifetimes, also getting more and more attention in conventional high-power inverters due to reasonable performance in terms of capacitance, ESR, ripple current capability, reliability and costs [101], [107].

For medium and high voltage inverters like the MMC MPPF capacitors are already well established due to higher voltage ratings, high ripple current capabilities, low losses, temperature stability, self-healing capability and also low costs [108]. Compared to this, the number of cascaded and parallelized units of electrolyte aluminum capacitors would become huge due to limited voltage ratings and low ripple current capability, driving the costs and
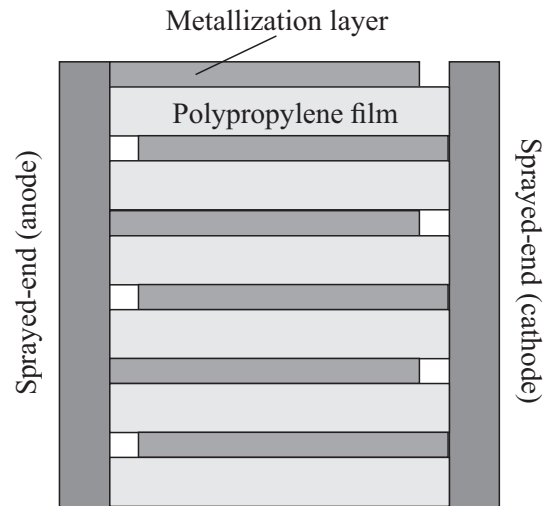
Figure 2.19: Basic structure of MPPF capacitor (side view) [57].

the volume. Instead with MPPF capacitors a reasonable and safe design becomes possible, managing high ripple currents with limited number of capacitor units [109].

The basic layout of an MPPF capacitor with alternating layers is depicted in Fig. 2.19. The alternating layers of metal elements with PP films in between are forming several capacitors, being connected by sprayed zinc contacts on each side [94]. By parallel connection the capacitance will be increased whereas the ESR and the ESL will be reduced [94], [110]. Beside increasing the thickness of the electrolyte, capacitor elements can be cascaded within the capacitor design for high voltage capability.

2.4.4 Reliability

For MPPF capacitors small differences in the quality and characteristics are common due to manufacturing and design effects. Degradation effects will deteriorate the performance during the component life. The degradation of MPPF capacitors is mainly driven by dielectric breakdowns (self-healing), electrochemical corrosion and connection instability (detachment) [111].

During dielectric breakdowns stored energy will be discharged, accompanied by arcs and high pressures for very short durations. Dielectric breakdowns are mainly caused by external overvoltages and voltage transients, affecting small areas with weakened block capability, accelerated by heat and chemical contaminates [57], [88], [94], [98]. Over the time tiny leakage currents can lead to a reduced blocking capability of the dielectric [98].

One of the most important benefits of MPPF capacitors is their unique self-healing capability in case of dielectric breakdowns [57], [94]. Self-healing capability means that the fault areas will be isolated because the very thin metal layers will be vaporized by the high current transients [99]. Each dielectric breakdown only leads to a very small loss in the dielectric material and the electrode area, corresponding in a small loss of capacitance and a small increase of the ESR [57], [88], [94], [99], [111]. The self-healing energy increases
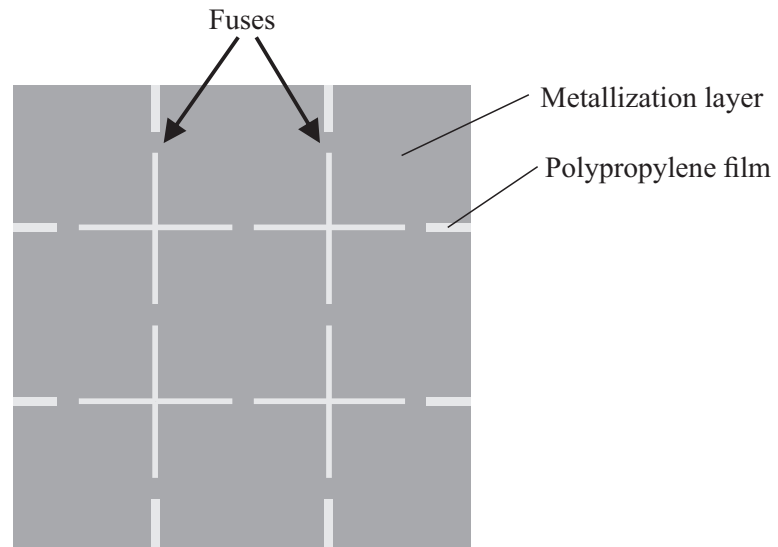
Figure 2.20: Segmented MPPF capacitor (top view) [57].

exponentially with the applied voltage at a power of 4.7 according to [107]. The stress of intact areas will increase by each breakdown, accordingly more advanced capacitance loss and ESR increase will inevitably lead to a limitation in a useful component life [88], [94].

For minimized damage and limited dielectric loss by self-healing MPPF capacitors the effective area can be divided in very small segments as illustrated in Fig. 2.20 [57]. Between these segments only small metalized interconnections are available for the current flow, acting as fuses [57]. For small self-healing events the fuses are not affected. However, in case of bigger dielectric breakdown, the current gates will evaporate due to their small cross section [57]. The fault area will be limited and isolated from the capacitor to prevent more severe short-circuits [57].

Another important degradation factor is the electrochemical corrosion, leading to an oxidation of the very thin metalized electrodes as well as moisture absorption by the plastic film [94]. The corrosion of the metalized electrodes is linked to a strongly increased ESR and can result in an open-circuit failure mode. Limited conductivity can cause local heating and hotspots in the capacitors, also attacking the dielectric material, decreasing the capacitance [89], [99]. Moisture absorption by the PP film can lead to increased leakage currents and dielectric loss of the material [94]. Corrosion processes are mainly driven by the environment, particularly the humidity and the temperature [95], [112]. Particularly in humid areas and offshore applications the housing and the placement of capacitors is from high importance.

Contact instability and detachments of the capacitor is another important degradation factors and can be also affected by electrochemical corrosion. Especially the sprayed zinc contacts are relatively vulnerable for detachments [94]. This degradation type is particularly relevant for pulsed power applications with high current peaks, linked to high electrical, thermal and mechanical stress, linked to an open-circuit fault type [94]. With the contact instability of outer contacts, the ESR is strongly increasing. However, also the capacitance can be reduced due to lost contacts [88], [99], [113]. After long service times, e.g. decades, also wear-

Table 2.3: Major degradation processes in MPPF capacitors.

Degradation processes	Main stressors	Electrical impact
Dielectric breakdown (self-healing)	V_{cap}, T_a, dV_{cap}/dt	$C \downarrow$, $R_{esr} \uparrow$
Connection instability	T_a, i_{cap}	$C \downarrow$, $R_{esr} \uparrow$
Wear-out	V_{cap}, T_a, i_{cap}, humidity	$C \downarrow$, $R_{esr} \uparrow$
Electrochemical corrosion	humidity	$C \downarrow$, $R_{esr} \uparrow$
Moisture absorption	humidity	$C \downarrow$, $R_{esr} \uparrow$

out failures are from high relevance, mainly driven by the cumulative electrical and thermal stress [114].

The capacitor lifetimes can be modeled based on different stress parameters. One widely used lifetime model is taking into account the operating voltage and the operating temperature [88]:

$$L_{f,cap} = L_{f,cap,0} \cdot \left(\frac{V_{cap}}{V_{cap,0}} \right)^{n_v} \cdot \exp \left(\frac{E_a}{K_B} \cdot \left(\frac{1}{T_{cap}} - \frac{1}{T_{cap,0}} \right) \right) \qquad (2.14)$$

The provided empirical model is valid for all capacitor types where K_B describes the Boltzmann's constant, E_a the activation energy and n_v the voltage stress exponent. The voltage stress exponent differs from around 7 to 9.4 for MPPF capacitors [98], being relatively sensitive to voltage stress. The voltage term becomes to 1 if the same voltage profile is applied.

The operating voltage, temperature and lifetime for specific test conditions are given by $V_{cap,0}$, $T_{cap,0}$ and $L_{f,cap,0}$, respectively and is commonly provided in the datasheet. Based on this information and the targeted operating voltage V_{cap} and the temperature T_{cap} the expected lifetime $L_{f,cap}$ can be approximated. The operating temperature can be measured or estimated based on the instantaneous power losses and the thermal impedance of the geometry. More extensive lifetime models are available as well, e.g. taking into account the humidity.

2.5 Neutral Point Clamped Inverter

The classical three-level NPC inverter is considered as the most promising high-power inverter solution for LV connection. This well-established topology will be further described and analyzed in this section. With the purpose of increased power ratings and modular configuration, the parallel inverter connection will be investigated.

2.5.1 Topology

The three-level NPC inverter is depicted in Fig. 2.21a with one single phase. Commonly, two IGBTs are switched on and the other two IGBTs switched off to block the applied DC-link voltage. Thus, three switching states can be defined during normal operation according to Table 2.4.
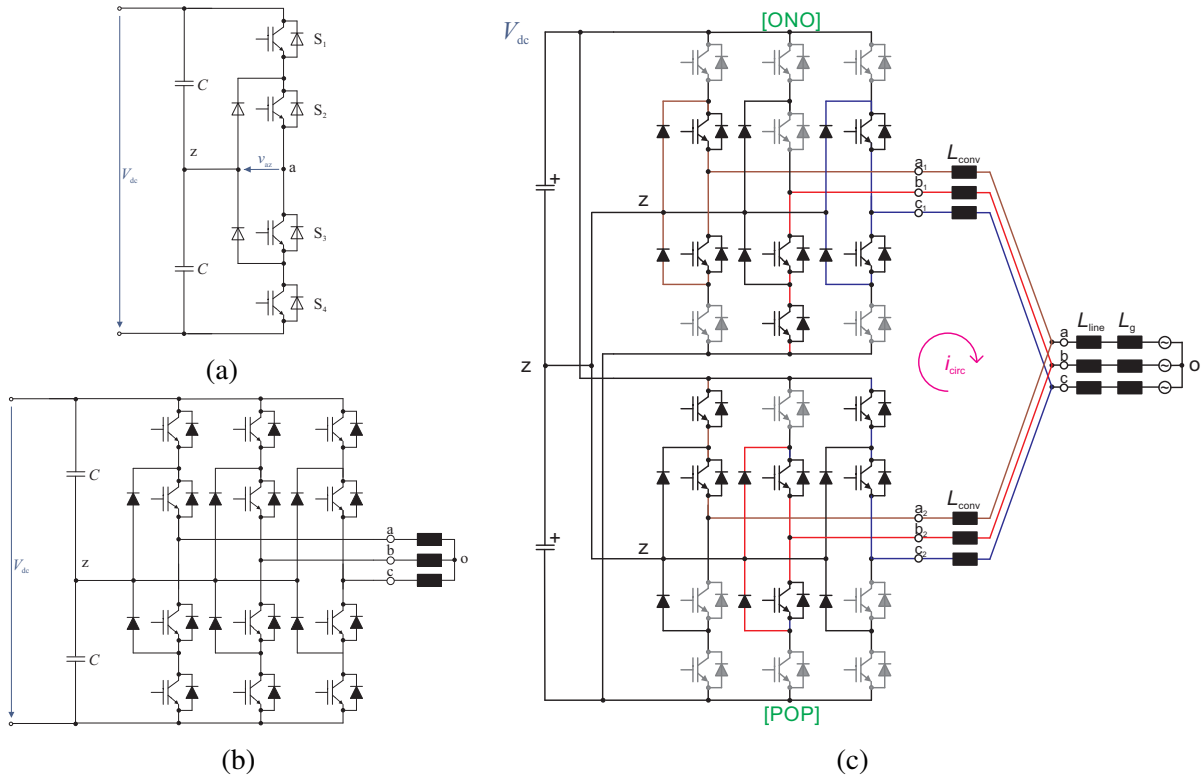
Figure 2.21: Three-level NPC inverter circuits: (a) One phase. (b) Three phases. (c) Parallel connection with a common DC-link and illustrated circulating current paths.

Table 2.4: Switching states and voltage levels of the three-level NPC inverter (one phase).

Switching state	S_1	S_2	S_3	S_4	v_{az}
P	1	1	0	0	$\frac{V_{dc}}{2}$
O	0	1	1	0	0
N	0	0	1	1	$-\frac{V_{dc}}{2}$

Three phase voltage levels can be generated, $-\frac{V_{dc}}{2}$, 0 and $\frac{V_{dc}}{2}$. The outer IGBT devices are only in use for positive (P) and negative (N) voltage generation, operating at a high switching frequencies. The inner IGBT devices are more frequently used, operating at the grid frequency.

The three-phase NPC circuit is shown in Fig. 2.21b. In three-phase systems the coupling between the phases needs to be taken into account. Furthermore, common-mode voltages can occur between the star point (o) and the neutral point (z) of the inverters, being described as follows:

$$v_{cm} = \frac{v_{az} + v_{bz} + v_{cz}}{3} \tag{2.15}$$

2.5.2 Parallel Connection

For three-level NPC inverters with standard semiconductor devices the power rating is limited and can be extended by parallel connection at the ac side as illustrated in Fig. 2.21. Each inverter provides an own filter L_{conv} and also an additional line filter L_{filter} can be applied. The dc side can be either paralleled or isolated from each other. With separated DC-links the circulating currents between the inverters can be minimized. Instead, a common DC-link allows current ripple cancellation. Furthermore, more design flexibility is provided since the number of inverters in a back-to-back system does not need to be equivalent in both stages. A common DC-link is also inherent in DC networks. However, circulating currents can occur between the inverters as highlighted in Fig. 2.21.

For two parallel inverters with common DC-link the following equations are obtained:

$$v_{\text{az}} = v_{\text{a1z}} - L_{\text{conv}} \cdot \frac{di_{\text{a1}}}{dt} \tag{2.16}$$

$$v_{\text{az}} = v_{\text{a2z}} - L_{\text{conv}} \cdot \frac{di_{\text{a2}}}{dt} \tag{2.17}$$

The voltage drops across the inductances are mainly driven by the shared line current, compensating each other for both inverters in symmetrical operation. Based on this assumption both equations can be simplified and summarized for the phase voltage according to (2.18).

$$v_{\text{az}} = \frac{v_{\text{a1z}} + v_{\text{a2z}}}{2} \tag{2.18}$$

Accordingly, two additional voltage levels can be generated, at $-\frac{V_{\text{dc}}}{4}$ and $\frac{V_{\text{dc}}}{4}$. For each additional three-level NPC inverter the number of available voltage levels will increase again by 2.

For parallel inverters the currents can be splitted into two parts, the contribution from the grid current i_{g} and a differential current i_{diff}, flowing between the inverters. Thus, for two inverters and a symmetrical system the following equations become valid in each phase:

$$i_{\text{a,conv1}} = \frac{i_{\text{g,a}}}{2} + i_{\text{diff,a}} \tag{2.19}$$

$$i_{\text{a,conv2}} = \frac{i_{\text{g,a}}}{2} - i_{\text{diff,a}} \tag{2.20}$$

Referring to Kirchhoff's second law, the differential currents can be defined in each phase according to (2.21).

$$\frac{di_{\text{diff,a}}}{dt} = \frac{v_{\text{az1}} - v_{\text{az2}}}{2L_{\text{conv}}} \tag{2.21}$$

The differential currents are forming the DC-side circulating current (zero-sequence) according to:

$$i_{\text{circ}} = i_{\text{diff,a}} + i_{\text{diff,b}} + i_{\text{diff,c}} \tag{2.22}$$

Consequently the circulating current can be defined by (2.23) depending on the filter inductances L_{conv} and the common mode voltage v_{cm}.

$$3 \cdot v_{\text{cm}} = 2L_{\text{conv}} \cdot \frac{di_{\text{circ}}}{dt} \tag{2.23}$$

The common mode voltage v_{cm} between the inverters is defined according to (2.24).

$$v_{\text{cm}} = v_{\text{cm1}} - v_{\text{cm2}} = \frac{v_{\text{az1}} + v_{\text{bz1}} + v_{\text{cz1}}}{3} - \frac{v_{\text{az2}} + v_{\text{bz2}} + v_{\text{cz2}}}{3} \tag{2.24}$$

Circulating currents are linked to higher currents and higher thermal stress in the semiconductor devices and the capacitors. Furthermore, higher voltage drops can occur. Between perfectly synchronized inverters the common mode voltage is zero and no circulating current will be generated. However, very small jitters from the drivers and other tiny time shifts cannot be avoided in real systems.

The inverters can also operate in interleaved mode where the switching sequences are shifted to each other, e.g. to use all available voltage levels in accordance with (2.18). In this case the given switching states can differ for the inverters. In Fig. 2.21 the switching states ONO and POP are applied as one example. For further illustration the IGBTs are colored in black (turned-on) and gray (turned-off). Based on (2.24) the common mode voltage between the inverters is half of the DC-link voltage in this case, representing the maximum and leading to circulating currents between the inverters. On the one hand the amplitude can be limited by the converter filters. On the other hand, also the switching frequency has a significant impact [115], [116].

2.6 Modular Multilevel Converter

For direct MV and HV connection the MMC is considered as the most promising high-power inverter. The MMC modeling and control will be further described in the following section.
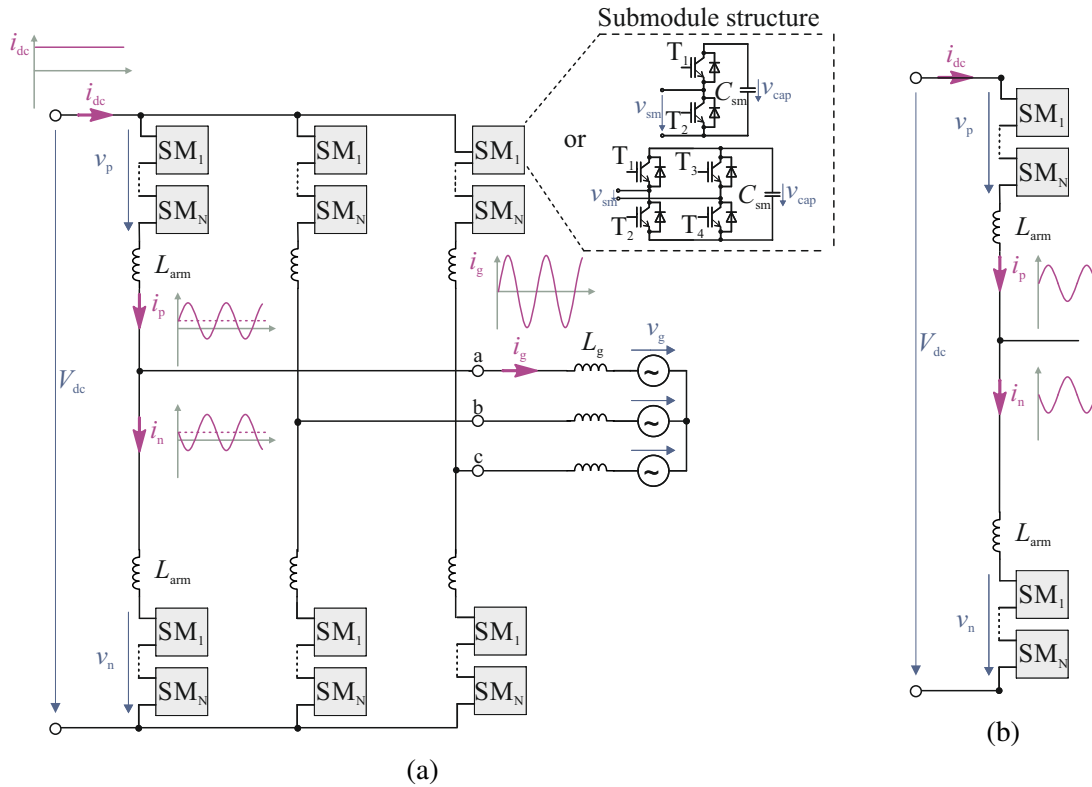
Figure 2.22: Modular multilevel converter circuit in double-star configuration: (a) Three phases with 50 Hz current waveforms. (b) One phase.

2.6.1 Topology

The MMC circuit in double-star configuration is depicted in Fig. 2.22, for three-phase and one-phase configuration, respectively. In each arm there are N series connected SMs, commonly realized by chopper-cells (CC, half-bridges) or bridge-cells (BC, full-bridges). Furthermore, an inductance L_{arm} is applied in each arm for current limitation and filtering.

2.6.2 Mathematical Model

Each CC is equipped with one capacitor storage, two IGBTs and two diodes. The terminal voltages at each CC can be switched between 0 and v_{cap} according to:

$$v_{\text{SM}}^{\text{CC}} = \begin{cases} v_{\text{cap}} & \text{if S=1} \\ 0 & \text{if S=0} \end{cases}$$

One BC requires two additional semiconductor devices and is very attractive due to its dc fault handling capability, e.g. being beneficial for HVDC overhead lines [117], [118]. The BC provides two zero states and also negative polarity according to:

$$v_{\text{SM}}^{\text{BC}} = \begin{cases} v_{\text{cap}} & \text{if S=1} \\ 0 & \text{if S=0} \\ -v_{\text{cap}} & \text{if S=-1} \end{cases}$$

The arm voltages can be described by the sum of the SM voltages according to (2.25) and (2.26), where x is corresponding to the switching state of the xth SM.

$$v_{\text{p}} = \sum_{x=1}^{N} |S_{\text{p}}(x)| \cdot v_{\text{cap,p}}(x) \tag{2.25}$$

$$v_{\text{n}} = \sum_{x=1}^{N} |S_{\text{n}}(x)| \cdot v_{\text{cap,n}}(x) \tag{2.26}$$

The MMC converter voltage is defined by half of the difference between the lower and upper arm voltage according to (2.27). It is valid as an approximation for the applied phase voltage, neglecting the voltage drops across the arm inductors.

$$v_{\text{conv}} = \frac{v_{\text{n}} - v_{\text{p}}}{2} \tag{2.27}$$

The phase voltage can be described as follows:

$$v_{\text{phase}} = R_{\text{g}} \cdot i_{\text{g}} + L_{\text{g}} \cdot \frac{\text{d}i_{\text{g}}}{\text{d}t} + v_{\text{g}} \tag{2.28}$$

The grid current can be expressed by Kirchhoff's first law and is composed by the arm currents according to (2.29).

$$i_{\text{g}} = i_{\text{p}} - i_{\text{n}} \tag{2.29}$$

One-Phase System

Based on the one-phase circuit, Kirchhoff's second law provides (2.30) and (2.31) for mesh I and II, respectively.

$$\frac{V_{\text{dc}}}{2} = v_{\text{p}} + L_{\text{arm}} \cdot \frac{\text{d}i_{\text{p}}}{\text{d}t} + R_{\text{arm}} \cdot i_{\text{p}} + v_{\text{phase}} \tag{2.30}$$

$$\frac{V_{\text{dc}}}{2} = v_{\text{n}} + L_{\text{arm}} \cdot \frac{\text{d}i_{\text{n}}}{\text{d}t} + R_{\text{arm}} \cdot i_{\text{n}} - v_{\text{phase}} \tag{2.31}$$

By subtracting (2.30) from (2.28) and plugging in (2.29) the following expression is obtained:

$$v_n - v_p = L_{arm} \cdot \frac{d(i_p - i_n)}{dt} + R_{arm} \cdot (i_p - i_n) + 2R_g \cdot i_g + 2L_g \cdot \frac{di_g}{dt} + 2v_g \qquad (2.32)$$

Thus, the grid current can be controlled by the converter voltage according to:

$$\frac{v_n - v_p}{2} = \left(\frac{L_{arm}}{2} + L_g\right)\frac{i_g}{t} + \left(\frac{R_{arm}}{2} + R_g\right)i_g + v_g \qquad (2.33)$$

The arm currents can be splitted into two components, composed by half of the phase current and the differential current.

$$i_p = \frac{i_g}{2} + i_{diff} \qquad (2.34)$$

$$i_n = -\frac{i_g}{2} + i_{diff} \qquad (2.35)$$

The differential currents are flowing from dc side and can be described by the outer mesh according to (2.36). The differential voltage represents the voltage drop across the arm inductors and can be used to control the differential current from the dc side [119].

$$v_{diff} = V_{dc} - (v_p + v_n) = 2L_{arm} \cdot \frac{di_{diff}}{dt} + 2R_{arm} \cdot i_{diff} \qquad (2.36)$$

Three-Phase System

For a conventional three-phase system the ac-side currents and voltages are not decoupled from each other. For taking into account the coupling between them, the line-to-line voltages are described in (2.37)-(2.39).

$$v_{ab} = v_{phase,a} - v_{phase,b} \qquad (2.37)$$

$$v_{bc} = v_{phase,b} - v_{phase,c} \qquad (2.38)$$

$$v_{ca} = v_{phase,c} - v_{phase,a} \qquad (2.39)$$

Based on (2.40)-(2.45) the line-to-line voltages can be rewritten as follows:

$$v_{ab} = v_{p,b} + L_{arm} \cdot \frac{di_{p,b}}{dt} + R_{arm} \cdot i_{p,b} - v_{p,a} - L_{arm} \cdot \frac{di_{p,a}}{dt} - R_{arm} \cdot i_{p,a} \tag{2.40}$$

$$= v_{n,a} + L_{arm} \cdot \frac{di_{n,a}}{dt} + R_{arm} \cdot i_{n,a} - v_{n,b} - L_{arm} \cdot \frac{di_{n,b}}{dt} - R_{arm} \cdot i_{n,b} \tag{2.41}$$

$$v_{bc} = v_{p,c} + L_{arm} \cdot \frac{di_{p,c}}{dt} + R_{arm} \cdot i_{p,c} - v_{p,b} - L_{arm} \cdot \frac{di_{p,b}}{dt} - R_{arm} \cdot i_{p,b} \tag{2.42}$$

$$= v_{n,b} + L_{arm} \cdot \frac{di_{n,b}}{dt} + R_{arm} \cdot i_{n,b} - v_{n,c} - L_{arm} \cdot \frac{di_{n,c}}{dt} - R_{arm} \cdot i_{n,c} \tag{2.43}$$

$$v_{ca} = v_{p,a} + L_{arm} \cdot \frac{di_{p,a}}{dt} + R_{arm} \cdot i_{p,a} - v_{p,c} - L_{arm} \cdot \frac{di_{p,c}}{dt} - R_{arm} \cdot i_{p,c} \tag{2.44}$$

$$= v_{n,c} + L_{arm} \cdot \frac{di_{n,c}}{dt} + R_{arm} \cdot i_{n,c} - v_{n,a} - L_{arm} \cdot \frac{di_{n,a}}{dt} - R_{arm} \cdot i_{n,a} \tag{2.45}$$

The arm currents can be replaced by (2.34) and (2.35), exemplary done for the voltage between the lines a and b.

$$
\begin{aligned}
v_{ab} = \;& v_{p,b} + L_{arm} \cdot \frac{d\left(i_{diff,b} + \frac{i_{g,b}}{2}\right)}{dt} + R_{arm} \cdot \left(i_{diff,b} + \frac{i_{g,b}}{2}\right) \\
& - v_{p,a} - L_{arm} \cdot \frac{d\left(i_{diff,a} + \frac{i_{g,a}}{2}\right)}{dt} - R_{arm} \cdot \left(i_{diff,a} + \frac{i_{g,a}}{2}\right)
\end{aligned}
\tag{2.46}
$$

$$
\begin{aligned}
= \;& v_{n,a} + L_{arm} \cdot \frac{d\left(i_{diff,a} - \frac{i_{g,a}}{2}\right)}{dt} + R_{arm} \cdot \left(i_{diff,a} - \frac{i_{g,a}}{2}\right) \\
& - v_{n,b} - L_{arm} \cdot \frac{d\left(i_{diff,b} - \frac{i_{g,b}}{2}\right)}{dt} - R_{arm} \cdot \left(i_{diff,a} - \frac{i_{g,a}}{2}\right)
\end{aligned}
\tag{2.47}
$$

Accordingly, the expression in (2.48) can be derived.

$$v_{ab} = \frac{v_{n,a} - v_{p,a}}{2} - \frac{v_{n,b} - v_{p,b}}{2} + \frac{L_{arm}}{2} \cdot \frac{d(i_{g,b} - i_{g,a})}{dt} + \frac{R_{arm}}{2} \cdot (i_{g,b} - i_{g,a}) \tag{2.48}$$

Based on the converter voltage from (2.27) and the phase voltages (2.28) the following equations are obtained:

$$v_{ab} = v_{conv,a} - v_{conv,b} + \frac{L_{arm}}{2} \cdot \frac{d(i_{g,b} - i_{g,a})}{dt} + \frac{R_{arm}}{2} \cdot (i_{g,b} - i_{g,a}) \tag{2.49}$$

$$= R_g \cdot (i_{g,a} - i_{g,b}) + L_g \cdot \frac{d(i_{g,a} - i_{g,b})}{dt} + v_{g,a} - v_{g,b} \tag{2.50}$$

$$v_{bc} = v_{conv,b} - v_{conv,c} + \frac{L_{arm}}{2} \cdot \frac{d(i_{g,c} - i_{g,b})}{dt} + \frac{R_{arm}}{2} \cdot (i_{g,c} - i_{g,b}) \tag{2.51}$$

$$= R_g \cdot (i_{g,b} - i_{g,c}) + L_g \cdot \frac{d(i_{g,b} - i_{g,c})}{dt} + v_{g,b} - v_{g,c} \tag{2.52}$$

$$v_{ca} = v_{conv,c} - v_{conv,a} + \frac{L_{arm}}{2} \cdot \frac{d(i_{g,a} - i_{g,c})}{dt} + \frac{R_{arm}}{2} \cdot (i_{g,a} - i_{g,c}) \tag{2.53}$$

$$= R_g \cdot (i_{g,c} - i_{g,a}) + L_g \cdot \frac{d(i_{g,c} - i_{g,a})}{dt} + v_{g,c} - v_{g,a} \tag{2.54}$$

Not only the voltages but also the phase currents are coupled among each others and its sum becomes to zero:

$$i_{g,a} + i_{g,b} + i_{g,c} = 0 \tag{2.55}$$

Accordingly, the line-to-line voltage can be rewritten to:

$$v_{ab} = v_{conv,a} - v_{conv,b} + \frac{L_{arm}}{2} \cdot \frac{d(2i_{g,b} + i_{g,c})}{dt} + \frac{R_{arm}}{2} \cdot (2i_{g,b} + i_{g,c}) \tag{2.56}$$

$$= -R_g \cdot (2i_{g,b} + i_{g,c}) + L_g \cdot \frac{d(2i_{g,b} + i_{g,c})}{dt} + v_{g,a} - v_{g,b} \tag{2.57}$$

$$v_{bc} = v_{conv,b} - v_{conv,c} + \frac{L_{arm}}{2} \cdot \frac{d(i_{g,a} + 2i_{g,c})}{dt} + \frac{R_{arm}}{2} \cdot (i_{g,a} + 2i_{g,c}) \tag{2.58}$$

$$= -R_g \cdot (i_{g,a} + i_{g,c}) + L_g \cdot \frac{d(i_{g,a} + 2i_{g,c})}{dt} + v_{g,a} - v_{g,b} \tag{2.59}$$

$$v_{ca} = v_{conv,c} - v_{conv,a} + \frac{L_{arm}}{2} \cdot \frac{d(2i_{g,a} + i_{g,b})}{dt} + \frac{R_{arm}}{2} \cdot (2i_{g,a} + i_{g,b}) \tag{2.60}$$

$$= -R_g \cdot (2i_{g,a} + i_{g,b}) + L_g \cdot \frac{d(2i_{g,a} + i_{g,b})}{dt} + v_{g,a} - v_{g,b} \tag{2.61}$$

For the expression of each phase current the equations have been combined in (2.62)-(2.64). (2.56) has been subtracted from (2.61), (2.58) from (2.57) and (2.60) from (2.59).

$$v_{\text{conv,b}} - 2v_{\text{conv,a}} + v_{\text{conv,c}} + \frac{3}{2}L_{\text{arm}} \cdot \frac{di_{\text{g,a}}}{dt} + \frac{3}{2}R_{\text{arm}} \cdot i_{\text{g,a}}$$

$$= -3R_{\text{g}} \cdot i_{\text{g,a}} - 3L_{\text{g}} \cdot \frac{di_{\text{g,a}}}{dt} + v_{\text{g,b}} - 2v_{\text{g,a}} + v_{\text{g,c}} \tag{2.62}$$

$$v_{\text{conv,a}} - 2v_{\text{conv,b}} + v_{\text{conv,c}} + \frac{3}{2}L_{\text{arm}} \cdot \frac{di_{\text{g,b}}}{dt} + \frac{3}{2}R_{\text{arm}} \cdot i_{\text{g,b}}$$

$$= -3R_{\text{g}} \cdot i_{\text{g,b}} - 3L_{\text{g}} \cdot \frac{di_{\text{g,b}}}{dt} + v_{\text{g,a}} - 2v_{\text{g,b}} + v_{\text{g,c}} \tag{2.63}$$

$$v_{\text{conv,b}} - 2v_{\text{conv,c}} + v_{\text{conv,a}} + \frac{3}{2}L_{\text{arm}} \cdot \frac{di_{\text{g,c}}}{dt} + \frac{3}{2}R_{\text{arm}} \cdot i_{\text{g,c}}$$

$$= -3R_{\text{g}} \cdot i_{\text{g,c}} - 3L_{\text{g}} \cdot \frac{di_{\text{g,c}}}{dt} + v_{\text{g,a}} - 2v_{\text{g,c}} + v_{\text{g,b}} \tag{2.64}$$

Consequently, the grid current can be described by (2.65)-(2.67), being dependent from the impedances, the grid voltages and the applied converter voltages.

$$\left(3L_{\text{g}} + \frac{3}{2}L_{\text{arm}}\right)\frac{di_{\text{g,a}}}{dt} + \left(3R_{\text{g}} + \frac{3}{2}R_{\text{arm}}\right)i_{\text{g,a}}$$

$$= 2v_{\text{conv,a}} - v_{\text{conv,b}} - v_{\text{conv,c}} + 2v_{\text{g,a}} - v_{\text{g,b}} - v_{\text{g,c}} \tag{2.65}$$

$$\left(3L_{\text{g}} + \frac{3}{2}L_{\text{arm}}\right)\frac{di_{\text{g,b}}}{dt} + \left(3R_{\text{g}} + \frac{3}{2}R_{\text{arm}}\right)i_{\text{g,b}}$$

$$= -v_{\text{conv,a}} + 2v_{\text{conv,b}} - v_{\text{conv,c}} + v_{\text{g,a}} - 2v_{\text{g,b}} + v_{\text{g,c}} \tag{2.66}$$

$$\left(3L_{\text{g}} + \frac{3}{2}L_{\text{arm}}\right)\frac{di_{\text{g,c}}}{dt} + \left(3R_{\text{g}} + \frac{3}{2}R_{\text{arm}}\right)i_{\text{g,c}}$$

$$= -v_{\text{conv,a}} - v_{\text{conv,b}} + 2v_{\text{conv,c}} - v_{\text{g,a}} - v_{\text{g,b}} + 2v_{\text{g,c}} \tag{2.67}$$

Instead, the differential currents can be considered as decoupled for DC-connected MMC applications. However, for STATCOM operation without DC-link connection the coupling between the phases (legs) needs to be taken into account. The three legs provide three meshes and the following equations are obtained:

$$(v_{\text{p,a}} + v_{\text{n,a}}) - (v_{\text{p,b}} + v_{\text{n,b}}) = 4L_{\text{arm}} \cdot \frac{d(i_{\text{diff,b}} - i_{\text{diff,a}})}{dt} + 4R_{\text{arm}} \cdot (i_{\text{diff,b}} - i_{\text{diff,a}}) \tag{2.68}$$

$$(v_{\text{p,b}} + v_{\text{n,b}}) - (v_{\text{p,c}} + v_{\text{n,c}}) = 4L_{\text{arm}} \cdot \frac{d(i_{\text{diff,c}} - i_{\text{diff,b}})}{dt} + 4R_{\text{arm}} \cdot (i_{\text{diff,c}} - i_{\text{diff,b}}) \tag{2.69}$$

$$(v_{\text{p,c}} + v_{\text{n,c}}) - (v_{\text{p,a}} + v_{\text{n,a}}) = 4L_{\text{arm}} \cdot \frac{d(i_{\text{diff,a}} - i_{\text{diff,c}})}{dt} + 4R_{\text{arm}} \cdot (i_{\text{diff,a}} - i_{\text{diff,c}}) \tag{2.70}$$

The sum of the differential currents becomes zero since no dc-side current can flow according to (2.71).

$$i_{\text{diff,a}} + i_{\text{diff,b}} + i_{\text{diff,c}} = 0 \qquad (2.71)$$

Accordingly, the mesh equations from (2.68-2.70) can be rearranged:

$$(v_{\text{p,a}} + v_{\text{n,a}}) - (v_{\text{p,b}} + v_{\text{n,b}}) = 4L_{\text{arm}} \cdot \frac{\text{d}(2i_{\text{diff,b}} + i_{\text{diff,c}})}{\text{d}t} + 4R_{\text{arm}} \cdot (2i_{\text{diff,b}} + i_{\text{diff,c}}) \qquad (2.72)$$

$$(v_{\text{p,b}} + v_{\text{n,b}}) - (v_{\text{p,c}} + v_{\text{n,c}}) = 4L_{\text{arm}} \cdot \frac{\text{d}(2i_{\text{diff,c}} + i_{\text{diff,a}})}{\text{d}t} + 4R_{\text{arm}} \cdot (2i_{\text{diff,c}} + i_{\text{diff,a}}) \qquad (2.73)$$

$$(v_{\text{p,c}} + v_{\text{n,c}}) - (v_{\text{p,a}} + v_{\text{n,a}}) = 4L_{\text{arm}} \cdot \frac{\text{d}(2i_{\text{diff,a}} + i_{\text{diff,b}})}{\text{d}t} + 4R_{\text{arm}} \cdot (2i_{\text{diff,a}} + i_{\text{diff,b}}) \qquad (2.74)$$

By combination of all three equations the expressions in (2.75)-(2.77) are obtained for the differential currents, being dependent from the arm impedances and the sum of the applied arm voltages.

$$(v_{\text{p,c}} + v_{\text{n,c}}) - 2(v_{\text{p,a}} + v_{\text{n,a}}) + (v_{\text{p,b}} + v_{\text{n,b}}) = 12R_{\text{arm}} \cdot i_{\text{diff,a}} + 12L_{\text{arm}} \cdot \frac{\text{d}i_{\text{diff,a}}}{\text{d}t} \qquad (2.75)$$

$$(v_{\text{p,a}} + v_{\text{n,a}}) - 2(v_{\text{p,b}} + v_{\text{n,b}}) + (v_{\text{p,c}} + v_{\text{n,c}}) = 12R_{\text{arm}} \cdot i_{\text{diff,b}} + 12L_{\text{arm}} \cdot \frac{\text{d}i_{\text{diff,b}}}{\text{d}t} \qquad (2.76)$$

$$(v_{\text{p,b}} + v_{\text{n,b}}) - 2(v_{\text{p,c}} + v_{\text{n,c}}) + (v_{\text{p,a}} + v_{\text{n,a}}) = 12R_{\text{arm}} \cdot i_{\text{diff,c}} + 12L_{\text{arm}} \cdot \frac{\text{d}i_{\text{diff,c}}}{\text{d}t} \qquad (2.77)$$

The model which has been developed and implemented based on the introduced mathematical model.

2.6.3 Control

The applied MMC control scheme is depicted in Fig. 2.23. The active and reactive power supply is directly linked to the grid currents. In rectifier mode the active power can be used to control the stored energy in the capacitors. Accordingly, for STATCOM applications the active power and stored energy can be controlled without any DC connection. The grid currents themselves can be properly controlled by the applied converter voltages.

For proper control of the stored energies in each arm and each leg, the differential current can be used. If DC connectivity is available, the stored energy can be regulated by the differential currents from the DC side. For the differential current the 100 Hz component is most characteristic to compensate the power oscillations in each leg. Furthermore, a DC component represents the active power transfer between the DC and AC side. The arm
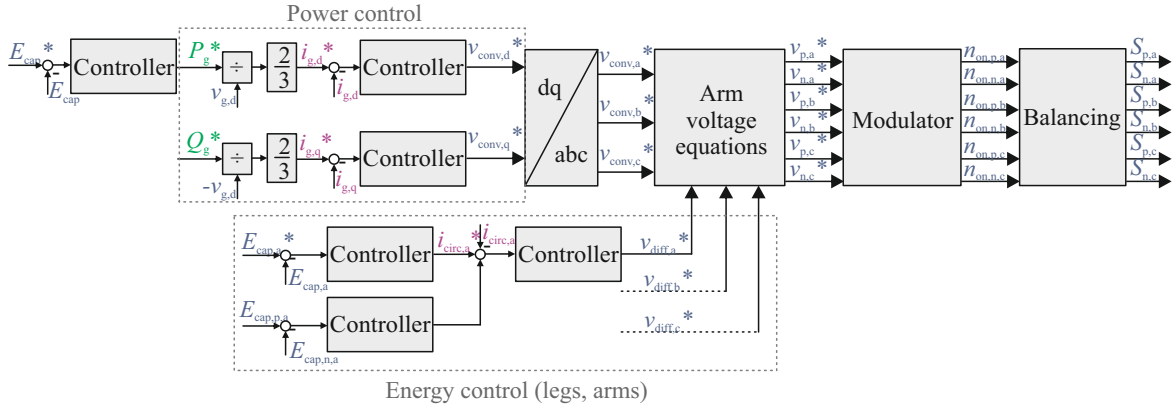
Figure 2.23: Overall control scheme for the modular multilevel converter.

currents are composed by half of the grid currents in symmetrical operation and the DC-side differential currents. For economical design the differential current oscillations need to be limited and therefore, the 50 Hz component from the grid current is dominant in the arm currents.

Both the converter voltages and the differential voltages can be set by the arm voltages. For the CC-MMC the required arm voltages is described in (2.78) and (2.79). The arm voltages are shifted by $\frac{V_{dc}}{2}$ since the CC-SMs only provide one polarity. In this way the converter voltage range is defined between $-\frac{V_{dc}}{2}$ and $\frac{V_{dc}}{2}$.

$$v_{p,CC}^* = -v_{conv}^* - \frac{v_{diff}^*}{2} + \frac{V_{dc}}{2} \tag{2.78}$$

$$v_{n,CC}^* = v_{conv}^* - \frac{v_{diff}^*}{2} + \frac{V_{dc}}{2} \tag{2.79}$$

For the BC-MMC an additional arm voltage shift can be avoided due to positive and negative SM voltage polarity. The theoretical converter voltage range has been doubled for the same number of SMs, being defined between $-V_{dc}$ and V_{dc}.

$$v_{p,BC}^* = -v_{conv}^* - \frac{v_{diff}^*}{2} \tag{2.80}$$

$$v_{n,BC}^* = v_{conv}^* - \frac{v_{diff}^*}{2} \tag{2.81}$$

```
                          ┌──────────────┐
                          │  Multilevel  │
                          │  Modulation  │
                          └──────────────┘
                ┌─────────────────┴──────────────────┐
        ┌───────────────┐                    ┌───────────────┐
        │ Space Vector  │                    │ Voltage Level │
        │    Based      │                    │    Based      │
        │  Algorithm    │                    │  Algorithm    │
        └───────────────┘                    └───────────────┘
```
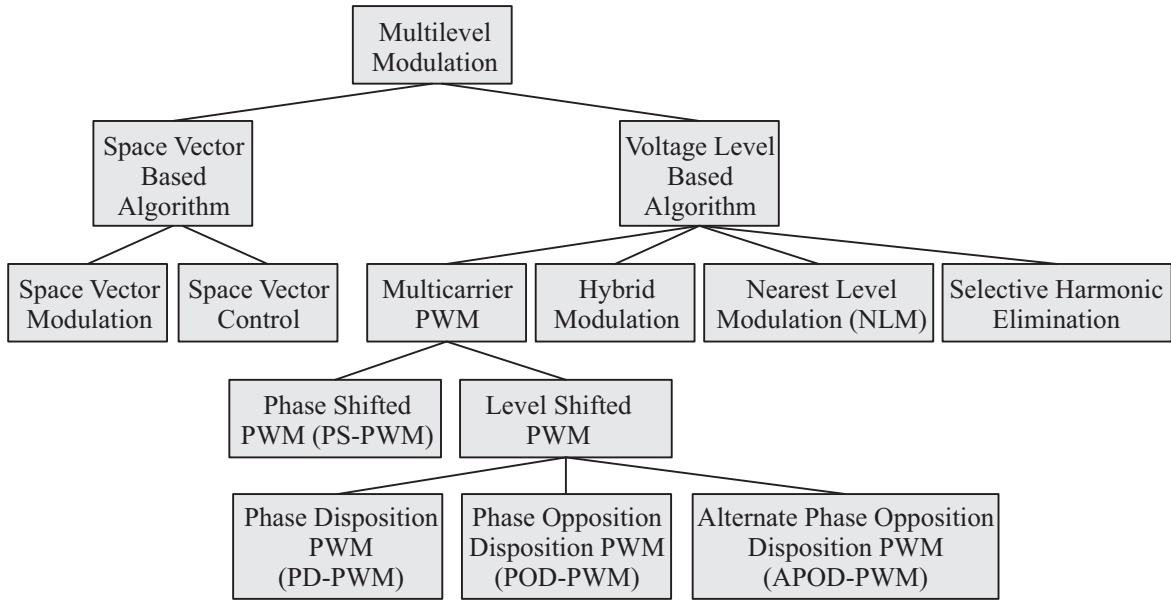
Figure 3.1: Classical multilevel modulation techniques.

3 Modulation Techniques for Modular Topologies

Suitable multilevel and interleaved modulation techniques are investigated for cascaded and paralleled modular power converters and analyzed for parallel three-level NPC inverters and the MMC.

3.1 Multilevel Modulation

One of the main benefits of multilevel inverters is linked to the multilevel voltage generation. The multilevel voltage generation provides additional degrees of freedom for performance optimization and a high variety of applicable modulation techniques. The standard multilevel modulation techniques are summarized in Fig. 3.1 and can be classified into space vector based and voltage-level based algorithms [25].

For the space vector modulation, the voltage reference vector is averaged by the three nearest switchable voltage vectors with a predefined switching frequency [120]. Instead, for the space vector control always the closest voltage vector is applied. In this way the number of commutations is reduced to a minimum. However, a high number of voltage steps is required for proper voltage generation. The space vector modulation is well-established for a low number of levels due to digital implementation and high performance. However, for a high number of voltage levels space vector based algorithms are becoming too complex, growing exponentially with the number of voltage levels [121], [122], [123].

The carrier-based PWM techniques are most established among the voltage level based algorithms. For carrier-based modulation techniques the carriers are compared with the voltage reference signal. The switching operations are determined by the intersection points and they linked to a relatively high switching frequency. Usually, for an n voltage level application
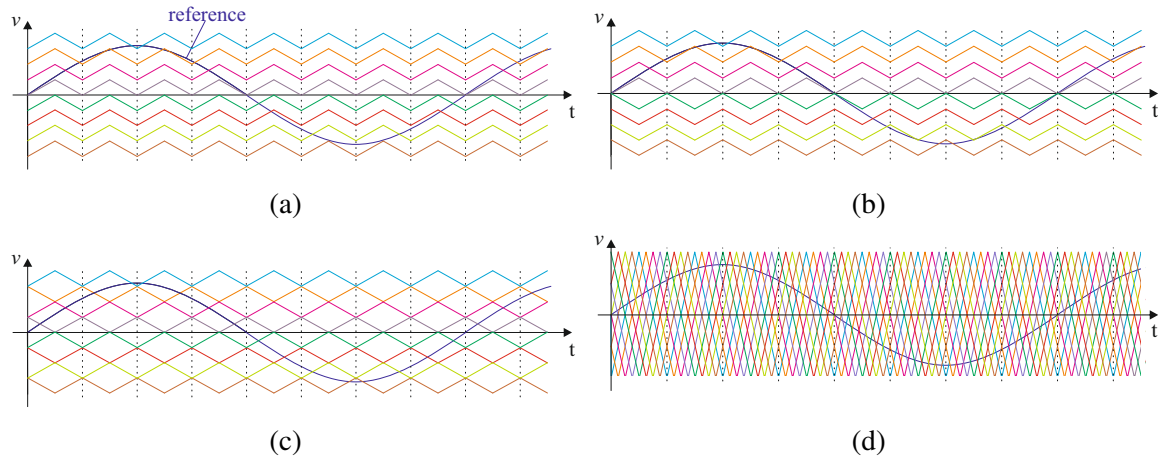
Figure 3.2: Multilevel PWM techniques (nine voltage levels): (a) PD-PWM. (b) POD-PWM. (c) APOD-PWM. (d) PS-PWM.

$n-1$ carriers are applied for proper waveform generation. In Fig. 3.2 the conventional multilevel PWM techniques are illustrated, namely the phase disposition (PD), the phase opposition disposition (POD), the alternative opposition disposition (APOD) and the phase-shifted (PS) PWM. The carriers of the PD-PWM, POD-PWM and APOD-PWM are level-shifted. All carriers are in phase for the PD-PWM. Instead, for the POD-PWM the upper carriers are shifted by $180°$ compared to the lower carriers. For the APOD-PWM each adjacent carrier is shifted to each other by $180°$. Furthermore, the PS-PWM can be applied where the carriers are evenly shifted horizontally.

Beyond that, the multilevel modulation can be also realized by algorithms. This is the case for the nearest level modulation (NLM) and selective harmonic elimination which can be classified both as staircase modulation techniques [124]. The NLM approximates the reference voltage to the closest available voltage step. In this way the number of commutations and the switching frequency are minimized. However, a high number of voltage levels is required for proper waveform generation. The selective harmonic elimination is also based on the NLM and it is optimizing the angles of the staircase waveform for minimized harmonic distortion. However, the computation effort becomes very high especially for a high number of voltage levels.

For hybrid modulation the features of different modulation techniques can be combined. For instance, the NLM can be combined with a PS-PWM to profit from a very low switching frequency and limited harmonic distortion at the same time [125]. However, it is also linked to high noises for a wide frequency range, being challenging to be filtered.

The proper choice of the modulation technique mainly depends on the target application and the preferred converter topology. Space vector based algorithms are well established due to its good performance, however being limited to a low number of voltage levels due to the high computational effort. Carrier-based PWM techniques are also well-proven and they showing a good performance, however being linked to relatively high switching frequencies. The NLM can be easily implemented and shows very low switching losses, however a high number of voltage levels is required. The selective harmonic elimination achieves a good
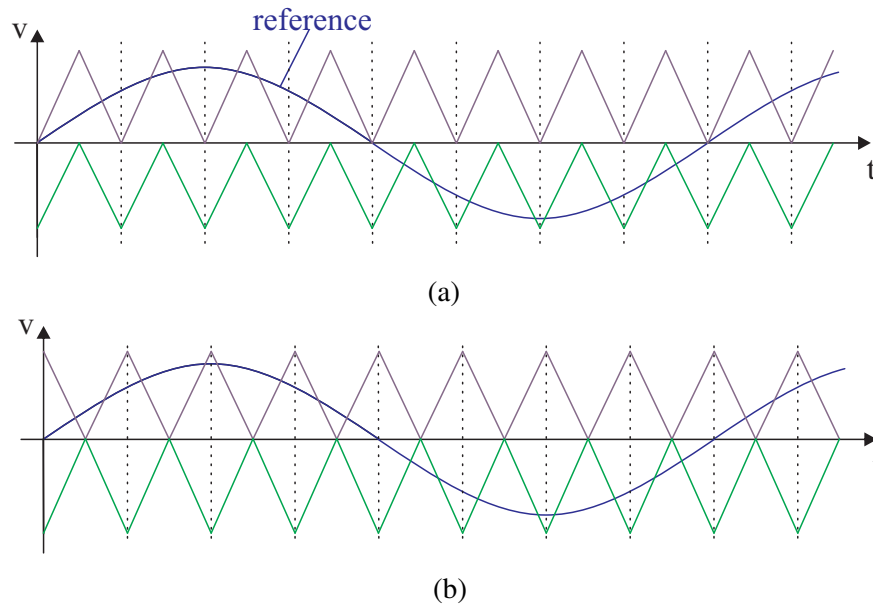
Figure 3.3: Three-level NPC inverter: (a) PD-PWM. (b) POD-PWM / APOD-PWM.

waveform quality with a lower number of voltage levels, however with a very high computation effort. Hybrid modulation combines the benefits of the NLM and PWM techniques, however also their drawbacks.

For the increase of the voltage range third harmonic injection can be applied for all classical modulation techniques, extending the available modulation range by around 15 % at the same DC-link voltage [126].

3.1.1 Three-Level NPC

For the three-level NPC the space-vector modulation and PWM techniques are well established due to the limited number of voltage levels [127], [128]. For the PWM techniques only two carries are required, being in phase for the PD-PWM. The POD-PWM and the APOD-PWM are equivalent for the three-level NPC, where both carriers are shifted by $180°$. The basic PWM schemes are illustrated in Fig. 3.3.

Among the carrier-based PWM techniques the PD-PWM provides the best waveform quality and therefore can be seen as the preferred choice for the NPC [129], [128]. For digital implementation the classical space vector modulation can be applied, being equivalent with the PD-PWM with third harmonic injection [130].

3.1.2 Modular Multilevel Converter

The MMC is usually connected to high or medium voltages, providing a very high number of voltage levels. Therefore, not only classical PWM techniques but also the NLM can be applied. Among the PWM techniques the PS-PWM benefits from its very homogenous switching profile which limits the spread in the capacitor voltages and the semiconductor
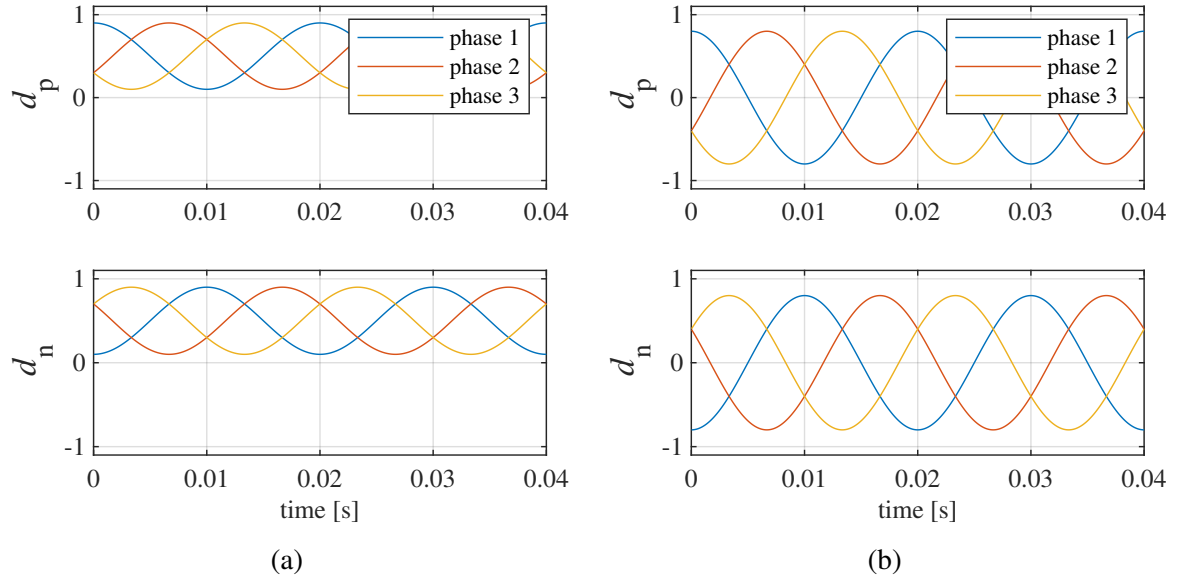
Figure 3.4: Duty cycles for upper and lower arm (m=0.8): (a) CC-MMC. (b) BC-MMC.

stress [131]. On the other hand, the NLM benefits from minimum switching losses and also the computation effort is limited. Since the number of voltage levels is very high the power quality by the NLM is already excellent even without additional filters. Since the efficiency is very crucial in high-power applications the focus is put on the NLM for the MMC, being scalable up to dozens and hundreds of SMs in each arm [31].

For determining the insertion numbers in each arm, the duty cycle can be determined by (3.1) for the MMC, independent from the SM topology. N describes the number of SMs in each arm and v_{cap}^* the reference capacitor voltage in each SM. For selection of the specific SMs it is advantageous to choose them to balance the capacitor voltages, being decoupled from the modulator itself. For a minimal number of switching events and maximum efficiency not more SMs should be turned on or off than demanded by the modulator to follow the sinusoidal reference.

$$d = \frac{v_{arm}^*}{N \cdot v_{cap}^*} \tag{3.1}$$

The linear modulation range is defined up to 1. For the CC-MMC the minimum modulation index is equal to 0 since each SM can only be switched between 0 and the applied capacitor voltage v_{cap}. Different to this, the SMs of the BC-MMC can also provide $-v_{cap}$ at the terminals. Accordingly, the modulation range has been extended from 1 to -1. By also using the negative voltage polarity, the available converter voltage can be doubled according to (2.27). The behavior of the duty cycle is depicted in Fig 3.4 for steady state conditions ($m = 0.8$). The insertion number is directly linked to the duty cycle according to (3.2).

$$n_{on} = \text{round}\left(d \cdot \frac{v_{dc}}{v_{cap}^*}\right) \tag{3.2}$$
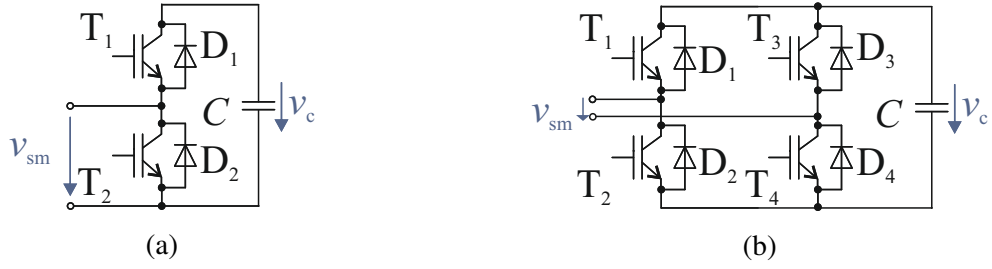
Figure 3.5: MMC submodule topologies: (a) Chopper-cell. (b) Bridge-cell.
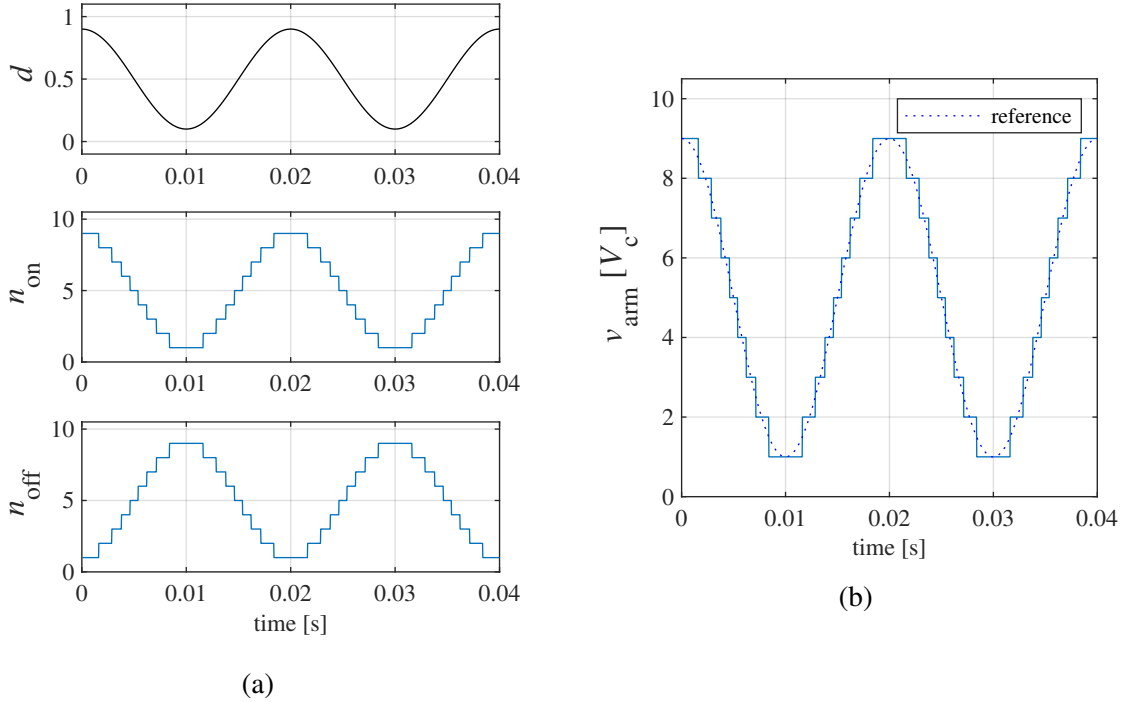
Figure 3.6: CC-MMC: (a) Insertion numbers (d=0.8, $N_{CC} = 10$). (b) Upper arm voltage.

CC-MMC

In Fig. 3.5a one SM in CC configuration is depicted. The conventional switching states and the corresponding current paths are summarized in Table 3.1. If one SM is turned-on ($S_{CC} = 1$) the capacitor voltage v_{cap} is applied at the terminals. Instead, for turned-off SMs zero voltage is applied. The current paths depend in both cases on the arm current direction. Each transient of the switching state is limited to one turning-off and one turning-on event in the semiconductor devices as summarized in Table 3.2. The insertion number n_{on} can be easily calculated based on (3.3), whereas the remaining SMs need to be bypassed ($S_{CC} = 0$) according to (3.4). In the ideal case, each SM has one turning-on and one turning-off event during each grid period, corresponding to a fundamental switching frequency of 50 Hz per SM if the full modulation range is used.

Table 3.1: Switching states and conduction paths of one CC-SM.

S_{CC}	T_1	T_2	i_{arm}	v_{sm}	Conduction path
1	ON	OFF	positive	v_{cap}	D_1
1	ON	OFF	negative	v_{cap}	T_1
0	OFF	ON	positive	0	T_2
0	OFF	ON	negative	0	D_2

Table 3.2: Switching transients of one CC-SM.

S_{CC}^{k-1}	S_{CC}^{k}	i_{arm}	Turning off	Turning on
0	1	positive	T_2	D_1
0	1	negative	D_2	T_1
1	0	positive	D_1	T_2
1	0	negative	T_1	D_2

$$n_{\text{on}} = \text{round}\left(d \cdot \frac{v_{dc}}{v_{cap}^*} \right) \tag{3.3}$$

$$n_{\text{off}} = N_{CC} - n_{\text{on}} \tag{3.4}$$

The insertion numbers and the upper arm voltage are exemplary shown in Fig. 3.6 for ten SMs in one arm. The number of available voltage levels is $N_{CC} + 1$. In the shown example the lowest and highest voltage level are not applied since the modulation index is limited ($m = 0.8$). The capacitor voltages v_{cap} in the SMs are approximated to be constant.

BC-MMC

One BC is depicted in Fig. 3.5b. For the application of SMs in BC configuration, all switching states and corresponding current paths are summarized in Table 3.3. The number of possible switching states increases to four, since a second switching state for the zero state and an additional switching state ($S_{BC} = -1$) with a terminal voltage of $-v_{cap}$ are available. For distinguishing between both available zero states the switching states $S_{BC} = -0.5$ and $S_{BC} = 0.5$ are defined. All the possible switching transients and the affected semiconductor devices are summarized in Table 3.4.

The sinusoidal waveform of the duty cycle is depicted in Fig. 3.7, divided into four different sectors, depending on the polarity and on its slope. Two generalized switching sequences are introduced in Fig. 3.8 with minimized number of commutations and the use of all three voltage levels of each SM. For the switching sequence 1 the switching states of the SMs will be changed one by one from $S_{BC} = 1$ to $S_{BC} = -0.5$ during sector I until the duty cycle is crossing 0. In sector II the turned-off SMs ($S_{BC} = -0.5$) will turned on stepwise to generate negative terminal voltages ($S_{BC} = -1$). After having reached the minimum negative duty

Table 3.3: Switching states and conduction paths of one BC-SM.

	S_{BC}	T_1	T_2	T_3	T_4	i_{arm}	v_{sm}	Conduction Path
🟦	1	ON	OFF	OFF	ON	positive	v_{cap}	D_1,D_4
🟦	1	ON	OFF	OFF	ON	negative	v_{cap}	T_1,T_4
🟧	0.5	ON	OFF	ON	OFF	positive	0	D_1,T_3
🟧	0.5	ON	OFF	ON	OFF	negative	0	T_1,D_3
🟩	-0.5	OFF	ON	OFF	ON	positive	0	T_2,D_4
🟩	-0.5	OFF	ON	OFF	ON	negative	0	D_2,T_4
🟥	-1	OFF	ON	ON	OFF	positive	$-v_{cap}$	T_2,T_3
🟥	-1	OFF	ON	ON	OFF	negative	$-v_{cap}$	D_2,D_3
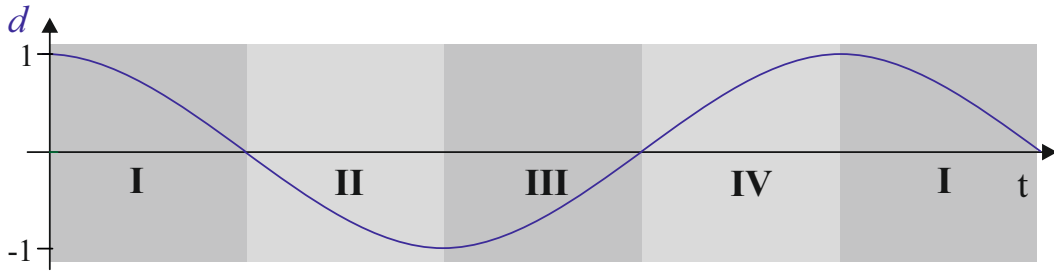
Figure 3.7: Sinusoidal duty cycle divided into four sectors (m=1.0).
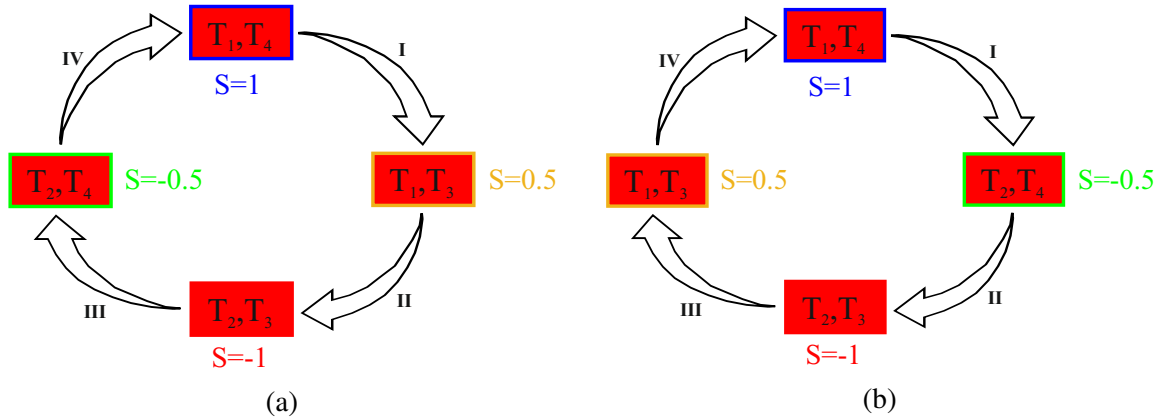
Figure 3.8: NLM switching sequences with minimized number of commutations for the BC-MMC: (a) Sequence 1. (b) Sequence 2.

cycle, the SMs will be turned off again ($S_{BC} = 0.5$) during sector III and finally turned on again to provide positive terminal voltages ($S_{BC} = 1$) during sector IV. For each single added or bypassed SM, only one semiconductor device needs to be changed within the circuit. The number of overall commutations has been minimized. For the switching sequence 2 the switching states for the zero state are used reversely without affecting neither the number of commutations nor the system performance of the MMC.

Based on the presented analysis, the insertion numbers for the SMs need to be determined dependent on the duty cycle. Positive duty cycles need to be generated by the insertion number n_{onP} ($S_{BC} = 1$) according to (3.5). The number of inserted SMs with negative terminal voltage n_{onN} ($S_{BC} = -1$) should be 0 to use the full modulation range. For generating

Table 3.4: Switching transients of one BC-SM.

S_{BC}^{k-1}	S_{BC}^{k}	i_{arm}	Turning off	Turning on
1	0.5	positive	D_4	T_3
1	0.5	negative	T_4	D_3
1	-0.5	positive	D_1	T_2
1	-0.5	negative	T_1	D_2
1	-1	positive	D_1,D_4	T_2,T_3
1	-1	negative	T_1,T_4	D_2,D_3
0.5	1	positive	T_3	D_4
0.5	1	negative	D_3	T_4
0.5	-0.5	positive	D_1,T_3	T_2,D_4
0.5	-0.5	negative	T_1,D_3	D_2,T_4
0.5	-1	positive	D_1	T_2
0.5	-1	negative	T_1	D_2
-0.5	1	positive	T_2	D_1
-0.5	1	negative	D_2	T_1
-0.5	0.5	positive	T_2,D_4	D_1,T_3
-0.5	0.5	negative	D_2,T_4	T_1,D_3
-0.5	-1	positive	D_4	T_3
-0.5	-1	negative	T_4	D_3
-1	1	positive	T_2,T_3	D_1,D_4
-1	1	negative	D_2,D_3	T_1,T_4
-1	0.5	positive	T_2	D_1
-1	0.5	negative	D_2	T_1
-1	-0.5	positive	T_3	D_4
-1	-0.5	negative	D_3	T_4

negative duty cycles, the calculation can be done vice versa according to (3.7)-(3.8) for the maximum modulation range.

If $d > 0$:

$$n_{onP} = \text{round}\left(d \cdot \frac{v_{dc}}{v_{cap}^*} \right) \tag{3.5}$$

$$n_{onN} = 0 \tag{3.6}$$

If $d < 0$:

$$n_{onN} = \text{round}\left(|d| \cdot \frac{v_{dc}}{v_{cap}^*} \right) \tag{3.7}$$

$$n_{onP} = 0 \tag{3.8}$$
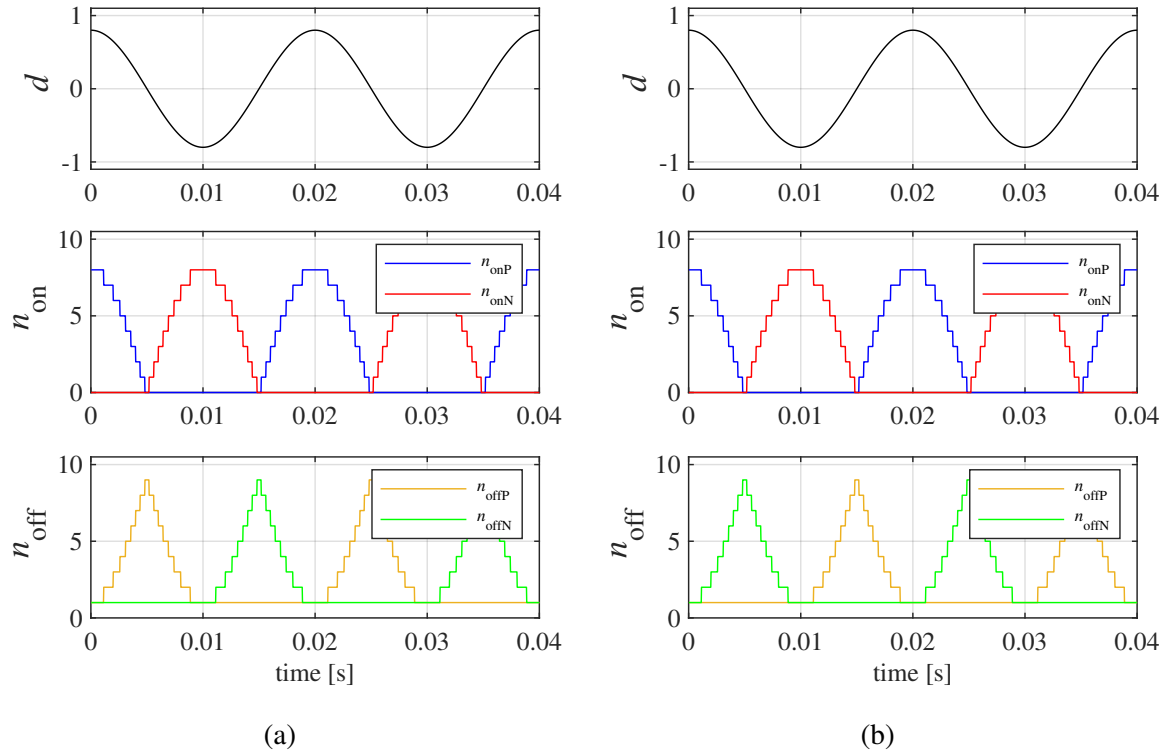
Figure 3.9: NLM switching sequences with minimized number of commutations for the BC-MMC: (a) Sequence 1. (b) Sequence 2.

The insertion numbers are exemplary depicted in Fig. 3.9 for both sequences, where only the switching states of the bypassed SMs are different. The arm voltages are properly generated as shown in Fig. 3.10, being equivalent for both sequences.

3.1.3 Laboratory Setup

For experimental validation the experimental setup of the MMC is depicted in Fig. 3.11, located in Aalborg, Denmark and provided by the Aalborg University. The cabinet in Fig. 3.11a consists of six floors, providing four SM boards in each converter arm. Alternatively, the SMs can be connected in one phase, providing twelve SMs per arm and up to 25 converter voltage levels.

One single SM is shown in Fig. 3.11b where most of the volume is taken from the capacitors and the heatsink for cooling the semiconductor devices. Each SM has its own FPGA control unit for blanking time generation, capacitor voltage measurement processing and protection (overcurrent, overvoltage, overtemperature). The control and modulation of the MMC is realized by a dSPACE system (DS1006 processor). The communication is ensured by optic fiber connection to minimize electromagnetic noises for safe and reliable operation. The main data of the MMC setup are summarized in Table 3.5.
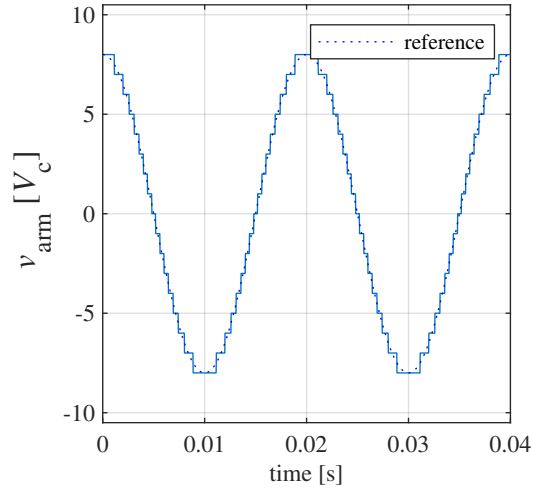
Figure 3.10: Generated arm voltage (upper arm, both sequences).

(a)   (b)
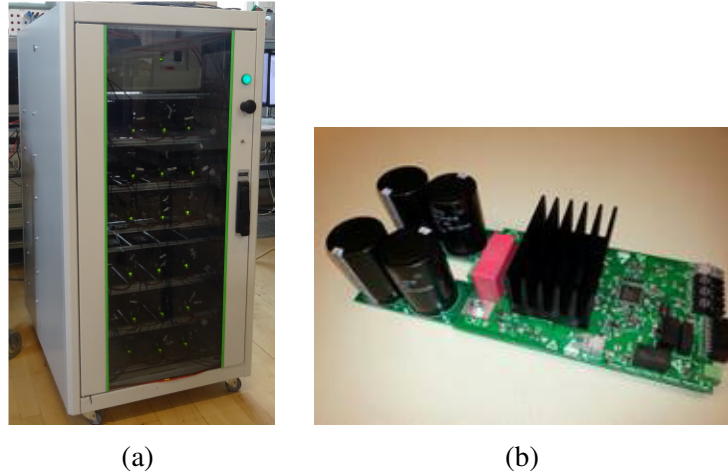
Figure 3.11: MMC prototype: (a) Cabinet with 24 SMs. (b) Board of one SM.

Table 3.5: Specifications and data of the experimental setup.

Description	Parameter	Value	Unit
Number of SMs per arm	N	4	
Arm inductance	L_arm	20	mH
SM capacitance	C_sm	4	mF
Capacitor voltage reference	v_cap^*	25	V

3.1.4 Experimental Validation

For the NLM a high number of SMs is beneficial. Therefore, the experimental MMC setup has been arranged for one phase. In this way the number of SMs per arm has been increased to twelve, corresponding to 13 available voltage levels in each arm. The NLM and a sorting algorithm for CVB have been implemented and applied in C code with SMs in CC configuration. The modulation index has been set to 0.95 for using the full number of available voltage steps.
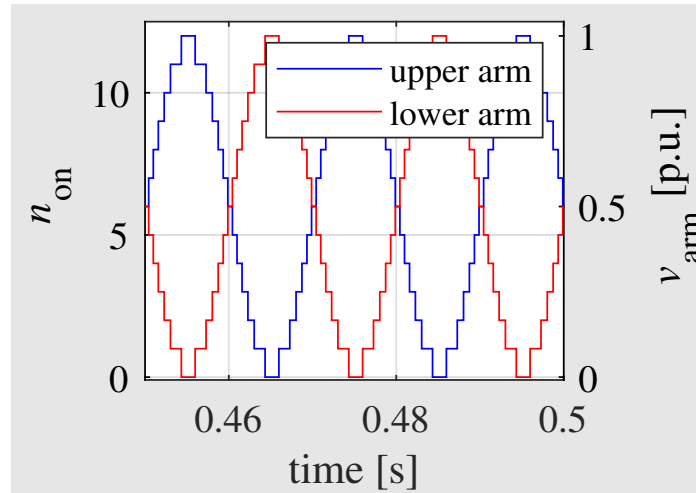
(a)
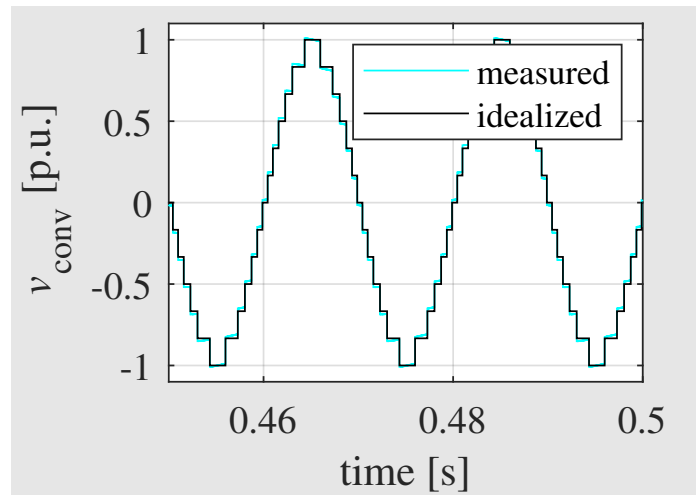
(b)

Figure 3.12: Experimental results for NLM with MMC (12 SMs per arm, one phase, $m = 0.95$): (a) Insertion numbers / arm voltages (p.u.). (b) Converter voltage (idealized: constant capacitor voltages).

The experimental setup is operating in open loop control to investigate the NLM performance. In Fig. 3.12a the insertion numbers and the normalized arm voltages are depicted in each arm. The waveforms are following the sinusoidal reference and all available voltage levels are used in both arms. The waveforms for both arms are shifted to each other by $180°$ as specified. The corresponding converter voltage waveform has been normalized and is shown in Fig. 3.12b based on the real and idealized capacitor voltages. The real capacitor voltages are oscillating up to a certain degree due to charging and discharging processes depending on the arm current direction. Instead, the idealized capacitor voltages are approximated to be constant.

Different to standard PWM techniques the spectrum for NLM is non-characteristic, containing a wide band of harmonics as illustrated in Fig. 3.13. Due to the high modulation index the 50 Hz component has a similar amplitude as the DC offset. The spectrum for the converter voltage is very similar due to the symmetrical behavior of the arm voltages. The DC
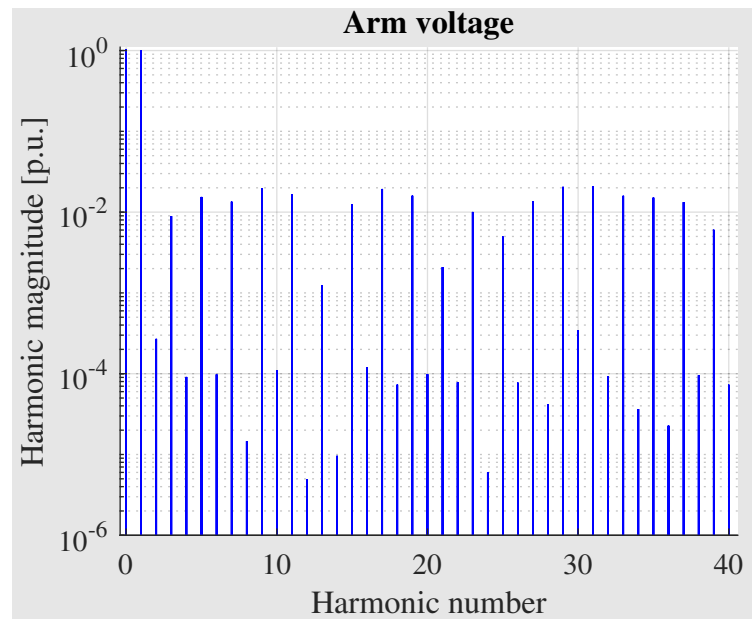
(a)
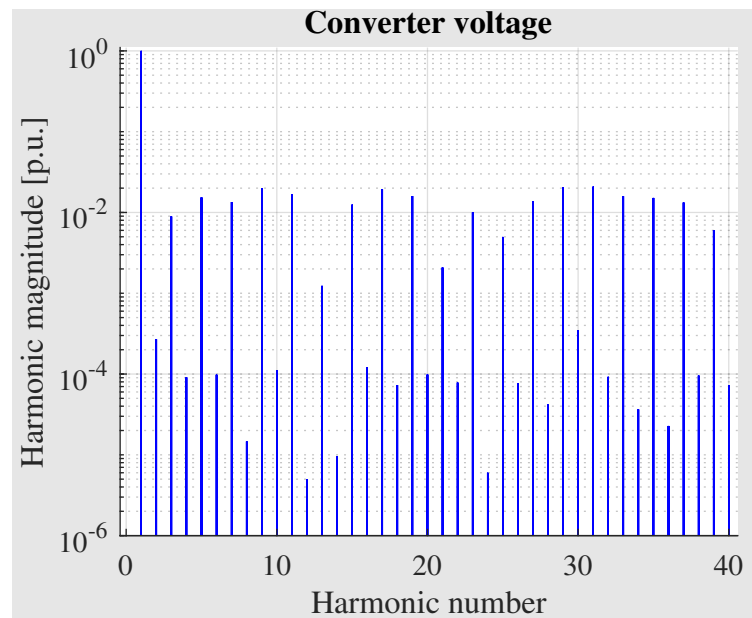
(b)

Figure 3.13: Harmonic spectra from experimental results for NLM applied for the MMC (12 SMs per arm, one phase, $m = 0.95$): (a) Arm voltage (upper arm). (b) Converter voltage.

offset is eliminated in the converter voltage due to the phase shift of $180°$ between the arm voltages. The harmonics can be further deceased by increasing the number of voltage levels [57].
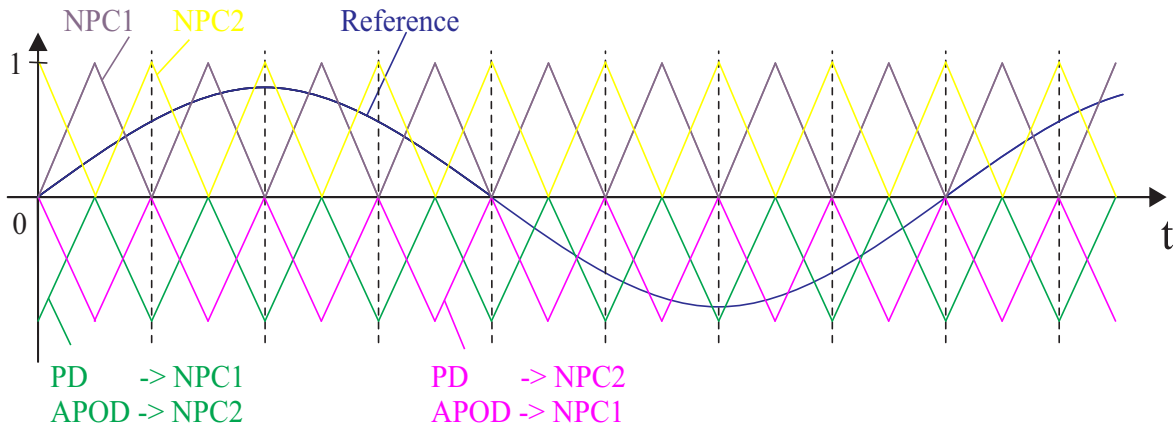
Figure 3.14: Carrier generation for interleaved modulation of two three-level NPC inverters (PD-PWM, APOD-PWM).

3.2 Interleaved Modulation

With the help of multilevel modulation, the increased number of voltage levels can be used for reduced harmonic content in multilevel converter topologies. Apart from the classical multilevel waveform generation the harmonic content can be also improved by interleaved operation in paralleled converters [132], [133]. For instance, for two parallel inverters the carries can be shifted among each other by $180°$ to reduce the current ripple in the superposed line current. This principle can be applied to each standard carrier-based PWM method and for each standard inverter. For n parallel inverters a carrier phase shift of $360°/n$ is obtained for the adjacent inverters.

3.2.1 Parallel NPC Inverters

The interleaved carrier waveforms for two parallel three-level NPC inverters are depicted in Fig. 3.14. The upper and lower carriers are interleaved by $180°$ between both inverters. For each inverter the upper and lower carrier are in phase for the PD-PWM. Instead, for the APOD-PWM the upper and lower carrier are shifted by $180°$ for each inverter. Due to the interleaved carriers between the inverters, also the current ripples are shifted, compensating each other up to a certain degree. At a duty cycle of 0.5 and for a symmetrical system the current ripple is completely eliminated.

3.2.2 Laboratory Setup

For experimental validation two parallel NPC inverters have been realized as depicted in Fig. 3.15. The IGBT modules F3L75R07W2E3_B11 from Infineon is rated for a nominal current of 75 A. Each inverter is equipped with a DC-link capacitance of 2 mF and a converter inductance of 1.8 mH in each phase.
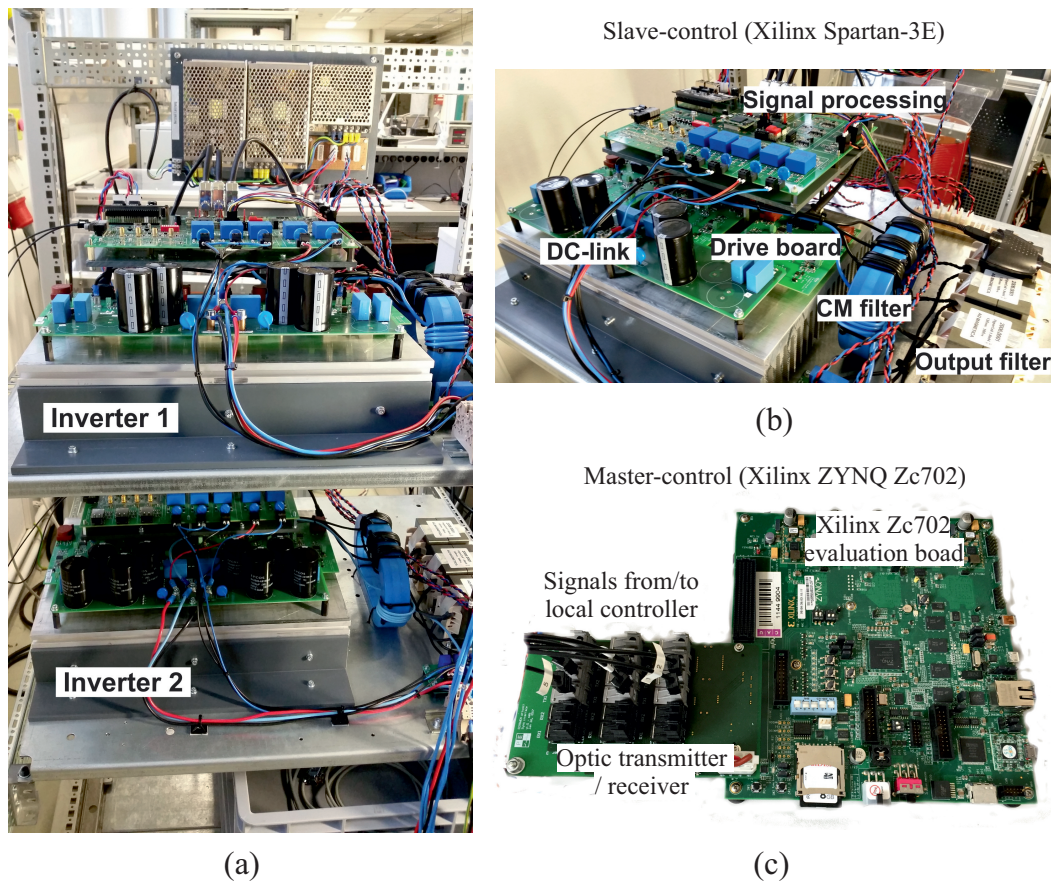
Figure 3.15: Experimental setup: (a) Two parallel NPC inverters. (b) NPC inverter 1. (c) Xilinx control board.

The control of both inverters is implemented on the Xilinx Zc702 evaluation board which includes field programmable gate arrays (FPGAs) and a Dual ARM processor. Each inverter uses a Xilinx Spartan-3 E FPGA control unit for voltage and current measurements, processing as well as monitoring and protection. The communication between the master and slave controllers is ensured by optic fiber to minimize electromagnetic noises for safe and reliable operation.

3.2.3 Experimental Validation

Both modulation techniques are considered for comparison with the laboratory setup. The DC-link is shared and a voltage of $700\,\text{V}$ is applied. They are investigated with a carrier frequency of $10\,\text{kHz}$. The system is operating in open loop control.

The current waveforms for the overall current are recorded in Fig. 3.16 for both the PD-PWM and the APOD-PWM in interleaved mode ($m = 0.85$). The current waveforms are properly generated with a current amplitude of around $10\,\text{A}$. The waveform quality is very similar for both modulation techniques.
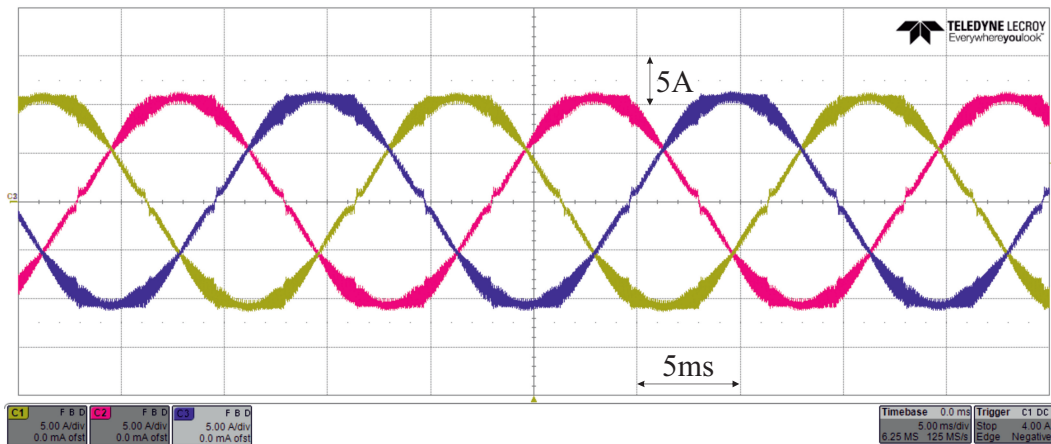
(a)
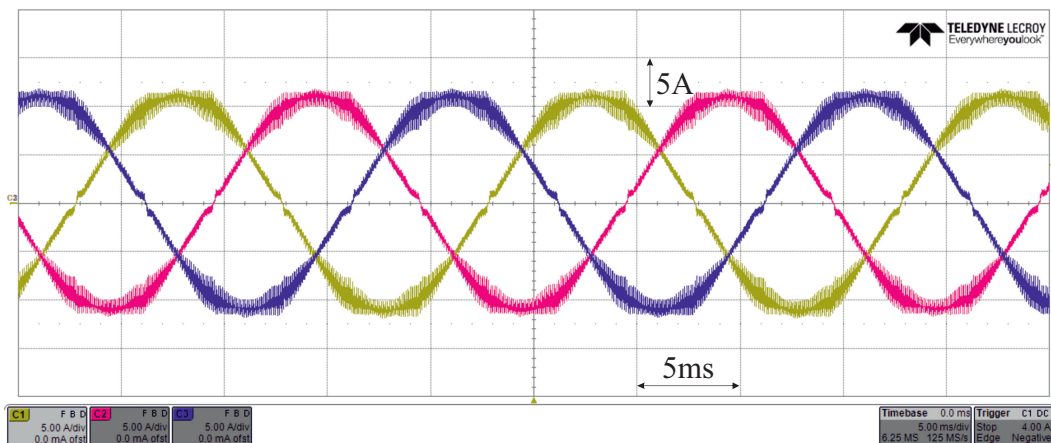
(b)

Figure 3.16: Measurements of the overall current of two parallel NPC inverters for interleaved operation ($m = 0.85$): (a) PD-PWM. (b) APOD-PWM.

The current spectra for both modulation techniques are compared in Fig. 3.17. The 200th harmonic is associated to the applied carrier frequency of 10 kHz. The APOD-PWM shows slightly higher sideband harmonics. Nevertheless, the THD$_i$ values are very similar with values of 5.96 % (PD-PWM) and 6.8 % (APOD-PWM).

Apart from the grid current quality the evaluation of the circulating current is from high importance since it is increasing the rating and losses of the devices. As described in Section 2.5 the circulating currents are mainly driven by common-mode voltages between the inverters due to differing applied switching states. The circulating currents have been recorded in Fig. 3.18 for both PD-PWM and APOD-PWM. The circulating current is significantly reduced by the application of APOD-PWM. Consequently, APOD-PWM provides the possibility to reduce the size of converter filters or the rating of the devices compared to the well-established PD-PWM.
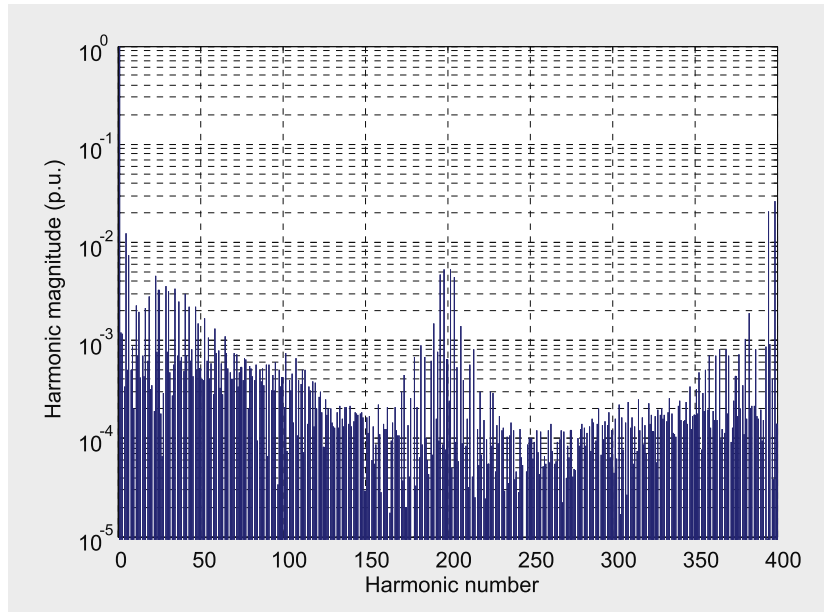
(a)
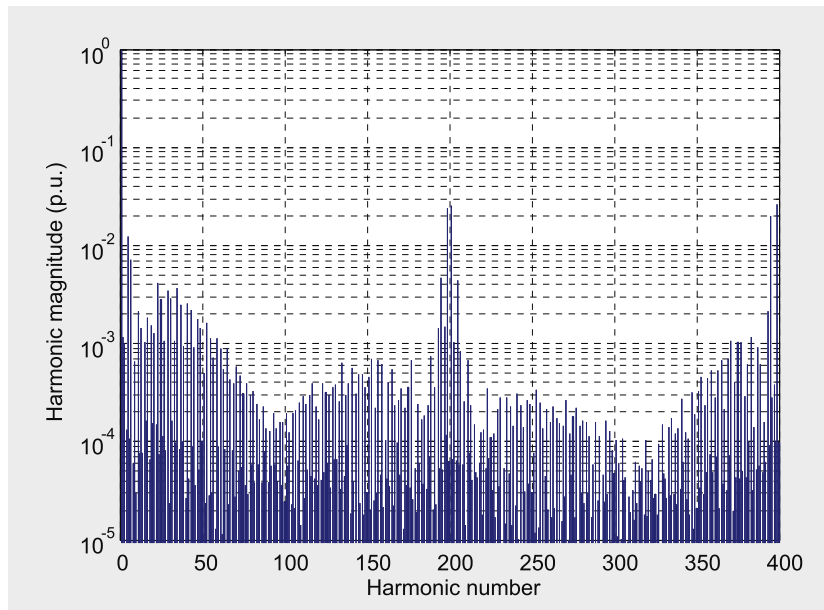
(b)

Figure 3.17: Amplitude spectrum of the measured overall current (phase a): (a) PD-PWM. (b) APOD-PWM.

Also for the application of parallel NPC inverters the PD-PWM shows a slightly reduced harmonic content compared to the APOD-PWM. However, the common-mode voltage and therefore the circulating current between the inverters have been strongly reduced by the APOD-PWM.

The PD-PWM shows a slightly reduced harmonic content than the APOD-PWM. The circulating currents between parallel NPC inverters have been significantly reduced by the APOD-PWM compared to the well-established PD-PWM. Consequently, the APOD-PWM can be seen as the preferred choice for parallel NPC inverters with common DC-link. Instead, if the

(a)

(b)
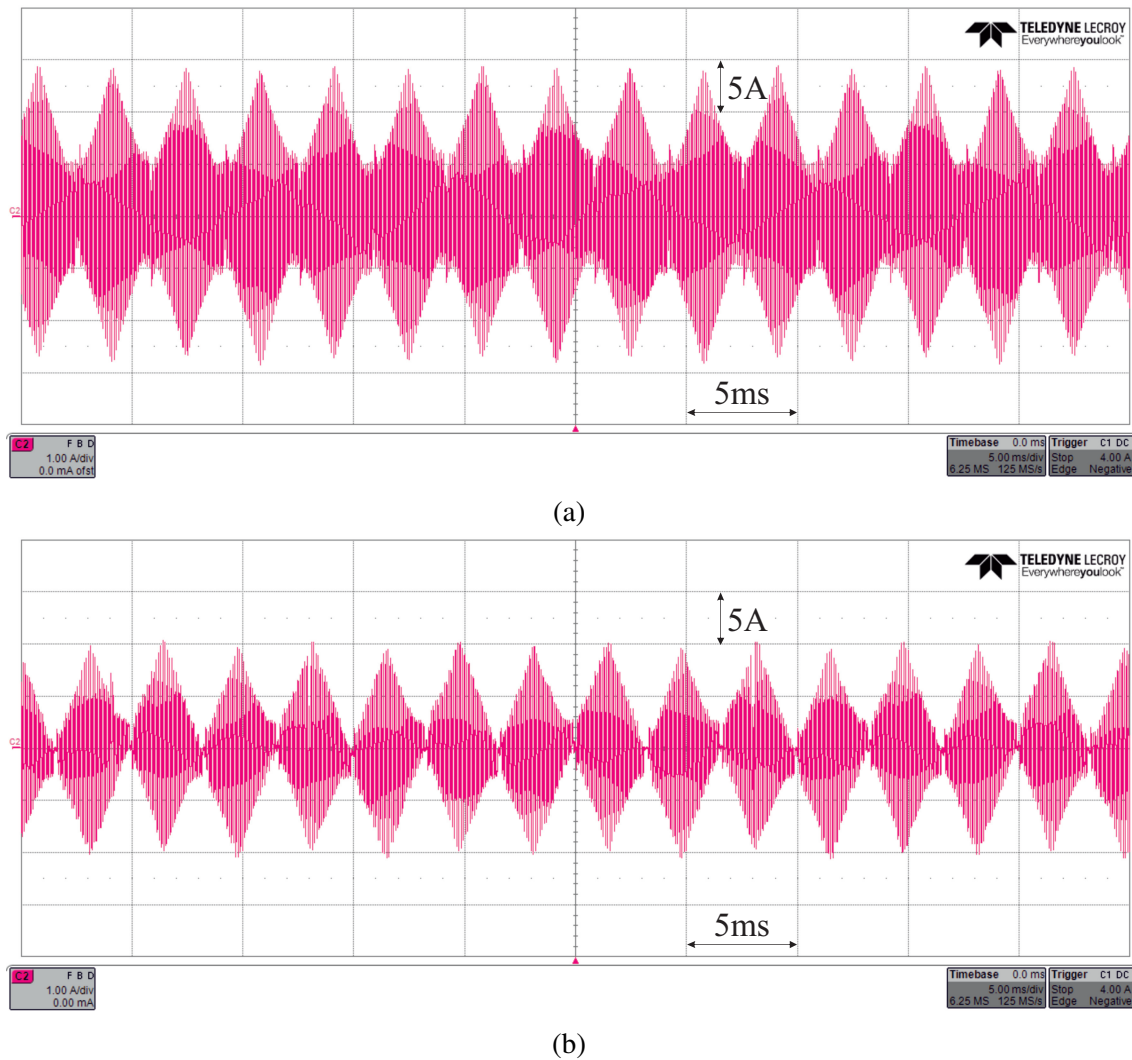
Figure 3.18: Recorded circulating current between both parallel NPC inverters ($m = 0.98$): (a) PD-PWM. (b) APOD-PWM.

DC-links are separated the PD-PWM can be applied due to minimized harmonic content on the AC side.

3.2.4 Modular Multilevel Converter

From modulation point of view also the MMC can be considered as two parallel inverters since the grid current is shared by the upper and lower arm. Therefore, also interleaved operation can be beneficial for harmonic cancellation. Depending on the number of SMs and the phase shift between the carriers improved waveform generation can be achieved on the DC or AC side by using the full number of available voltage levels ($2N + 1$) [57]. By the use of different sampling frequencies in the upper and lower arm similar effects can be also achieved for NLM [57].

3.3 Summary and Conclusions of the Section

In this chapter classical multilevel modulation techniques have been presented and evaluated for the three-level NPC inverter and for the MMC to benefit from their multilevel waveform generation. For the NPC inverter the PD-PWM has been identified as the preferred choice for reduced harmonic content. The interleaved operation of the NPC inverters has been applied for harmonic cancellation. However, if the DC link is shared, circulating currents emerge between the paralleled inverters. These circulating currents have been significantly reduced by the application of the APOD-PWM at a comparable harmonic distortion in the AC current (THD of 6.8 % instead of 5.96 %). Accordingly, the APOD-PWM has been presented as the preferred solution for the interleaved operation of parallel NPC inverters with a shared DC link. All these findings have been validated by experimental results.

For the MMC the NLM has been identified as the preferred choice to achieve high-efficient operation, being very crucial especially in high-power applications. Both the CCs and the BCs are investigated as SM topologies, highlighting all possible switching states and switching transients. Based on this analysis the switching patterns of the NLM are presented for both SM topologies. For the BC-MMC two possible switching sequences with minimum number of commutations have been introduced by taking profit from the redundant zero voltage switching states inside the BC-SMs. The practicability and the performance of the NLM have been experimentally validated by a one-phase MMC prototype with twelve SMs in each arm. The staircase waveforms have been properly generated, following the sinusoidal reference waveform very well due to the high number of available voltage levels.

4 Neutral-Point Clamped Inverter Optimization for High-Power Applications

Parallel LV NPC inverters are considered for the connection to the MV grid by step-up transformers. A wind power application and a MV grid impedance analyzer are investigated as study cases. The voltage adaption by the transformers is directly linked to the turns ratio T_R according to (4.1). The transformer impedance and inductance can be calculated according to (4.2) and (4.3).

$$\hat{v}_{g,\lambda}^{LV} = T_R \cdot \hat{v}_{g,\lambda}^{MV} \tag{4.1}$$

$$Z_{sc,trafo} = u_{sc} \cdot \frac{(V_{g,\Delta}^{LV})^2}{S_{g,n}} \tag{4.2}$$

$$L_{sc,trafo} = \frac{Z_{sc,trafo}}{2\pi f_g} \quad (R_{sc,trafo} \approx 0) \tag{4.3}$$

The parallel NPC inverters are taken into account for the connection to the transformer stage. As power units IGBT modules with 1200 V breakdown voltage are applied. The maximum DC-link voltage is set to 1500 V, corresponding to 62.5 % of the IGBT blocking capability. It provides sufficient reserve for possible voltage overshoots, e.g. due to parasitic inductances, and allows to operate at the upper limit of the LV range. Third harmonic injection provides sinusoidal voltage amplitudes of up to 862.5 V.

$$\hat{v}_{phase,\lambda}^{3rd} = \frac{2}{\sqrt{3}}\hat{v}_{phase,\lambda} = \frac{2}{\sqrt{3}} \cdot \frac{V_{dc}}{2} = 862.5\,\text{V} \tag{4.4}$$

4.1 Wind Power Application

A wind park (onshore) with a rated power of 30 MW is considered as the first study case. Seven wind generator units rated for 4.286 MW each are taken into account. Each generator is equipped with a back-to-back conversion system and with one step-up transformer. The use of back-to-back conversion system enables high power capabilities and flexible power control. The focus of this section lies on the grid-side connected inverter stage.

4.1.1 System Design

Each wind turbine generator system can be connected by an own transformer, linked to a power of 4.286 MVA and an overall LV current of 3586 A. This current is too high for conventional IGBT modules. Therefore, the parallel connection of NPC inverters is required

to fulfill the defined power ratings. By parallel connection at the AC side the overall current can be splitted among the NPC inverters. Instead, on the DC side it is advantageous to separate the DC-links from each other to avoid circulating paths between the inverters. For this purpose, each back-to-back inverter can use its own DC-link in a symmetrical inverter system.

For wind power plants LV connections of 400 V and 690 V are very common. The three-level NPC inverters gives the possibility for connection to the latter one even with 1200 V IGBT modules, limiting the system current rating and the number of paralleled inverter units. Six parallel NPC inverters are considered to handle the total LV current of 3586 A by reducing the inverter current rating to a reasonable value of 597.7 A each. The grid voltage can vary up to 10 %, corresponding to a maximum LV voltage amplitude of 619.7 V.

$$\hat{v}_{g,\lambda}^{\mathrm{LV}} = 1.1 T_{\mathrm{R}} \sqrt{2} \cdot \frac{V_{g,\Delta}^{\mathrm{MV}}}{\sqrt{3}} = 619.7\,\mathrm{V} \tag{4.5}$$

The capacitor voltage oscillations will be limited to $\pm 5\,\%$, corresponding to a minimum available phase voltage of 782.3 V.

$$\hat{v}_{\mathrm{phase},\lambda,\mathrm{min}}^{\mathrm{3rd}} = \frac{\hat{v}_{\mathrm{phase},\lambda,\mathrm{max}}^{\mathrm{3rd}}}{1.05^2} = 782.3\,\mathrm{V} \tag{4.6}$$

The voltage drop at the transformer can be simply calculated by (4.7) for a monofrequent current and for a frequency stable short-circuit impedance. The short-circuit voltage ratio is defined with 6 % in accordance with the local grid requirements [134], corresponding to a voltage drop across the transformer of 33.8 V at nominal current.

$$\hat{v}_{\mathrm{L,trafo},\lambda} = \sqrt{2} \cdot u_{\mathrm{sc,trafo}} \cdot \frac{V_{g,\Delta}^{\mathrm{LV}}}{\sqrt{3}} \cdot \frac{f_{\mathrm{m}}}{f_{\mathrm{g}}} = 33.8\,\mathrm{V} \tag{4.7}$$

The filters are designed very small with $46.5\,\mu\mathrm{H}$ in the line and $100\,\mu\mathrm{H}$ for each single inverter to limit space, costs and voltage drops. At nominal current, this corresponds to overall voltage drops of 74.1 V and 26.6 V across the filters. Voltage drops across cables can be neglected.

For pure active power injection ($\cos\varphi = 1$) the required voltage can be calculated, assuming an ideal inductive behavior of transformers, filters, cables and the grid. Based on these simplifications a sufficient voltage reserve of 147.8 V (18.9 %) is obtained according to (4.8).

$$\hat{v}_{\mathrm{req},\lambda} = \sqrt{\left(\hat{v}_{g,\lambda}^{\mathrm{LV}}\right)^2 + (\hat{v}_{\mathrm{L,trafo},\lambda} + \hat{v}_{\mathrm{L,line},\lambda} + \hat{v}_{\mathrm{L,conv},\lambda})^2} = 634.2\,\mathrm{V} \tag{4.8}$$

Table 4.1: NPC parameters for wind power plant.

Description	Parameter	Value	Unit
Nominal power	$S_{g,nom}$	30	MW
Number of wind power units		7	
Nominal power per wind power unit		4.29	MW
Connected inverters per wind power unit		6	
Nominal power injection per inverter		714	kW
Line filter inductance	L_{line}	46.5	μH
Converter filter inductance	L_{conv}	100	μH
IGBT breakdown voltage		1200	V
Nominal current (50 Hz, rms)		597.7	A
PWM carrier frequency	f_c	1600	Hz
Capacitor voltage reference	v_{cap}^*	1428.6 ($\pm$5%)	V
Capacitor voltage limitation	$V_{c,lim}$	1500	V
Grid voltage (rms)	$V_{g,\Delta}^{MV}$	20	kV
Transformer input voltage (rms)	$V_{g,\Delta}^{LV}$	690	V
Transformer inductance ($u_{sc} = 6\%$)	$L_{sc,trafo}$	21.22	μH
Grid inductance	L_g	0.19	μH

The obtained parameters for the NPC-based solution are summarized in Table 4.1. The system includes seven equivalent wind power units, where each one is connected by back-to-back inverters and one transformer to the MV grid. The behavior of one transformer unit will be considered exemplary, fed by six parallel NPC inverters to achieve sufficient current capability. The DC-link capacitor banks of the inverters are isolated from each other to avoid circulating currents. Small filters are integrated in each NPC inverter and at the common transformer.

4.1.2 System Performance

The PD-PWM shows the best harmonic performance for the AC current generation. By interleaved operation harmonic cancellation becomes possible for reduced harmonic content and minimized switching frequencies. The PD-PWM is applied with interleaved carriers and a carrier frequency of 1.6 kHz.

In Fig. 4.1 the nominal wind power of 4.286 MW is transferred to the grid by the parallel NPC inverters at a unity power factor ($\cos\varphi = 1$). The required transformer input current of 3586 A (rms) is properly generated and injected at a transformer voltage of 690 V. Although, the filter effort as well as the switching frequencies are limited to low values, the current and voltage waveforms are excellent and voltage transients are limited in interleaved operation.
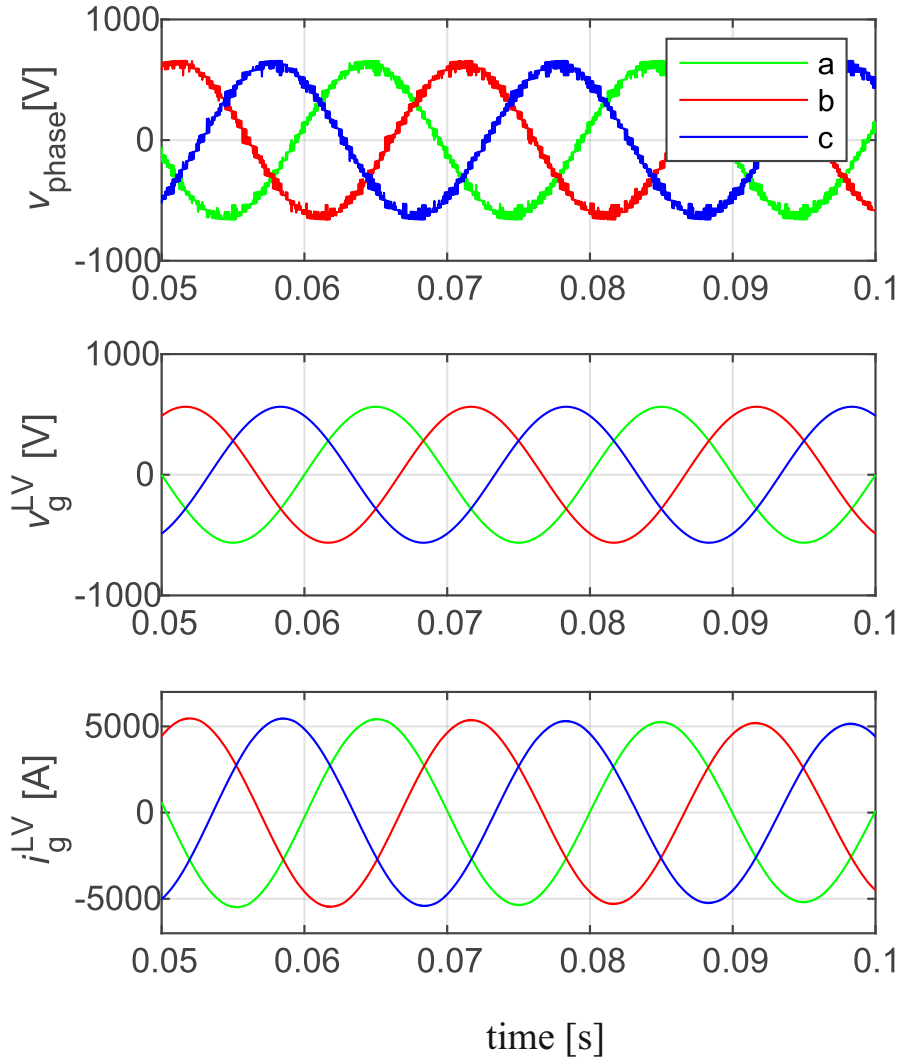
Figure 4.1: Parallel NPC inverters: phase voltages, transformer input voltages, transformer input currents ($P_g = 4.286\,\text{MW}$, $\cos\varphi = 1$).

The three-phase currents of each single NPC inverter are depicted in Fig. 4.2. The currents are properly controlled to an rms value of 598 A.

For deeper analysis the inverter currents are illustrated for one phase together with the superposed current at the transformer (divided by six for the same scale) in Fig. 4.3. Current ripples of up to almost 400 A occur in each inverter. However, these ripples are widely eliminated at the transformer due to harmonic cancellation. The excellent waveform quality from the interleaved NPC inverters is equivalent at each of the six transformer units. At MV level even a further reduction of harmonics would be possible by also interleaving the seven transformer units with its inverter systems among each other.
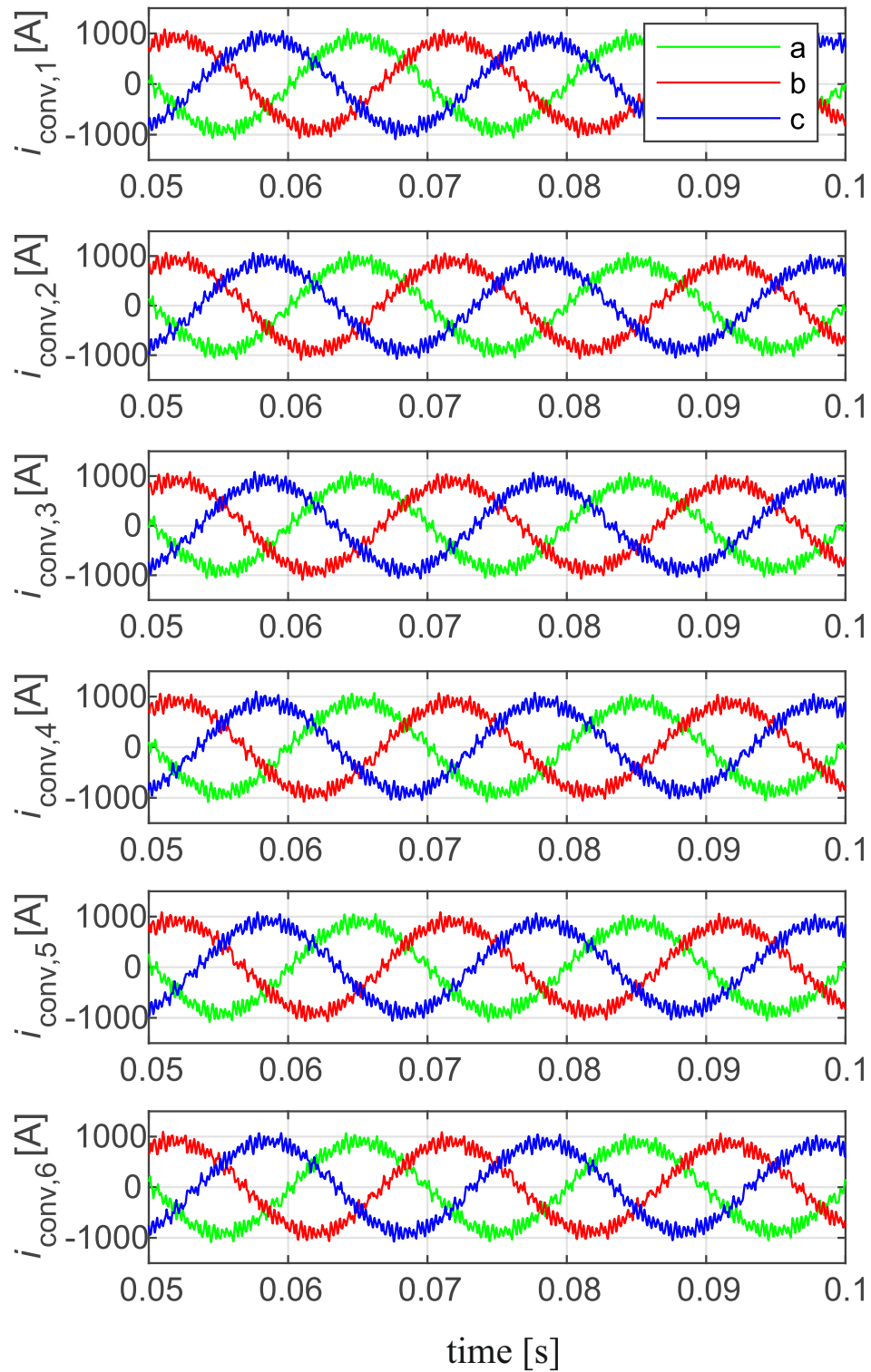
Figure 4.2: NPC inverter currents ($P_g = 30\,\mathrm{MW}$, $\cos\varphi = 1$).
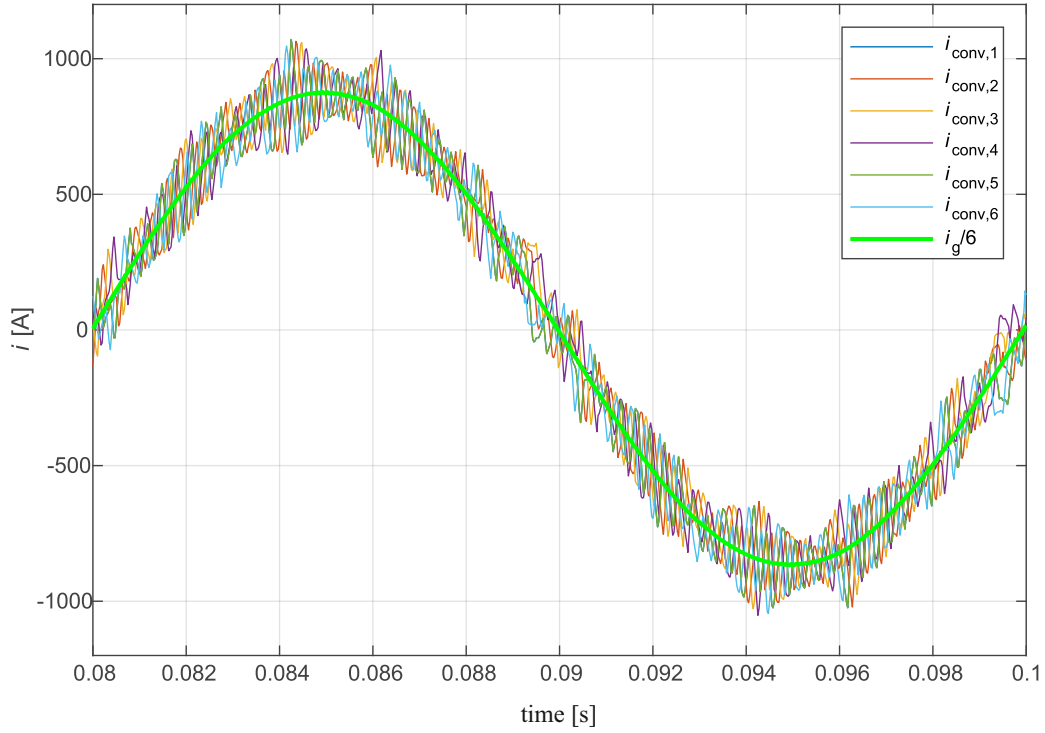
Figure 4.3: Interleaved NPC inverter currents and resulting transformer input current (phase a): $P_g = 30\,\text{MW}$, $\cos\varphi = 1$.

Table 4.2: Basic data for 20 kV MV grid for the connection of decentralized energy systems

	$V_{g,\Delta}^{\text{MV}}$ [kV]	$S_{g,\text{sc}}$ [MVA]	Ψ_g [°]
Range	$20\ldots22$	$30\ldots500$	$50\ldots85$

4.2 Medium Voltage Grid Analyzer

The MV grid impedance analyzer serves as the second study case. It needs to be able to inject monofrequent currents within a wide frequency range from 100 Hz up to 10 kHz.

4.2.1 Converter Design

Compared to LV grids MV grids are very stiff, requiring high powers for proper excitation. The basic grid characteristics for Germany, Russia and Brazil are summarized in Table 4.2, linked to short-circuit powers up to 500 MVA. Accordingly, the minimum possible grid impedance is calculated with (4.9). For simplification an ohmic-inductive behavior is assumed up to $f = 100\,\text{Hz}$. Accordingly, the grid impedance angle $\Psi_{\text{min}} = 50°$ corresponds to the highest resistive part in (4.10) and thus to the lowest inductive part in (4.11), corresponding to the minimum grid impedance at 100 Hz in (4.12).

$$Z_{g,sc,min}^{MV,50\,Hz} = \frac{\left(V_{g,\Delta}^{MV}\right)^2}{S_{sc,max}} = \frac{(20\,kV)^2}{500\,MVA} = 0.8\,\Omega \tag{4.9}$$

$$R_{g,sc}^{MV} = Z_{g,sc,min}^{MV,50\,Hz} \cdot \cos\left(\Psi_{g,min}\right) = 0.514\,\Omega \tag{4.10}$$

$$L_{g,sc}^{MV} = \frac{Z_{g,sc,min}^{MV,50\,Hz} \cdot \sin\left(\Psi_{g,min}\right)}{2\pi f_g} = 1.95\,mH \tag{4.11}$$

$$Z_{g,sc,min}^{MV,100\,Hz} = \sqrt{(R_{g,sc}^{MV})^2 + (2\pi f_m \cdot L_{g,sc}^{MV})^2} = 1.33\,\Omega \tag{4.12}$$

This minimum impedance requires the highest current injection to achieve a voltage excitation of 1 %. The final specifications are adapted to 0.55 % grid excitation, corresponding to 1 % grid excitation for short-circuit powers up to minimum 275 MVA. In this way, the required power injection is almost halved, by covering most of the MV grid connection points. An excitation of 0.55 % in the worst case is still acceptable and reasonable to limit the costs. According to (4.13), the MV grid analyzer needs to be designed for a current injection of 47.78 A, corresponding to an injected power of $S_g^{55\%} = 1.655\,MVA$.

$$I_{g,exc}^{MV,100\,Hz} = \frac{V_{g,exc,\lambda}}{Z_{g,sc,min}^{MV,100\,Hz}} = 0.55 \cdot \frac{0.01\frac{V_{g,\Delta}^{MV}}{\sqrt{3}}}{Z_{g,sc,min}^{MV,100\,Hz}} = 47.48\,A \tag{4.13}$$

Due to inductive behaviors of the grid, an increase of the grid impedance is assumed at higher frequencies. Since the frequency behavior of MV grids has not been investigated deeply and due to possible unknown resonances, the system will be designed for the rated current up to frequencies of 1000 Hz to ensure full flexibility. For frequencies above, the current rating is decreasing according to Fig. 2.7b. At the maximum current frequency of 10 kHz still 10 % of the rated current are demanded. The demand of high powers in a high frequency range is linked to different goal conflicts especially because the device switching frequencies are usually limited if high powers need to be handled.

However, high switching frequencies of up to 30 kHz are required to properly generate current frequencies up to 10 kHz by maintaining a very small filter design. Switching frequencies of $f_{sw} = 15\,kHz$ are applied at nominal current to limit occurring current ripples. The DC-link voltages at nominal current with frequencies of 1000 Hz can be assumed as constant since only very small energies are oscillating. Nevertheless, this operation point is most crucial for the voltage design since high voltage drops occur across the applied inductances (transformer, filter, cabling). Also the dead time generation needs to be taken into account at those frequencies, corresponding to a maximum voltage decrease of around 5 % as expressed in (4.14).

$$\hat{v}_{\text{phase},\lambda}^{\text{3rd,dead\_time}} = 0.95 \hat{v}_{\text{phase},\lambda}^{\text{3rd}} \tag{4.14}$$

Taking into account grid voltage variations of 1 % due to the current injection and additional possible 1 % during normal grid operation, the LV-side transformer input voltage can be defined by (4.15).

$$\hat{v}_{\text{g},\lambda}^{\text{LV}} = 1.02 \cdot \sqrt{2} \cdot \frac{V_{\text{g},\Delta}^{\text{LV}}}{\sqrt{3}} \tag{4.15}$$

Since the LV range is already limited, additional voltage drops in the system should be minimized, being particularly relevant at higher current frequencies. Therefore, the transformer has been designed with a low short-circuit voltage of 2.5 %. The turns ratio of the transformer can be adapted depending on the available inverter voltage and the voltage drops across the passive components. For this purpose, the voltage drops across the filter and the cable impedances need to be taken into account as well.

For proper high-frequent current generation the dead time for the IGBTs need to be minimized. However, this results in fast voltage transients, causing high stress for the transformer windings. A du/dt filter will be applied to limit the current ripples and to reduce the voltage slope by a factor above 8, corresponding to $L_{\text{filter}} = \frac{6.36\,\mu\text{H}}{1000\,\text{A}} \cdot I_{\text{LV}}$ depending on the nominal current [135]. For the cabling the overall LV side related inductance is approximated by $L_{\text{cable}} = 0.7\,\mu\text{H}$. All these inductances need to be taken into account for a proper voltage design. Furthermore, a voltage reserve for proper control and modulation is taken into account according to (4.16), verified by simulation studies.

$$\hat{v}_{\text{mod},\lambda} = (L_{\text{g}} + L_{\text{sc,trafo}} + L_{\text{filter}} + L_{\text{cable}}) \cdot \frac{0.15 \cdot \sqrt{2} I_{\text{g,nom}}^{\text{LV}}}{\frac{1}{f_{\text{c}}}} \tag{4.16}$$

Fig. 4.4 has been created for a proper voltage design. It shows the available phase voltage amplitudes for the three-level NPC as well as for the classical two-level inverter. The voltage drops in the system are illustrated for a current frequency of 1000 Hz and depending on the LV-side input voltage of the transformer. The three-level NPC inverter allows a transformer input voltage of 510 V, being more than 2.5 times higher compared to the classical two-level inverter. In this way, the LV current can be limited to 1874 A, corresponding to a converter rating of 2986 kVA.
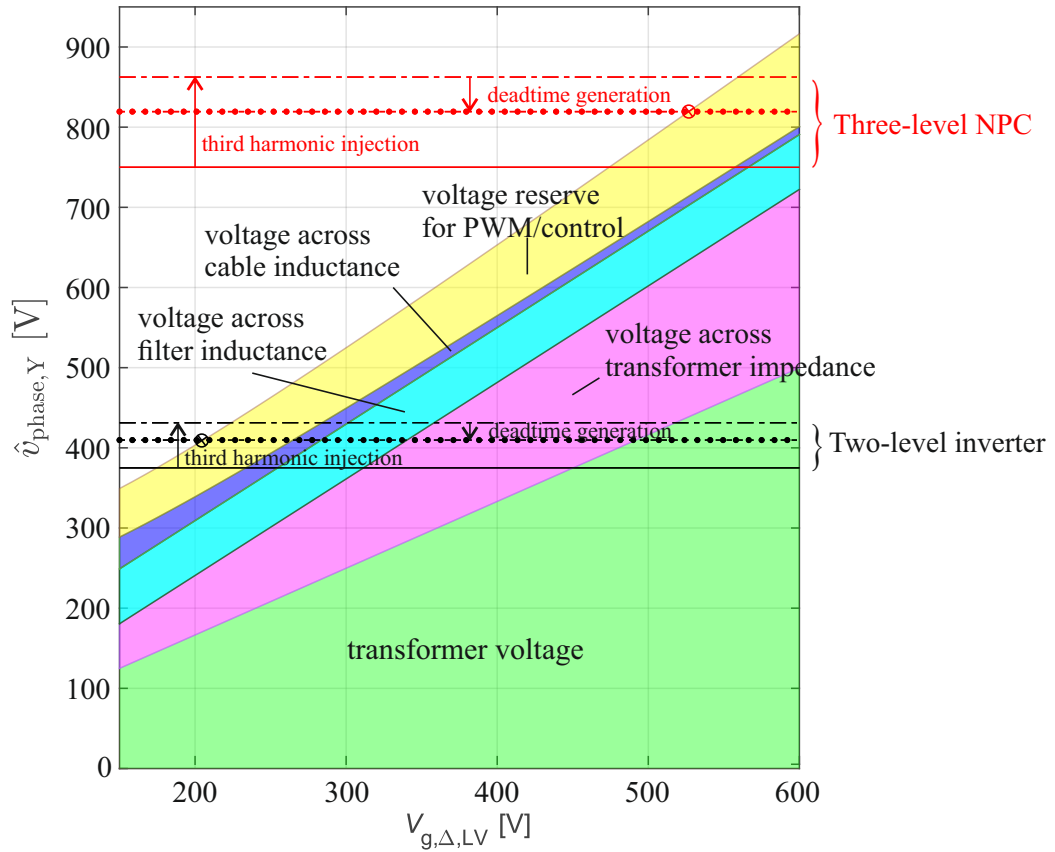
Figure 4.4: Voltage design for the MV grid analyzer based on the available phase voltage amplitude of the inverter solutions $\hat{v}_{\text{phase},\lambda}$ and the voltage drops depending on the transformer input rms voltage $V_{\text{g},\Delta,\text{LV}}$ at nominal power at a current frequency of 1000 Hz.

The MV grid analyzer can be realized by six parallel NPC inverters and two parallel transformers, specially designed for a wide current frequency range. The full system has been realized within two mobile containers as illustrated in Fig. 4.5. The NPC inverters, both transformers, the measuring technique and the MV switch gear are housed in these containers. The cabinet of one NPC inverter and of one MV transformer are depicted as well.

Position	Room for
A	MV switch gear
B	LV transformer (supply)
C	MV transformers
D	NPC inverters
E	Measuring equipment
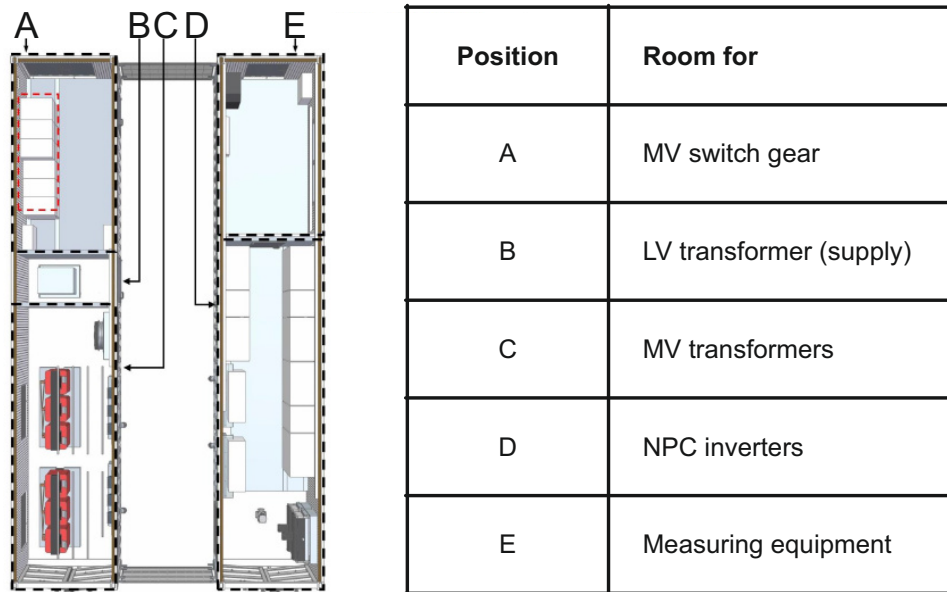
(a)
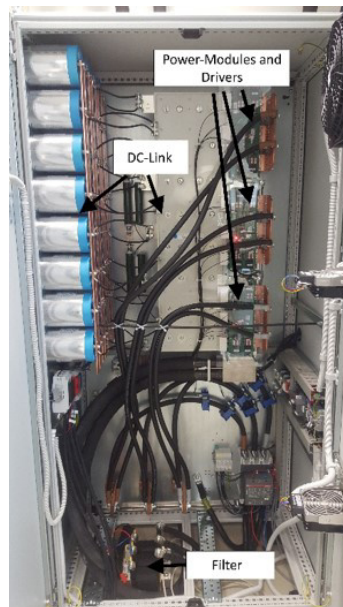
(b)

(c)

Figure 4.5: Final realization: (a) Containers (length: 12.2 m). (b) Cabinet of one NPC inverter. (c) MV transformer.

4.2.2 System Performance

In Fig. 4.6-4.8 the behavior of the six parallel NPC inverters is shown at nominal current injections at up to 10 kHz. The current waveforms are properly generated by interleaved modulation although the filter effort and the switching frequencies have been minimized.

(a)

(b)
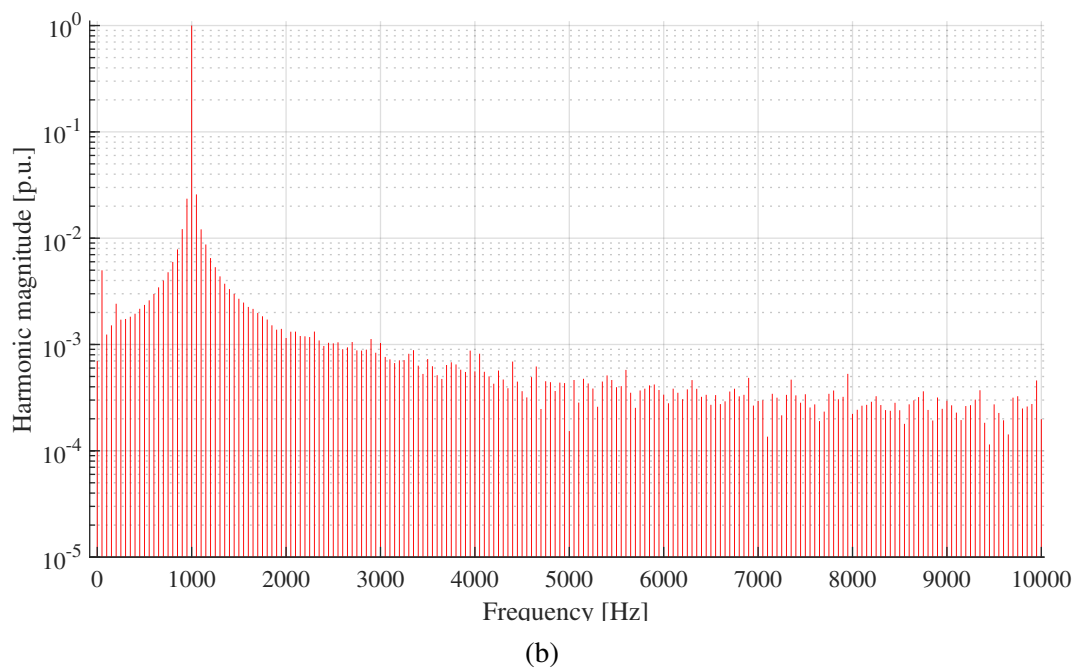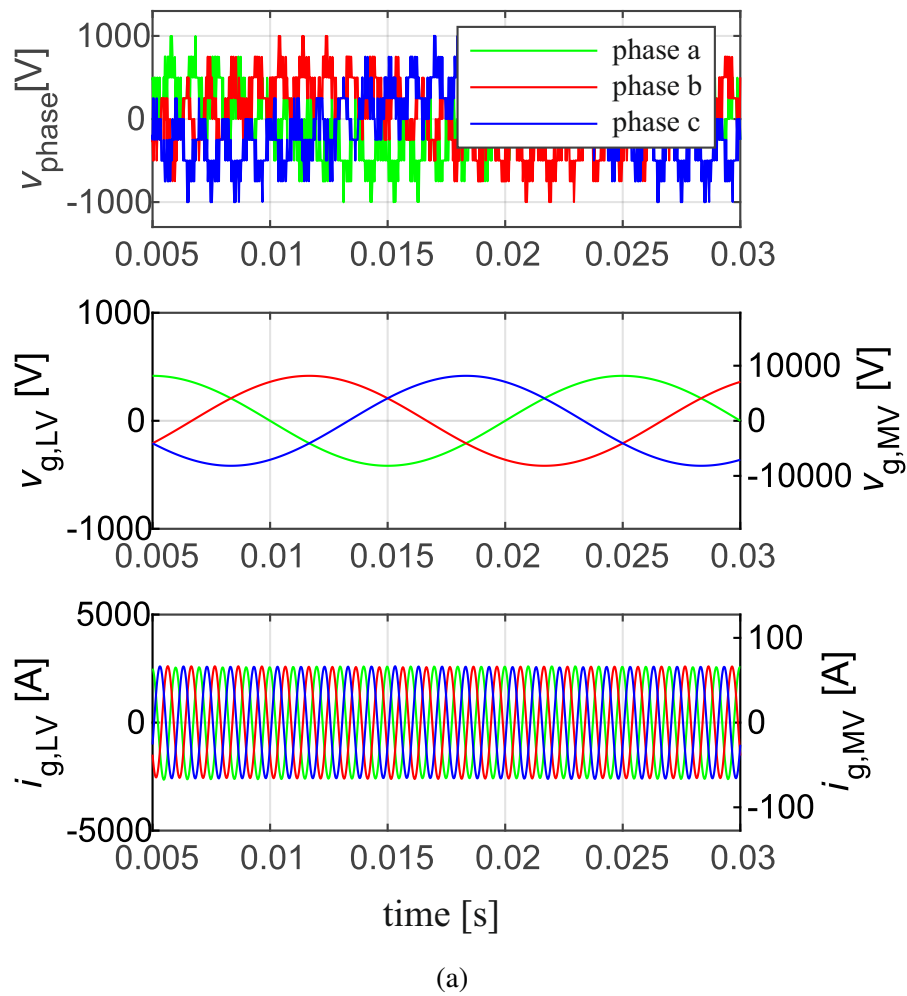
Figure 4.6: Current injection at $1000\,\mathrm{Hz}$ ($\hat{i}_{\mathrm{g}}^{1000\,\mathrm{Hz}} = 2070.9\,\mathrm{A}$): (a) Phase voltages, grid voltages (LV-side) and grid currents (PD-PWM, $f_{\mathrm{c}} = 15\,\mathrm{kHz}$). (b) Normalized grid current spectrum (LV-side).
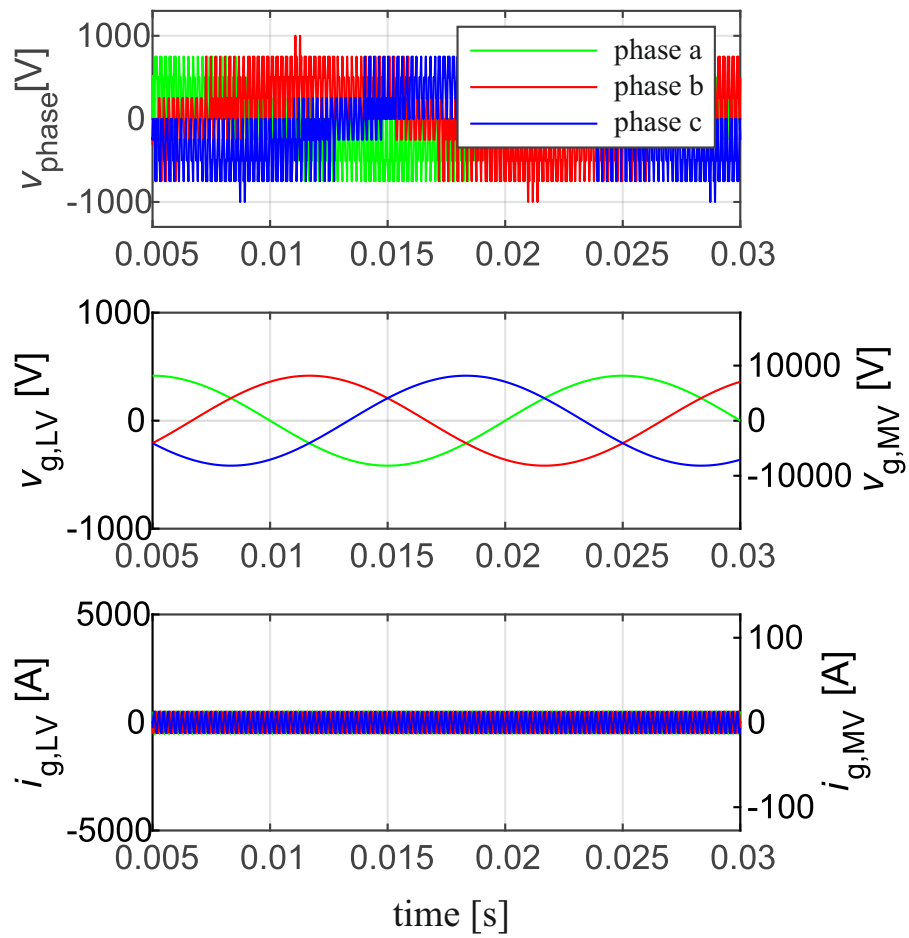
(a)
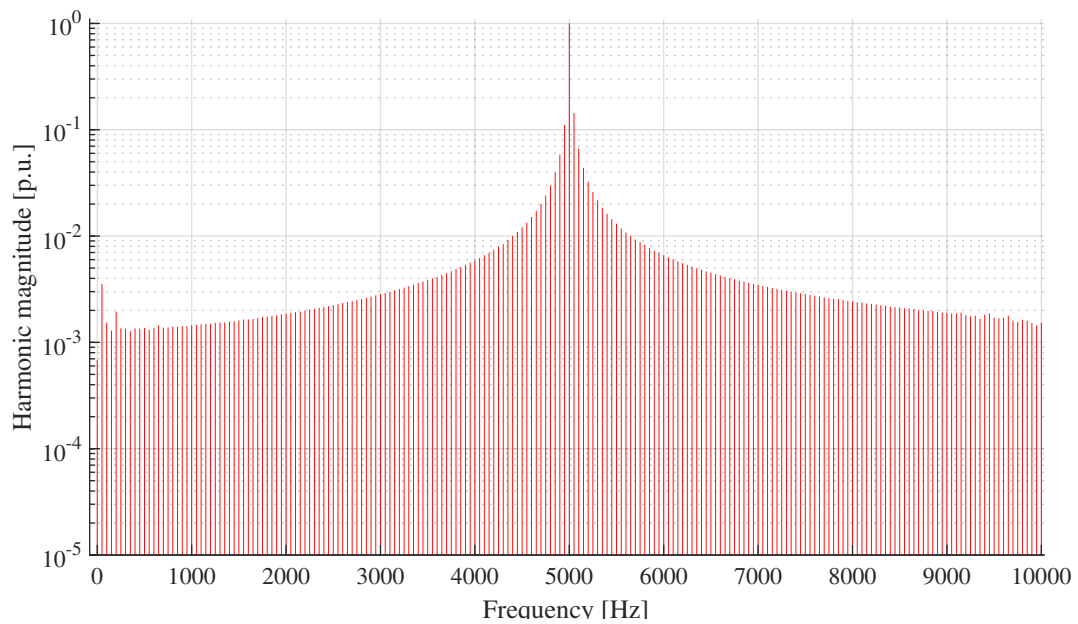
(b)

Figure 4.7: Current injection at 5000 Hz ($\hat{i}_g^{5000\,\text{Hz}} = 464.8\,\text{A}$): (a) Phase voltages, grid voltages (LV-side) and grid currents (PD-PWM, $f_c = 30\,\text{kHz}$). (b) Normalized grid current spectrum (LV-side).
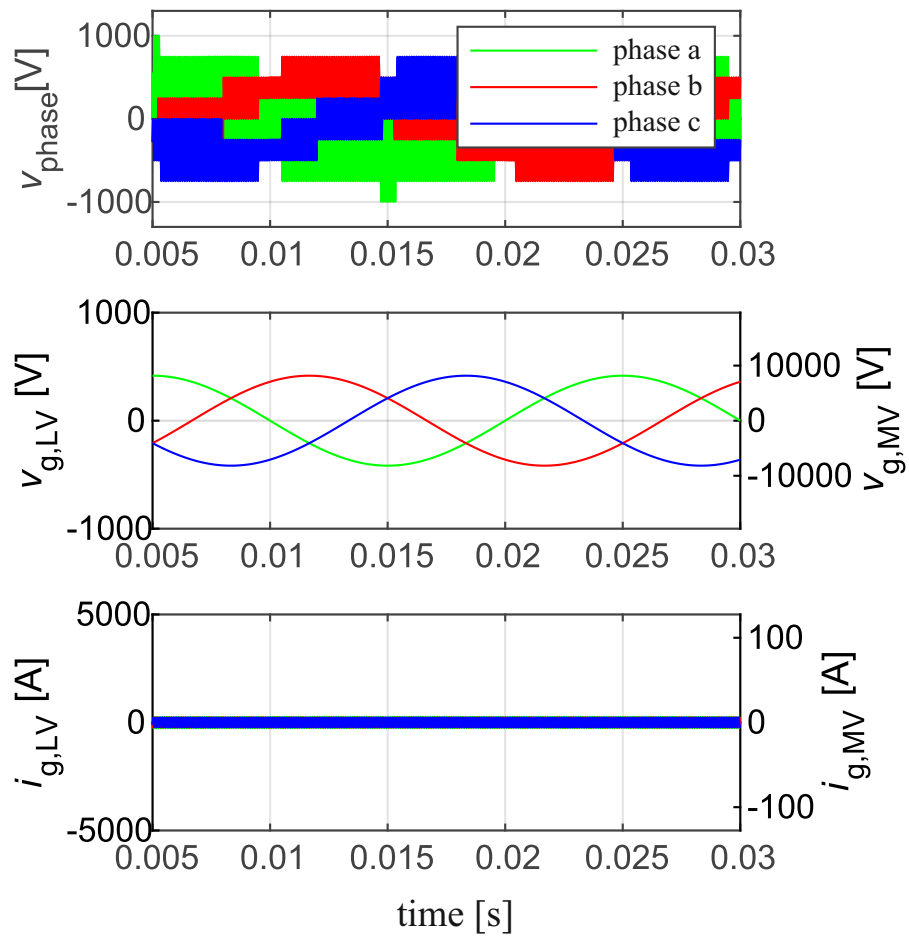
(a)
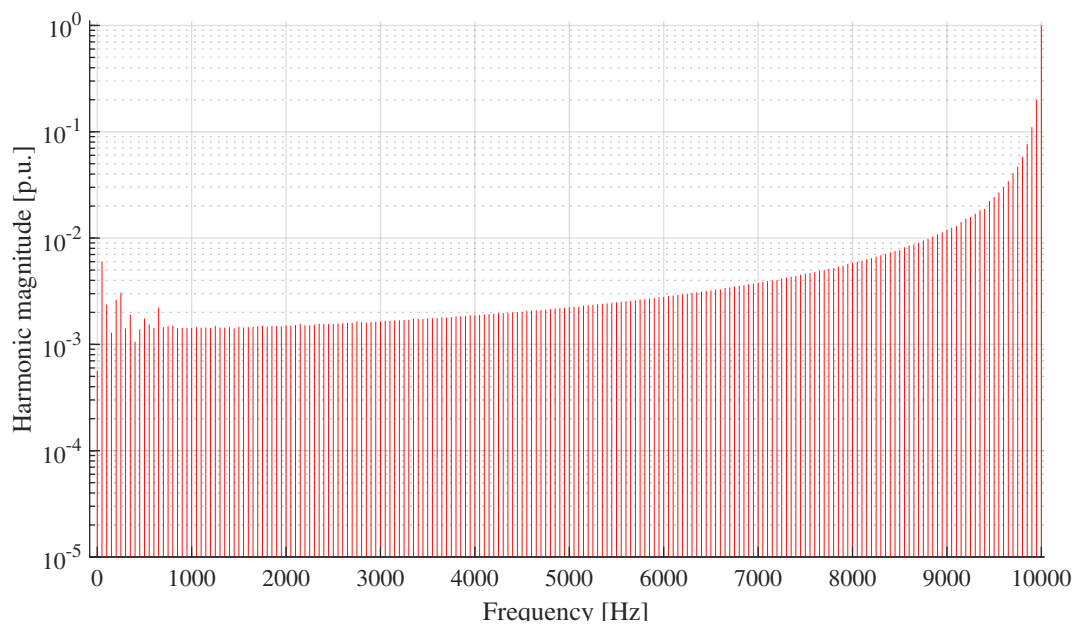
(b)

Figure 4.8: Current injection at $10\,\mathrm{kHz}$ ($\hat{i}_g^{10\,\mathrm{kHz}} = 188.2\,\mathrm{A}$): (a) Phase voltages, grid voltages (LV-side) and grid currents (PD-PWM, $f_c = 30\,\mathrm{kHz}$). (b) Normalized grid current spectrum (LV-side).

4.3 Summary and Conclusions of the Section

In this chapter parallel NPC inverters have been considered for connection to the MV grid by step-up transformers. One wind power plant and a grid impedance analyzer have been considered as target applications. The grid impedance analyzer is able to inject 1.655 MVA into the MV grid for proper grid excitation and impedance measurements. The design procedure has been fully described, resulting in a new practical application. Current harmonics up to 10 kHz are properly generated by six interleaved parallel NPC inverters and two parallel transformers, being designed for a wide frequency bandwidth.

For connection of higher powers huge LV currents are required and consequently a very high number of parallel NPC inverters. Already for one single wind generator of a wind park six NPC inverters have been applied to handle the currents. By means of the interleaved modulation both the filter design and the switching frequency have been minimized. Inverter current ripples of almost 400 A has been almost completely eliminated just by harmonic cancellation. From design point of view, it has become obvious that the number of required NPC inverters, filters and step-up transformers would be huge for achieving powers of 30 MW and more. Therefore, particularly for high power applications, the direct connection to the MV grid can be seen as very beneficial to limit the current ratings and the footprint of the system.

5 Modular Multilevel Converter Optimization for High-Power Applications

Compared to the classical three-level NPC inverter the MMC provides much higher voltage capability, enabling direct connection to medium and high voltage grids. In this way much higher system power ratings become possible at limited currents and at very high efficiencies. For the application of the MMC, STATCOM and DC transmission systems are considered, covering power ratings from 30 MVA up to 300 MW. For minimized power losses and maximum efficiency the NLM is applied and evaluated for the selected systems.

5.1 STATCOM Application

First, the MMC will be considered for a STATCOM application, being directly operating at the 20 kV MV grid. The converter will be designed for a maximum power of 30 MVA for grid support by reactive power injection.

5.1.1 Converter Design

For the MMC with high number of SMs the use of AC-side filters can be avoided. However, even without DC connection arm inductors are required to limit circulating currents between the phase legs. The arm inductors are designed with 3 mH, corresponding to a short-circuit voltage ratio of 20 %.

$$L_{\text{arm}} \geq \frac{u_{\text{sc,arm}} \cdot \left(\frac{V_g}{\sqrt{3}}\right)^2}{2\pi f P} \approx 3\,\text{mH} \tag{5.1}$$

The induced voltage drops across both arm inductors by the circulating currents are compensating each other on the AC side. Different to this, the voltage drops caused by the grid current need to be taken into account for the phase voltage amplitude according to (5.2). For 20 kV MV grid and a rated power of 30 MVA the grid current need to be controlled to 866 A, being splitted among both arms.

$$\hat{v}_{\text{L,arm},\curlywedge} = \sqrt{2} \cdot 2\pi f_g \cdot \frac{1}{2} L_{\text{arm}} \cdot \sqrt{2} \cdot I_g^{\text{MV}} \approx 816\,\text{V} \tag{5.2}$$

Grid voltage variations of up to 1 % and voltage drops need to be taken into account for both applications according to (5.3).

Table 5.1: Voltage design, required number of SMs per arm.

Δv_{cap}	$V_{\text{cap,lim}}$	$V_{\text{cap,min}}$	$V_{\text{dc,min}}$	N_{min}	$1.05N_{\text{min}}$
$\pm 5\%$	750 V	714.3 V	678.6 V	46	48
$\pm 10\%$	750 V	681.8 V	613.6 V	51	54
$\pm 5\%$	1062.5 V	1011.9 V	961.3 V	34	36
$\pm 10\%$	1062.5 V	965.9 V	869.3 V	38	40

$$\hat{v}_{\text{g},\curlywedge} = \sqrt{2} \cdot 1.01 \cdot (1 + u_{\text{g}} \cdot 1.01) \cdot \frac{V_{\text{g},\Delta}}{\sqrt{3}} \tag{5.3}$$

The minimum required DC voltage can be calculated according to (5.4), where possible very small voltage drops across the cablings are neglected. A minimum DC-side voltage $V_{\text{dc,min}}$ of 32288 V is obtained.

$$V_{\text{dc,min}} = \sqrt{3} \cdot (\hat{v}_{\text{g},\curlywedge}^{\text{MV}} + \hat{v}_{\text{L,arm},\curlywedge}) \tag{5.4}$$

The maximum capacitor voltage is selected to 62.5 % of the semiconductor voltage rating, as well. The capacitor voltage oscillations need to be taken account for calculation of the minimum capacitor voltage:

$$V_{\text{c,min}} = \frac{V_{\text{cap,lim}}}{(1 + |\Delta v_{\text{cap}})|^2} \tag{5.5}$$

The minimum number of SMs can be calculated based on the minimum capacitor voltage and the required DC voltage according to (5.6).

$$N_{\text{min}} = \left\lceil \left(\frac{V_{\text{dc,min}}}{V_{\text{cap,min}}} \right) \right. \tag{5.6}$$

The number of required SMs is calculated based on IGBT modules with 1200 V and 1700 V breakdown voltages, showing a high availability and reasonable costs at the market. For the capacitor voltage oscillations ranges of $\pm 5\%$ and $\pm 10\%$ are compared.

IGBT module with 1700 V breakdown voltages are selected for connection to the MV grid to limit the number of SMs to a reasonable value. Furthermore, capacitor voltage oscillations up to $\pm 10\%$ will be accepted to limit the size of the capacitor storages. This is particularly crucial in STATCOM applications since the highest voltage fluctuations occur at reactive power supply. Furthermore, STATCOM applications are not continuously operating at nominal power and therefore a temporary higher capacitor voltage stress can be accepted. Higher capacitor voltage oscillations are linked to reduced minimum capacitor voltages within the system. The minimum capacitor voltage is obtained in Table 5.1.

Table 5.2: MMC STATCOM simulation parameters (CC-MMC I BC-MMC).

Description	Parameter	Value	Unit
Rated power	$S_{g,nom}$	30	MVA
SMs per arm	N	40 I 20	
SM's capacitance	C_{sm}	30 I 9	mF
Arm inductance	L_{arm}	3	mH
IGBT breakdown voltage		1700	V
AC current (50 Hz, rms)		866	A
Capacitor voltage reference	v^*_{cap}	965.9 ($\pm$10%)	V
Capacitor voltage limitation	$V_{cap,lim}$	1062.5	V
Grid voltage (rms)	$V^{MV}_{g,\Delta}$	20	kV
Grid inductance (8%)	L_g	1.13	mH

$$V_{cap,min} = \frac{V_{cap,lim}}{1.1^2} = 869.3\,\text{V} \tag{5.7}$$

For the CC-MMC 40 SMs per arm are required, taking into account additional redundant SMs of 5 %. Due to the doubled modulation range the number of SMs for the BC-MMC is theoretically halved, obtaining 20 SMs per arm. The parameters for one MMC system with CCs and one with BCs are summarized in Table 5.2.

5.1.2 System Performance

Both MMC configurations will be evaluated and compared in terms of the performance and the capacitor design. The NLM is applied for both MMC configurations to maximize the efficiency. Third harmonic injection is applied to limit the number of SMs and the size of the capacitors. The focus is put on nominal positive reactive supply as benchmark case, being the most challenging operation point for the system. The grid current is properly controlled, exchanging 30 Mvar with the 20 kV medium voltage grid. The performance is excellent without any need of additional filters, as demonstrated in Fig. 5.1.

The insertion numbers, provided by the NLM, are shown in Fig. 5.2 for both SM configurations, approximating the closest available level of the arm voltage references with minimum numbers of commutations.

The DC-side behavior is depicted in Fig. 5.3. The circulating current is limited for the CC-MMC and even suppressed for the BC-MMC. The stored energy in the capacitors is properly controlled in each arm. The SM capacitances are selected to achieve an equivalent capacitor voltage oscillations in the arms, being crucial for the converter design.
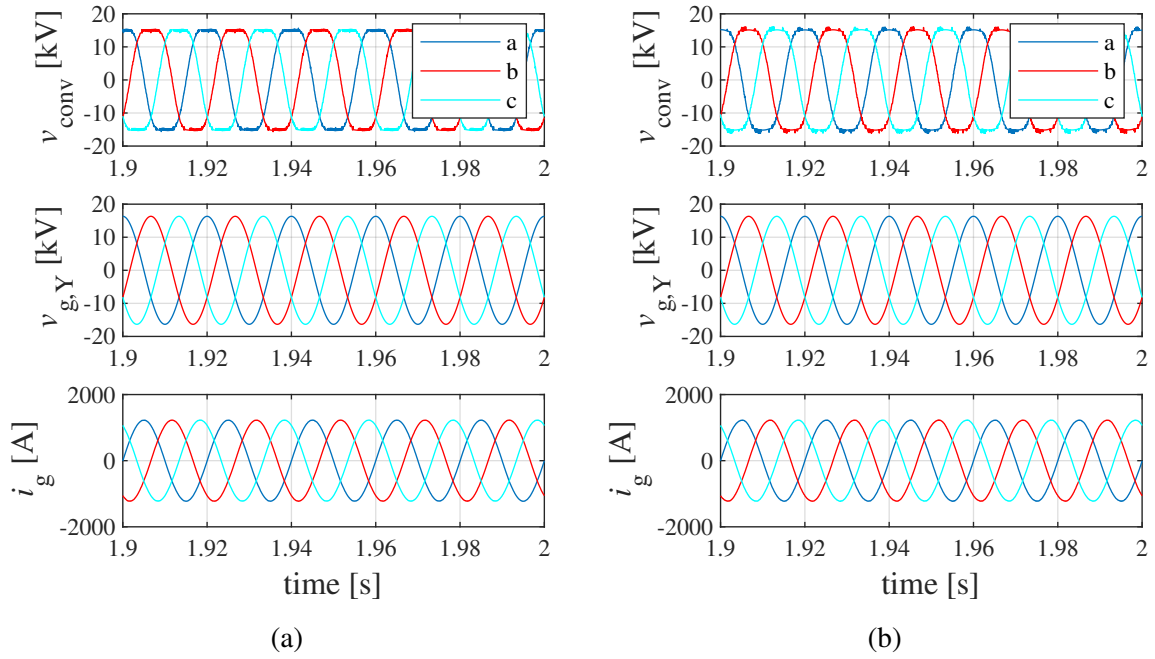
Figure 5.1: AC-side behavior: (a) CC-MMC. (b) BC-MMC (NLM sequence 1).
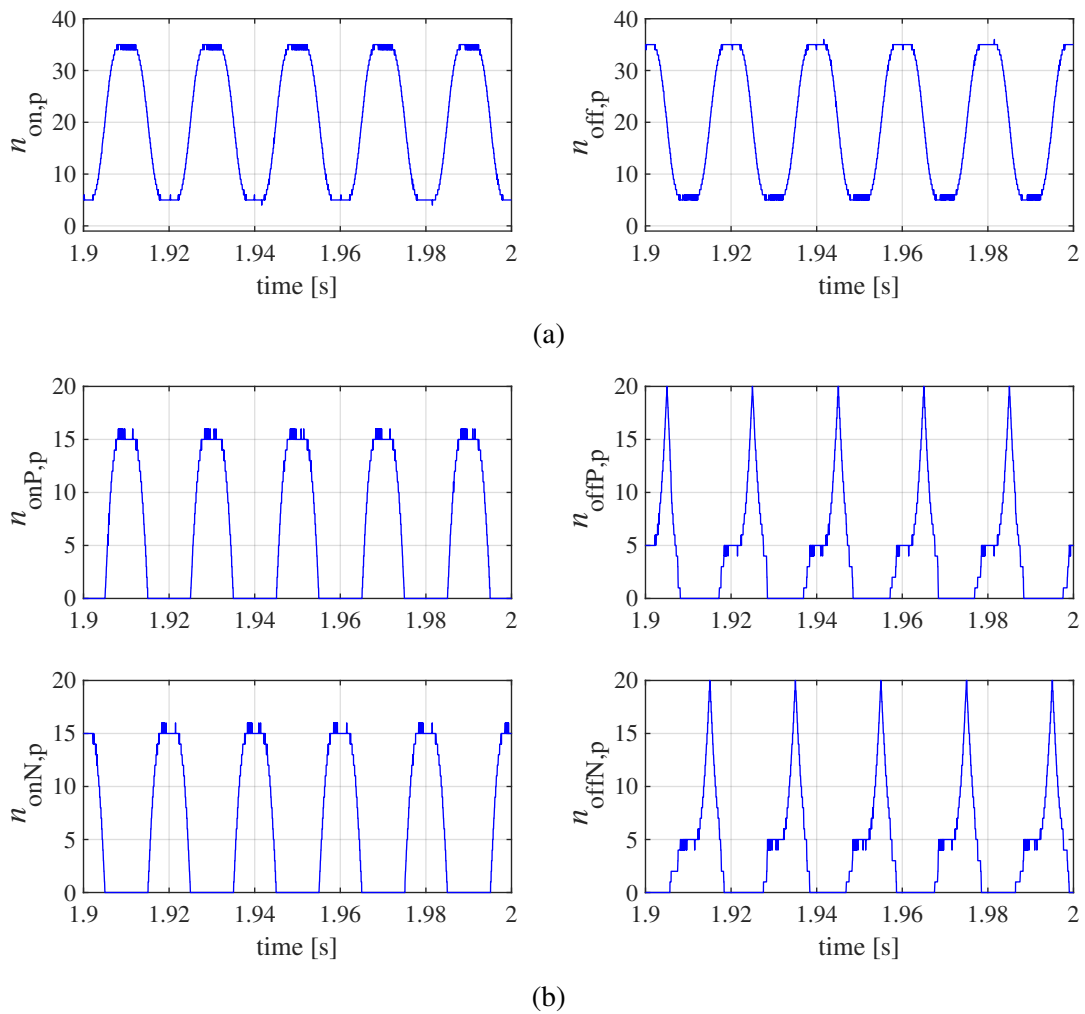
Figure 5.2: Insertion numbers (upper arm, phase a): (a) CC-MMC. (b) BC-MMC.
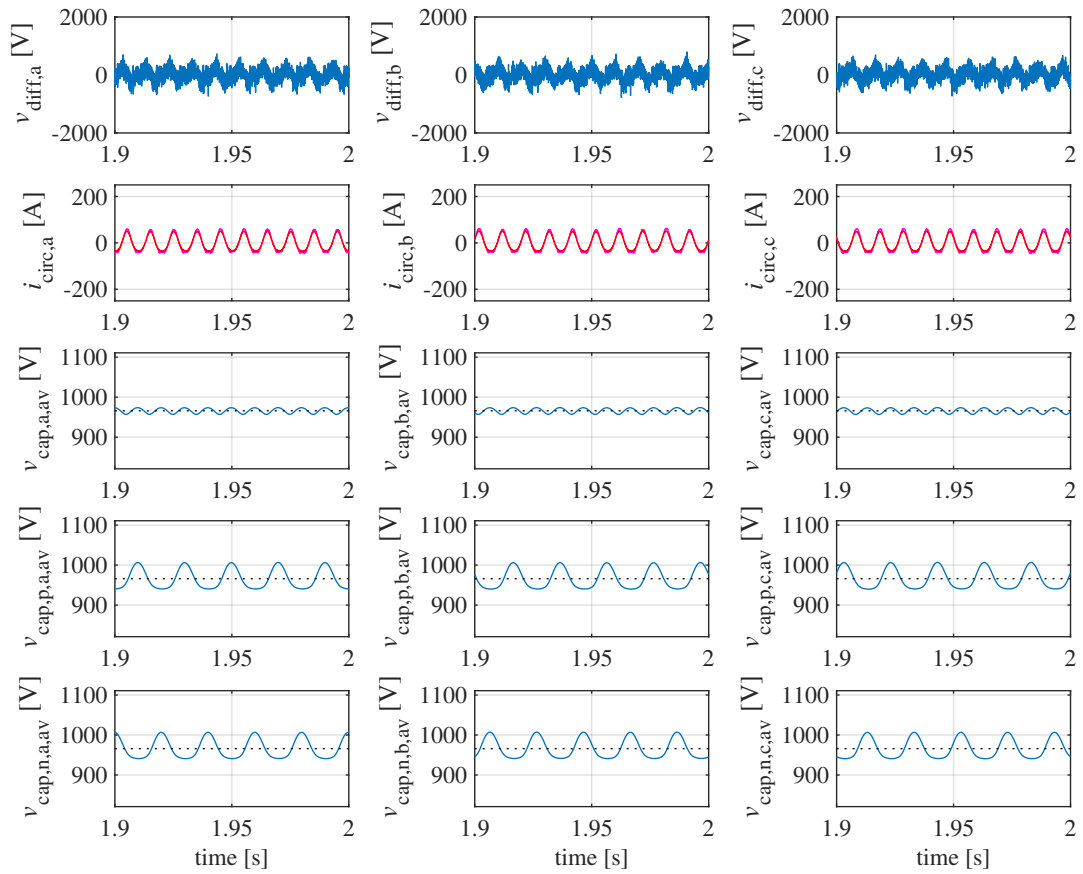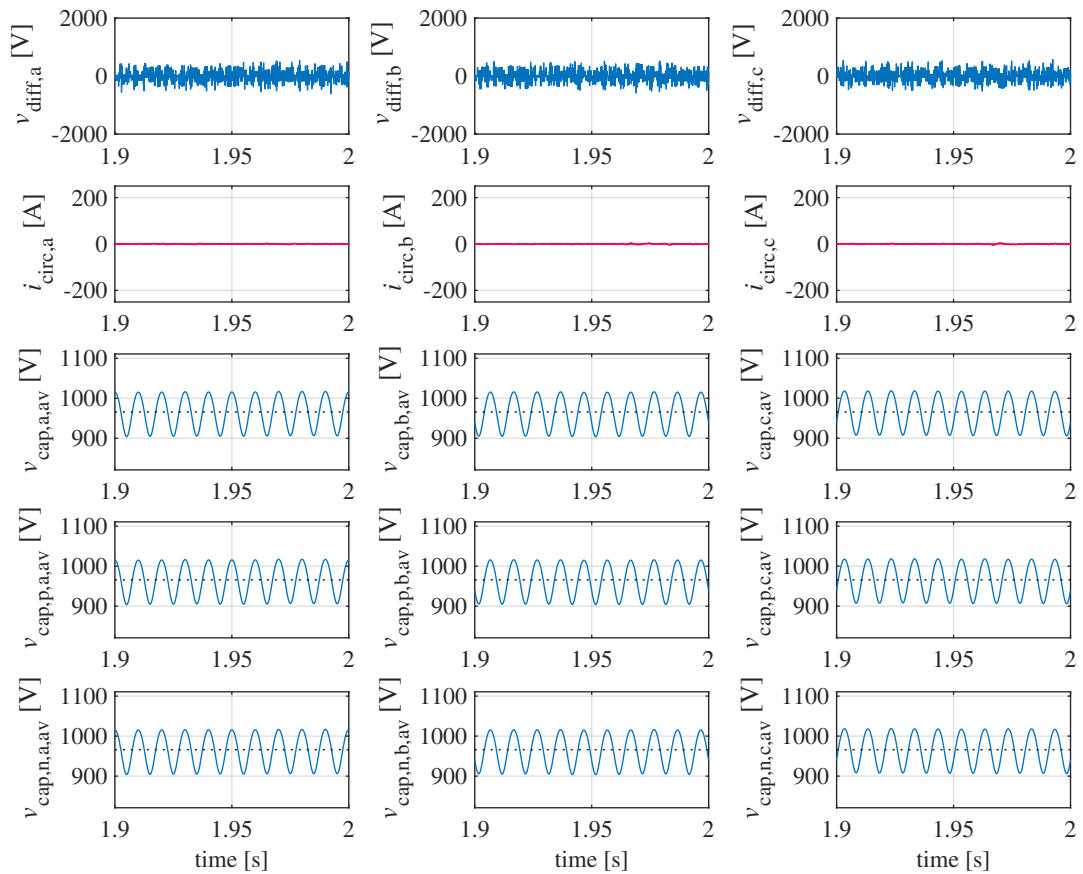
Figure 5.3: DC-side behavior: (a) CC-MMC. (b) BC-MMC.
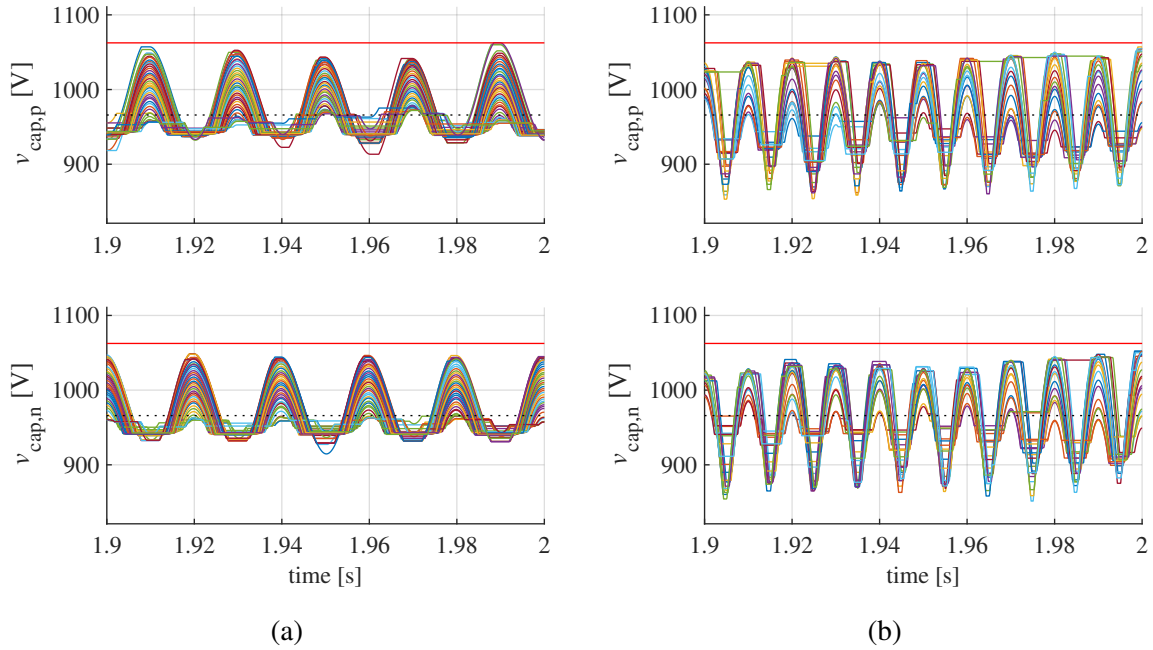
Figure 5.4: Capacitor voltages (phase a): (a) CC-MMC. (b) BC-MMC.

All capacitor voltages in one leg are shown in Fig. 5.4, being kept within the predefined limits. For this purpose, the SM capacitances of the CC-MMC have been designed with 30 mF. Instead for the BC-MMC the capacitor voltages are already kept within the range by capacitances of 9 mF. Accordingly, the capacitor size of the MMC has been strongly reduced by the application of BC-SMs. Since the size and costs of the capacitors are one of the main challenges in practical MMC projects, the BC-MMC provides a significant benefit to limit the investment costs and the footprint of the system.

The MMC setup from Aalborg University has been introduced in Section 3.1.3. For experimental validation it has been configured in three-phase mode (four SMs per arm) at the electric grid for fault-ride through operation. In Fig. 5.5 a symmetrical three-phase fault is emulated by an AC voltage source for 0.2 s. The current is properly controlled also during transient conditions even by the applied NLM and only with four SMs in each arm.

The circulating currents are limited to a very low value even in transient conditions, as shown in Fig. 5.6. The capacitor voltages are properly controlled and kept within the limits by the embedded capacitor voltage algorithm.

Instead, in Fig. 5.7 a phase-to-phase fault (a,c) is emulated by an AC voltage source for 0.2 s. During the grid fault, a reactive current of 5 A is injected for grid voltage support. Also during this unsymmetrical grid fault the circulating currents are properly controlled, as shown in Fig. 5.8. The capacitor voltages are kept within the limits.

The fault-ride-through capability of the MMC has been demonstrated for both symmetrical and asymmetrical grid fault conditions. The grid current and the stored energies in the legs and in the arms are properly controlled from the AC side without any DC-side connection.
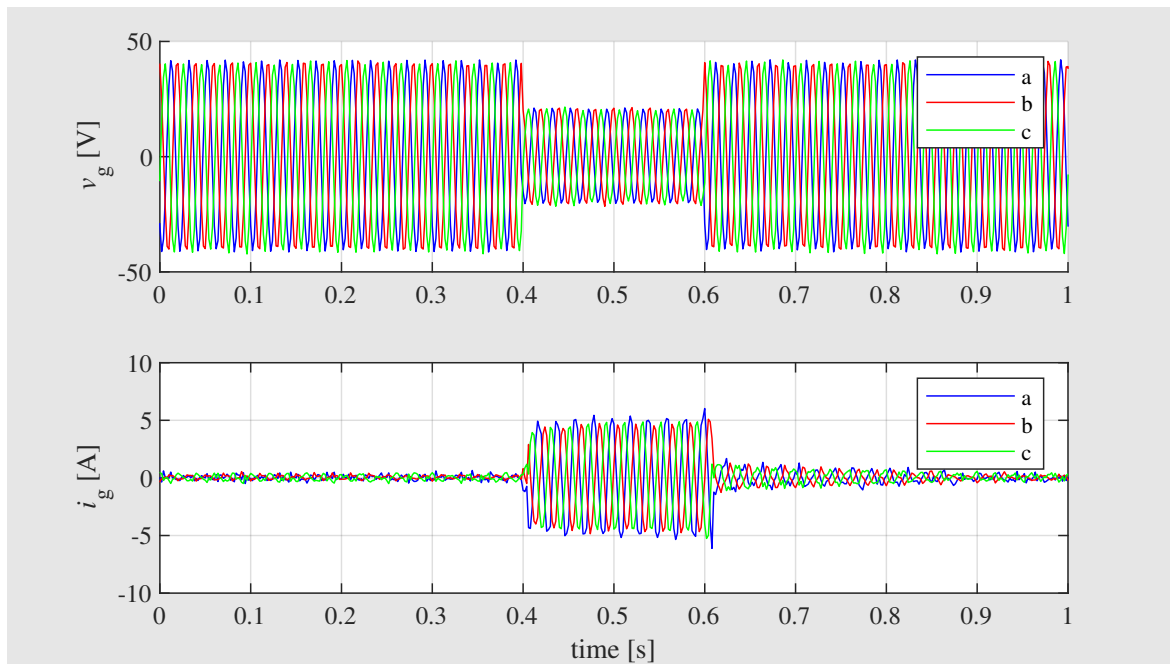
Figure 5.5: Experimental results, grid voltages and grid currents during a three-phase fault, positive sequence ($V_{g,\Delta} = \sqrt{3} \cdot 30\,\mathrm{V}$).
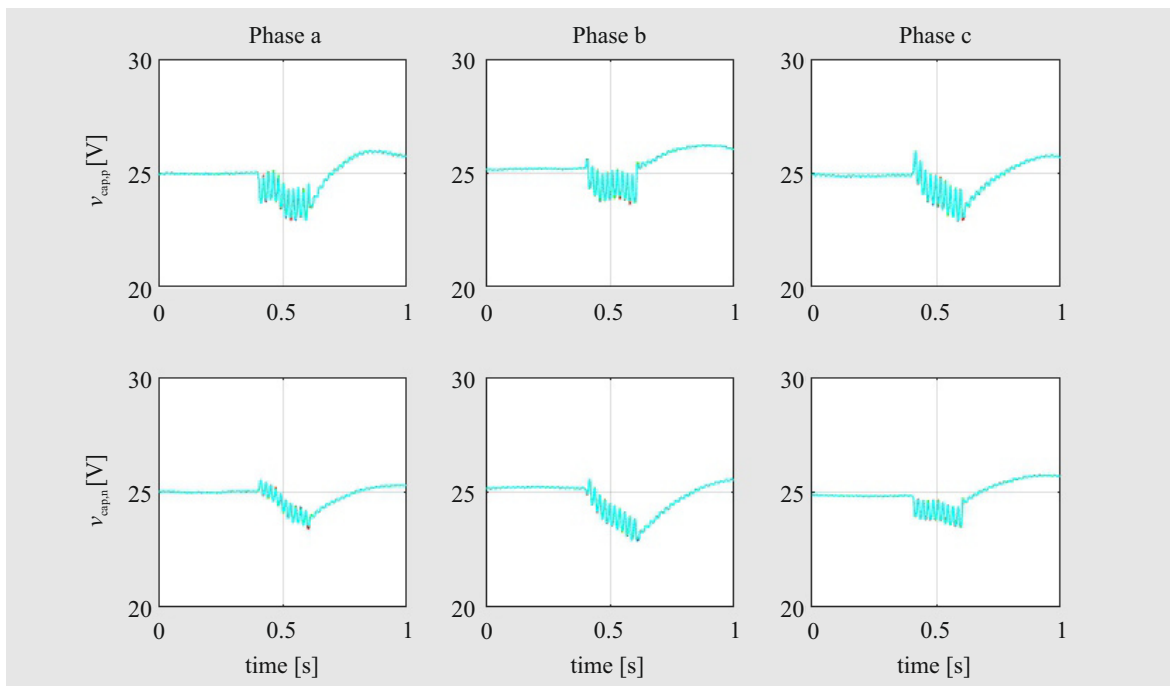
Figure 5.6: Experimental results, circulating currents and capacitor voltages during a three-phase fault ($V_{g,\Delta} = \sqrt{3} \cdot 30\,\mathrm{V}$).
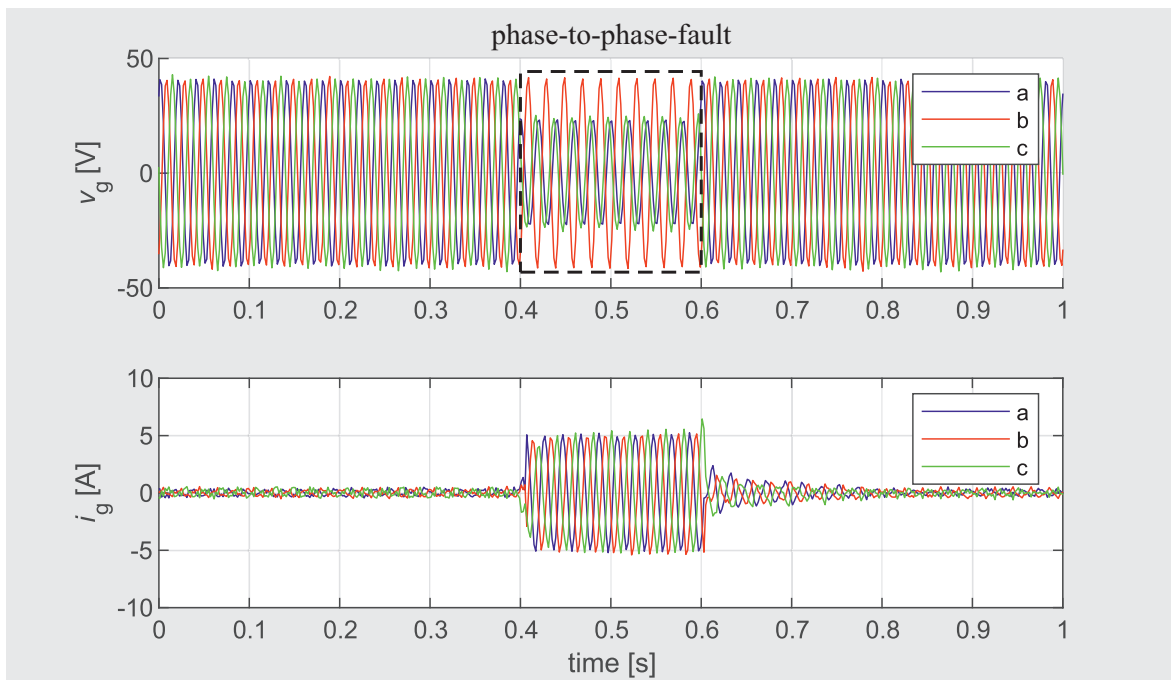
Figure 5.7: Experimental results, grid voltages and grid currents during a phase-to-phase fault, positive sequence ($V_{g,\Delta} = \sqrt{3} \cdot 30\,\text{V}$).
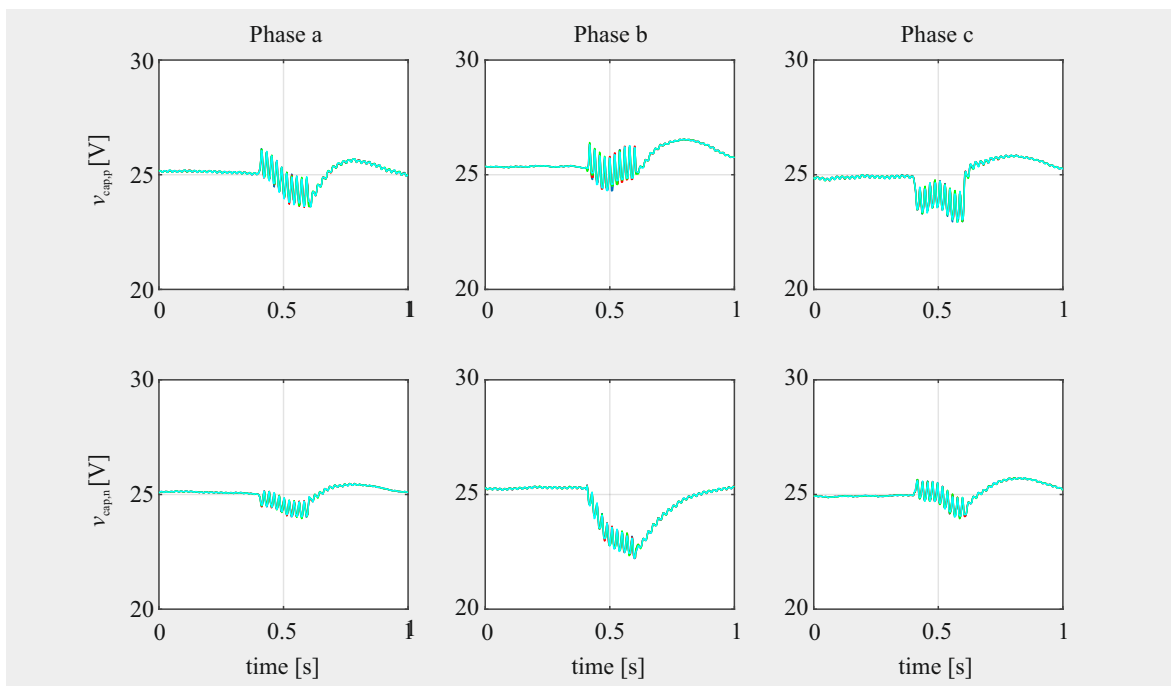
Figure 5.8: Experimental results, circulating currents and capacitor voltages during a phase-to-phase fault ($V_{g,\Delta} = \sqrt{3} \cdot 30\,\text{V}$).

Table 5.3: Harmonic content of a six-pulse line commutated rectifier.

Harmonic order	5th	7th	11th	13th	17th	19th
Harmonic percentage	23 %	14.3 %	9.1 %	7.7 %	5.9 %	5.3 %
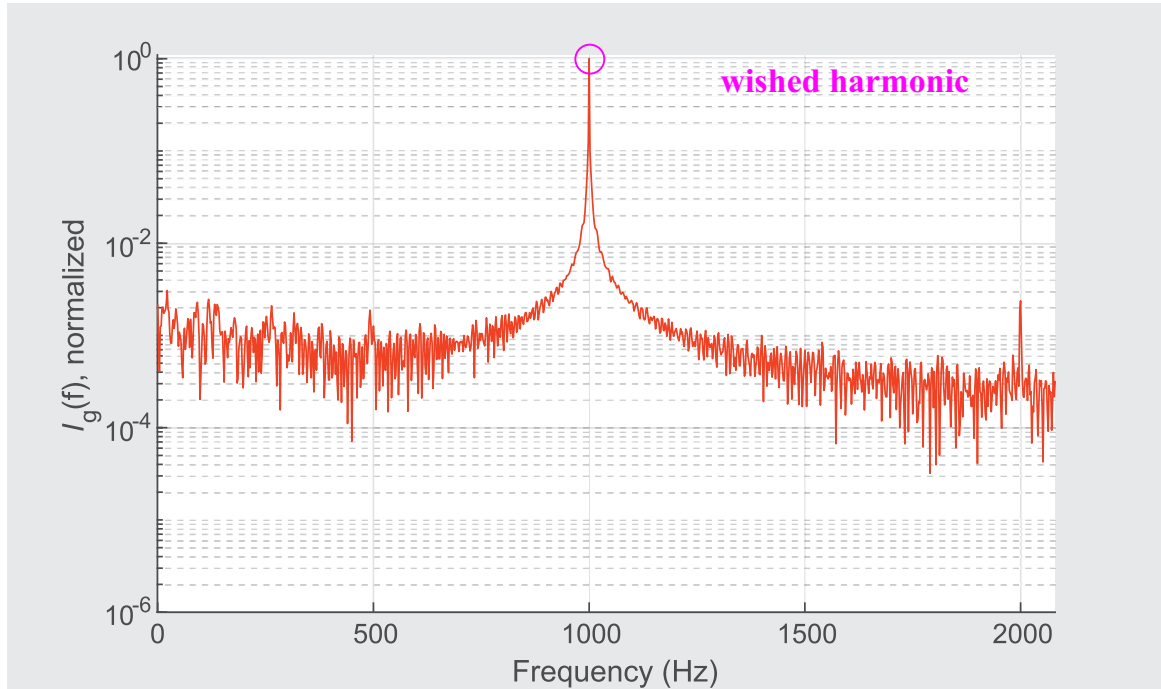
Figure 5.9: Experimental results for the MMC (12 SMs per arm, one phase, NLM): Current spectrum ($f_s = 20\,\text{kHz}$).

The converter voltages are properly generated even by the NLM and the capacitor voltages are effectively balanced in each arm.

Advanced STATCOM applications are not only able to apply reactive power for grid stabilization but also active power filtering capability to compensate unwanted harmonics at the grid. As demonstrated in Fig. 5.9 and Fig. 5.10 the number of voltage levels is already more than sufficient even into the kHz range, exemplary shown at 1 kHz.

For practical demonstration the MMC has been used to compensate a six-pulse line-commutated rectifier. The required harmonics are summarized in Table 5.3 [136]. The currents are properly generated by the one-phase MMC setup with twelve SMs per arm by the NLM as demonstrated in Fig. 5.11. The current spectrum is provided in Fig. 5.12 in comparison with the well-established PS-PWM $f_c = 200\,\text{Hz}$ as a benchmark case. The waveform quality by using the NLM is almost similar to the PS-PWM due to the high number of available voltage levels.

Hence, active power filter capability can be even provided by low-switching frequency modulation techniques as the NLM, taking advantage of the high number of available voltage levels of the MMC. As demonstrated before, all harmonic currents are properly generated at limited switching losses even up to voltage and current frequencies of 2 kHz.
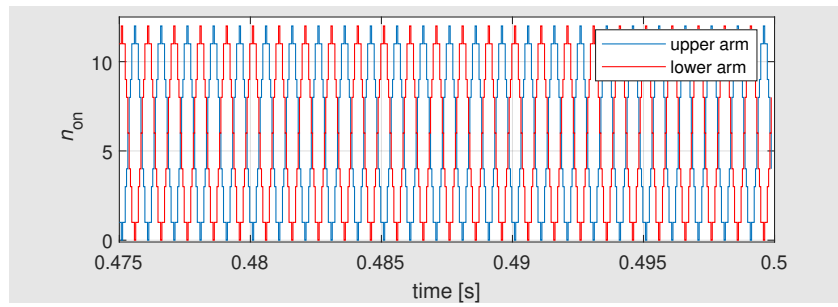
(a)
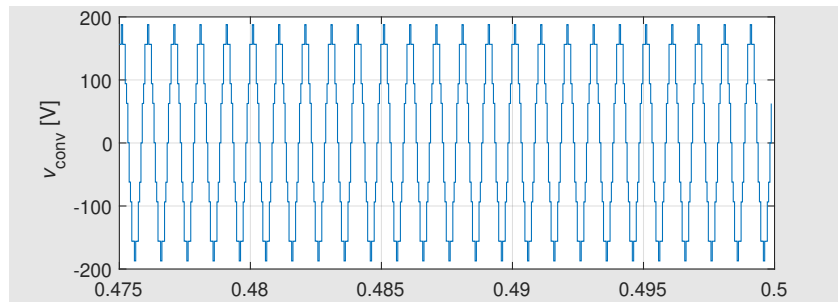
(b)
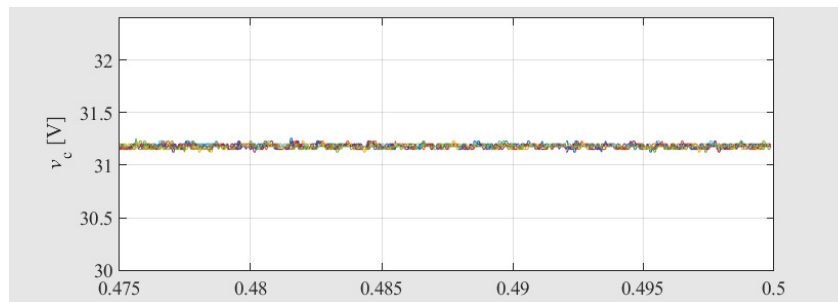
(c)
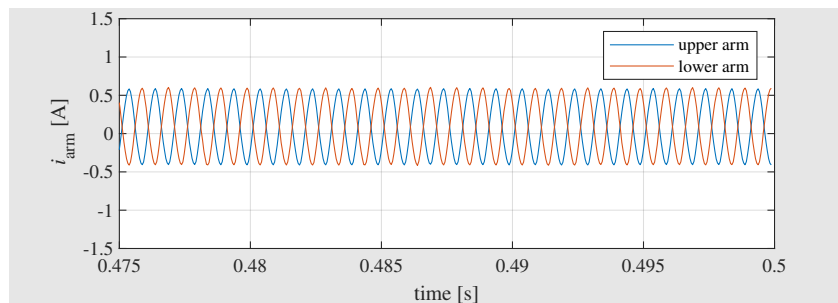
(d)
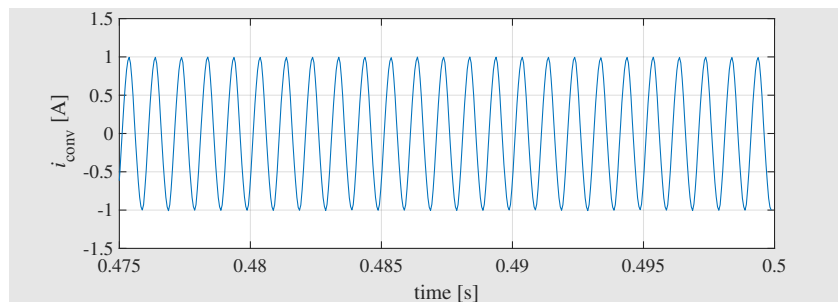
(e)

Figure 5.10: Experimental results for the MMC (12 SMs per arm, one phase, NLM): (a) Insertion numbers. (b) Converter voltage. (c) Capacitor voltages (upper arm). (d) Arm currents. (e) Phase current.

(a)

(b)

(c)

(d)

(e)
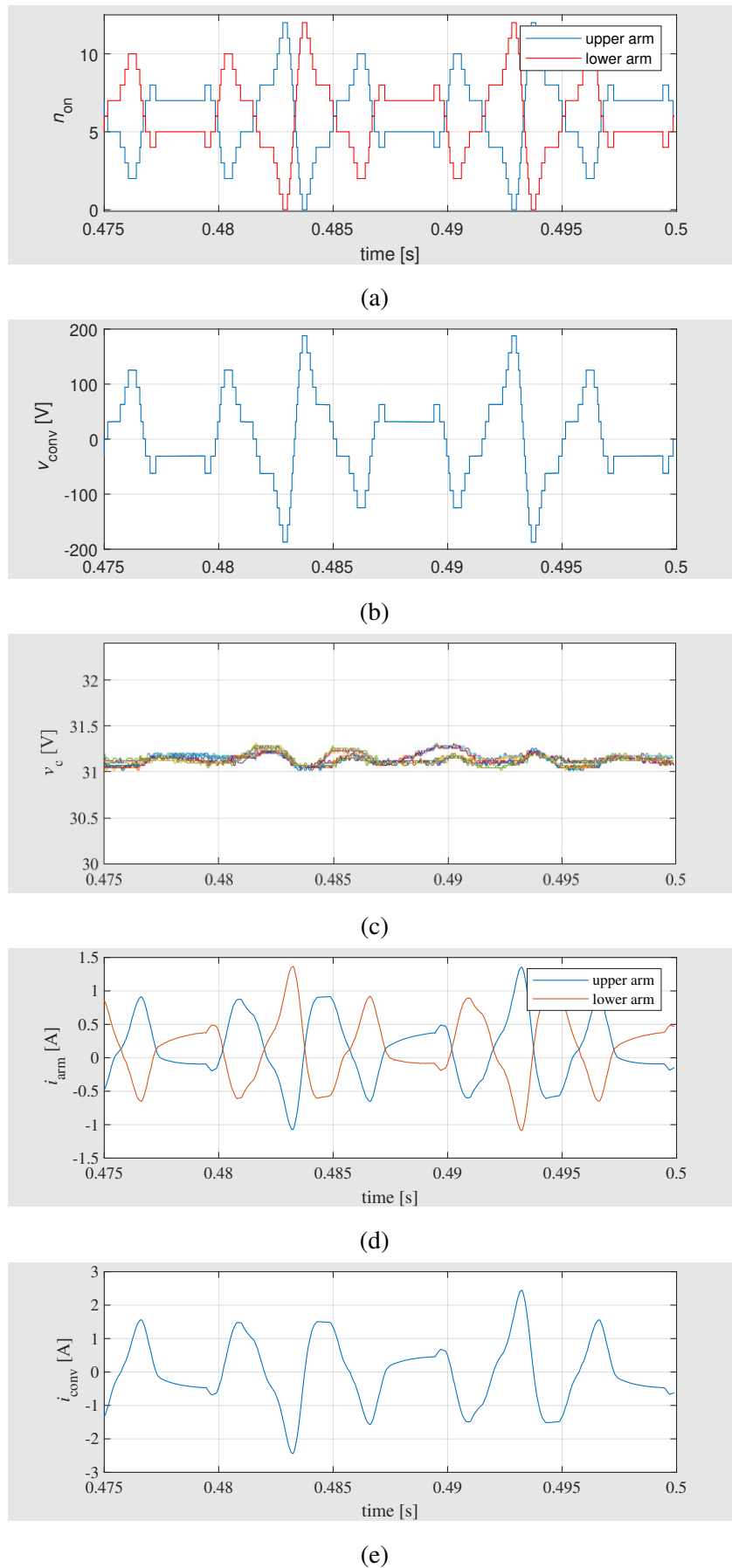
Figure 5.11: Experimental results for the MMC, active power filtering (12 SMs per arm, one phase, NLM): (a) Insertion numbers. (b) Converter voltage. (c) Capacitor voltages (upper arm). (d) Arm currents. (e) Phase current.
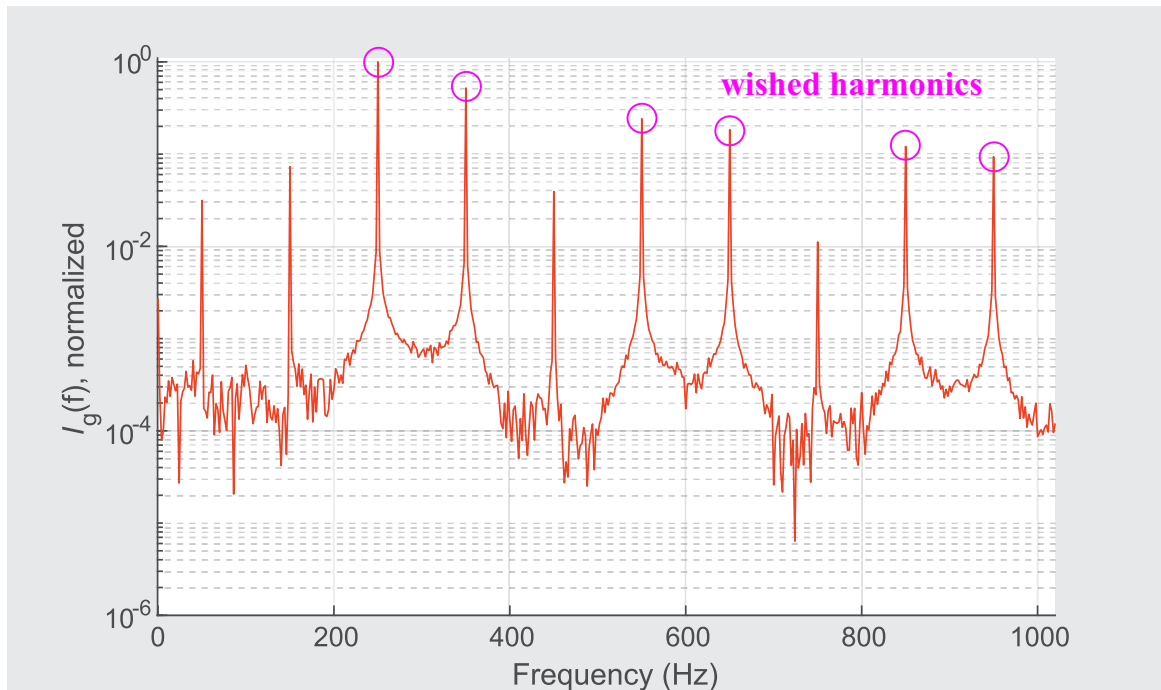
(a)
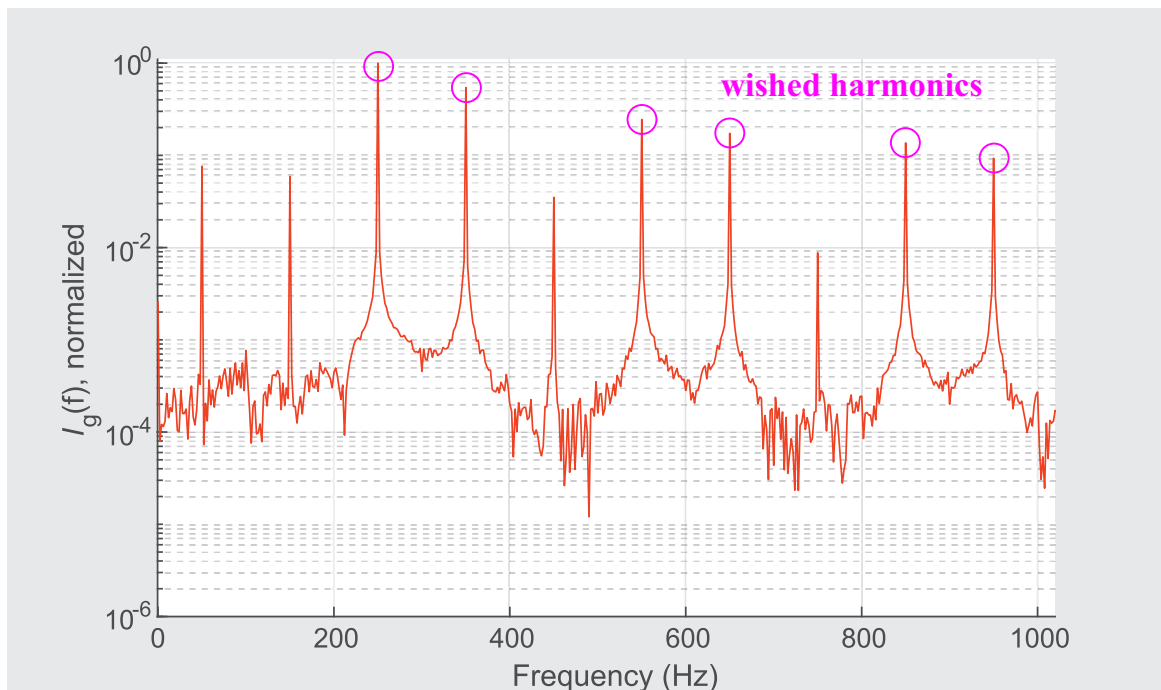
(b)

Figure 5.12: Current spectrum ($f_\mathrm{s} = 20\,\mathrm{kHz}$) for experimental results (MMC, 12 SMs per arm, one phase): (a) NLM, (b) PS-PWM ($f_\mathrm{c} = 200\,\mathrm{Hz}$).

Table 5.4: MMC simulation parameters for an MVDC application.

Description	Parameter	Value	Unit
Rated power	$S_{g,nom}$	30	MVA
SMs per arm	N_{CC}	36	
SM's capacitance	C_{sm}	30	mF
Arm inductance	L_{arm}	3	mH
IGBT breakdown voltage		1700	V
AC current (50 Hz, rms)		866	A
Capacitor voltage reference	v_{cap}^*	1011.9 ($\pm 5\%$)	V
Capacitor voltage limitation	$V_{cap,lim}$	1062.5	V
Grid voltage (rms)	$V_{g,\Delta}^{MV}$	20	kV
Grid inductance ($u_g = 8\%$)	L_g	1.13	mH

5.2 DC Transmission Systems

DC transmission systems on MV or HV level require very high blocking capabilities not only at the AC side but also at the DC side. For blocking the DC-link voltage, the arm voltages need to be shifted by $+\frac{V_{dc}}{2}$ not only for the CC-MMC but also for the BC-MMC. Consequently, the extended modulation range of the BC-MMC cannot be utilized for DC transmission systems. Therefore, the number of semiconductor devices for the BC-MMC strongly increases compared to the CC-MMC. Accordingly, the CC-MMC can be seen as the preferred choice for DC transmission systems to limit the system costs. Again, the NLM is applied to profit from the high number of voltage levels at fundamental switching frequencies. The focus is put on the inverter stage, transmitting the power into the AC grid.

5.2.1 MVDC

The parameters for the CC-MMC are summarized in Table 5.4 for a MVDC application. The system is rated for an active power of 30 MW and consists of 36 SMs per arm for direct connection to the 20 MV AC grid.

The AC-side behavior of the MMC is shown in Fig. 5.13a at nominal power and a unity power factor. The converter voltage waveforms are very smooth due to high number of available voltage levels. The third harmonic injection is set to one sixth of the amplitude. The grid current is properly controlled to 866 A, being directly injected into the 20 kV MV grid. The generated waveforms are excellent even without any AC-side filters.

In Fig. 5.13c the DC-side behavior is shown. The circulating currents are properly controlled by the differential voltages. The positive DC part in the circulating current represents the active power transfer from DC to AC side. Furthermore, a small AC amplitude at 100 Hz is inherent to compensate the power oscillations in each phase. For economical component
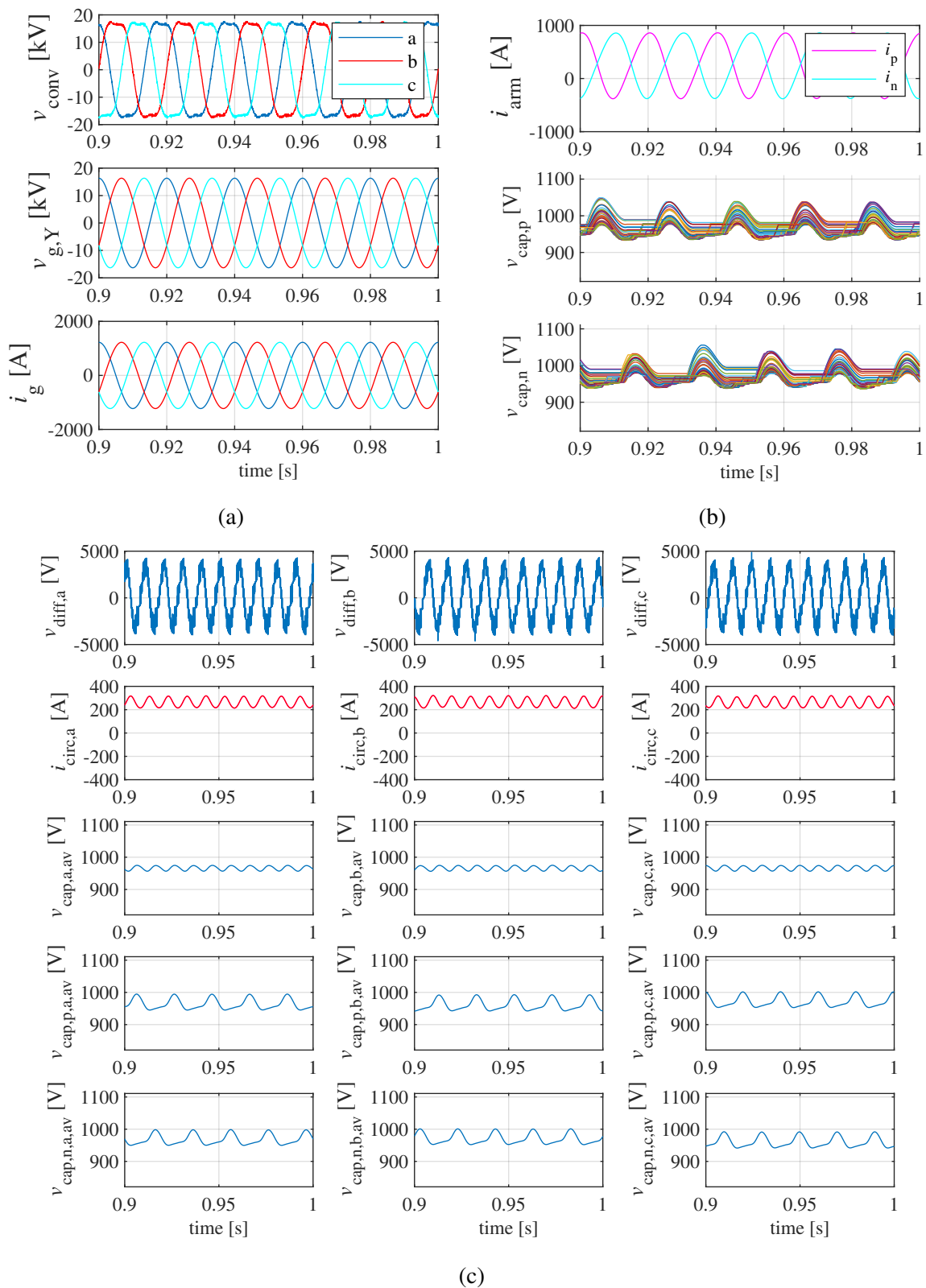
Figure 5.13: Electrical behavior of the MMC for an MVDC application ($P_\mathrm{g} = 30\,\mathrm{MW}$, $\cos\varphi = 1$): (a) AC-side behavior. (b) Arm currents and capacitor voltages (phase a). (c) DC-side behavior.

Table 5.5: MMC simulation parameters.

Description	Parameter	Value	Unit
SMs per arm	N_{cc}	150	
DC-link voltage	V_{dc}	300	kV
SM's capacitance	C_{sm}	10	mF
Arm inductance	L_{arm}	72	mH
Grid voltage	$V_{g,\Delta}$	120	kV
Grid inductance	L_g	25	mH
Cooling resistance (T)	$R_{th,CH,T}$	5.2	$\frac{K}{kW}$
Cooling resistance (D)	$R_{th,CH,D}$	11.7	$\frac{K}{kW}$

design, it is limited to around 10 % of the 50 Hz amplitude in the arm currents. The energies, being stored in each phase and in each arm, are properly controlled and regulated.

In Fig. 5.13b the capacitor voltages are shown for each single SM, exemplary for one phase. All capacitor voltages are kept within the limits just by the modulator despite of the very low switching frequencies, and no additional commutations are required.

5.2.2 HVDC

For connection to the HV grid the MMC has been scaled up, being designed for a rated power of 300 MW. In each arm 150 SM per arm are applied with 4.5 kV IGBT modules. The increase of the IGBT voltage class is required to limit the number of SMs to a reasonable value, even if it leads to higher costs. The capacitor voltages are well balanced and limited to 2500 V for protection. The basic system data are summarized in Table 5.5.

The electrical behavior of the MMC is exemplary shown in Fig. 5.14 at nominal power transfer at a $\cos\varphi$ of 0.95. The power factor corresponds to a reactive power of 98.6 Mvar. The waveform generation is excellent even with NLM due to the huge number of available voltage levels. The AC current is properly controlled, showing an amplitude of around 2150 A. The circulating current shows a positive DC part and a peak-to-peak ripple of around 120 A. The DC part is particularly characteristic for the active power supply, illustrating the power transfer from the DC to the AC side. With the help of the circulating current control the average capacitor voltage is oscillating within around 70 V. The capacitor voltages are properly balanced in each arm, being limited to 2500 V for protection of the devices.

5.3 Summary and Conclusions of the Section

In this chapter the MMC has been investigated and optimized for a MV STATCOM application and for two DC transmission systems based on very detailed simulation studies from the
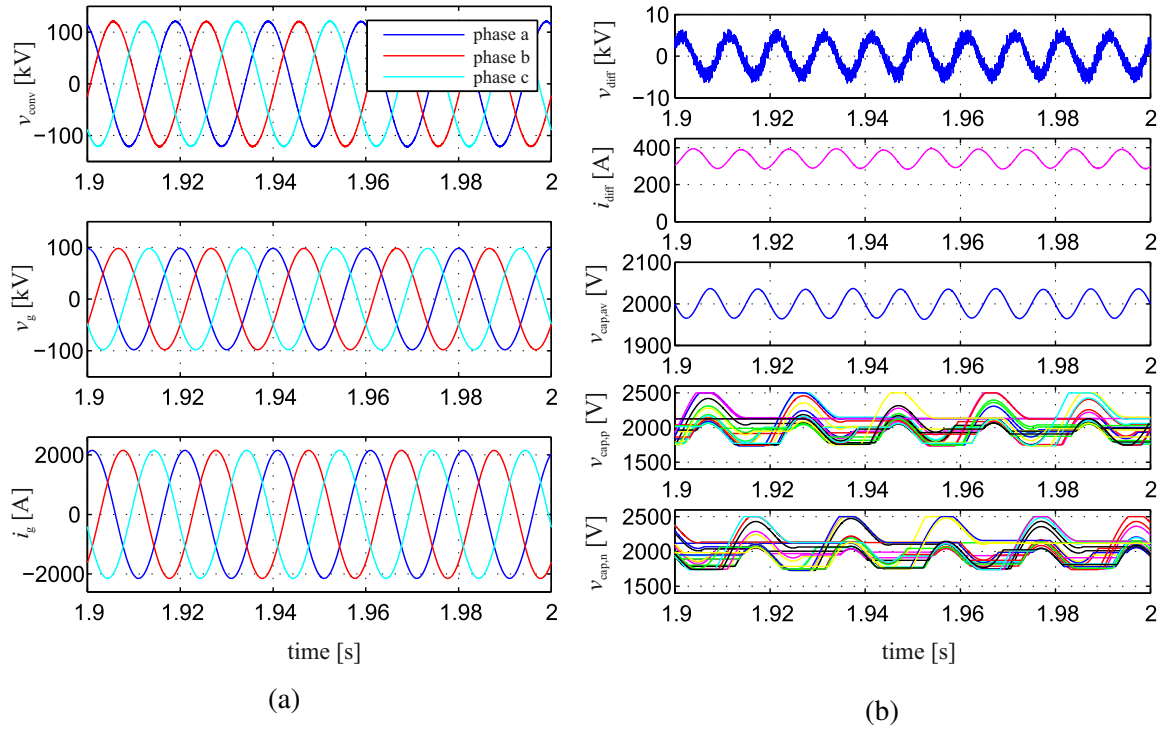
Figure 5.14: Electrical behavior of the MMC for an HVDC application ($P_g = 300\,\text{MW}$, $\cos\varphi = 0.95$): (a) AC side. (b) DC side (phase a).

system level down to the component level. The behavior of each single SM has been modeled in detail, even for an HVDC application with 150 SMs per arm. Powers up to 300 MW are properly controlled for flexible exchange with the 50 Hz AC grid.

The STATCOM application has been considered and fully controlled without any DC-link connection. The stored energies in the capacitors have been properly regulated from the AC side both in simulation and experiments. Different grid fault conditions have been investigated in the laboratory. As an additional feature active power filtering capability has been adopted. For a study case the harmonics from a six-pulse line commutated rectifier have been compensated by proper current generation up to frequencies of 1000 Hz.

Both the CC-MMC and the BC-MMC have been investigated and compared for STATCOM applications. It has been shown that the number of SMs can be strongly reduced for the BC-MMC by using the full available modulation range. The capacitances of the energy storages have been downsized by the application of BC-SMs instead of CC-MMCs. In this way the investment costs and the footprint of the system can be limited.

For all investigated MMC systems the NLM has been applied to achieve a fundamental switching frequency by using all available SMs and all available voltage levels. This goal has been accomplished for both the CC-MMC and the BC-MMC. It has been demonstrated that even with the NLM the available voltage levels in conventional MV applications are sufficient to achieve excellent waveform quality based on standard 1.7 kV IGBT modules. The use of fast-switching PWM techniques has been avoided in MV and HV applications, allowing extremely high efficiencies.
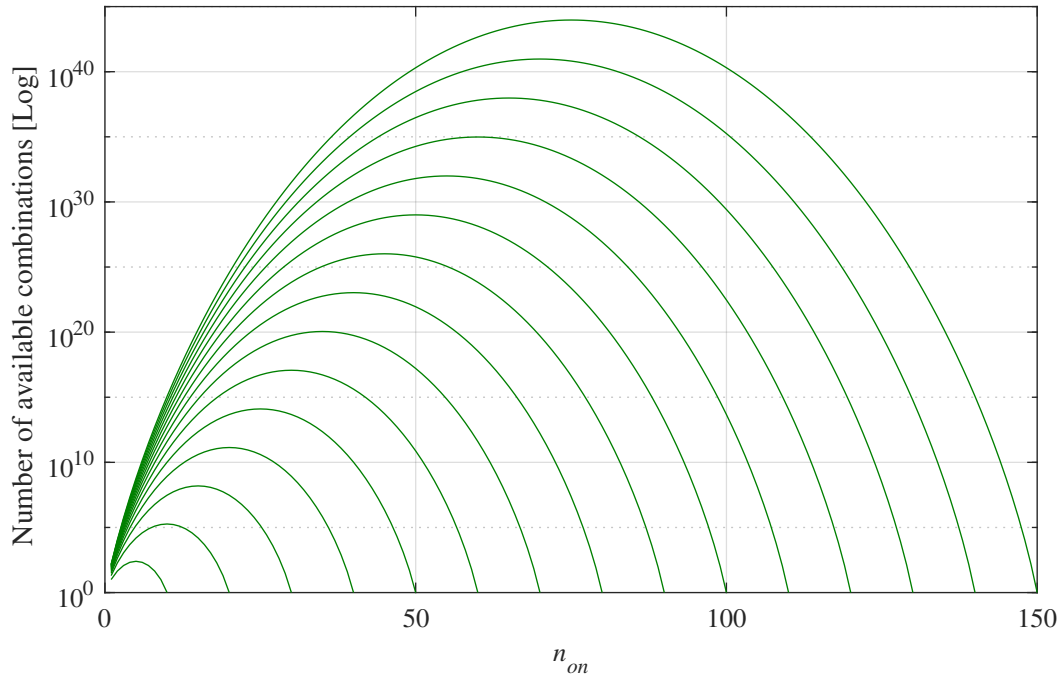
Figure 6.1: Available switching combinations in one MMC arm with 10 SMs to 150 SMs (CCs).

6 Thermal Management for the Modular Multilevel Converter

The MMC can be seen as the preferred choice for high-power applications as further demonstrated in Chapter 5. Apart from its high efficiency and excellent waveform generation the MMC particularly benefits from its modular structure. The high number of SMs in MMC applications is linked to very high numbers of redundant switching states as illustrated in Fig. 6.1 with 10 SMs to 150 SMs in each arm.

Conventionally, the redundant switching states are used only for the CVB to minimize the capacitor voltage spread and the required SM capacitances. However, the huge number of redundant switching states also provides high potential for multi-objective optimization.

For safe and reliable operation not only the capacitor voltages but also the temperatures of the components are crucial. The temperatures of the semiconductors and capacitors are one limiting factor for an economical design and safe operation. At the same time, the temperature profiles are directly linked to the component lifetimes.

Usually, a certain reserve of additional SMs is provided for high system availability, over-fulfilling the actual voltage design requirements. Accordingly, failed SMs can be bypassed without affecting the safe operation and availability of the system. Nevertheless, the number of additional SMs needs to be selected carefully to limit investment costs and also the footprint of the system.

An effective thermal management for the MMC will be introduced in this chapter. On the one hand it allows a very economical component design tailored for the requirements of the system. An optimization of the temperature profiles of the system is linked to a huge saving potential for the component design, e.g. limiting the dimensions of each component (semiconductors, capacitors) as well as of the cooling system. Consequently, the investment costs of the system can be significantly reduced. On the other hand, an effective thermal management allows the limitation of thermal strain of the components, being linked to longer lifetimes and maintenance intervals as well as the capability for overload conditions. Consequently, also the operating costs of the system can be significantly reduced.

All different optimization goals are directly linked to the temperatures of the components. For the economical design the maximum temperatures of the semiconductor devices and capacitors are very crucial. For long reliability, the thermal cycles and maximum temperatures of the semiconductor devices as well as the operating temperature of the capacitors need to be limited. For overload conditions a temperature reserve needs to be provided to avoid overtemperatures in the semiconductors and capacitors.

In Section 6.1 the thermal behavior of the MMC is analyzed and investigated. Section 6.3 introduces different thermal management approaches to optimize the temperature profiles of the semiconductor devices for the CC-MMC as well as the BC-MMC. Section 6.4 puts the focus on the thermal management of the capacitor storages for both MMC configuration. In Section 6.5 the introduced approaches will be combined to optimize the temperature profiles of all main components for each CC-SM and for each BC-SM.

6.1 Thermal Modeling and Investigation

Occurring power losses in semiconductor devices and capacitors are mainly revealed by heat. Therefore, for an adequate thermal modeling the losses need to be taken into account. For condition monitoring the power losses and temperatures can be approximated in real time based on available system information without any need of additional sensors. This is particularly beneficial for MMC applications where a huge number of temperature sensors would be required to monitor the whole system.

6.1.1 Power Losses and Efficiency

For the calculation of semiconductor power losses a numerical approach is applied. The power losses are approximated by the corresponding datasheet characteristics at a junction temperature of $125\,°C$ and the available information during operation. The real-time calculation of the power losses is presented for both, the CC-MMC and the BC-MMC.
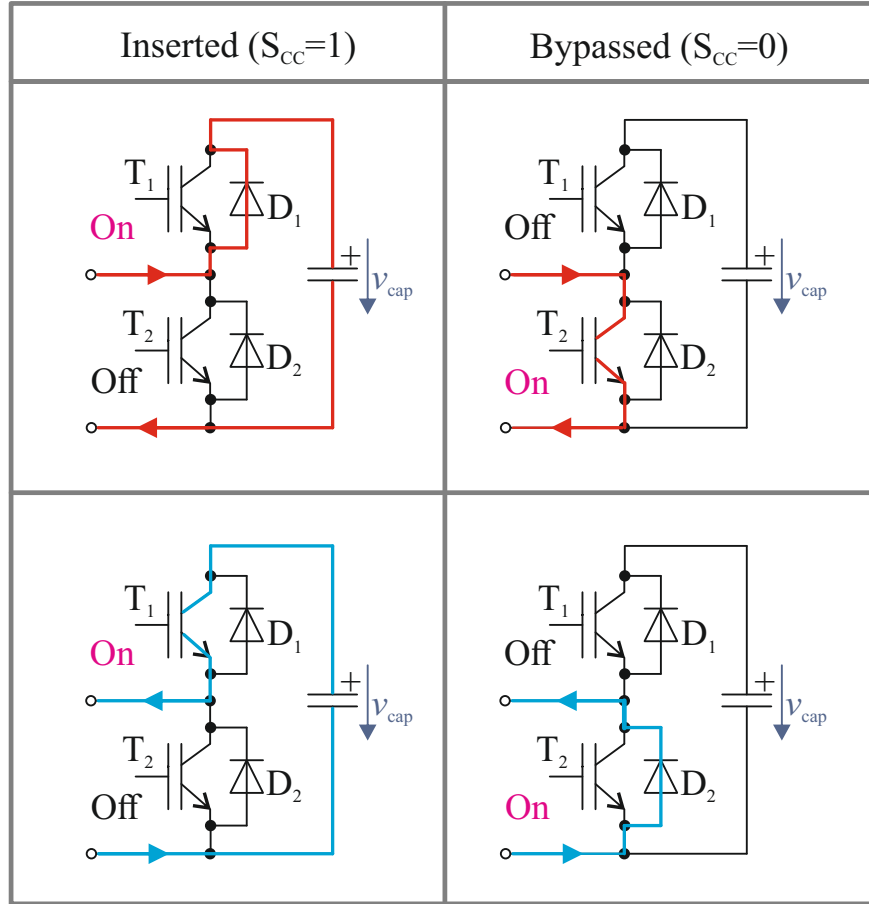
Figure 6.2: Current paths for one CC during normal MMC operation.

CC-SM

The conduction losses can be calculated based on the conduction paths and the loaded arm current. The conduction paths in CC configuration are illustrated in Fig. 6.2. During the positive wave of the arm current the semiconductors D_1 and T_2 are loaded. Instead, for the negative wave the semiconductors T_1 and D_2 are conducting the arm current.

The corresponding conduction losses $P_{loss,con}$ are approximated in Table 6.1. The forward voltages of the IGBT and diodes are defined as v_{ce} and v_f, respectively. Both voltages are influenced by the current load.

Table 6.1: Conduction losses in one CC.

S_{CC}	$i_{arm}(t)$	Conduction losses
1	positive	$P_{l,con,D1}(t) = v_{f,D1}(t, i_{arm}) \cdot i_{arm}(t)$
1	negative	$P_{l,con,T1}(t) = v_{ce,T1}(t, i_{arm}) \cdot i_{arm}(t)$
0	positive	$P_{l,con,T2}(t) = v_{ce,T2}(t, i_{arm}) \cdot i_{arm}(t)$
0	negative	$P_{l,con,D2}(t) = v_{f,D2}(t, i_{arm}) \cdot i_{arm}(t)$
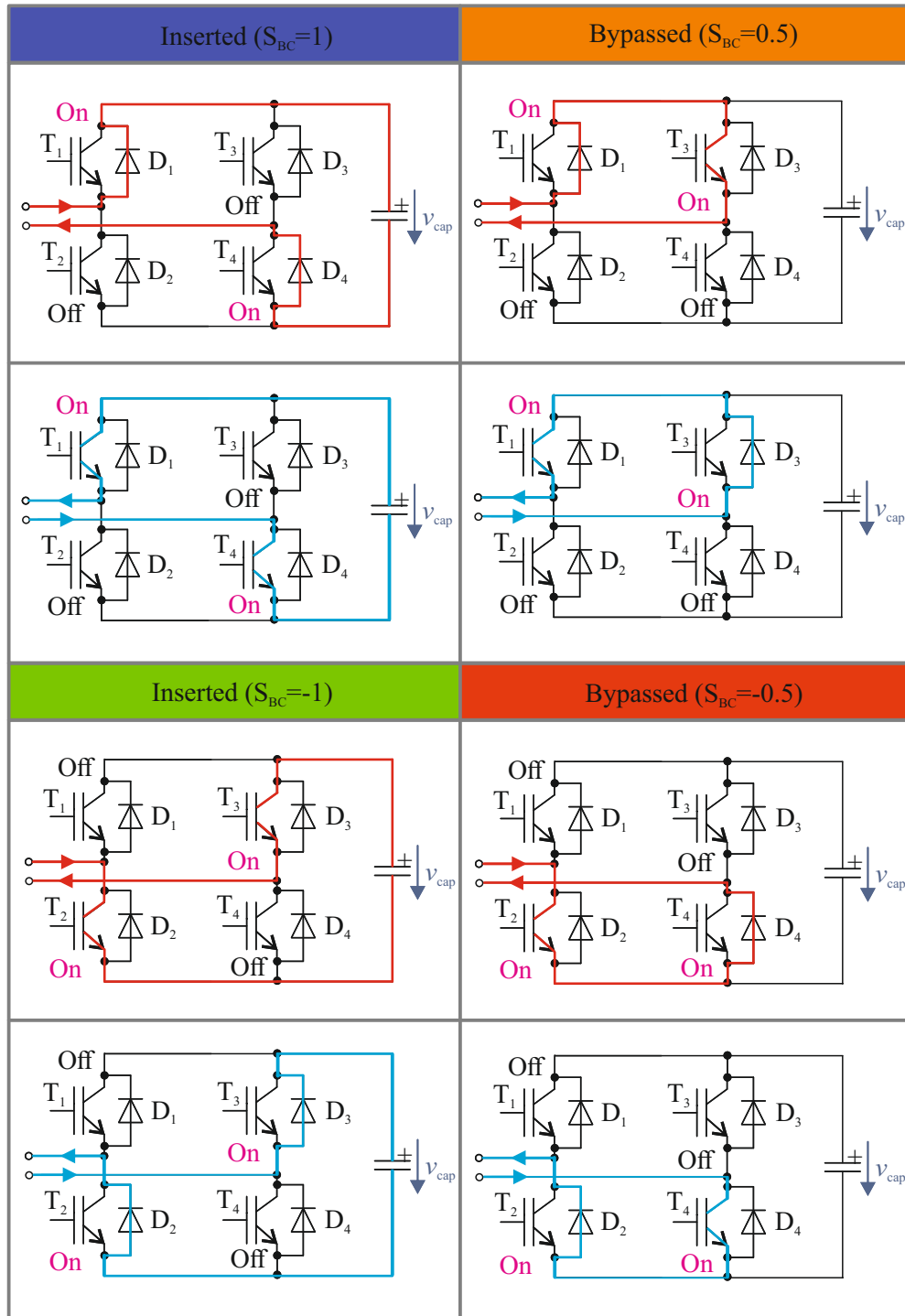
Figure 6.3: Current paths for one BC during normal MMC operation.

BC-SM

For the SMs in BC configuration the conduction paths are depicted in Fig. 6.3. For each of the eight switching states during normal operation two semiconductors are loaded. The corresponding semiconductor conduction losses are approximated in Table 6.2 in dependence from the switching state and the arm current direction.

Table 6.2: Conduction losses in one BC.

	S_{BC}	$i_{arm}(t)$	Conduction losses
	1	positive	$P_{l,con,D1}(t) = v_{f,D1}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,D4}(t) = v_{f,D4}(t,i_{arm}) \cdot i_{arm}(t)$
	1	negative	$P_{l,con,T1}(t) = v_{ce,T1}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,T4}(t) = v_{ce,T4}(t,i_{arm}) \cdot i_{arm}(t)$
	0.5	positive	$P_{l,con,D1}(t) = v_{ce,D1}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,T3}(t) = v_{ce,T3}(t,i_{arm}) \cdot i_{arm}(t)$
	0.5	negative	$P_{l,con,T1}(t) = v_{f,T1}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,D3}(t) = v_{f,D3}(t,i_{arm}) \cdot i_{arm}(t)$
	-0.5	positive	$P_{l,con,T2}(t) = v_{ce,T2}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,D4}(t) = v_{ce,D4}(t,i_{arm}) \cdot i_{arm}(t)$
	-0.5	negative	$P_{l,con,D2}(t) = v_{f,D2}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,T4}(t) = v_{f,T4}(t,i_{arm}) \cdot i_{arm}(t)$
	-1	positive	$P_{l,con,T2}(t) = v_{f,T2}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,T3}(t) = v_{f,T3}(t,i_{arm}) \cdot i_{arm}(t)$
	-1	negative	$P_{l,con,D2}(t) = v_{ce,D2}(t,i_{arm}) \cdot i_{arm}(t)$ $P_{l,con,D3}(t) = v_{ce,D3}(t,i_{arm}) \cdot i_{arm}(t)$

For the IGBTs the switching energies E_{sw} are taken into account, distinguishing between turning-on and turning-off energies $E_{sw,on}$ and $E_{sw,off}$, respectively. For the diodes the turning-off losses E_{rec} are considered, whereas turning-on losses can be neglected. All switching loss energies can be interpolated by the arm current and the applied voltage from the SM capacitors.

CC-MMC

The electrical behavior of an MMC STATCOM application is illustrated in Fig. 6.4 referring to Section 5.1. The IGBT module FF450R17IE4 from Infineon is considered, being rated with 1700 V breakdown voltage and for a nominal current of 450 A.
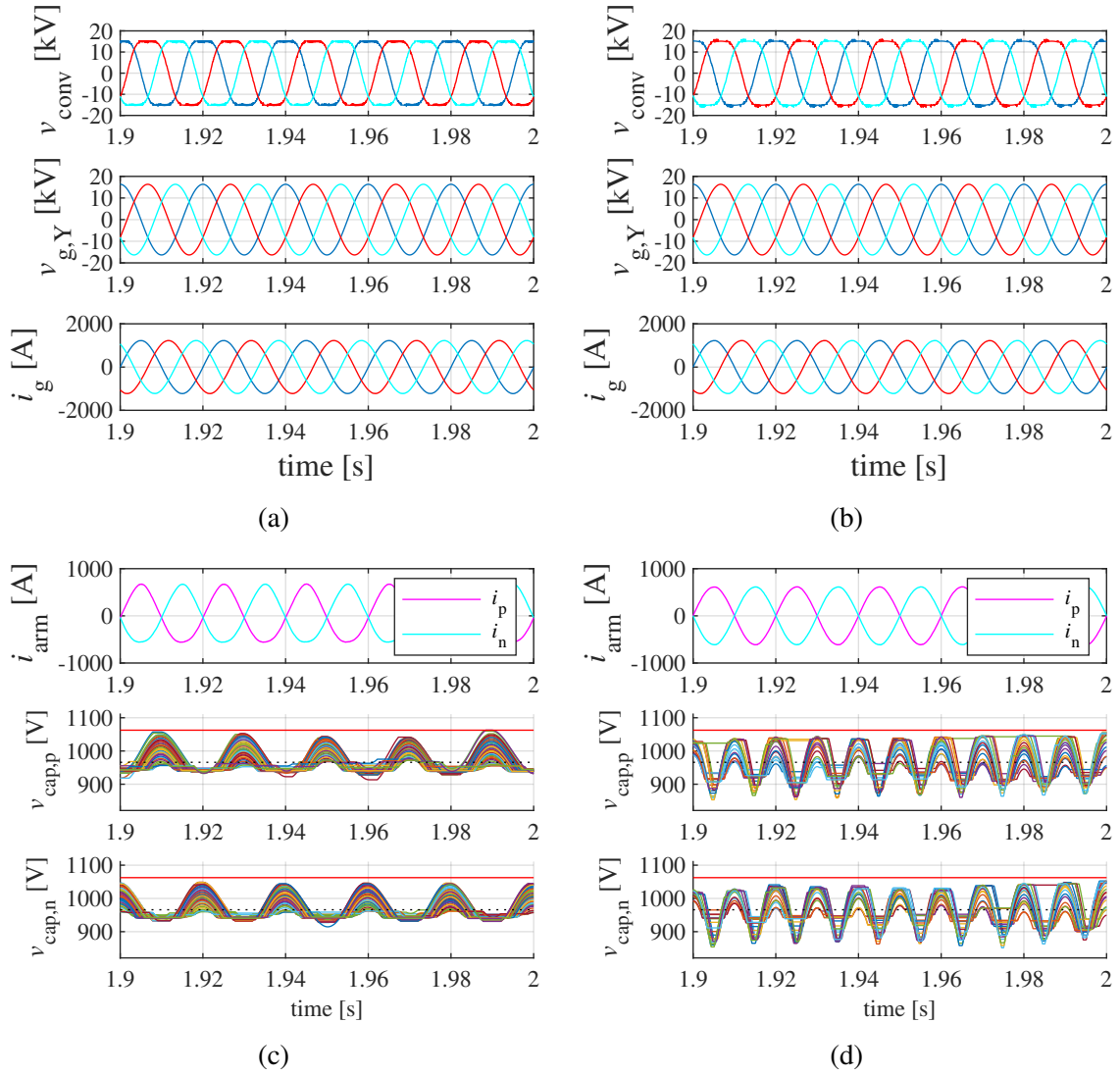
Figure 6.4: STATCOM operation ($Q_\mathrm{g} = 30\,\mathrm{Mvar}$): Grid-side behavior of the (a) CC-MMC and (b) BC-MMC. Arm currents and capacitor voltages (phase a) of the (c) CC-MMC and (d) BC-MMC.

The switching profile of one SM (no. 3) is exemplary shown in Fig. 6.5 with a very homogenous switching profile during the shown time interval. The SM is being switched on and switched off once during each grid period, corresponding to a fundamental switching frequency of 50 Hz. The conduction losses are distributed well among the different semiconductor devices in this case. However, during most of the time the switching profiles of the SMs are more inhomogeneous particularly due to the SM selection based on CVB algorithms as it will be shown in Section 6.3.
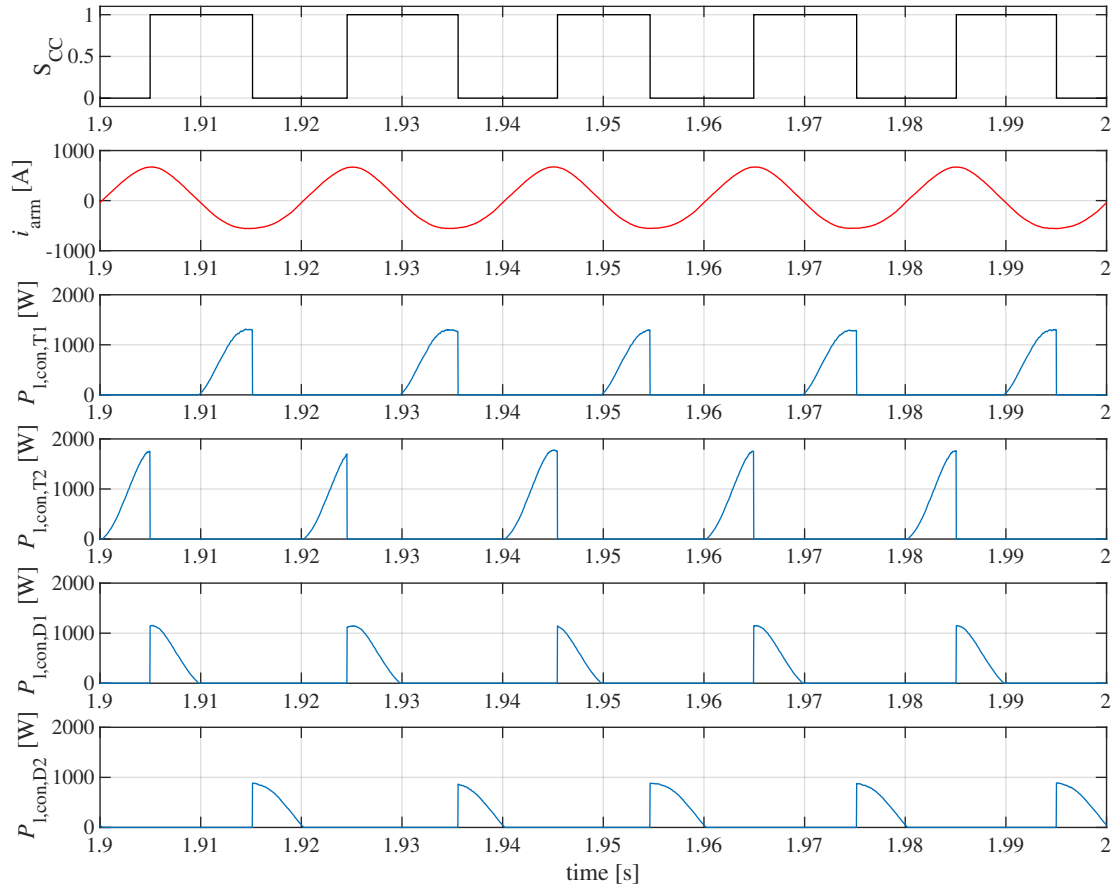
Figure 6.5: Switching profile (NLM) and semiconductor power losses for one CC-SM.

In Fig. 6.6 the instantaneous and averaged power losses in one MMC arm are illustrated. The power losses in the different semiconductor devices mainly depend on the insertion number and the arm current. The averaged semiconductor losses are calculated with ca. 29.65 kW in one arm, mainly driven by conduction losses of ca. 28.44 kW. The switching losses of ca. 1.22 kW are very low, being minimized by the NLM. The overall averaged losses are shared between the IGBTs and diodes with 17.72 kW and 11.93 kW, respectively.

The semiconductor losses of 29.65 kW in one arm are corresponding to 177.9 kW in the full MMC. This results in an inverter efficiency of around 99.4 % if the losses of the further equipment like drivers, cables and passive components are neglected.
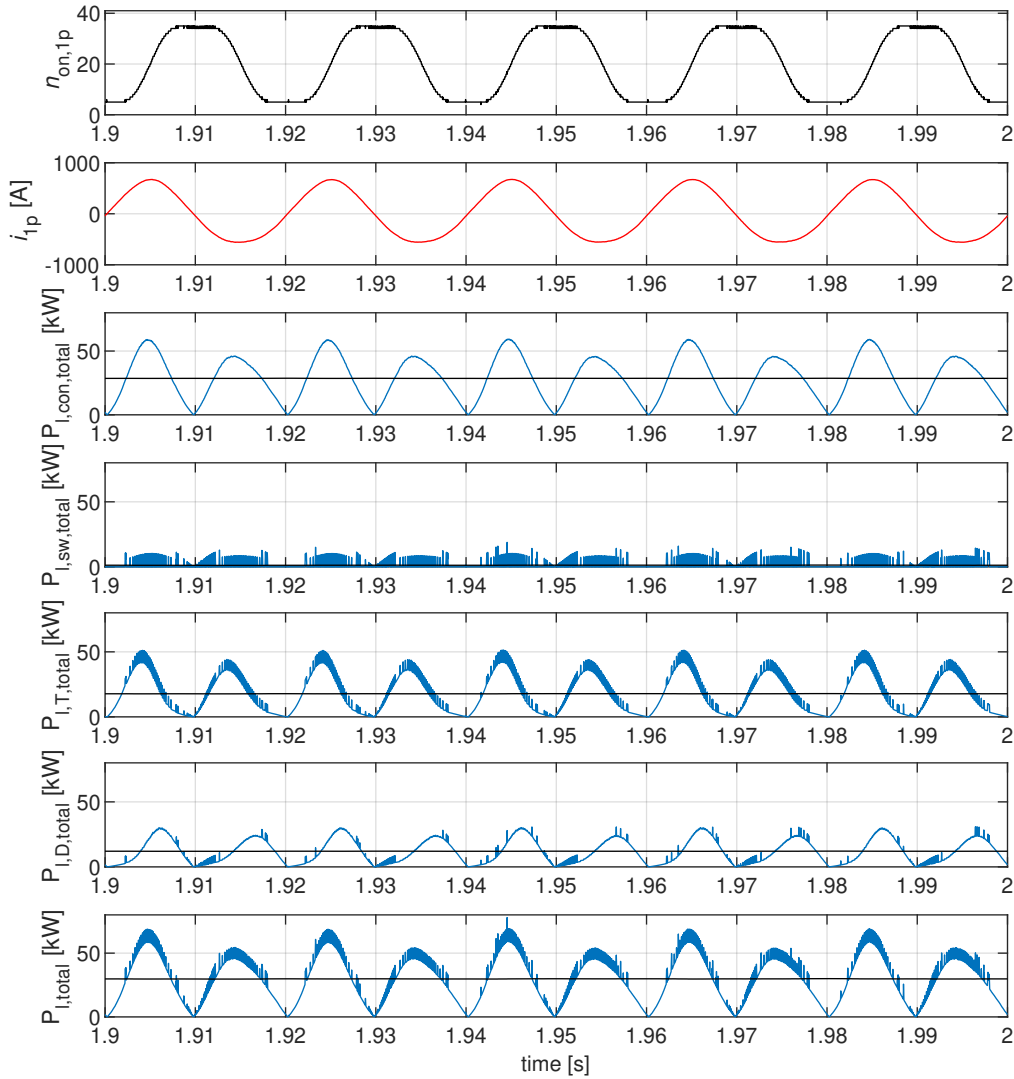
Figure 6.6: Switching profile (NLM) and semiconductor power losses for the CC-MMC.

BC-MMC

Instead, the semiconductor losses for one BC-SM are depicted in Fig. 6.7. The highlighted switching sequence is corresponding to the NLM sequence 1 in accordance with Section 3.1.2. In BC-SMs not only one but two semiconductors are always loaded by the arm current. However, the number of SMs can be reduced for the BC-MMC since the modulation range can be extended $(-1...1)$.

Also in this example the selected SM is showing a very homogenous switching profile during the shown time interval. Each semiconductor device is turning on and turning off one time per SM during each grid period. Again the switching pattern shows a very homogeneous case for good illustration. However, also for the BC-MMC applied CVB algorithms have a significant impact, acting on the switching profiles of each SM and its variety.
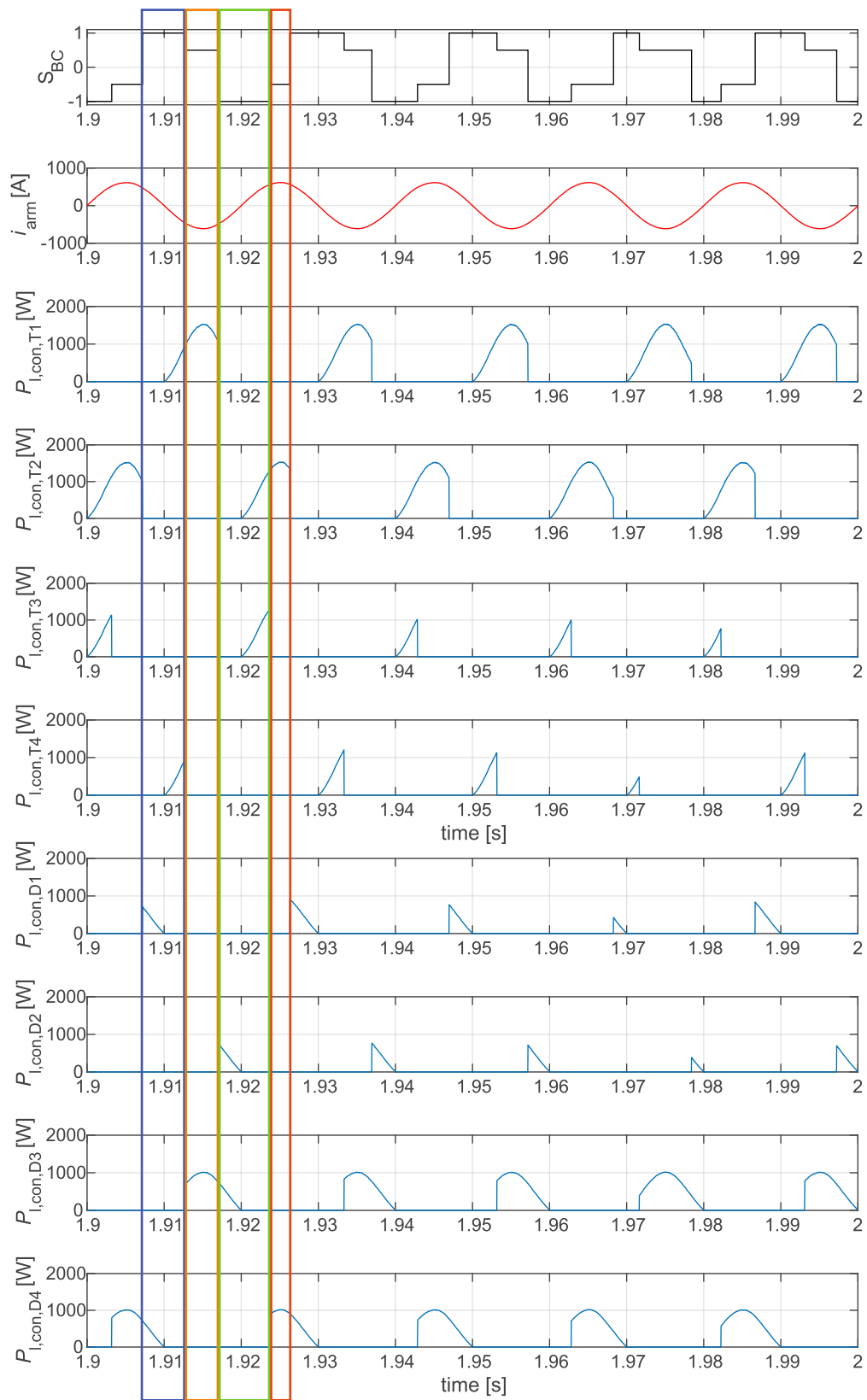
Figure 6.7: Switching profile (NLM, sequence 2) and semiconductor power losses for one BC-SM.
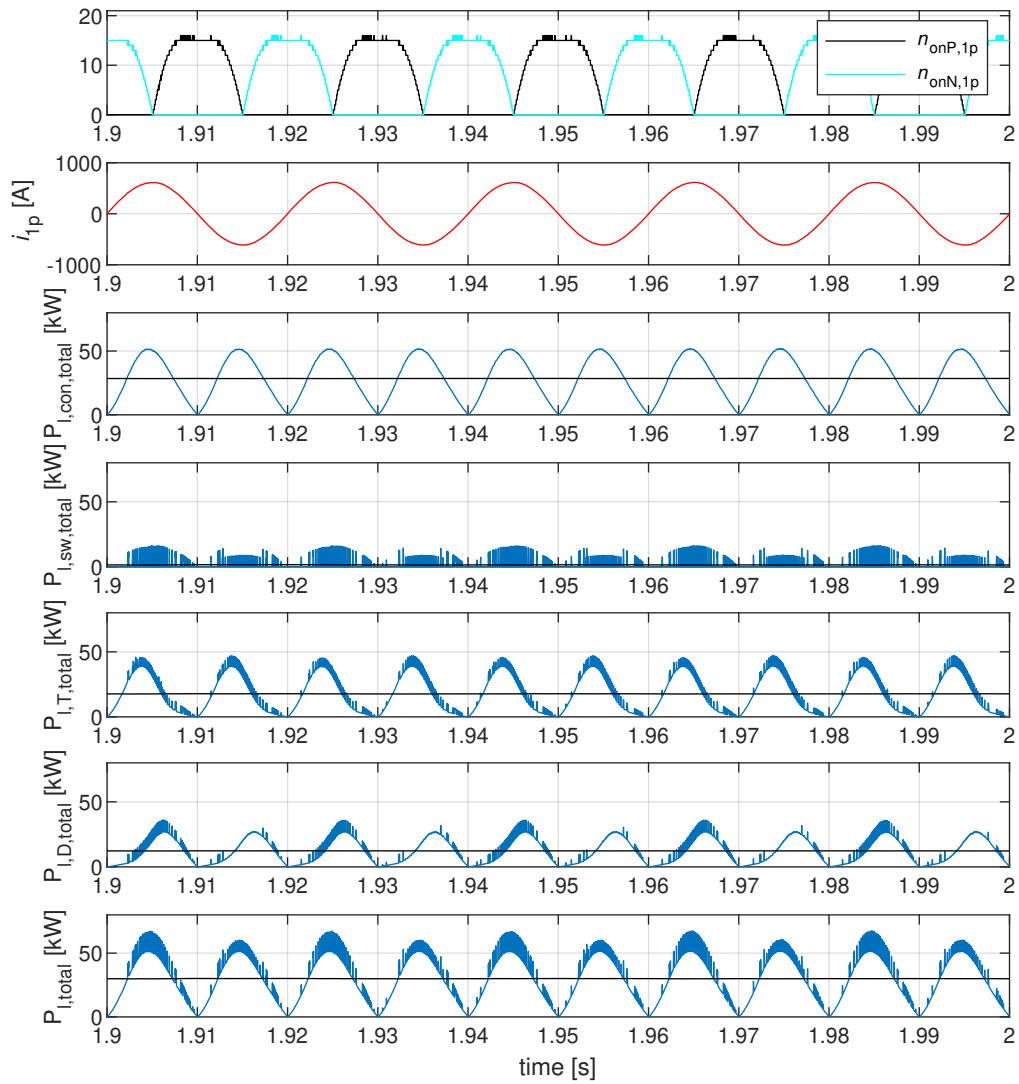
Figure 6.8: Switching profile (NLM, sequence 2) and semiconductor power losses for the BC-MMC.

The total losses of the BC-MMC are illustrated in Fig. 6.8. The doubled number of loaded semiconductor devices in each SM is more or less compensated by the reduced number of required SMs in terms of losses. The averaged total losses in one arm are calculated with 29.85 kW, being divided into conduction losses of 28.35 kW and minimized switching losses of 1.5 kW. Averaged power losses of 17.6 kW and 12.24 kW occur in the IGBTs and diodes, respectively. The overall losses in the inverters can be summed up to 179.1 kW and again a very high efficiency of around 99.4 % is achieved based on the semiconductor losses.
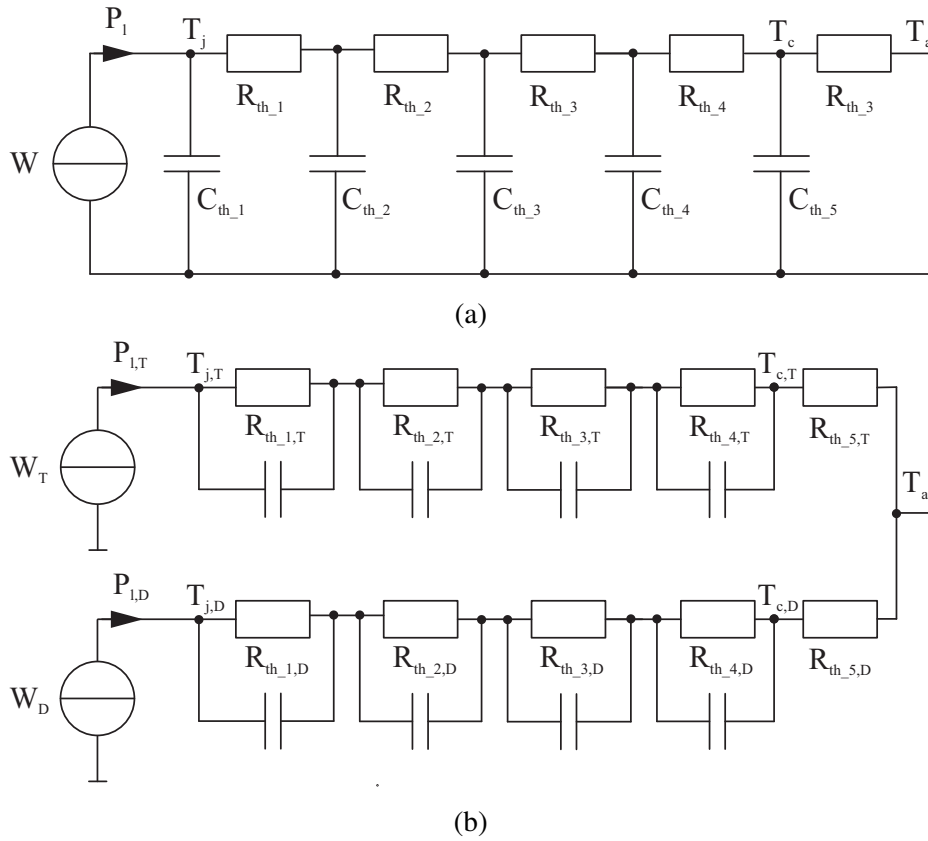
Figure 6.9: Thermal equivalent circuits: (a) Cauer model for one semiconductor device with cooling system. (b) Foster model for one IGBT module with cooling system.

For the presented HVDC transmission application from Section 5.2.2 the IGBT module CM1200HC-90R from Mitsubishi is applied. It is rated for a nominal current of 1200 A and provides a breakdown voltage of 4500 V. The power losses in one arm are approximated with 395.3 kW for active power supply (300 MW, $\cos\varphi = 0.95$) and pure reactive power supply (300 Mvar, $\cos\varphi = 0$) with 297.5 kW. The averaged SM switching frequency has been minimized to 53 Hz and 51 Hz, respectively. The total semiconductor losses are around 2371.8 kW and 1785 kW. For the active power supply of 300 MW, this corresponds to an efficiency of around 99.2 %.

6.1.2 Thermal Behavior

The semiconductor power losses are mainly dissipated by heat. The physical thermal Cauer model for one semiconductor device is depicted in Fig. 6.9a. The instantaneous power losses are represented by a current flow, facing several heat resistances. The voltage drops across these resistances represent the temperature difference between different layers or geometries. Temperature changes are damped due to specific heat capacities of the materials, being represented by thermal capacitances. The temperature T_j represents the junction temperature and T_c the case temperature of the device. An additional thermal resistance is applied for the water cooling system.

The Cauer model can be transformed into a Foster model as depicted in Fig. 6.9b for one complete IGBT module. The thermal impedances of the IGBTs and the diodes from junction to case can be applied from the datasheets. The equivalent thermal resistances from the cases to the heatsink are approximated with $R_{\mathrm{th,CH,T}} = 24\mathrm{K} \cdot \mathrm{kW}^{-1}$ and $R_{\mathrm{th,CH,D}} = 46\mathrm{K} \cdot \mathrm{kW}^{-1}$. Furthermore, the thermal coupling between each IGBT and its anti-parallel diode is taken into account by a common thermal resistance ($R_{\mathrm{th,coupl}} = 10\mathrm{K} \cdot \mathrm{kW}^{-1}$). Since the time constants of the cooling system are very high, a constant temperature difference between cooling system and the case of the device is assumed. All semiconductor devices are cooled by water with a cooling temperature of $T_{\mathrm{a}} = 40\,^{\circ}\mathrm{C}$.

The temperature behavior of the CC-MMC and of the BC-MMC are depicted in Fig. 6.10 for the 30 MVA STATCOM application, covering all semiconductor devices in one arm. The cyclic behavior of the power losses is linked to thermal cycles in the semiconductor devices, being predominant at the grid frequency of 50 Hz.

For the CC-MMC the highest junction temperatures occur in diode D_1 at nominal reactive power of 30 Mvar. Maximum temperatures of around $100\,^{\circ}\mathrm{C}$ and thermal ripples of almost 20 K occur in the system. It becomes visible that there is a significant spread for the semiconductor devices among the different SMs. The most stressed SMs at a specific time are mainly determined by stochastic effects as long as an ideal system is considered. Taking into account asymmetries within the system due to manufacturing or aging processes, the maximum temperatures and thermal cycles would be even higher. However, already for the ideal case a high potential for thermal optimization becomes obvious.

For the BC-MMC the highest junction temperatures can be seen in IGBT T_1 at around $95\,^{\circ}\mathrm{C}$ for nominal power ($Q_{\mathrm{g}} = 30\,\mathrm{Mvar}$). The thermal cycles are smaller and below 20 K, since the semiconductor devices in one BC are more frequently changed. For the NLM sequence 1 the thermal cycles occur in semiconductors T_1, T_2, D_1 and D_2. These semiconductor devices are much more loaded than the semiconductor devices T_3, T_4, D_3 and D_4. Since the temperature distribution among the semiconductor devices is very inhomogenious, also for the BC-MMC there is a high potential for thermal optimization.

6.2 Experimental Bench

In addition to the theoretical analysis, practical evaluation is required for the electrical and thermal behavior of the most crucial components. Based on the real electrical and thermal profiles the design of the semiconductor devices and the capacitor storages can be optimized in accordance with the aimed nominal temperatures and expected lifetimes, being aligned with scheduled maintenance intervals. However, for modular structures as the MMC with hundreds or even thousands of semiconductor devices and storage capacitors, the building of full converters just for testing would be neither practical nor economical. However, after commissioning the change of components in the system is not desired. Furthermore, existing systems cannot cover all requirements for future systems due to different grid conditions, voltage levels, power requirements, load profiles, control strategies or SM configurations.

(a)

(b)
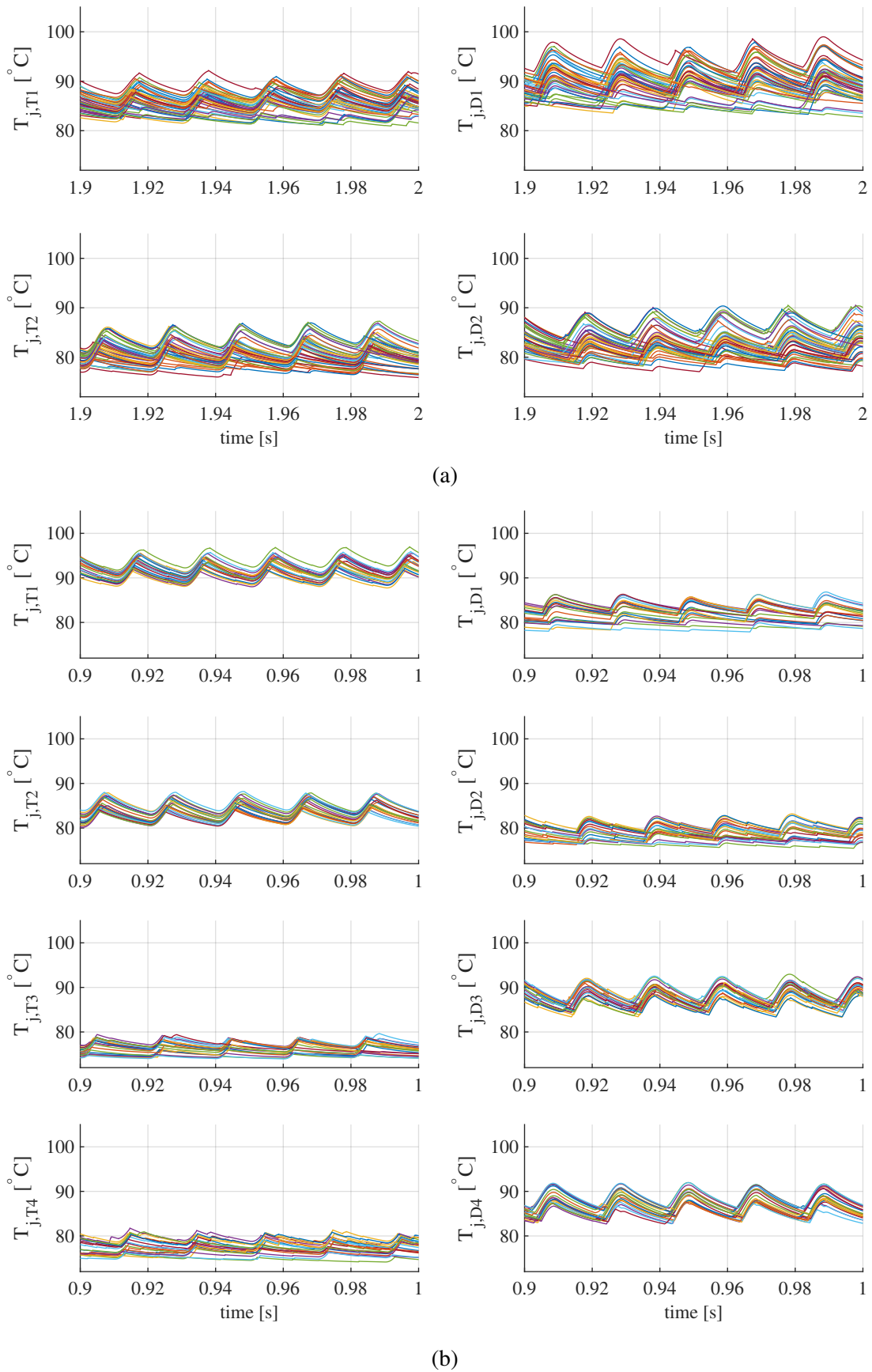
Figure 6.10: Thermal behavior of all the semiconductor devices (one arm): (a) CC-MMC. (b) BC-MMC (NLM, sequence 2).
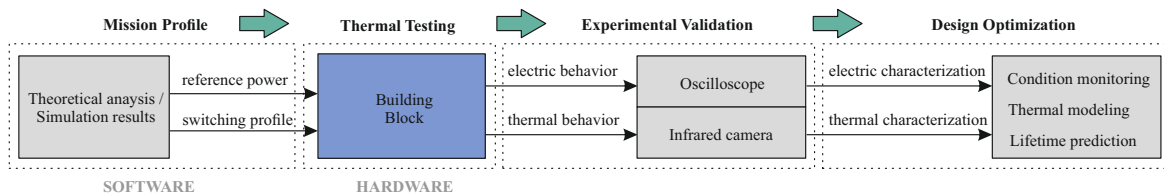
Figure 6.11: Block scheme of the experimental bench to emulate building blocks of modular power converters.

These practical limitations become even stronger if the chip temperatures inside all semiconductor devices need to be measured in high resolution (in space and time) to detect hotspots and thermal cycles. However, this information is required for an economical design and to evaluate overload capabilities and lifetime limitations. The overall saving potential in terms of component size and costs is huge due to the very high number of components. By means of cycling tests the system design can be optimized on SM and component level for longer lifetimes. Based on cycling tests lifetime models can be improved as well to extend and to optimally adapt the scheduled maintenance intervals. Furthermore, thermal models for simulations and real-time condition monitoring can be optimized based on the available measurement data. For these purposes, a universal experimental bench is introduced.

6.2.1 Basic Concept

The experimental bench, being introduced in this section for safe and economical test procedures, is taking benefit from the modular and redundant structure of modular inverters. Due to the redundant structure of big modular inverter systems the focus for evaluation can be put on its building blocks, e.g. CC-SMs or BC-SMs. These building blocks can be tested under real mission profiles, monitoring both the electrical and the thermal behavior of the semiconductor devices.

The basic concept is highlighted in Fig. 6.11. Based on theoretical analysis and simulation results the mission profile of each cell can be derived depending on the operation point and on the applied modulation technique for the software. The corresponding load profiles and switching patterns can be applied to such a building block for electrical and thermal testing of the hardware.

By the emulation of each single brick of the inverter the behavior of the full modular inverter can be evaluated under realistic conditions. The electrical and thermal behavior of each building block and of each semiconductor device can be emulated in any operation conditions for improved thermal modeling and condition monitoring, a more economical design, to detect hidden reserves for overload capabilities, to enhance component lifetimes and to detect aging mechanisms by cycle tests. The impact of advanced control methods can be taken into account as well. Also testing and optimization of single SMs under severe conditions becomes possible for evaluating temperature hotspots, tolerable operation ranges and withstand capabilities.
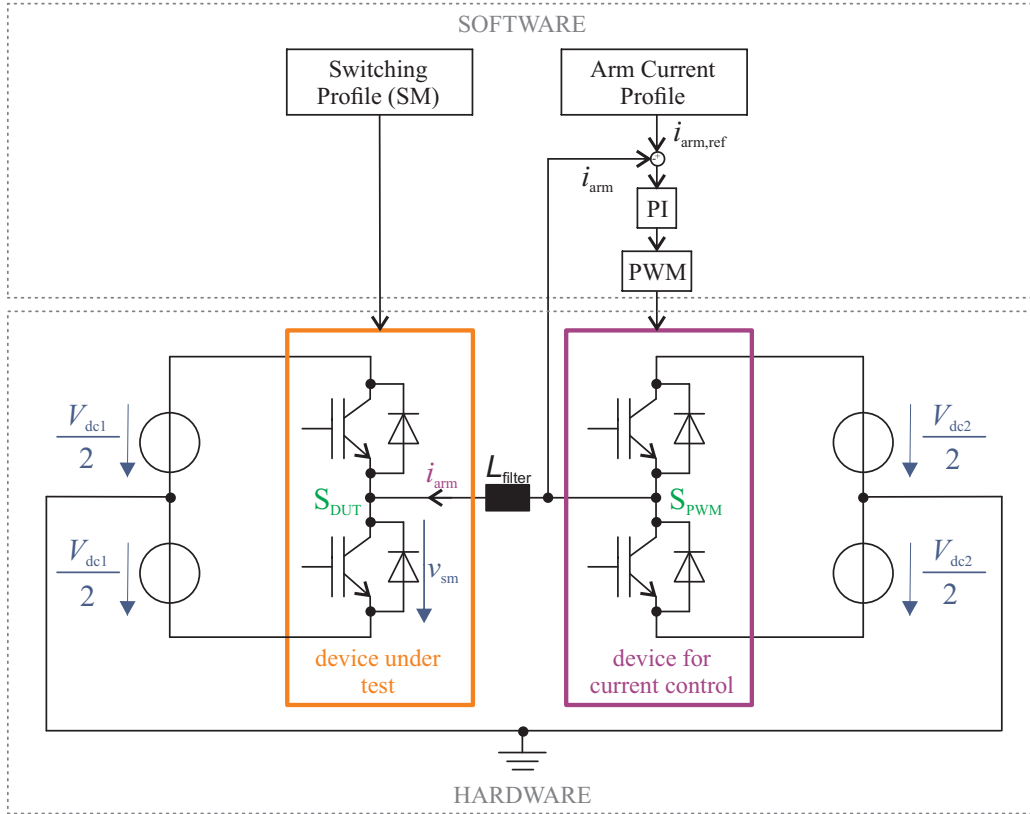
Figure 6.12: Experimental bench for electrical and thermal evaluation of one MMC SM.

Table 6.3: Switching states of the experimental bench ($V_{dc2} > V_{dc1}$).

S_{DUT}	S_{PWM}	v_L	i_L
0	0	$-\frac{V_{dc1}}{2} - \frac{V_{dc2}}{2} < 0$	↓
0	1	$-\frac{V_{dc1}}{2} + \frac{V_{dc2}}{2} > 0$	↑
1	0	$\frac{V_{dc1}}{2} + \frac{V_{dc2}}{2} > 0$	↑
1	1	$\frac{V_{dc1}}{2} - \frac{V_{dc2}}{2} < 0$	↓

The simplified power circuit of the experimental bench is depicted in Fig. 6.12. One half-bridge represents the device-under test (DUT) and another half-bridge is applied to control the arm current load. The arm current can be properly controlled by a PI controller if the applied DC voltage V_{dc2} is higher than V_{dc1}. In this way the polarity of the voltage across the inductance v_L can be changed by the controllable switching state S_{DUT}. All available switching states of the introduced experimental bench are summarized in Table 6.3. Independently from the switching state of the DUT the polarity of the voltage and the current slope can be turned for flexible current control.

The challenge to even control the DC component of the arm current on SM level is potentially solved by the introduced experimental bench. However, active power would be transmitted by the controlled DC component. For instance, if the DC component is positive, the DC source V_{dc1} needs to absorb energy from the DC source V_{dc2}. Accordingly, the use of bidirectional DC sources would be required for safe operation.
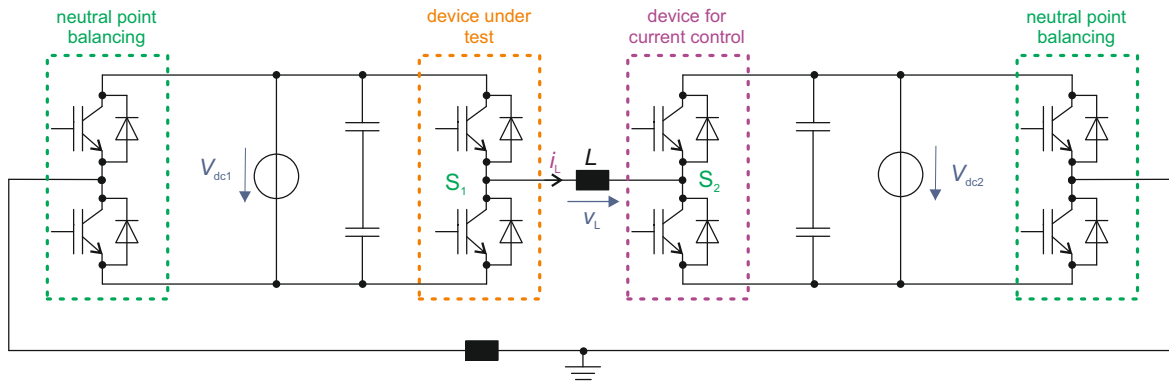
Figure 6.13: Experimental bench for evaluation of one SM, detailed circuit.

Instead, the problem can be also solved by a proper neutral point balancing. For this purpose, an additional half-bridge block is connected to each DC link where the midpoints of both half-bridges are connected to each other, as illustrated in Fig. 6.13. Both half-bridges are operated synchronously at high switching frequencies (e.g. $f_{sw} = 10\,\text{kHz}$) in block operation, corresponding to a duty cycle of 50 %. In this way, the virtual midpoints of the DC links and the powers between the DC sources can be balanced in an appropriate way.

Additionally to the introduced neutral point balancing, the paralleling of semiconductor chips or half-bridge circuits can be useful for the auxiliary units for safe and reliable operation. Relying on a very symmetrical hardware design, also high arm currents can be splitted among the semiconductor devices even at high switching frequencies. Consequently, the DUT can be operated and monitored even at very high loads at limited stress for the outer half-bridge blocks.

6.2.2 Practical Realization

The realized laboratory prototype is depicted in Fig. 6.14 and its main system data summarized in Table 6.4. The open 1200 V IGBT module *DP25F1200T101666* from Danfoss is applied as a building block to emulate the behavior of one CC-SM. The module is rated for 1200 V and 25 A and therefore reduced compared to standard IGBT modules for MV or HV applications. However, the usage of smaller devices is not a critical issue since the qualitative behavior of different modules is highly correlated. Nevertheless, the experimental bench also allows to apply the real semiconductor devices from MV or HV applications with a multiple power capability.

The experimental bench is fed by a dSPACE system and the switching pattern and the arm current load provided from theoretical analysis and simulation studies. Both the electrical and thermal behavior of each SM can be investigated. For evaluation of both the electrical mission profiles and the thermal cycles oscilloscopes and an infrared camera are available, providing high accuracy within a wide frequency bandwidth. For evaluation of both the electrical mission profiles and the thermal cycles oscilloscopes and the IR camera Image IR from InfraTec are connected, providing high accuracy within a wide bandwidth. In this

(a) (b)
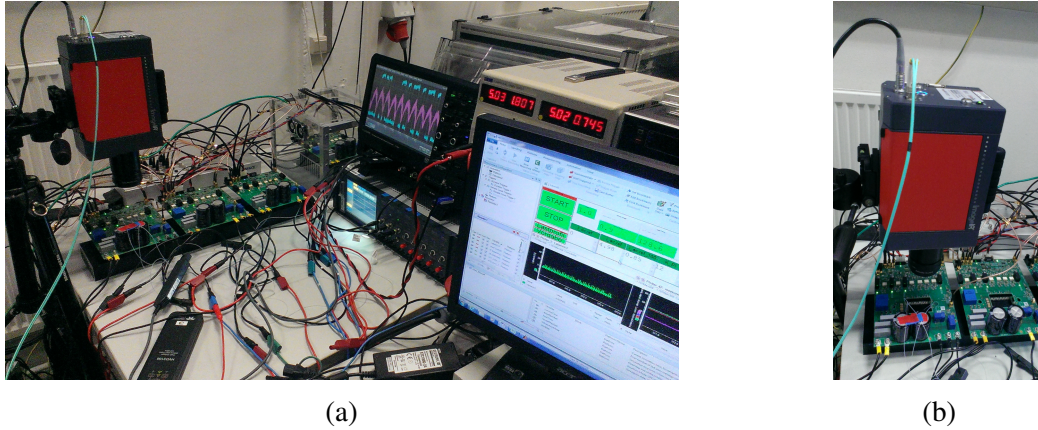
Figure 6.14: Experimental bench: (a) Setup, at a glance. (b) Setup, zoom.

Table 6.4: System data of the experimental bench.

Building block:	Half-bridge cells
IGBT module:	*DP25F1200T101666*
Breakdown voltage:	1200 V
DC-link voltage:	max. 600 V
Nominal current (DC):	max. 75 A
Switching frequency:	max. 20 kHz
IR camera:	InfraTec Image IR
Optic sensors:	OPSens PSR-100

way, the SM voltage and the current waveforms can be recorded as well as the temperature profiles of the full IGBT module. The IR camera cannot only resolve thermal cycles at a very high bandwidth, but also provides spatial resolution, revealing critical hotspots related to the hardware design.

Furthermore, fiber optic sensors can be applied to identify the temperatures at one or at several specific measuring points, e.g. for a high number of components at different locations. However, each fiber optic sensor is restricted to a certain measuring point and limited in the bandwidth, damping the detected thermal cycles.

6.3 Thermal Management of Semiconductor Devices

As highlighted in the section before there is a high motivation for an effective thermal management in MMC applications. The following section puts the focus on the thermal management of the semiconductor devices. Based on the introduced thermal models real-time modeling of the semiconductor devices become possible and can be further tuned and optimized by the suggested experimental bench.

It is worth to be mentioned that fully symmetrical systems are considered in this section, without taking into account any component parameter variations. Parameter tolerances in

the components (e.g. semiconductors, capacitors, cooling system) due to manufacturing and aging processes would further increase the spread in the temperatures, making the demand of intelligent solutions even higher for practical applications [137]. Different factors can further increase thermal mismatches in practical applications e.g. due to different assembling and pressures, environmental impacts, thermal couplings depending on the geometries. Potentially, for very accurate thermal modeling, these phenomena can be also taken into account. However, the complexity and the computation effort need to be limited to a certain extent, depending on the installed computation power and the number of SMs to ensure real-time estimation. In this way, the use of additional temperature sensors for hundreds or even thousands of semiconductor devices can be avoided.

6.3.1 CC-MMC

The CVB is one of the central parts for proper control and operation of the MMC, being usually decoupled from the modulator itself. CVB algorithms are not only balancing the state of charge of the capacitors but also the thermal stress between the SMs up to a certain degree. Due to the charging and discharging processes of the capacitors the turn-on times will be usually automatically limited by the CVB algorithms. However, particularly for modulation techniques linked to low switching frequencies the switching profiles can be very inhomogeneous, also linked to relatively long turn-on times. Furthermore, CVB algorithms are kind of blind for switched-off SMs because their states of charge remain approximately constant. Accordingly, one SM can be bypassed for longer time, linked to conduction losses and high stress for the semiconductors T_2 and D_2. These phenomena occur at all power factors and lead to a high spread in the semiconductor stress among the SMs [31], [138]. These effects become particularly strong at low power factors as demonstrated in Section 6.1.2 where conventional sorting algorithms with limited number of commutations are not effective for low-frequency modulation techniques as the NLM.

For the thermal management of the semiconductor devices a thermal balancing algorithm is proposed. Within each SM there are two events for which the conduction losses can be shifted between the semiconductor devices. On the one hand a change in the arm current direction shifts the conduction losses between the IGBT and its anti-parallel diode. However, the arm current waveform is mainly determined by the operation point and the related grid current waveform. The arm current can also be manipulated by the circulating current, however only within limited ranges and potentially causing additional losses in the system. On the other hand with the help of the switching state of each SM the conduction losses can be shifted between upper and lower semiconductor devices. Therefore, the required switching operations provided by the modulator can be used for both the balancing of capacitor voltages and of the semiconductor junction temperatures for multi-objective optimization just by available redundant switching states.

Table 6.5: Approach of advanced submodule balancing (chopper-cells) by minimization of cost functions.

i_{arm}	Switching on $(0 \rightarrow 1)$	Switching off $(1 \rightarrow 0)$
positive	$\min\{c_1\}$	$\min\{c_2\}$
negative	$\min\{c_3\}$	$\min\{c_4\}$

For the optimization of the capacitor voltages and the temperatures of each semiconductor devices, these quantities need to be monitored and stored in arrays as indicated in (6.1)-(6.2). The capacitor voltages are usually measured for safe operation of the system. Instead, the temperatures can be modeled by the available system information as shown in Section 6.1.2. Additional temperature sensors are applicable to take into account possible asymmetries and environmental impacts. However, the high amount of sensors would be linked to high costs and high communication effort due to the high number of semiconductor devices.

$$\vec{v}_{\text{cap}} = \begin{pmatrix} v_{\text{cap},1} \\ v_{\text{cap},2} \\ ... \\ v_{\text{cap,N}} \end{pmatrix} \tag{6.1}$$

$$\vec{T}_{\text{j,T1}} = \begin{pmatrix} T_{\text{j,T1},1} \\ T_{\text{j,T1},2} \\ ... \\ T_{\text{j,T1,N}} \end{pmatrix}, \ \vec{T}_{\text{j,T2}} = \begin{pmatrix} T_{\text{j,T2},1} \\ T_{\text{j,T2},2} \\ ... \\ T_{\text{J,T2,N}} \end{pmatrix}, \ \vec{T}_{\text{j,D1}} = \begin{pmatrix} T_{\text{j,D1},1} \\ T_{\text{j,D1},2} \\ ... \\ T_{\text{j,D1,N}} \end{pmatrix}, \ \vec{T}_{\text{j,D2}} = \begin{pmatrix} T_{\text{j,D2},1} \\ T_{\text{j,D2},2} \\ ... \\ T_{\text{j,D2,N}} \end{pmatrix} \tag{6.2}$$

The semiconductor junction temperatures can be seen as one suitable and powerful optimization parameters for a reliable MMC system. The optimization of the capacitor voltages and the semiconductor junction temperatures can be combined by multi-objective cost functions. As a first step the conventional CVB algorithm can be realized in this way. For minimum number of commutations the CVB should only become active if the number of inserted SMs needs to be increased or reduced. Furthermore, for the CVB the arm current direction is crucial for the charging processes. Four possible events need to be considered to decide about the proper selection of the SM(s) to be inserted or bypassed. These four events are summarized in Table 6.5.

For each event an own cost function can be assigned. Four cost functions are defined in (6.3)-(6.6). The cost function c_1 becomes minimal for the SM with the lowest capacitor voltage and is equivalent to c_4. Instead, the cost function c_2 becomes minimal for the SM with the highest capacitor voltage and is equivalent to c_3. Depending on the requested switching
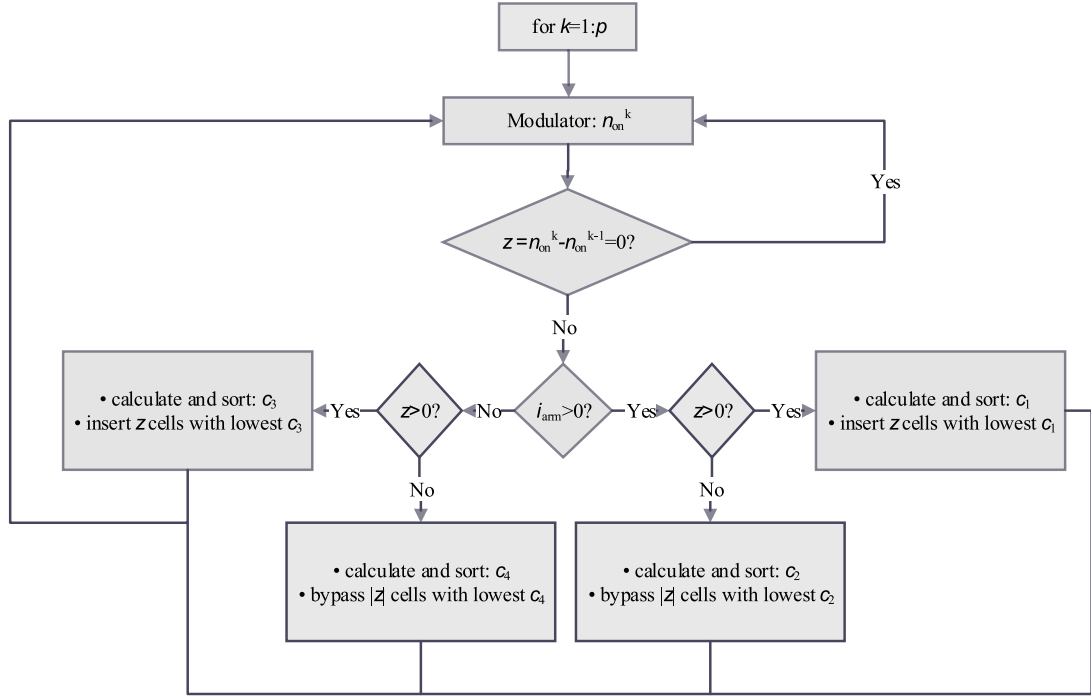
Figure 6.15: Simplified flowchart for SM selection in each arm based on cost functions for multi-objective optimization (p: number of iterations, z: auxiliary variable).

event and the arm current direction the cost functions need to be minimized according to Table 6.5.

$$c_1 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) \qquad (6.3) \qquad\qquad c_3 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) \qquad (6.5)$$

$$c_2 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) \qquad (6.4) \qquad\qquad c_4 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) \qquad (6.6)$$

A simplified flowchart is depicted in Fig. 6.15 where all relevant actions are summarized. By the parameter z the updated number of inserted SMs is compared with the number from the previous iteration. For minimized number of commutations the CVB only becomes active if this number has changed and z is unequal to 0. In accordance with Table 6.5 the SMs will be selected based on the cost functions in (6.3)-(6.6).

Based on the introduced cost functions multi-objective optimizations become possible. For an effective thermal management of the semiconductor devices the junction temperatures can be linked to the cost functions. The suggested approach is summarized in Table 6.6. SMs, which need to be inserted, should show low junction temperatures in the semiconductor devices D_1 or T_1, depending on the arm current direction. Instead SMs, which need to be bypassed, should show low junction temperatures in the devices T_2 or D_2 to avoid overtemperatures.

This thermal management approach for the semiconductor devices can be included into the conventional CVB algorithm. For this purpose, the cost functions from (6.3)-(6.6) can be extended according to (6.11)-(6.14). By minimizing the obtained functions according to Table 6.5 and the flowchart in Fig. 6.15 the SM selection will be optimized based on both the

Table 6.6: Basic principle for thermal management of semiconductor devices.

$n_{\mathrm{on}}^{\mathrm{k}} - n_{\mathrm{on}}^{\mathrm{k-1}}$	i_{arm}	Action
positive	> 0	insert SM(s) with lowest temperature in D_1
positive	< 0	insert SM(s) with lowest temperature in T_1
negative	> 0	bypass SM(s) with lowest temperature in T_2
negative	< 0	bypass SM(s) with lowest temperature in D_2

capacitor voltages and the semiconductor junction temperatures. For proper integration of the thermal management inside the CVB the weighting factors need to be selected carefully to achieve a similar weighting between the capacitor voltages and the thermal management. Due to stability issues the multi-objective optimization of several critical control parameters by simple weighting factors is very challenging. For instance, this would be the case for combining a direct power control on the AC side with the DC-side control in one single cost function.

Instead, the thermal balancing of the semiconductor temperatures is not mandatory for safe and stable operation of the system since the junction temperatures are already balanced up to a certain degree by the CVB. Accordingly, the weighting factor can be selected in a very conservative way, even close to 0. The impact of the thermal management on the CVB itself is limited, also due to the high inertia provided by the SM energy storages. Additional safety measures are provided by software, e.g. by replacing the SMs which are close to the operating limit. Furthermore, the weighting factors can be tuned for different conditions and different operation points. Potentially, also additional online tuning criteria can be defined, e.g. the spread in the capacitor voltages. The introduced approach can be applied to all classical modulation techniques with decoupled CVB algorithms.

$$c_1 = (v_{\mathrm{cap}} - \min\{v_{\mathrm{cap}}\}) + \alpha_{\mathrm{D1}}(T_{\mathrm{j,D1}} - \min\{T_{\mathrm{j,D1}}\}) \tag{6.7}$$

$$c_2 = (\max\{v_{\mathrm{cap}}\} - v_{\mathrm{cap}}) + \alpha_{\mathrm{T2}}(T_{\mathrm{j,T2}} - \min\{T_{\mathrm{j,T2}}\}) \tag{6.8}$$

$$c_3 = (\max\{v_{\mathrm{cap}}\} - v_{\mathrm{cap}}) + \alpha_{\mathrm{T1}}(T_{\mathrm{j,T1}} - \min\{T_{\mathrm{j,T1}}\}) \tag{6.9}$$

$$c_4 = (v_{\mathrm{cap}} - \min\{v_{\mathrm{cap}}\}) + \alpha_{\mathrm{D2}}(T_{\mathrm{j,D2}} - \min\{T_{\mathrm{j,D2}}\}) \tag{6.10}$$

For further investigations the weighting factors α are set constant to $50\,\mathrm{V \cdot K^{-1}}$ for all cost functions. This weighting factor corresponds to a realistic temperature range of around $15\,\mathrm{K}$. Both the benchmark case from Section 6.1.2 with standard CVB and the optimized case with included thermal management for the semiconductor devices are compared in Fig. 6.16. The maximum temperatures which can occur in semiconductor devices have been significantly reduced. Furthermore, the thermal cycles have been more than halved, liming the thermo-mechanical stress inside the semiconductor devices.
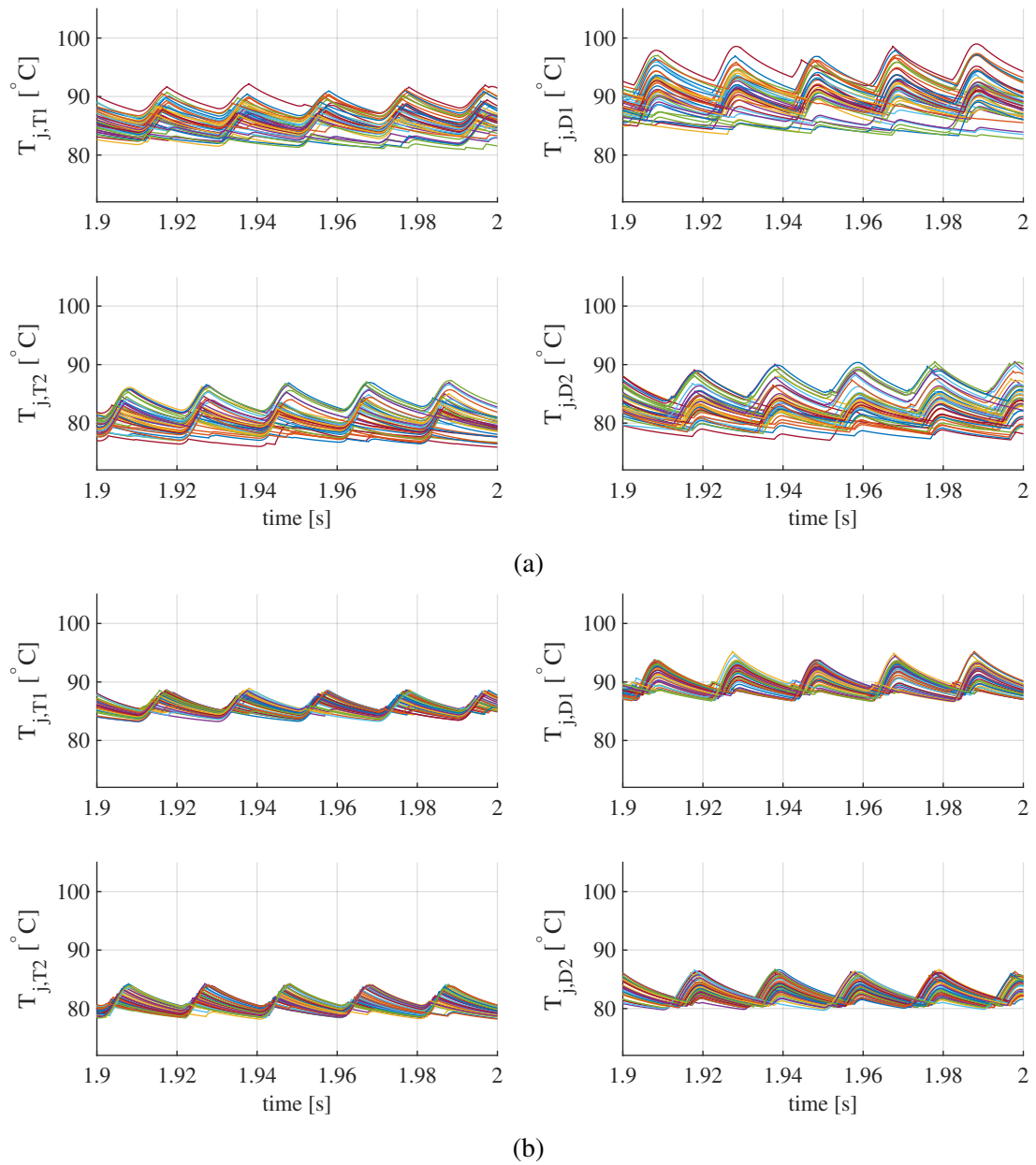
Figure 6.16: Thermal behavior of the CC-MMC (STATCOM, Q_g=30 Mvar): (a) Conventional CVB. (b) Optimized SM selection by thermal management.
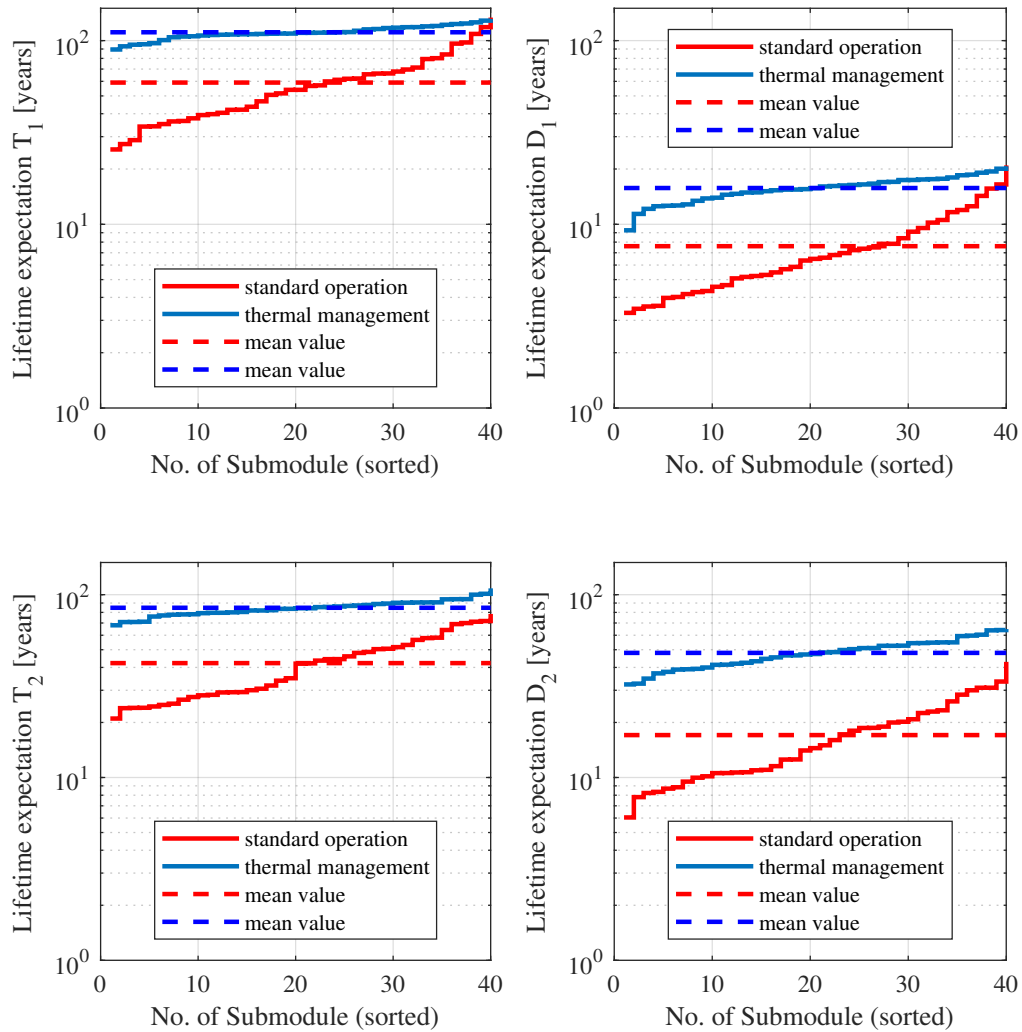
Figure 6.17: Semiconductor lifetime expectations for conventional CVB (red) and with thermal management (blue) for semiconductor devices T_1, T_2, D_1 and D_2.

Based on the temperature profiles and the applied lifetime models from (2.7)-(2.8) the lifetime expectation of each semiconductor devices is determined and illustrated in Fig. 6.17. Among the different SMs there are some variations in the expected lifetime which might become resembled in an idealized symmetrical system after longer time as long as aging effects are not taken into account. For better interpretation the mean values of the lifetimes is also provided.

An exceptionally strong extension of the lifetime expectations has been achieved for each single semiconductor device, being approximately doubled. Consequently, IGBT modules need to be exchanged less often and the maintenance intervals can be strongly extended, particularly beneficial for systems with limited access. In this way, the maintenance costs can be significantly reduced as one important item of the system operating costs.

The semiconductor lifetimes are still within a realistic range, if the hardware is optimized for a very reliable operation. Even if the expected lifetimes need to be interpreted very carefully, the revealed trend is very clear. The semiconductor lifetimes can be extended
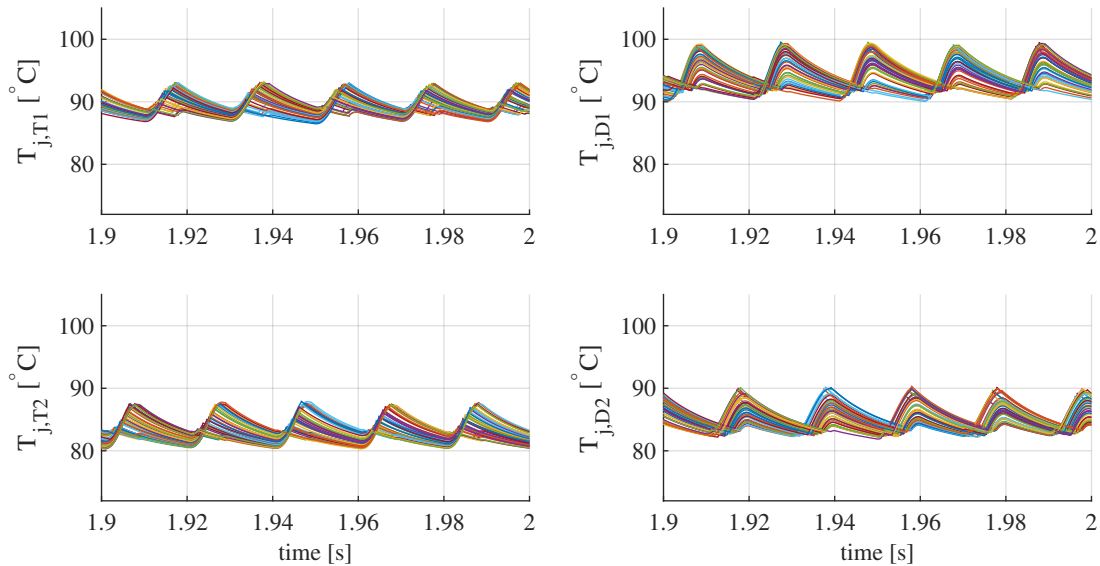
Figure 6.18: Thermal behavior of the CC-MMC (STATCOM) with thermal management in overload conditions (overrating of 15 %).

a lot by the introduced and proposed thermal management. This can be explained by the strongly reduced thermal cycles in all semiconductor devices. Besides, the power losses and the average junction temperatures are not significantly affected.

From thermal point of view both the maximum temperatures and the thermal cycles have been reduced by the introduced thermal management. Particularly, the achieved reduction in the maximum temperatures provide a high potential for a more economic converter design, linked to a smaller chip area and less cooling effort. The performance and efficiency of the MMC are not affected. Instead, the investment costs of the MMC system can be significantly reduced.

Alternatively, the gained temperature margin can be utilized for a higher current and power rating of the MMC. For this purpose, the injected reactive current has been increased by 15 %. In Fig. 6.18 the junction temperatures are depicted that do not exceed the maximum temperature of 100 °C. Also the capacitor voltages are kept within the limits as shown in Fig. 6.19.

The maximum temperatures and thermal cycles are summarized in Table 6.7 for the conventional CVB (I) and with the introduced thermal management (II, III). At nominal power the maximum temperatures have been reduced between 1 K and 5 K and the thermal cycles by between 33 % and 44 % by means of the thermal management (II). An increase of 4.5 Mvar (15 %) has been achieved by the thermal management (III) without exceeding maximum temperatures of 100 °C. Although, the power rating has been significantly increased just by software the thermal cycles are still significantly lower than for the conventional CVB at nominal power. Despite of the inherent goal conflict, both the rated power has been increased and the thermo-mechanical cycles have been reduced, enabling highly flexible and reliable operation.
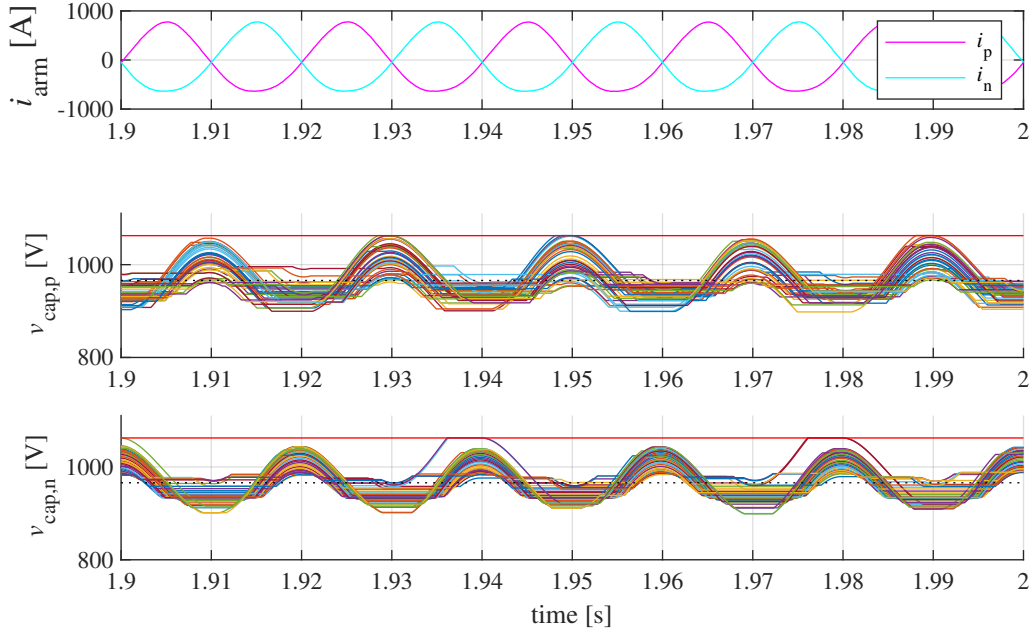
Figure 6.19: Arm currents and capacitor voltages of the CC-MMC (STATCOM) with thermal management in overload conditions, phase 1, upper arm (overrating of 15 %).

Table 6.7: Semiconductor temperatures for the CC-MMC (STATCOM) for nominal power with conventional CVB (study case I) and with thermal management (II), and in overload conditions (15 %) with thermal management (III).

Study cases:	I	II	III
S_g [MVA]	30	30	34.5
α [V/W]	0	0.02	0.02
$T_{j,T1,max}$ [°C]	92	89	93
$T_{j,T2,max}$ [°C]	87	84	88
$T_{j,D1,max}$ [°C]	99	95	99
$T_{j,D2,max}$ [°C]	91	87	90
$\Delta T_{j,T1}$ [°C]	11.3	5.8	6.7
$\Delta T_{j,T2}$ [°C]	11.4	6.1	7.7
$\Delta T_{j,D1}$ [°C]	15.6	8.6	9.6
$\Delta T_{j,D2}$ [°C]	13.4	7.1	8.1

The obtained overload capability by the introduced thermal management can be also used in fault conditions. For this purpose, a three-phase-to-ground fault is considered and generated in Fig. 6.20 where the nominal reactive power is provided for grid support. The occurring junction temperatures in each semiconductor device (one arm) are depicted in Fig. 6.21 for conventional CVB. The maximum temperatures in D_1 are around 100 °C.
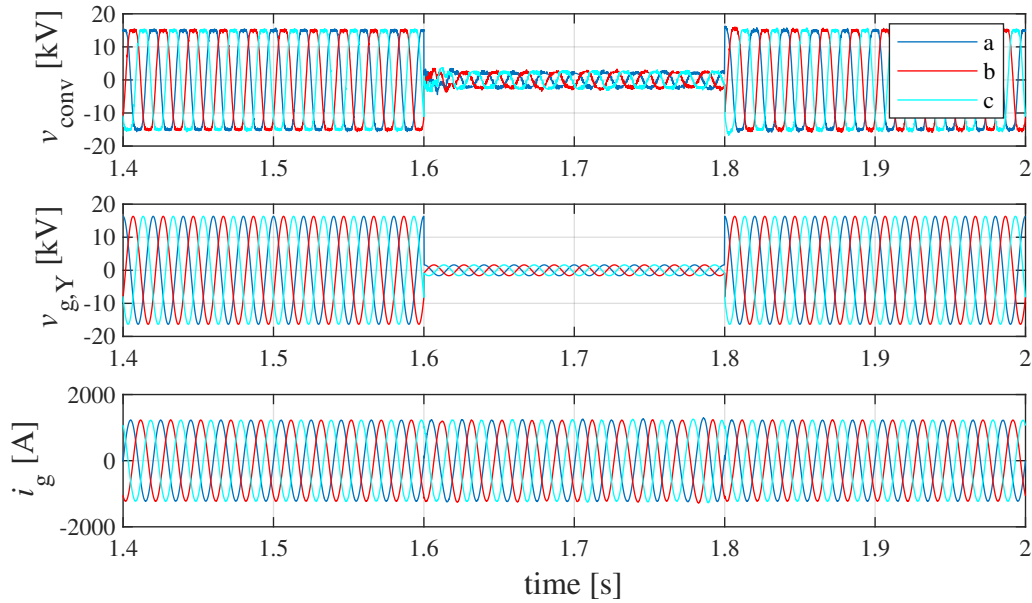
Figure 6.20: Electrical behavior of the CC-MMC (STATCOM, $Q_g = 30\,\text{Mvar}$) in case of a three-phase-to-ground grid fault.
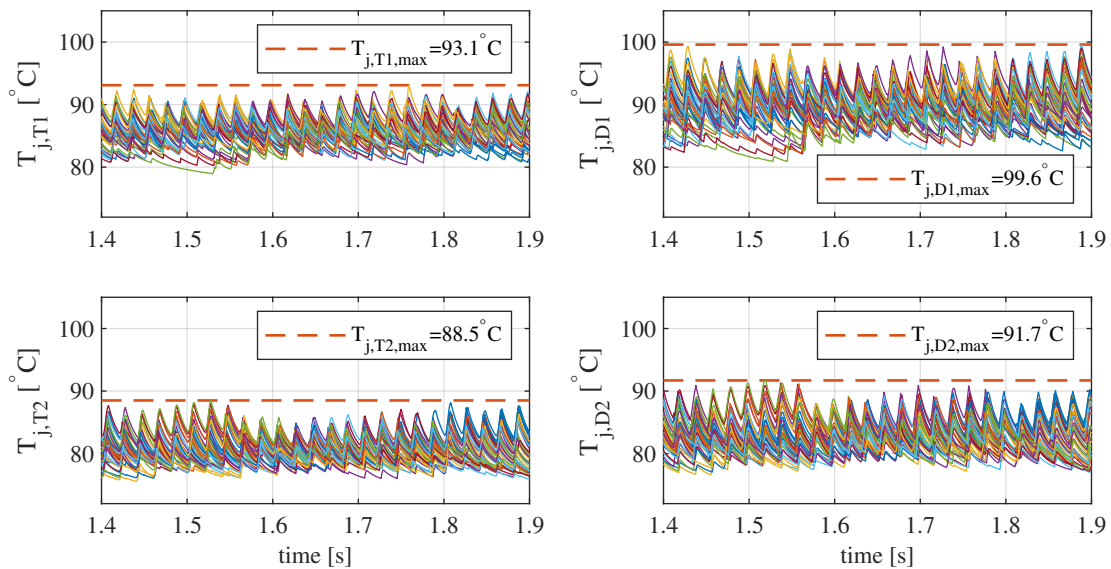
Figure 6.21: Thermal behavior of the CC-MMC (STATCOM, $Q_g = 30\,\text{Mvar}$) in case of a three-phase-to-ground grid fault.

Instead, the reactive power supply is increased by 20 % during the three-phase-to-ground fault for optimal voltage support as depicted in Fig. 6.22. Although the power has been strongly increased the temperatures can be kept within the range by the introduced thermal management just by software implementation as demonstrated in Fig. 6.23. Despite of 20 % higher currents during the fault conditions the thermal cycles are significantly reduced compared to the conventional scenario.
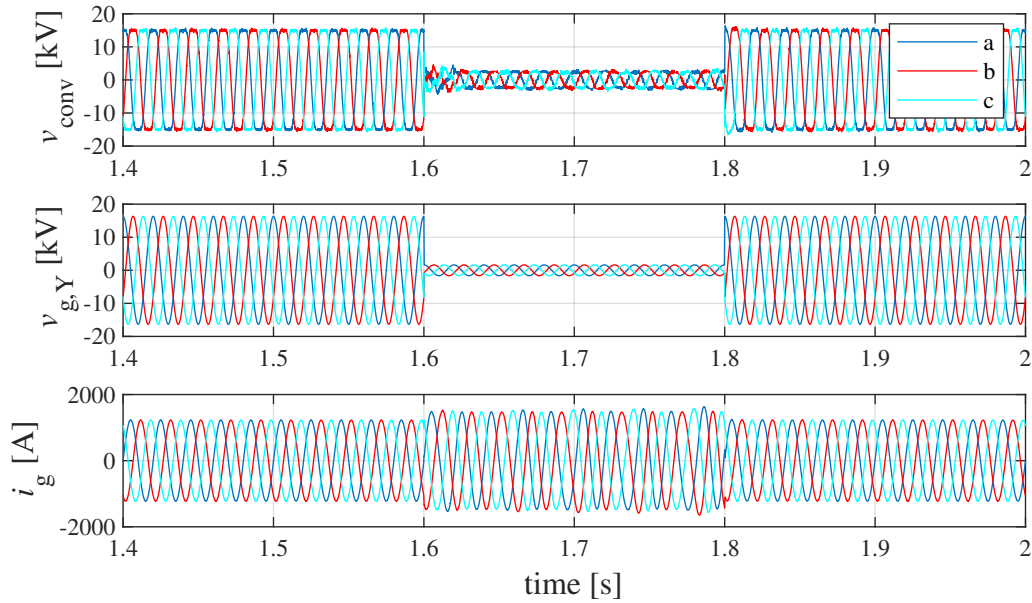
Figure 6.22: Electrical behavior of the CC-MMC (STATCOM) in overload conditions (20 %) with thermal management during a three-phase-to-ground grid fault.
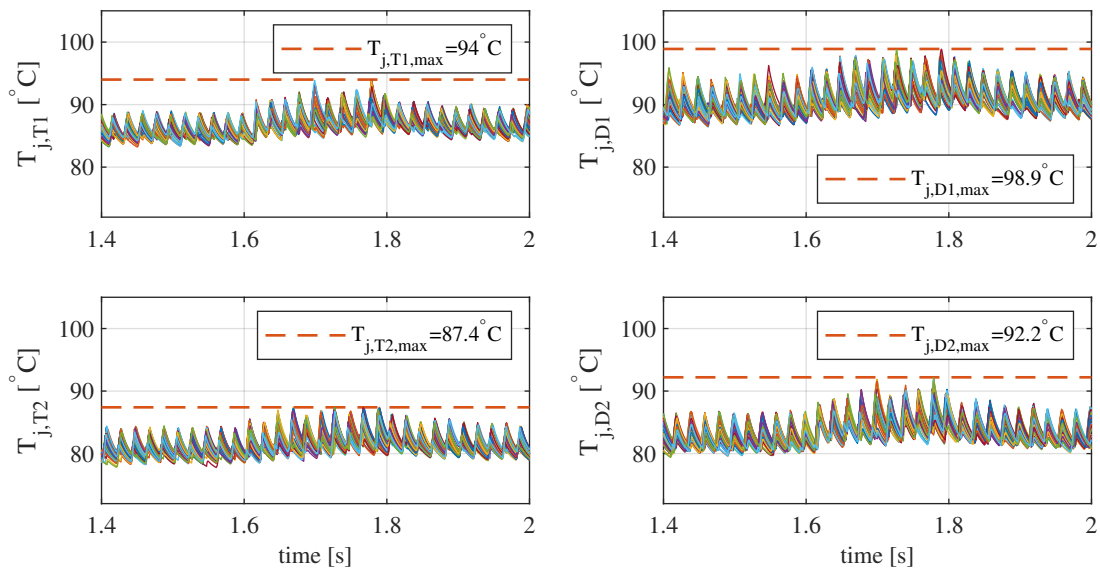
Figure 6.23: Thermal behavior of the CC-MMC (STATCOM) in overload conditions (20 %) with thermal management during a three-phase-to-ground grid fault.

The computation effort for approximating the junction temperatures of each single semiconductor device is relatively high, especially if it comes to HVDC applications. On the other hand a very high number of accurate sensors and communication would be required for temperature detection which is not practical. For limiting the computation effort in real time the stress of the semiconductor devices can be also regulated by taking into account the power losses as calculated in Section 6.1.1.

By taking into account the real-time conduction power losses, being averaged over one grid period (20 ms), the following cost functions can be derived:

$$c_1 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{D1}}(\overline{P}_{\text{l,con,D1}} - \min\{\overline{P}_{\text{l,con,D1}}\}) \tag{6.11}$$

$$c_2 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{T2}}(\overline{P}_{\text{l,con,T2}} - \min\{\overline{P}_{\text{l,con,T2}}\}) \tag{6.12}$$

$$c_3 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{T1}}(\overline{P}_{\text{l,con,T1}} - \min\{\overline{P}_{\text{l,con,T1}}\}) \tag{6.13}$$

$$c_4 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{D2}}(\overline{P}_{\text{l,con,D2}} - \min\{\overline{P}_{\text{l,con,D2}}\}) \tag{6.14}$$

In Fig. 6.24 it is demonstrated that the thermal management is only slightly reduced by taking into account the averaged power losses. However, the computation effort is strongly reduced since the thermal modeling is not required. It becomes also obvious that it is sufficient to balance the conduction losses for optimal power routing instead of the overall losses. The real-time calculation of the switching losses can be avoided to minimize the computation effort.

The introduced thermal management approach is not only applicable to each standard modulation technique but also to all standard applications, voltage levels and operation points. For further demonstration the thermal management will be applied for the HVDC application from Section 5.2 with a rated power of 300 MW and 150 SMs per arm.

The junction temperatures are considered for two operation points, active power supply (300 MW, $\cos\varphi = 0.95$) and reactive power supply (300 Mvar, $\cos\varphi = 0$). In Fig. 6.25a and 6.25b the junction temperatures are exemplary shown for the first 21 SMs. The temperature spread among the SMs is very significant, particularly strong for pure reactive power supply.
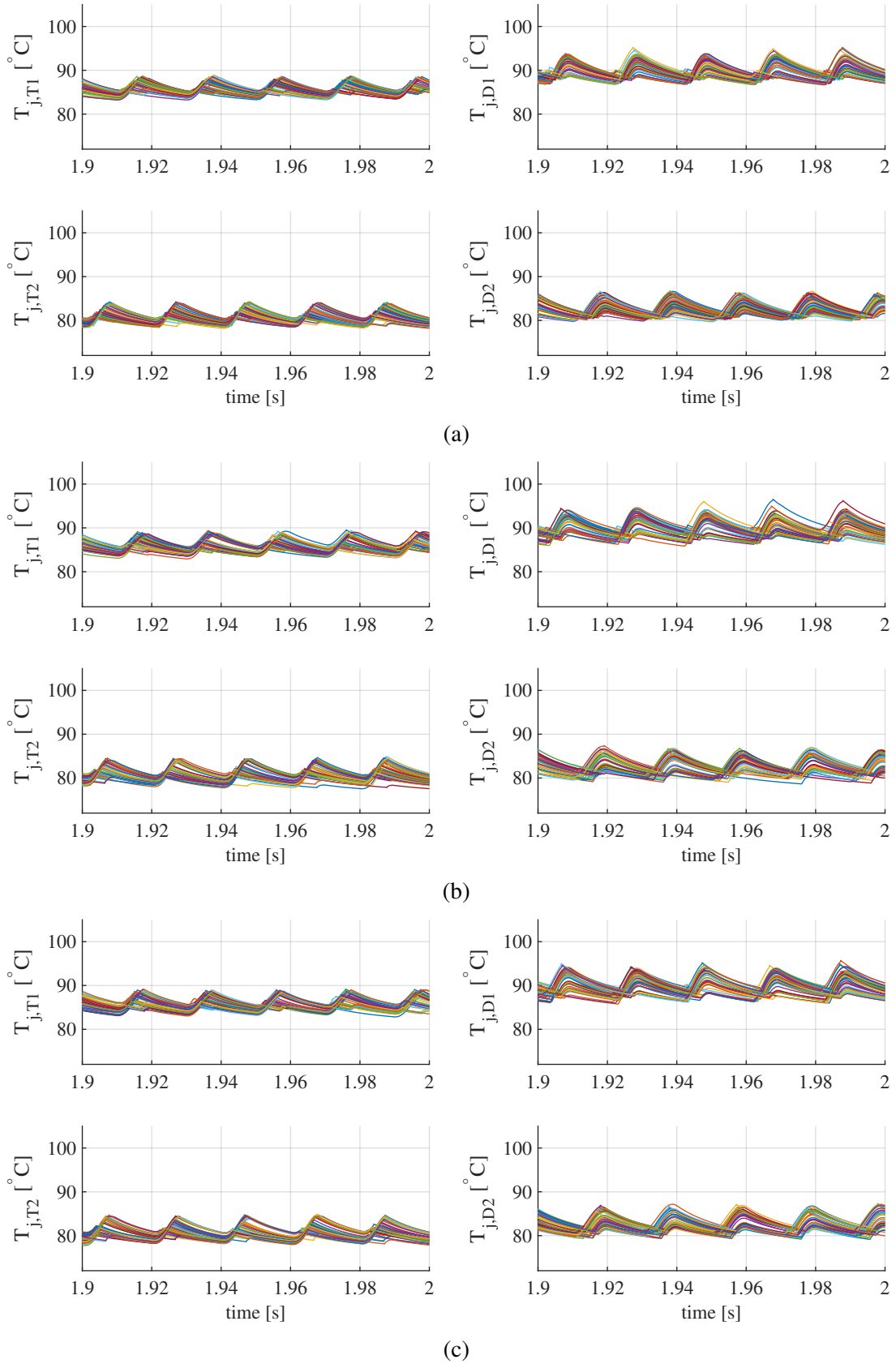
Figure 6.24: Limitation of computation effort for thermal management (CC-MMC, STAT-COM, $Q_g = 30\,\mathrm{Mvar}$), based on: (a) Junction temperatures (benchmark, $\alpha = 50$). (b) Averaged semiconductor power losses ($\alpha = 0.2$). (c) Averaged semiconductor conduction losses ($\alpha = 0.2$).
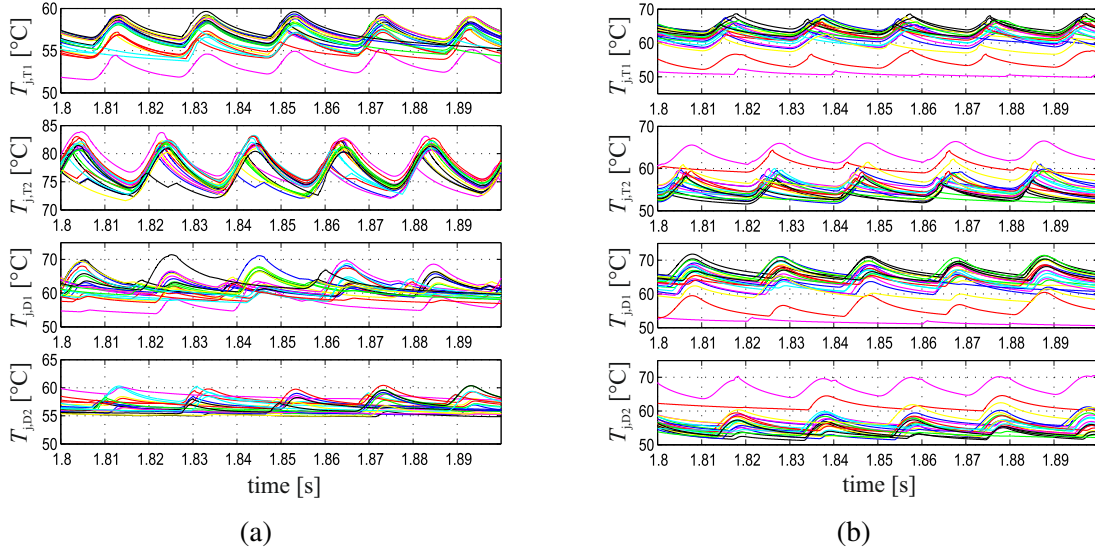
Figure 6.25: Semiconductor junction temperatures for the CC-MMC (HVDC): (a) $P_g = 300\,\text{MW}$, $\cos\varphi = 0.95$. (b) $Q_g = 300\,\text{Mvar}$, $\cos\varphi = 0$.

In Fig. 6.26 the junction temperatures are further analyzed. Based on the date for all 150 SMs in one arm the maximum, minimum and averaged semiconductor junction temperatures are depicted for active ($\cos\varphi = 0.95$) and for reactive ($\cos\varphi = 0$) power supply. The average temperatures for the conventional CVB and for the thermal management are congruent since the efficiency is kept constant. The maximum, minimum and averaged capacitor voltages are shown as well. The CVB is operating very effectively, even if the thermal management is applied.

Different to this, the spread in the temperatures has been significantly reduced by the thermal management. This becomes particularly evident in the averaged difference between the maximum and minimum temperatures which have been reduced by between 19.5 % (T_2) and 35.1 % (D_1) without affecting the system efficiency and performance. For reactive power supply the impact of the thermal management is even stronger. The difference between the highest and lowest junction temperature has been reduced by between 12.4 K (T2) and 21.6 K (D1), corresponding to 71.4 % and 79.7 %. The system optimization can be used for a more economic design and for reliable operation.

All SMs of the MMC and its electrical and thermal stress can be validated and further investigated by the experimental bench, introduced in Section 6.2. For practical reasons the operating powers have been limited. For the arm current profile, a downscaling factor of 50 is applied. The DC voltage V_{dc1} at the DUT is limited to 100 V for safety reasons due to the absence of filling gel whereas V_{dc2} is set to 200 V. The main data are summarized in Table 6.8. For the MMC the conduction losses are predominant due to the low switching frequencies as demonstrated in Section 6.1.1. Therefore, the application of reduced voltages is not a critical issue for the loss behavior. Also capacitor voltage oscillations can be neglected due to this fact and would be also mostly filtered due to higher thermal time constants.

(a)   (b)
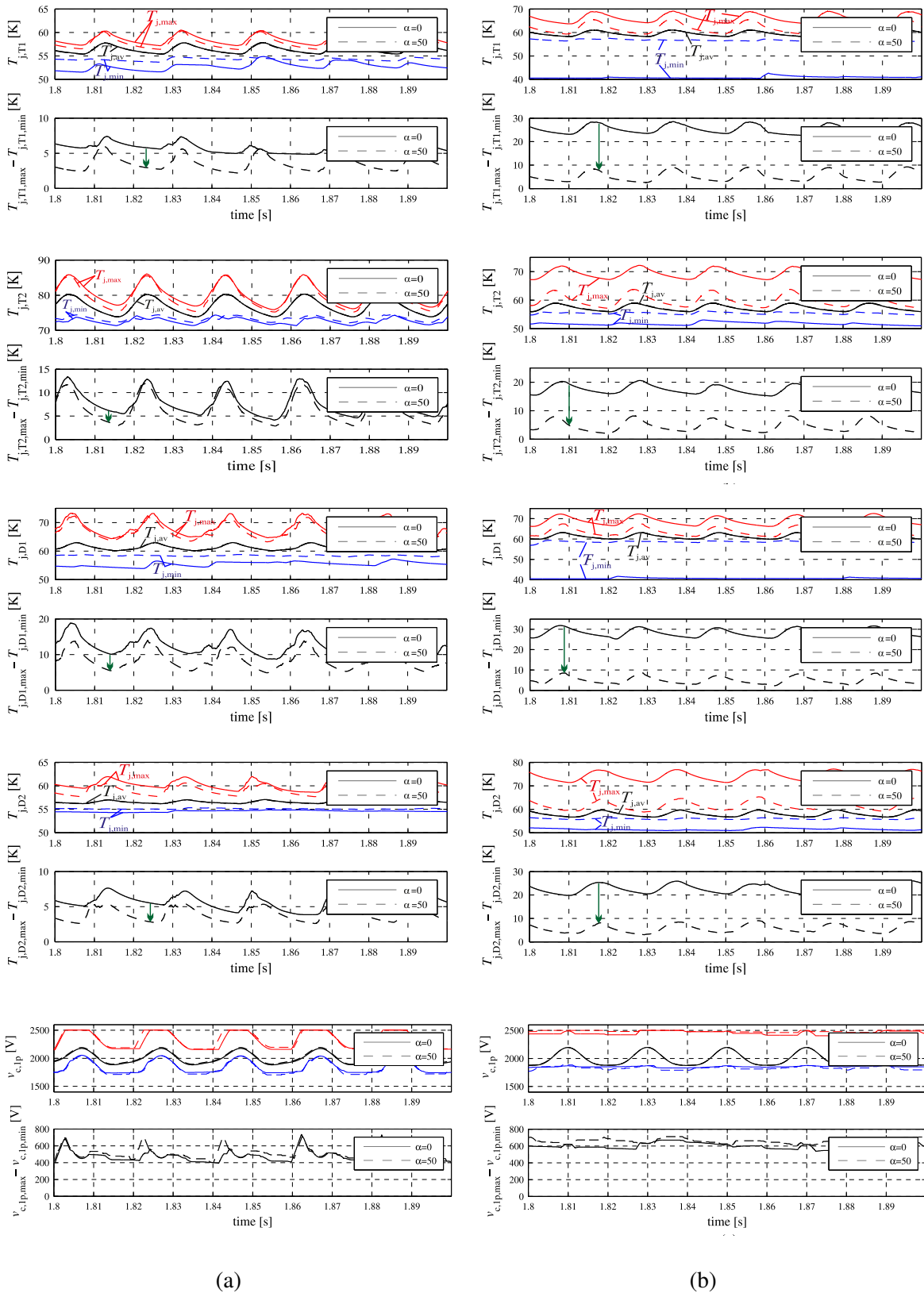
Figure 6.26: Maximum, minimum, and averaged junction temperatures and capacitor voltages in the upper arm (ph. 1) for IGBTs T_1, IGBTs T_2, diodes D_1, diodes D_2: (a) $P_g = 300\,\mathrm{MW}$, $\cos\varphi = 0.95$. (b) $Q_g = 300\,\mathrm{Mvar}$, $\cos\varphi = 0$.

Table 6.8: System parameters for experimental bench.

V_{dc1}	100 V
V_{dc2}	200 V
L_{filter}	3.6 mH
f_c	10 kHz
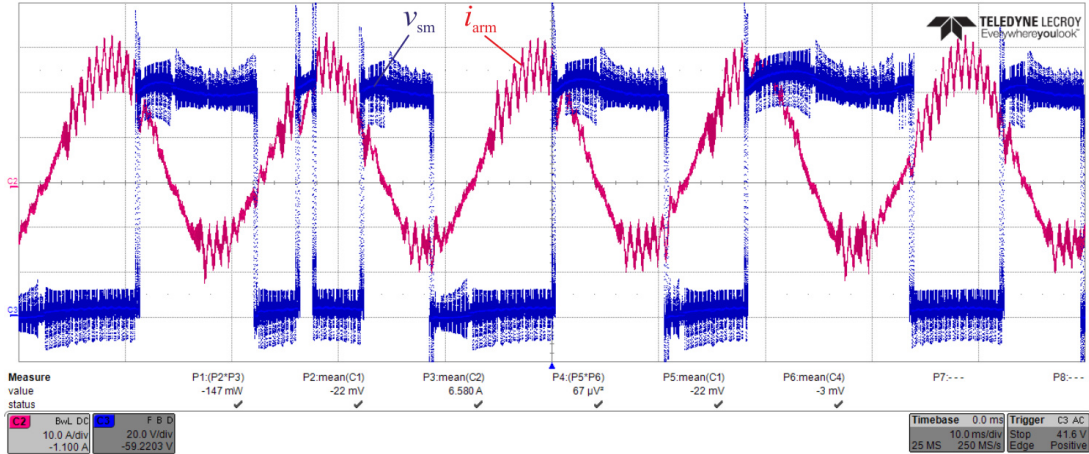
Figure 6.27: Experimental validation of arm current and voltage at one SM (no. 61).

The electrical behavior of one SM (no. 61) at full nominal power ($P_g = 300\,\text{MW}$, $\cos\varphi = 0.95$) is exemplary shown in Fig. 6.27, where the SM voltage as well as the downscaled arm current is properly generated. The SM voltage is obtained according to the NLM switching profile. For the arm current both the DC and AC components are flexibly controlled, independently from the switching sequence of the DUT.

The temperature distribution of the SM is depicted in Fig. 6.28. The occurring hotspots are mainly determined by the operation point and the related power factor. At high power factors the IGBT T_2 is the most stressed semiconductor device.

The hotspots of all four semiconductor devices have been recorded by the IR camera. The corresponding temperature profiles are depicted in Fig. 6.29 for the applied Danfoss IGBT modules, being rated for 1200 V and 25 A. For comparison, the modeled temperature profiles are shown for the Mitsubishi IGBT module, being rated for 4500 V and 1200 A. The use of lower powers in the downscaled system with different semiconductor explains the lower operating temperatures. Furthermore, also the detected thermal cycles are reduced. Despite of these variations the characteristic temperature profiles from the simulation and the experimental bench are perfectly matching together. For optimized fine-tuning of the thermal modeling in a practical application, high-power semiconductor devices can be directly applied and evaluated by the experimental bench.
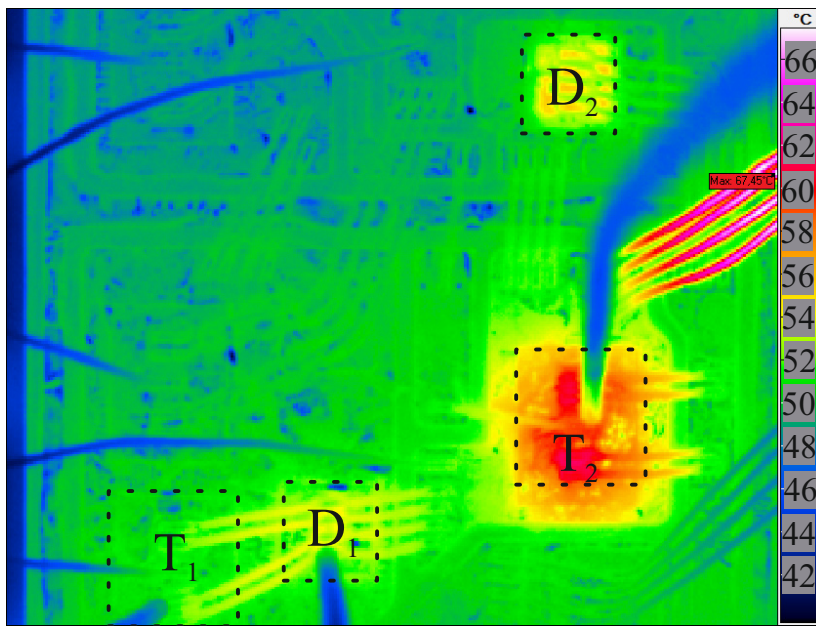
Figure 6.28: Temperature distribution in the IGBT module recorded by IR camera for one SM (no. 61).
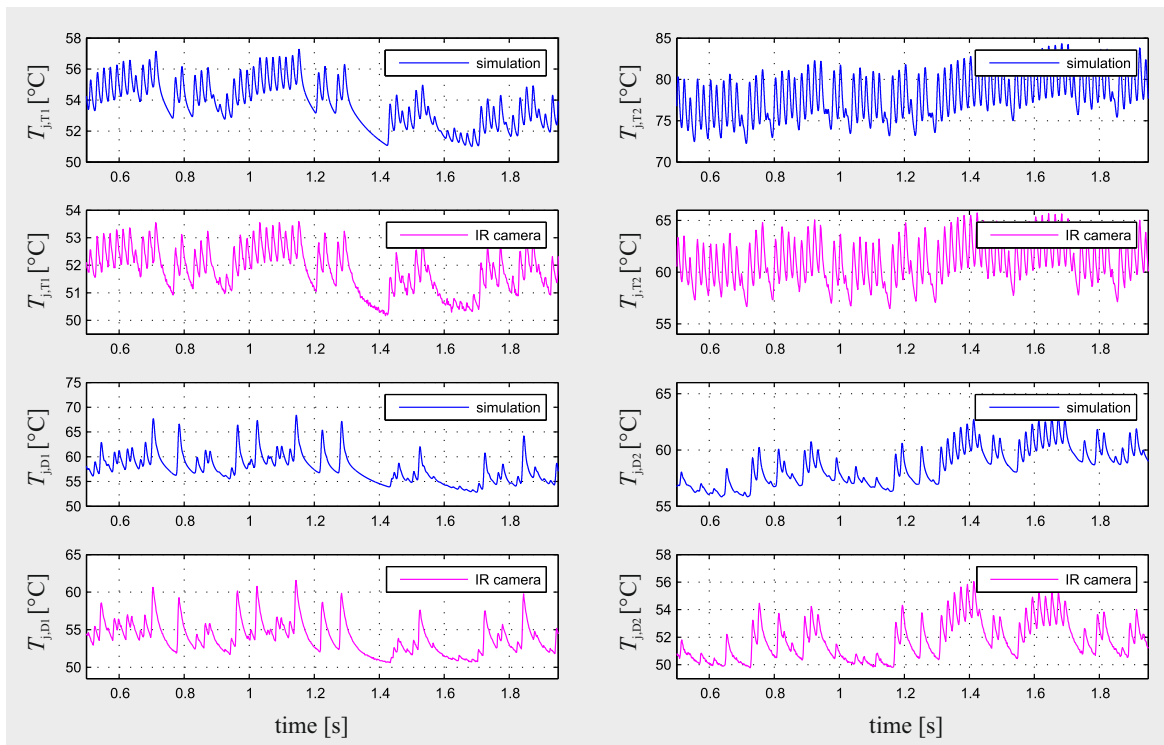
Figure 6.29: Junction temperature profile for one SM (no. 61) from simulation and from the experimental bench from infrared camera ($P_\mathrm{g} = 300\,\mathrm{MW}$, $\cos\varphi = 0.95$).

For experimental validation of the introduced thermal management three different SMs are selected for each operation point. For active power supply the switching profiles and the recorded junction temperatures are depicted in Fig. 6.30. The SM no. 122 serves as kind of a benchmark because its switching profile is relatively homogenous during the shown time interval. Instead, the switching profiles from SMs no. 61 and 94 are very inconsistent. This leads to high variations among the junction temperatures, being relevant for all four semiconductor devices. The thermal spread in the different semiconductor devices can be effectively reduced by the applied thermal management. The thermal management is automatically acting on the switching profiles if one SM is inserted or bypassed for longer time.

The thermal cycles are particularly strong at low power factors, as validated in Fig. 6.31. During full reactive power supply, SM no. 67 serves as kind of a benchmark. During conventional CVB the switching profiles can become very inhomogeneous as it can be seen for SM no. 146. This SM is bypassed almost during the full time interval, leading to very high temperatures in the loaded semiconductor devices T_2 and D_2. It becomes obvious that conventional CVB algorithms can become very ineffective for a proper stress management for the devices. Instead, the junction temperatures can be controlled by the thermal management, equalizing the SM switching profiles.

The introduced thermal management acts on the switching states of the SMs and is able to reduce the thermal cycles and also the maximum temperatures for each single SM, even in huge and very cost intensive HVDC applications. These optimizations have been achieved by maintaining the high performance and the high efficiency of the MMC. Not only the imbalanced loading of the SMs has been prevented but also the number of fast temperature changes for long and reliable operation of the semiconductor devices.
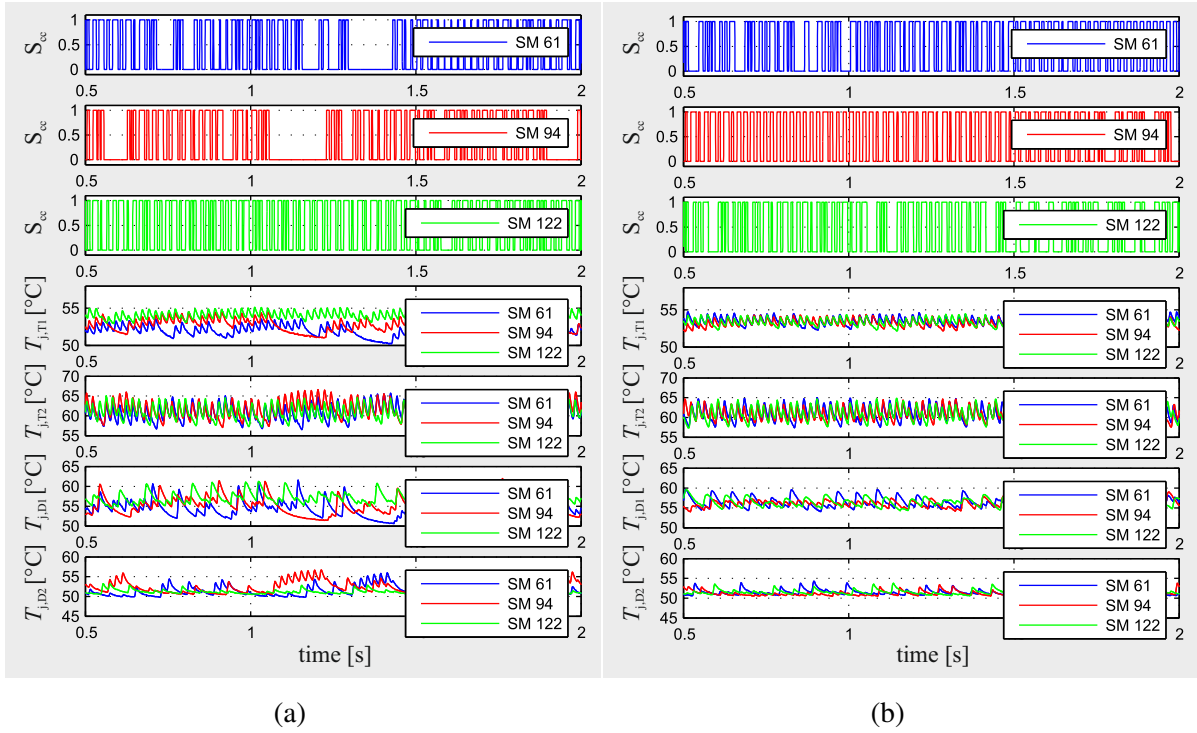
Figure 6.30: Switching states and junction temperatures in three MMC SMs (no. 61, 94, 122) recorded by IR ($P_\mathrm{g} = 300\,\mathrm{MW}$, $\cos\varphi = 0.95$): (a) Conventional CVB balancing ($\alpha = 0$). (b) Thermal management ($\alpha = 50$).
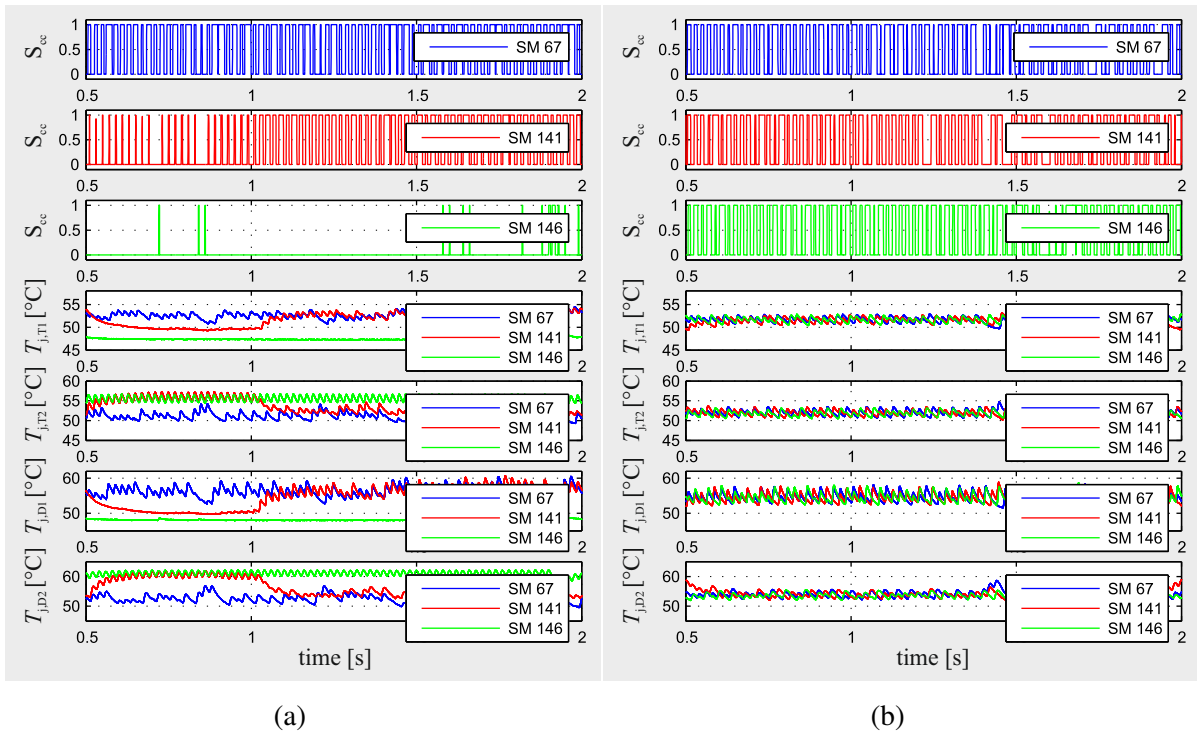
Figure 6.31: Switching states and junction temperatures in three MMC SMs (no. 67, 141, 146) recorded by infrared camera ($Q_\mathrm{g} = 300\,\mathrm{Mvar}$, $\cos\varphi = 0$): (a) Conventional CVB balancing ($\alpha = 0$). (b) Thermal management ($\alpha = 50$).

6.3.2 BC-MMC

For the BC-MMC there is a strong motivation to benefit from the high number of redundant switching states, as well. The BC-MMC does not only provides a high degree of redundancy for selecting the SMs but also an additional degree of freedom within each SM due to both redundant zero switching states. In Chapter 3 two different NLM switching sequences with minimum number of commutations have been defined for the BC-MMC. For both suggested NLM sequences the waveform generation and quality are equivalent.

The temperatures of all semiconductor devices (one arm) are depicted in Fig. 6.32 for both NLM sequences at nominal reactive power injection ($Q_g = 30\,\text{Mvar}$). The semiconductor junction temperatures among the different SMs are already well balanced by the conventional CVB. However, for an improved thermal management the temperatures within each SM need to be better regulated. For the NLM sequence 1 the highest junction temperatures are identified in diodes D_1, corresponding to $101.2\,^\circ\text{C}$. Different to this, the maximum junction temperatures in diodes D_1 are reduced by almost 15 K to $86.5\,^\circ\text{C}$ by the applied NLM sequence 2. Instead of the diodes D_1, the IGBTs T_1 are more heavily loaded for sequence 2, reaching temperatures of up to $96.2\,^\circ\text{C}$. All other semiconductor junction temperatures are kept within a comfortable range below $92\,^\circ\text{C}$.

In accordance to this, the power losses, thermal stress and hotspot temperatures can be managed up to a certain degree between the semiconductor devices depending on the applied switching sequence and the applied load profile. For the shown study case the heavy load has been shifted from diode D_1 to IGBT T_1 just by changing the NLM sequence. In addition to this, the maximum junction temperatures of the system have been reduced from $101.2\,^\circ\text{C}$ to $96.2\,^\circ\text{C}$, providing an additional margin for design optimizations, overload capability and reliable operation.

On the one hand, the sequence 1 is linked to very high temperatures in the diodes D_1. On the other hand, the sequence 2 causes high temperatures in the IGBTs T_1. For an improved thermal regulation a mixed sequence is proposed, alternating both switching sequences after each grid period. In this way a trade-off becomes possible to more equalize the stress in the IGBTs T_1, T_2, T_3, T_4 and diodes D_1, D_2, D_1, D_2.

The junction temperatures of the semiconductor devices are depicted in Fig. 6.33a where the maximum occurring temperatures have been reduced compared to both conventional NLM switching sequences. Compared to sequence 1 the maximum temperatures have been reduced from $101.2\,^\circ\text{C}$ (D_1) to $95\,^\circ\text{C}$ (D_1). Accordingly, the maximum temperatures also have been reduced compared to sequence 2 ($96.2\,^\circ\text{C}$, T_1) for more flexible and reliable operation.

For an optimized thermal management, the maximum junction temperatures in IGBT T_1 and D_1 would be similar for an economical design and for effective thermal stress regulation. For this purpose, the weighting of the switching sequences can be further optimized. In Fig. 6.33b the junction temperatures are depicted for alternating sequence 1 and sequence 2 after one and after two grid periods, respectively. The temperatures are regulated very well in

both, IGBT T_1 and diode D_1. The obtained maximum junction temperatures of 92.2 °C (T_1) and 92.7 °C (D_1) are almost identical. The junction temperatures of all other semiconductor devices are even kept below 90 °C.

The introduced thermal management for the BC-MMC provides additional temperature margins. For instance, this margin can be used for an increased power rating of the system. This is demonstrated in Fig. 6.34a where the nominal power has been increased by 10 %. Although, the current increase also induces additional power losses in the system, the maximum junction temperatures are kept below 96 °C. Accordingly, not only the maximum temperatures have been reduced by the introduced thermal management but also the semiconductor power rating has been increased. By allowing maximum junction temperatures of 100 °C, even an overload capability of 20 % becomes possible. This is demonstrated in Fig. 6.34b, where the junction temperatures are still kept lower than for conventional sequence 1 at nominal power. Accordingly, an additional reactive power of up to 6 Mvar has been achieved just by software, profiting from the redundant switching states of each single SM.

The electrical behavior of the BC-MMC during a three-phase-to-ground fault is depicted in Fig. 6.35. On the one hand, the MMC provides full nominal power for stabilizing the voltages. On the other hand, an overload capability of 20 %, corresponding to 6 Mvar, is provided during the grid fault for additional grid support.

The junction temperatures of the semiconductor devices at nominal power are depicted in Fig. 6.36 for both NLM sequences. The transients during the fault conditions also have an impact on the semiconductor stress and temperatures. Compared to steady-state operation the maximum temperatures can increase during the fault conditions, leading up to 102.7 °C in D_1 (sequence 1) and 97.1 °C in IGBT T_1 (sequence 2), respectively.

The proposed thermal management for the BC-MMC also provides an overload capability during grid faults where a strong reactive power supply is very important for safe and stable operation. The optimized mixed switching sequence is able to provide an additional power of 20 % for grid support, maintaining the maximum temperatures at around 97.5 °C in the diodes and the IGBTs T_1 as demonstrated in Fig. 6.37. Accordingly, the thermal stress is effectively regulated within all SMs, enabling a significant overload capability also during grid fault conditions.

The improved thermal management for the BC-MMC can be used for a more economic converter and cooling design and for safer and more reliable operation, as well. Since the introduced algorithms are only acting on the zero voltage states, the waveform quality and the number of commutations are not affected. The system performance and efficiency are not affected.

The switching sequences can be optimized for different operation points and for different grid fault conditions. On the one hand, this can be done online by monitoring the junction temperatures by real-time estimations or low-cost sensors. On the other hand, an offline implementation is also possible to cover the most relevant operation profiles by look-up tables to limit the computation effort.
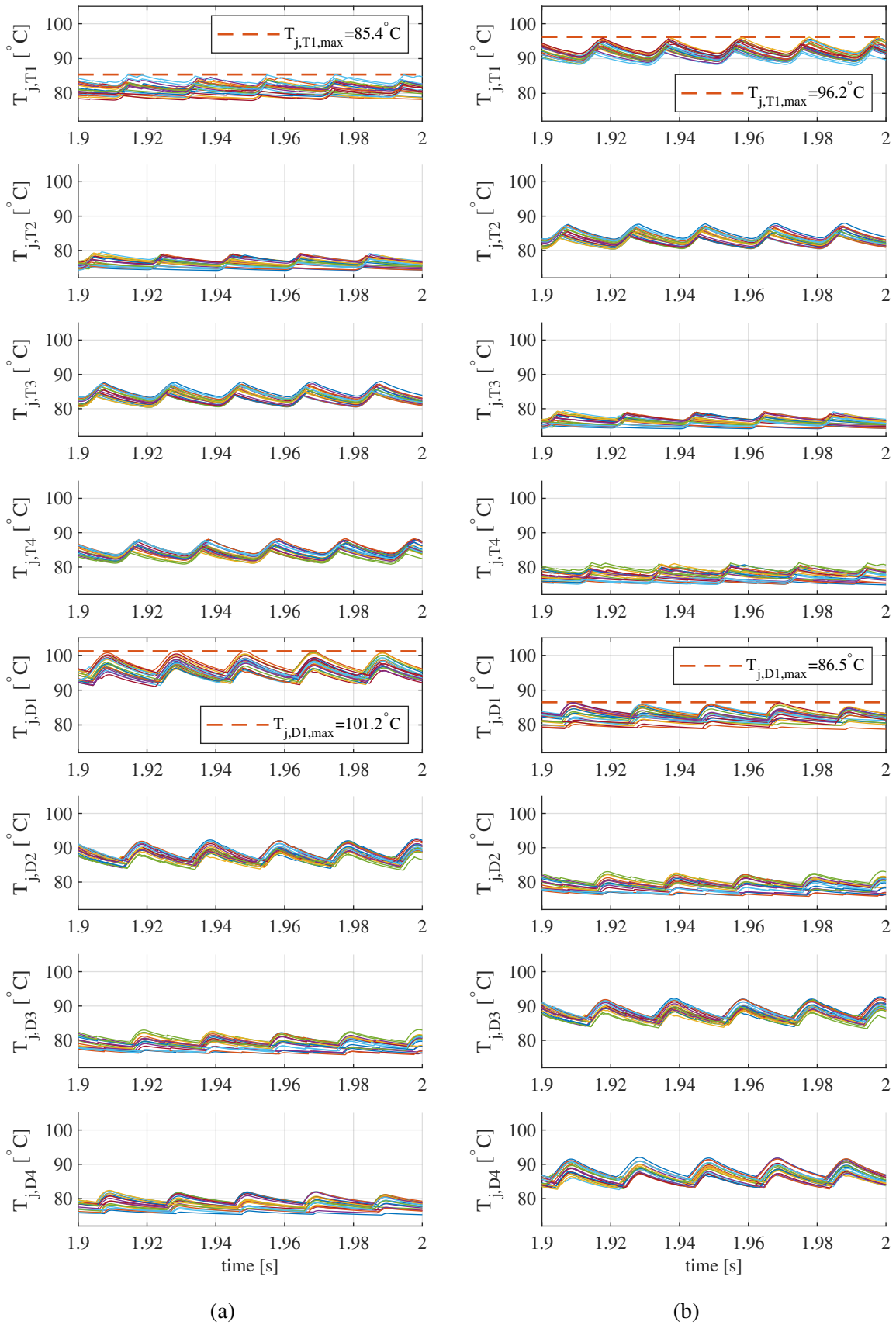
Figure 6.32: Thermal behavior of the BC-MMC (STATCOM, $Q_\text{g} = 30\,\text{Mvar}$, NLM): (a) Sequence 1. (b) Sequence 2.
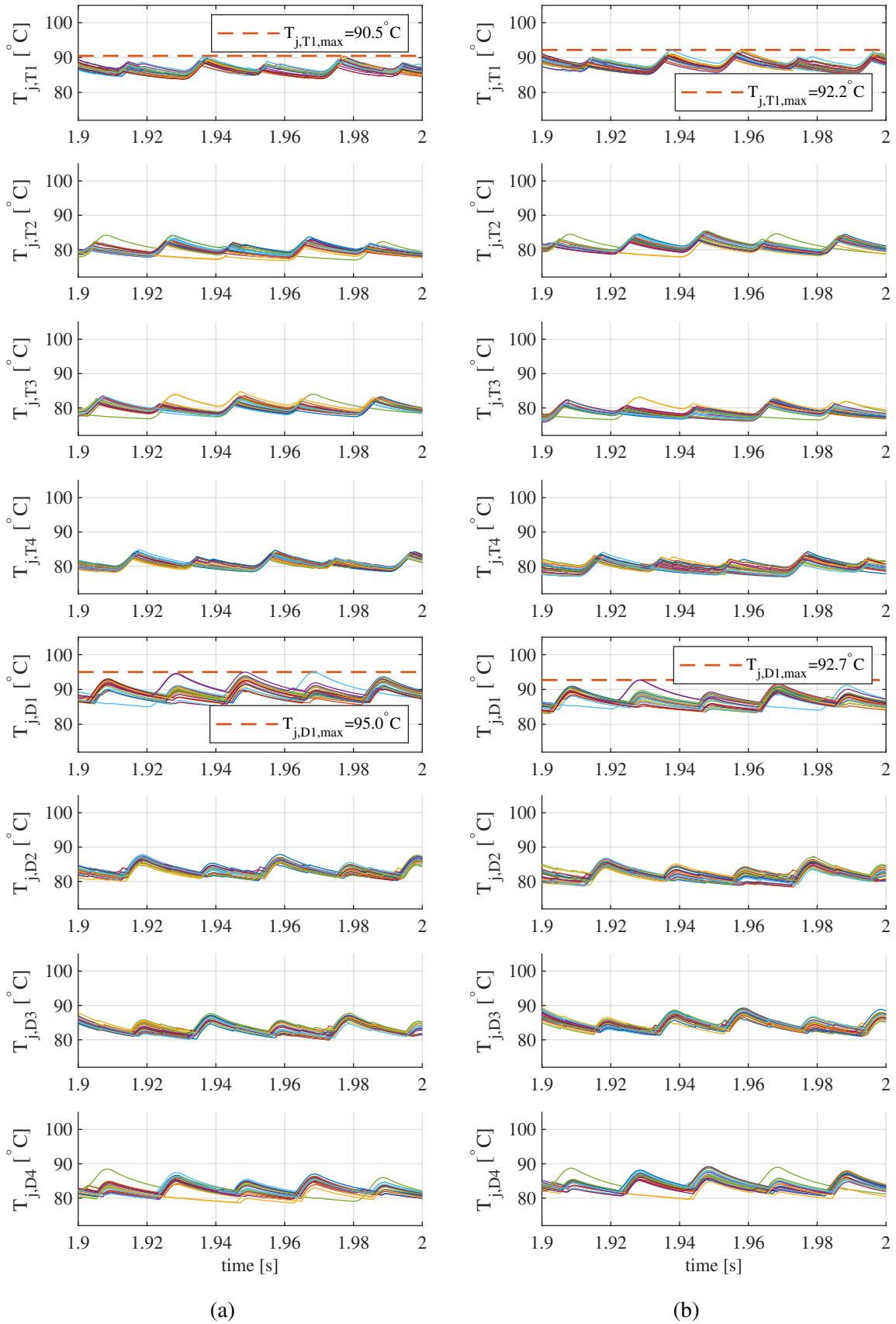
Figure 6.33: Thermal behavior of the BC-MMC (STATCOM, $Q_g = 30\,\text{Mvar}$), mixed NLM sequences: (a) Sequence 1 / sequence 2 (evenly alternating: 50 % / 50 %). (b) Sequence 1 / sequence 2 (optimized: 33.3 % / 66.7 %).
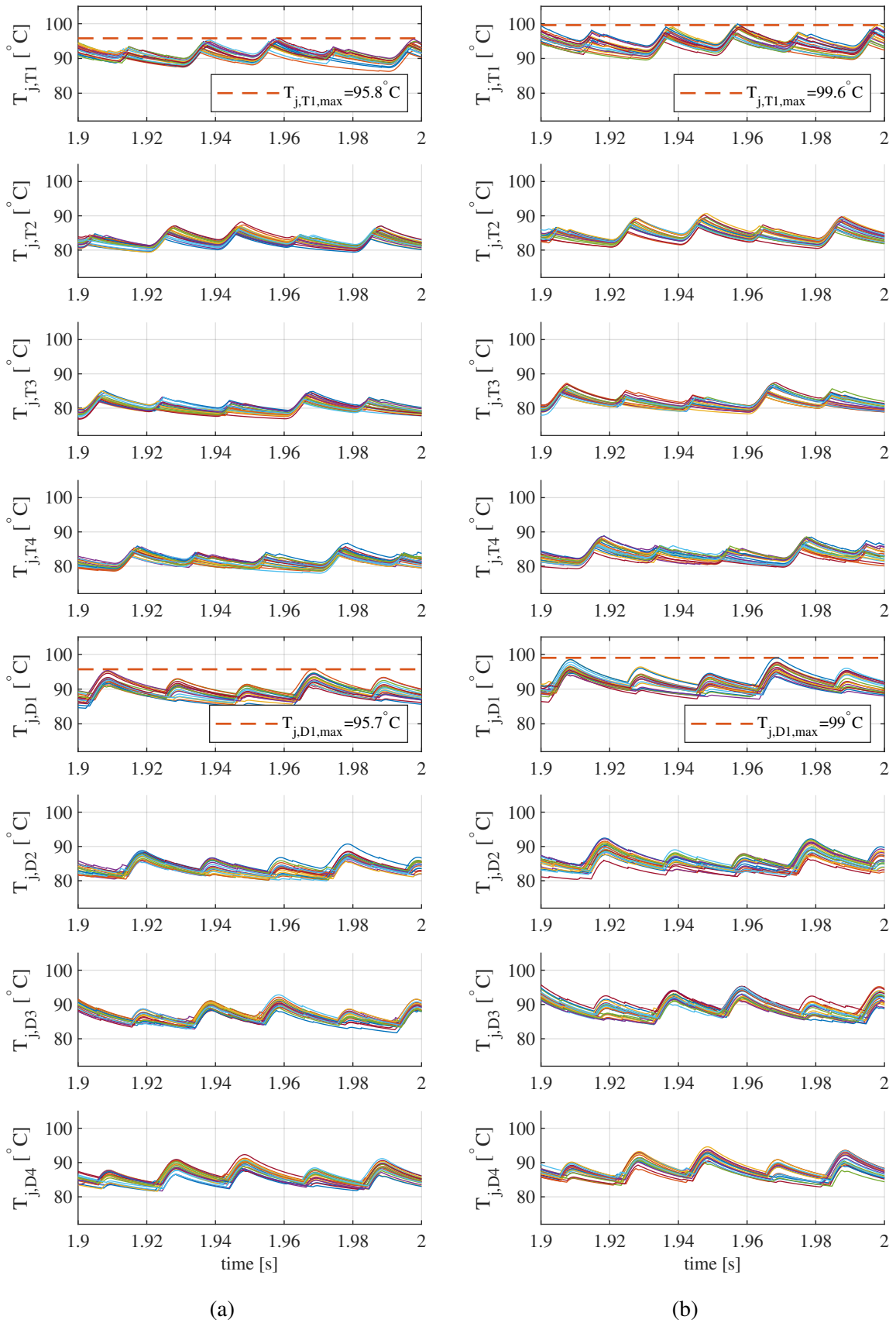
Figure 6.34: Thermal behavior of the BC-MMC (STATCOM, optimized NLM sequence), overload conditions: (a) $Q_g = 33\,\text{Mvar}\ (\equiv 110\,\%)$. (b) $Q_g = 36\,\text{Mvar}\ (\equiv 120\,\%)$.
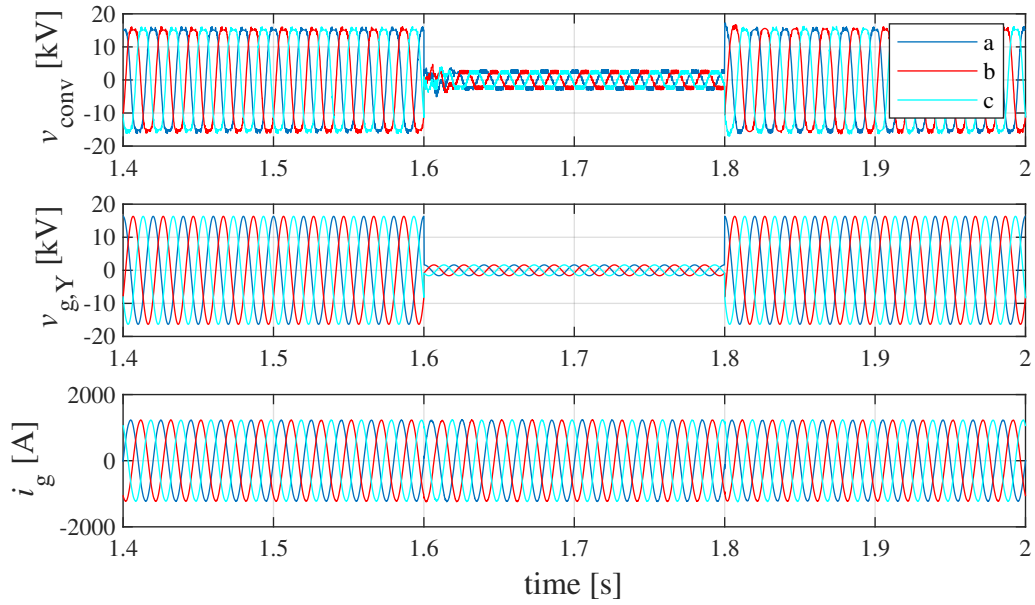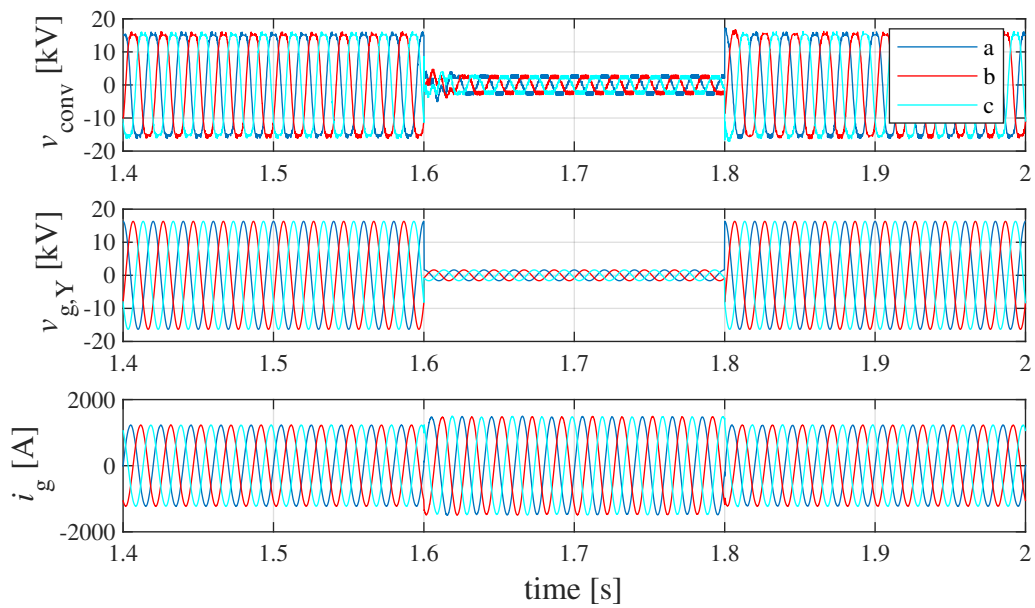
Figure 6.35: Electrical behavior of the BC-MMC in case of a three-phase-to-ground grid fault: (a) Nominal power ($Q_g = 30$ Mvar). (b) Overload capability (20 %).
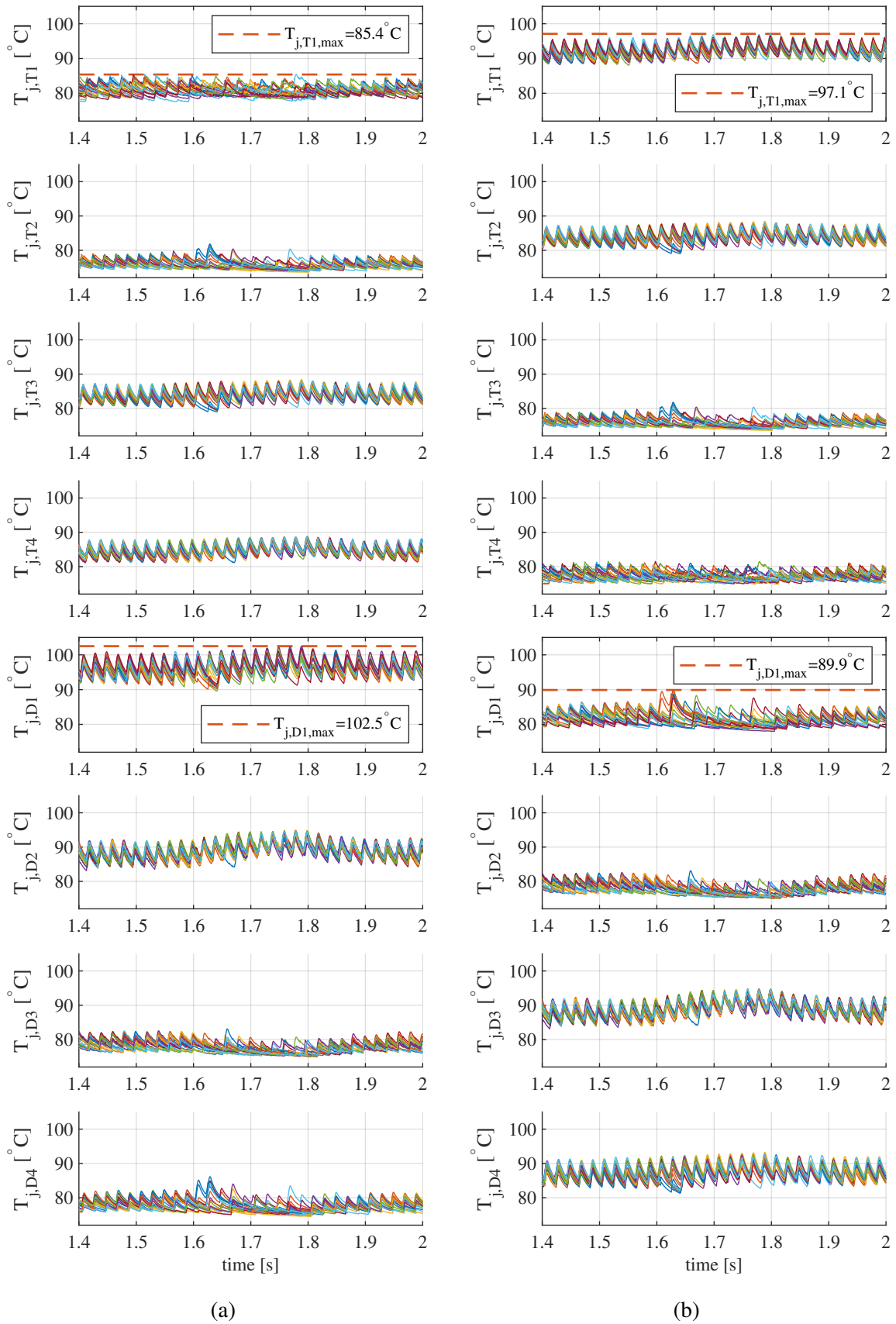
Figure 6.36: Thermal behavior of the BC-MMC (STATCOM, $Q_g = 30\,\mathrm{Mvar}$) in case of a three-phase-to-ground grid fault: (a) NLM sequence 1. (b) NLM sequence 2.
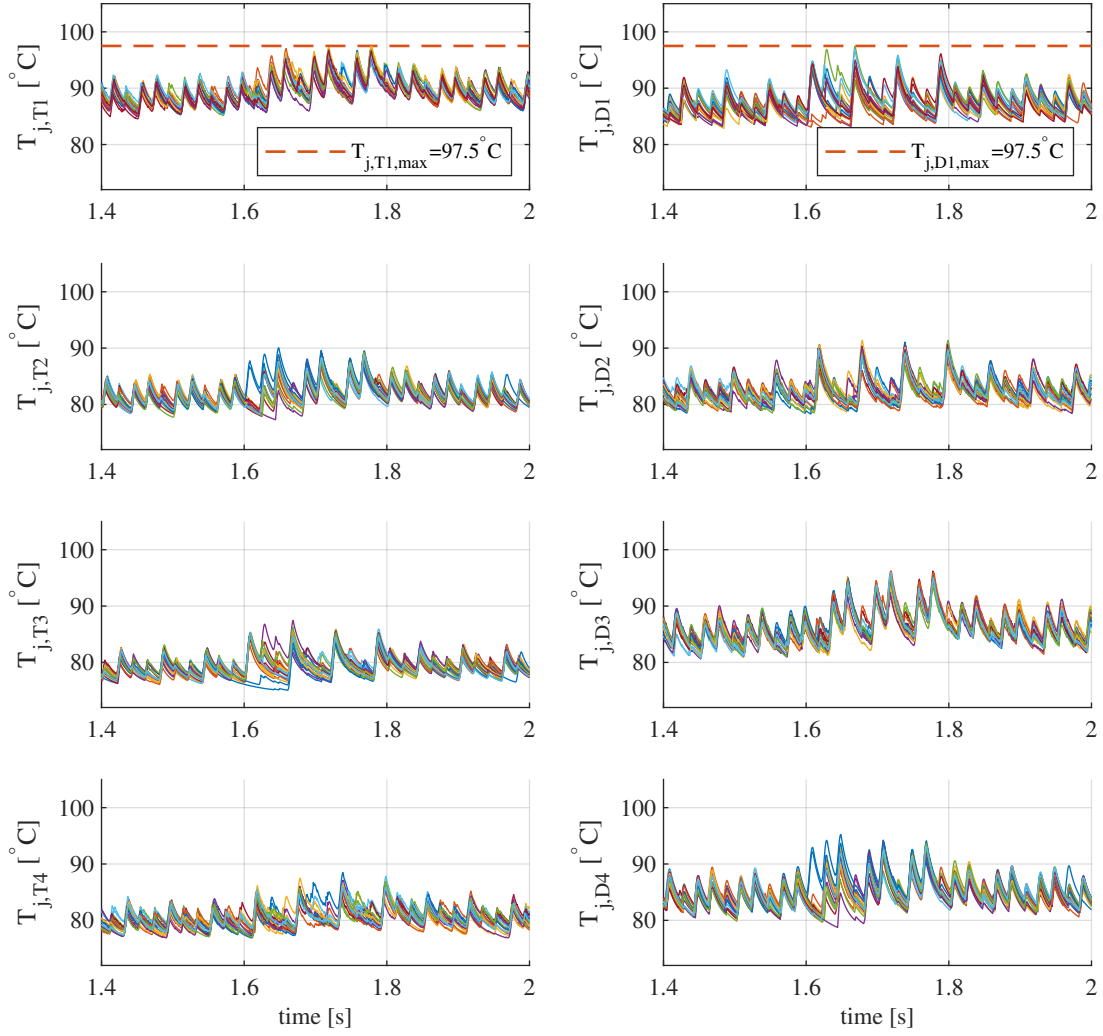
Figure 6.37: Thermal behavior of the BC-MMC (STATCOM) in overload conditions (20 %) with optimized NLM sequence in case of a three-phase-to-ground grid fault.

The optimization of the switching sequences can be done offline for different operation points and different grid conditions to limit the implementation and computation effort. Instead, it is also possible to calibrate the switching sequences online based on available temperature information (e.g. by real-time estimators) to manage the thermal behavior in real time. Additional information as expected remaining semiconductor lifetimes can be taken into account, as well.

6.4 Thermal Management of Capacitor Storages

Beside the semiconductor devices the capacitor storages are the most important and most expensive components in MMC applications. Therefore, it is proposed to also take into account the thermal stress of the capacitors. Four cost functions are introduced in (6.15)-(6.18) for an effective thermal management. In these cost functions the capacitor voltage of each SM is combined with the occurring capacitor losses, being averaged over five grid periods (100 ms). Since the thermal time constants of bulky capacitors are very high and

temperature changes very slow, it is sufficient to simply take into account the averaged power losses for an effective thermal management of the capacitor storages. Consequently, also the weighting factors can be selected in a very sensitive way since it is even sufficient to balance the capacitor losses over hundreds or thousands of grid periods due to the high thermal time constants.

$$c_1 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{cap}} \cdot (\overline{P}_{\text{l,cap}} - \min\{\overline{P}_{\text{l,cap}}\}) \tag{6.15}$$

$$c_2 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{cap}} \cdot (\max\{\overline{P}_{\text{l,cap}}\} - \overline{P}_{\text{l,cap}}) \tag{6.16}$$

$$c_3 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{cap}} \cdot (\overline{P}_{\text{l,cap}} - \min\{\overline{P}_{\text{l,cap}}\}) \tag{6.17}$$

$$c_4 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{cap}} \cdot (\max\{\overline{P}_{\text{l,cap}}\} - \overline{P}_{\text{l,cap}}) \tag{6.18}$$

All capacitor banks of the CC-MMC and BC-MMC are equipped with the film capacitor B25620B1198K103 from TDK. Each capacitor provides a capacitance of $1.9\,\text{mF}$, an ESR of $1.3\,\text{m}\Omega$ and a thermal resistance of $1.4\,\text{K} \cdot \text{W}^{-1}$. The expected lifetime is approximated with $100{,}000\,\text{h}$ at an operating temperature of $75\,°\text{C}$. Each capacitor is rated for voltages up to $1100\,\text{V}$ and for currents up to $34.4\,\text{A}$ in continuous operation. An overall capacitance of $30.4\,\text{mF}$ and a nominal current of $550.4\,\text{A}$ is obtained by parallel connection of 16 capacitor units to fulfill the requirements of the MMC STATCOM study cases.

The instantaneous power losses of the capacitor banks in each CC-SM can be calculated based on the overall ESR, the arm current and the switching state according to (6.19). Only inserted SMs ($S_{\text{CC}} = 1$) are loaded by the arm current. Accordingly, the BC-SMs are loaded for the switching states $S_{\text{BC}} = 1$ and $S_{\text{BC}} = -1$.

$$P_{\text{l,cap}} = S_{\text{CC}} \cdot R_{\text{esr}} \cdot i_{\text{arm}}^2 \tag{6.19}$$

The introduced thermal management for the storage capacitors can be applied for both the CC-MMC and the BC-MMC. The effectiveness is exemplary demonstrated for the CC-MMC whose arm current spectrum is exemplary shown in Fig. 6.38 for nominal STATCOM operation. The most significant components can be identified at $50\,\text{Hz}$ (half of the grid current) and at $100\,\text{Hz}$ (circulating current).

For the ideal case the capacitance and the ESR are completely identical for each SM capacitor, neglecting tolerances which can occur due to manufacturing and degradation processes. The parameter distribution is depicted in Fig. 6.39 for all SMs in one arm.
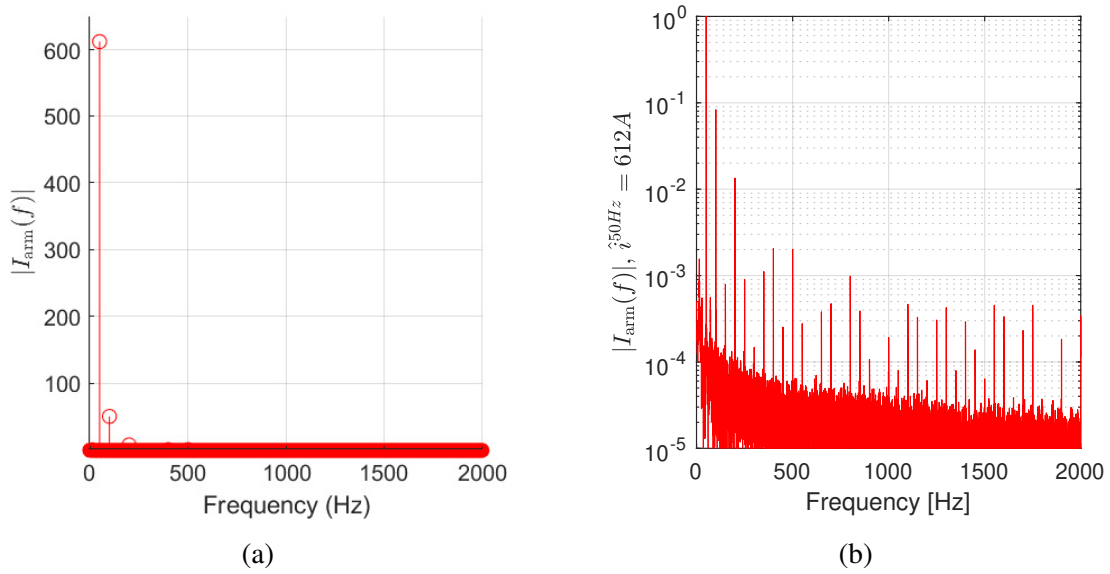
Figure 6.38: Spectrum of the arm current ($Q_g = 30\,\mathrm{Mvar}$): (a) Linear scale. (b) Logarithmic scale.
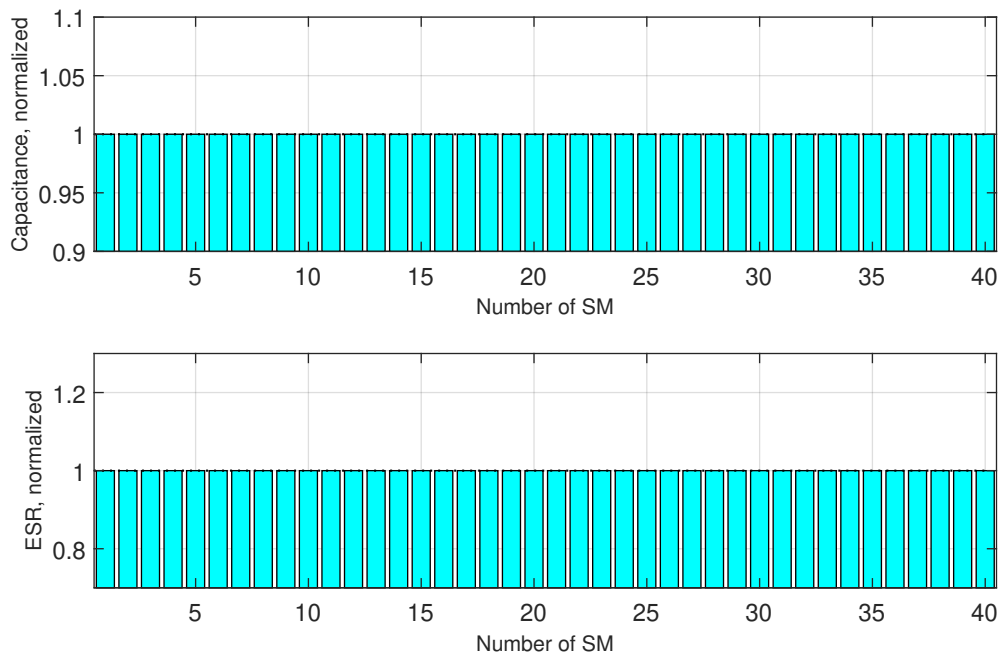
Figure 6.39: Idealized distribution of capacitances and ESR in the SM capacitor banks (CC-MMC).

The main goal for the thermal management of the capacitors can be seen in the stress regulation among the different SMs to also balance the relative lifetimes for prolonged maintenance intervals. The distribution of the normalized losses for the conventional CVB is depicted in Fig. 6.40. Taking into account longer time intervals, the losses become more and more similar among the SMs due to the identical parameters. Different to the semiconductor devices the thermal time constants of bulky capacitor storages are much higher and therefore short-term deviations among the SMs would be filtered up to a certain degree.

(a)

(b)

(c)

(d)
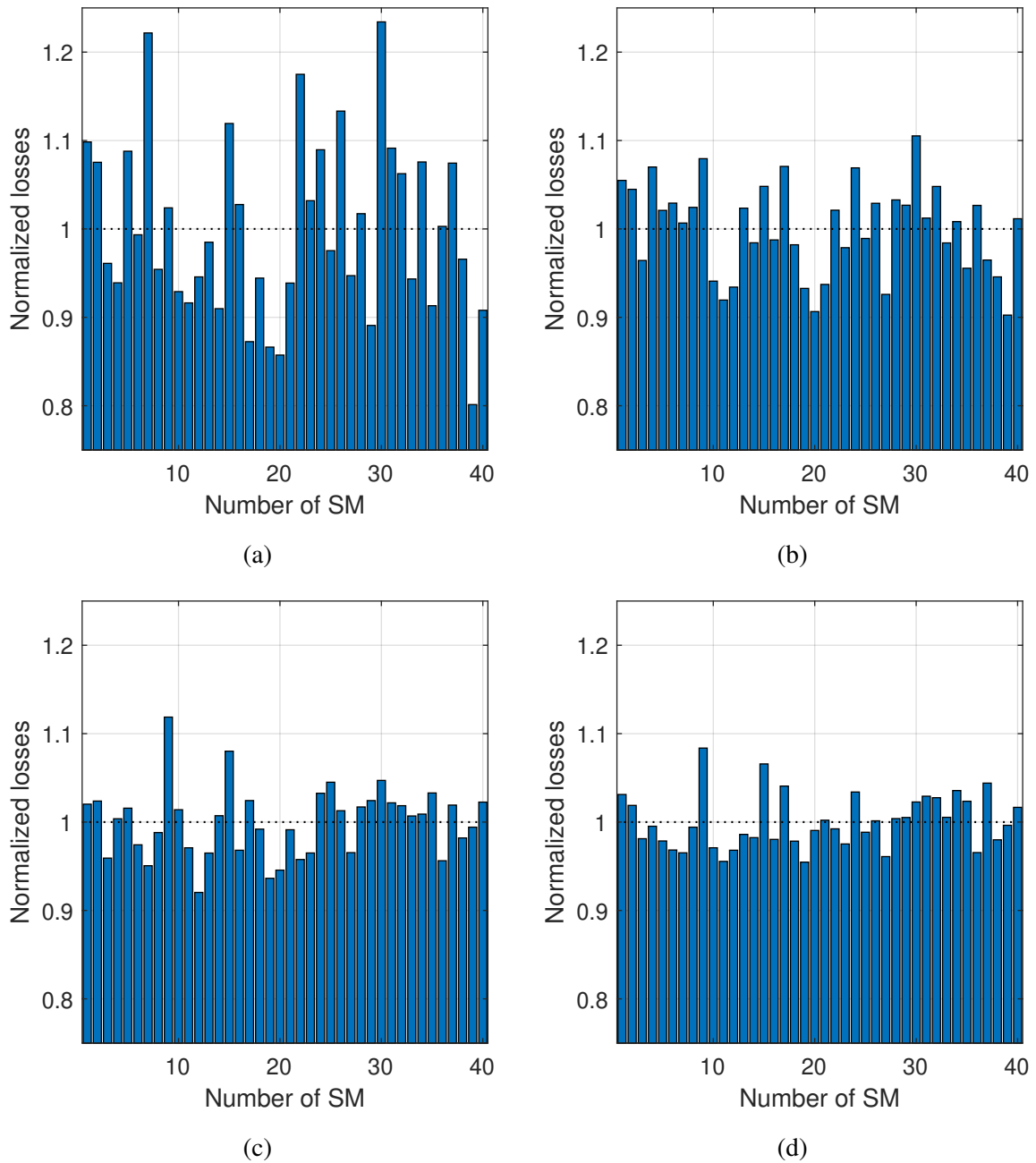
Figure 6.40: Normalized losses (CC-MMC, standard operation), time intervals: (a) 2 s. (b) 5 s. (c) 10 s. (d) 15 s.

The relative lifetimes based on time intervals of 5 s and 15 s are depicted in Fig. 6.41. Although the lifetimes are balanced up to a certain degree, small differences can still be observed even after time intervals of 15 s and more, since the power losses are not effectively regulated. Compared to this, the balancing of the power losses and of the relative lifetimes can be further improved and accelerated as exemplary demonstrated in Fig. 6.42 for a time interval of 5 s.

(a)   (b)
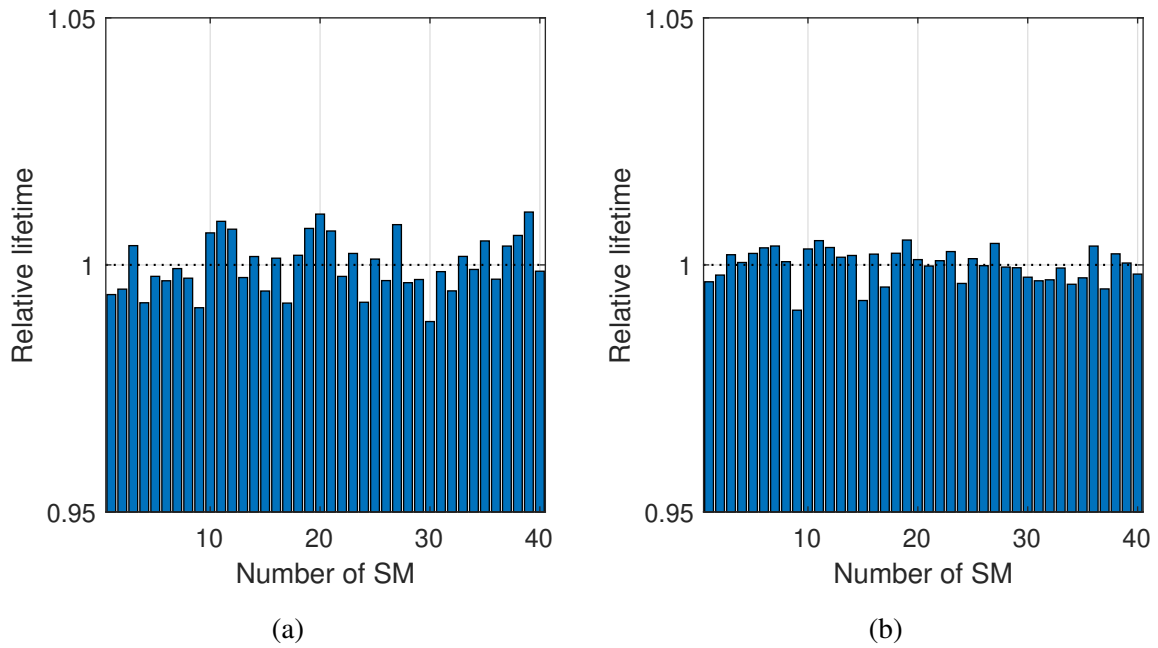
Figure 6.41: Relative lifetimes (CC-MMC, standard operation) for time intervals of: (a) 5 s. (b) 15 s.

(a)   (b)
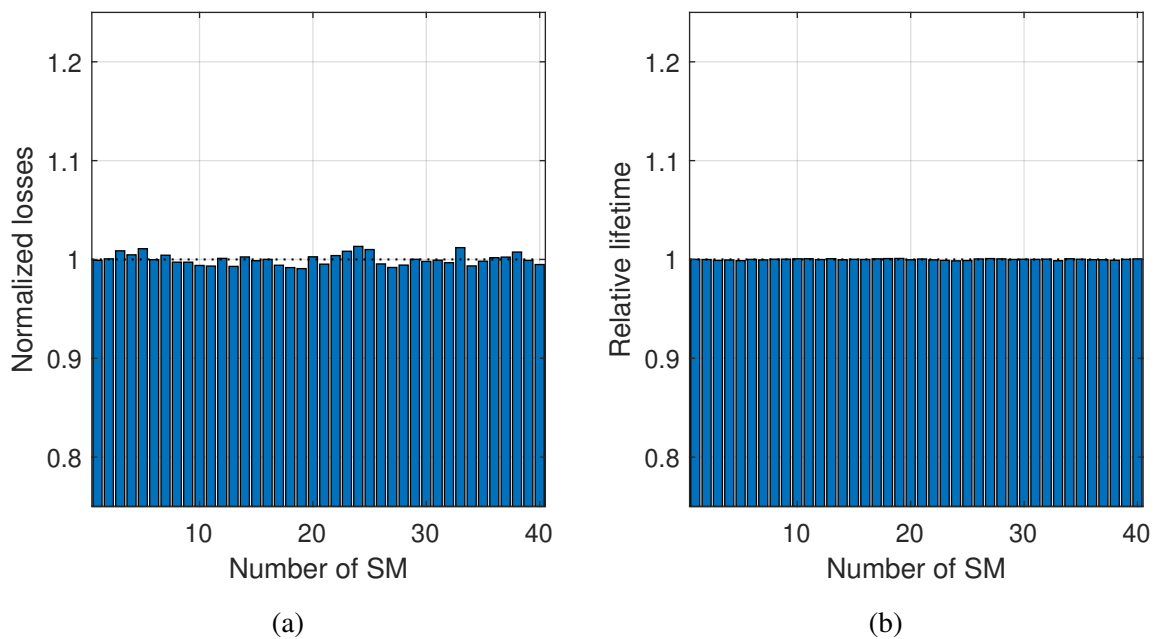
Figure 6.42: Relative lifetimes (CC-MMC, time interval: 5 s): (a) Standard operation. (b) Thermal management.

In a realistic practical application, the capacitance is not equal for each single SM. Instead, there is a small spread in the capacitance due to manufacturing tolerances being illustrated in Fig. 6.43 where a tolerance of up to $\pm 5\%$ is assumed among the SMs.

In standard operation the capacitor banks with higher capacitances are more loaded than capacitor banks with lower capacitances since the capacitor voltages are changing slower. Therefore, the conventional CVB algorithms are acting later on SMs with high capacitances
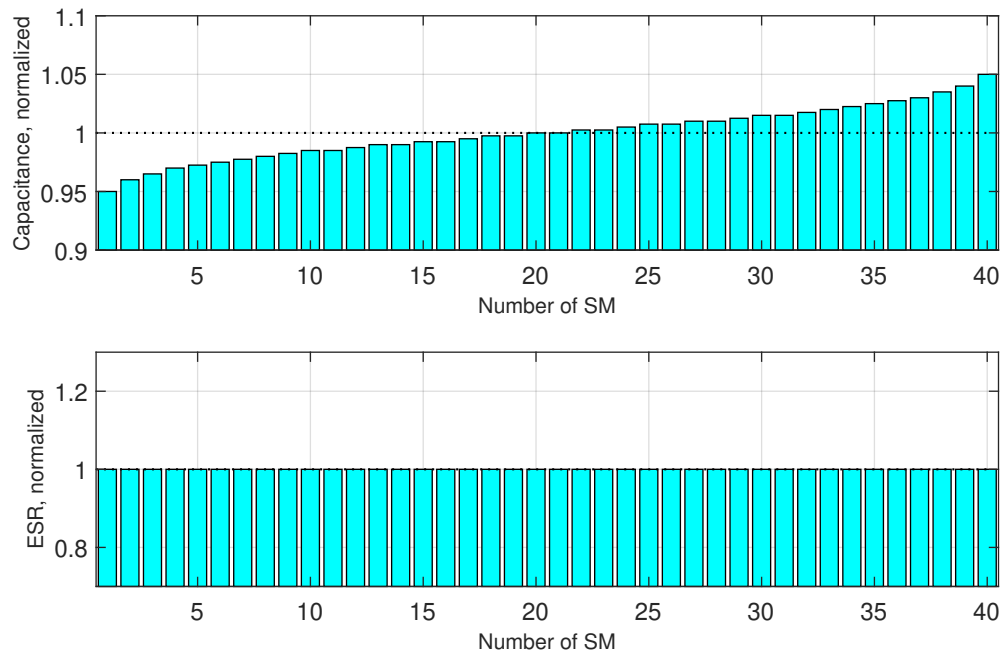
Figure 6.43: Distribution of capacitances and ESR in the SM capacitor banks (CC-MMC) with manufacturing tolerances (capacitances: 95 %...105 %).
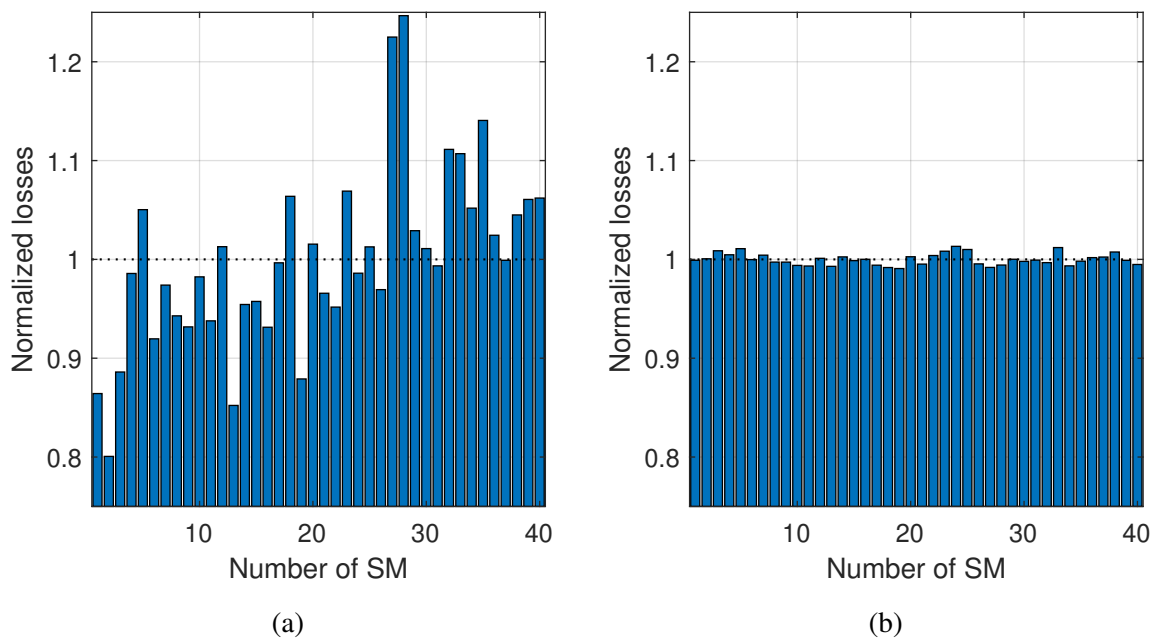
Figure 6.44: Normalized losses (CC-MMC, time interval: 5 s): (a) Standard operation. (b) Thermal management.

as long as no further useful decision criteria is taken into account. Consequently, the normalized losses tend to be higher as illustrated in Fig. 6.44.

Instead, by the introduced thermal management the differences in the normalized losses can be neutralized since not only the capacitor voltages but also the capacitor losses are balanced among all SMs. Consequently, also the lifetime expectations are further equalized
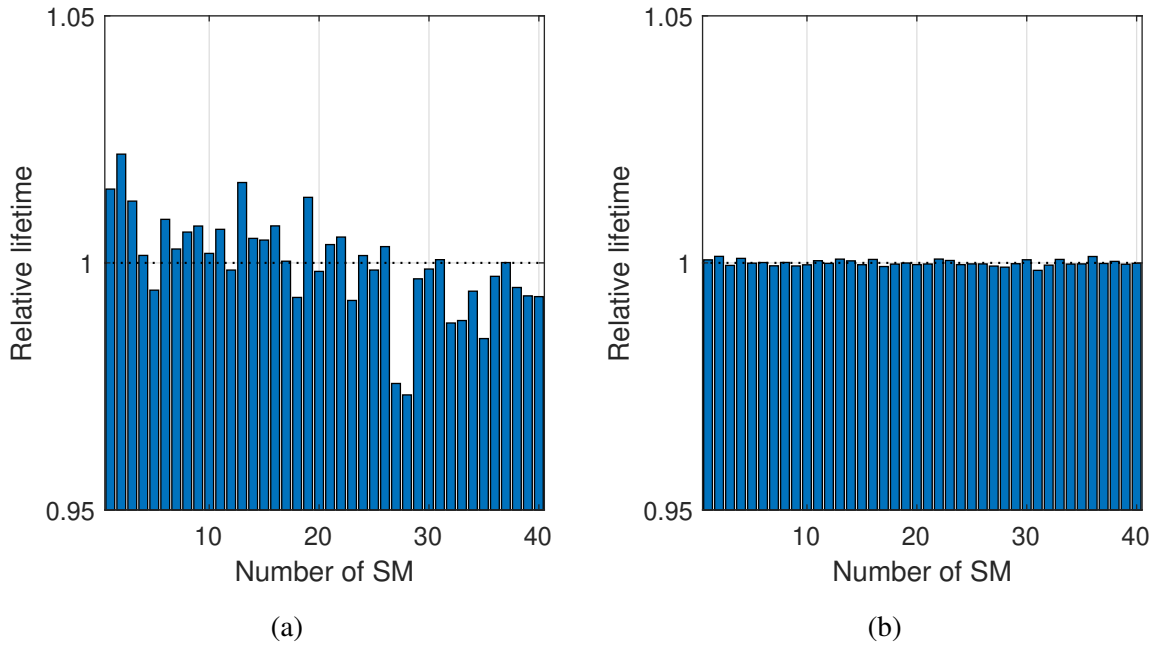
Figure 6.45: Relative lifetimes (CC-MMC, time interval: 5 s): (a) Standard operation. (b) Thermal management.
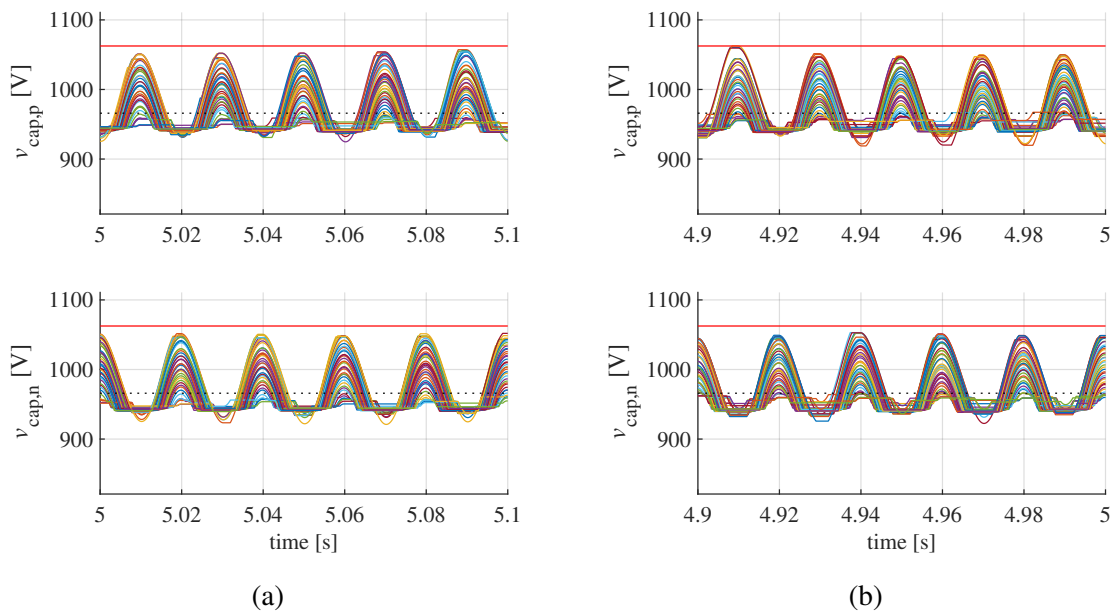
Figure 6.46: Capacitor voltages in one arm: (a) Standard operation. (b) Thermal management

by the thermal management as shown in Fig. 6.45. The power losses of the SM capacitor storages are effectively regulated by the thermal management without affecting the spread of the capacitor voltages as demonstrated in Fig. 6.46. This is particularly important for film capacitors since the applied voltage profile is one of the main degradation parameters beside the temperature and the humidity. It becomes obvious that the system performance and stability are not affected at all with the selected weighting factors.
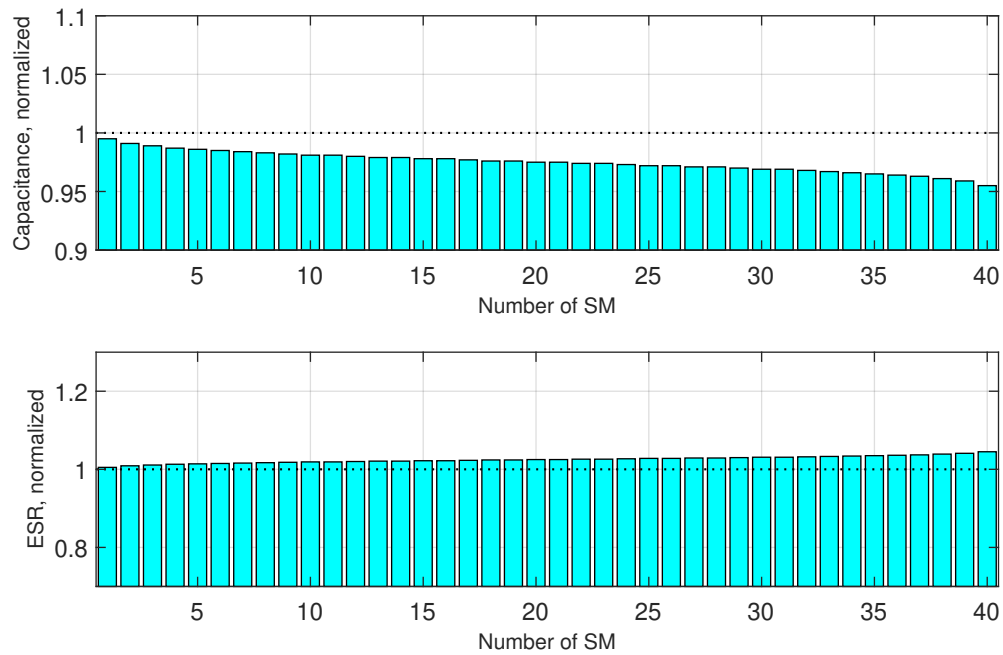
Figure 6.47: Distribution of capacitances and ESR in the SM capacitor banks (CC-MMC) taking into account aging processes (capacitances: 95 %...100 %, ESR: 100 %...105 %).

In the next step the aging of the capacitors is taken into account. Aging mechanisms are mainly linked to a decrease of the capacitance and an increase of the ESR. Tolerances of up to 5 % are assumed for the capacitance and it is assumed that the capacitor storages will be replaced after reaching this threshold. The relation between the capacitance and the ESR can differ depending on the selected capacitor type and the predominant aging mechanisms. Tolerances of up to 5 % and of up to 20 % are considered to evaluate its impact on the thermal behavior.

First, the distribution of the capacitances and the ESR are depicted in Fig. 6.47 with tolerances up to 5 %. The power losses of the capacitors are properly regulating by the thermal management as demonstrated in Fig. 6.48. Consequently, the expected lifetimes are perfectly balanced by the approach as illustrated in Fig. 6.49.
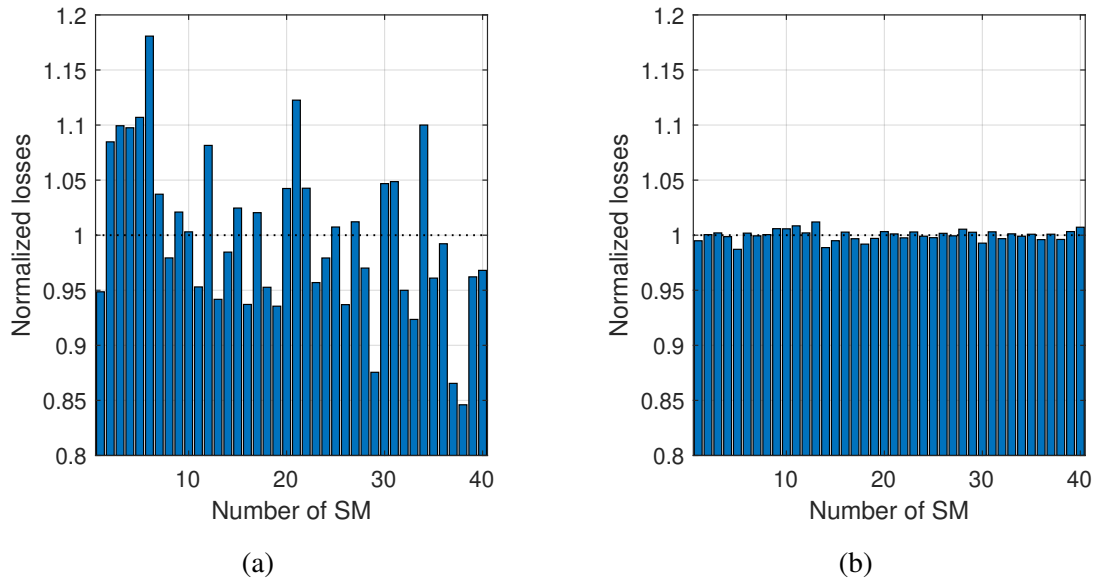
Figure 6.48: Normalized losses (CC-MMC, time interval: 5 s): (a) Standard operation. (b) Thermal management.
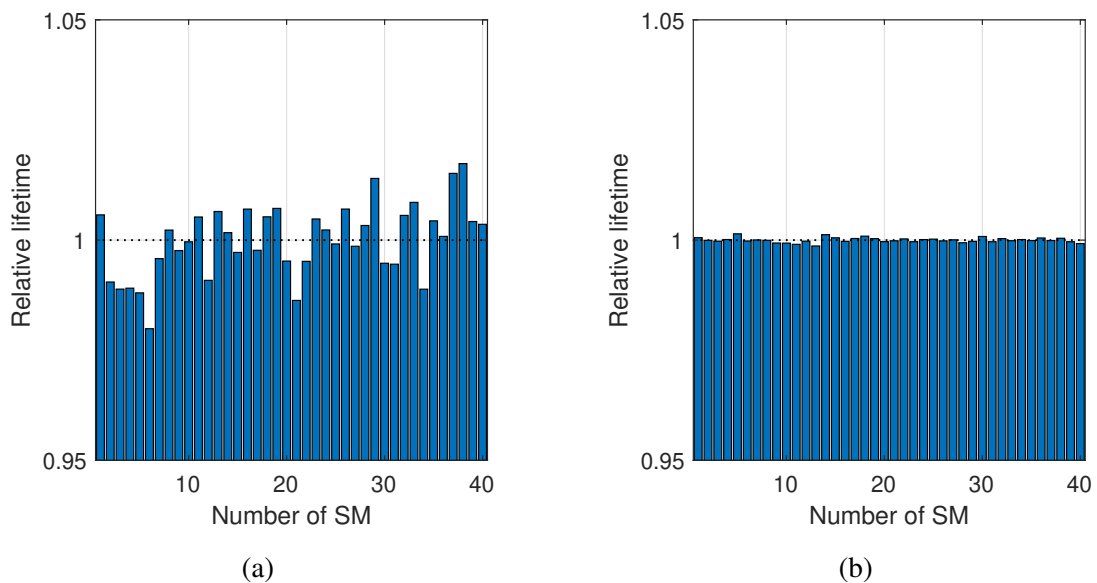
Figure 6.49: Relative lifetimes (CC-MMC, time interval: 5 s): (a) Standard operation. (b) Thermal management.

ESR values with tolerances of up to 20 % are depicted in Fig. 6.50. The spread in the distributed losses and the relative lifetimes are depicted in Fig. 6.51. Independent from the ESR parameter tolerances the thermal management of the capacitors is working very effectively.

In general, the thermal management of the capacitors is not affecting the system performance and efficiency at all if the weighting factor is selected carefully. Even if the temperatures and the lifetimes of the capacitor storages are already balanced up to a certain degree due to long thermal time constants the performance has been further improved by equalizing the thermal stress of the components. The thermal management approach becomes particularly effective
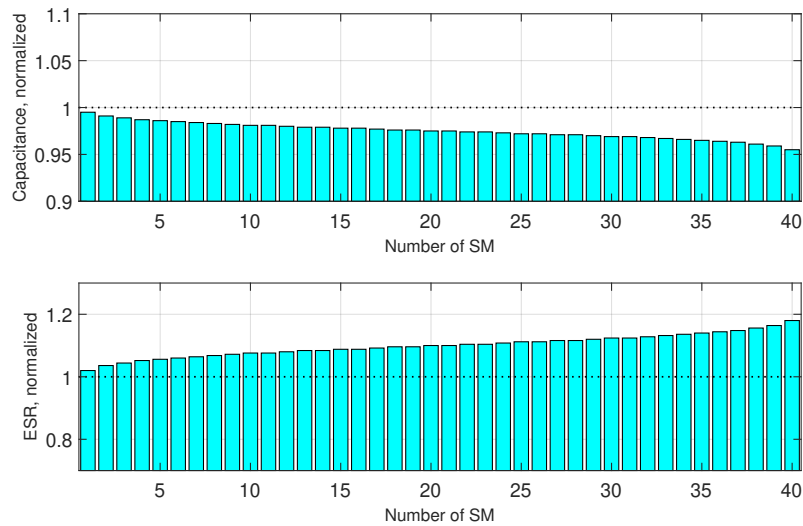
Figure 6.50: Distribution of capacitances and ESR in the SM capacitor banks (CC-MMC) taking into account aging processes (capacitances: 95 %...100 %, ESR: 100 %...120 %).

(a)

(b)

(c)

(d)
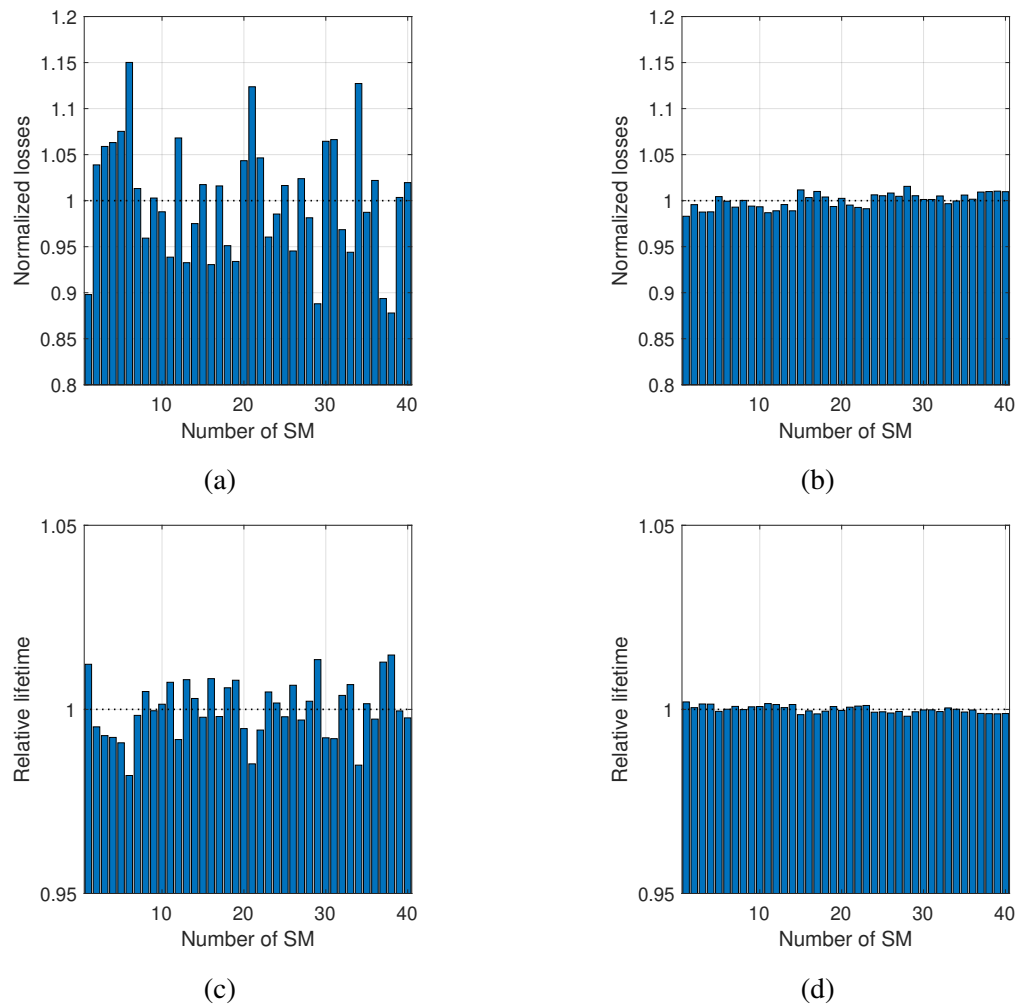
Figure 6.51: Normalized losses and relative lifetimes (CC-MMC, time interval: 5 s): (a,c) Standard operation. (b,d) Thermal management.

for higher tolerances in the system. However, also for very small tolerances the suggested approach provides high potential, e.g. for active thermal control approaches. For instance, in a real application different health conditions of the capacitors can be assumed already due to different physical ages after having replaced the first SMs after commissioning. In a practical application the expected remaining capacitor lifetimes could be monitored by its electric behavior (capacitance, ESR) and could be controlled by the load of the capacitors.

6.5 Thermal Management of Submodules

For an optimized thermal management not only either the semiconductor stress or the capacitor stress should be balanced. Instead, the thermal management should be applied to both the semiconductor devices and the capacitor storages. For the semiconductor devices it is worth to note that the thermal time constants are relatively small. Therefore, its thermal management needs to be properly weighted to react fast enough without affecting the performance of the system. Instead, the capacitor storages are linked to very high thermal time constants and the weighting of its thermal management can be selected very small. Both optimization goals can be combined very well due to the different time constants.

6.5.1 CC-MMC

For the CC-MMC all optimization goals can be combined in each of the cost functions according to (6.20)-(6.23).

$$c_1 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{cap}} \cdot (\overline{P}_{\text{l,cap}} - \min\{\overline{P}_{\text{l,cap}}\}) + \alpha_{\text{D1}}(T_{\text{j,D1}} - \min\{T_{\text{j,D1}}\}) \quad (6.20)$$

$$c_2 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{cap}} \cdot (\max\{\overline{P}_{\text{l,cap}}\} - \overline{P}_{\text{l,cap}}) + \alpha_{\text{T2}}(T_{\text{j,T2}} - \min\{T_{\text{j,T2}}\}) \quad (6.21)$$

$$c_3 = (\max\{v_{\text{cap}}\} - v_{\text{cap}}) + \alpha_{\text{cap}} \cdot (\overline{P}_{\text{l,cap}} - \min\{\overline{P}_{\text{l,cap}}\}) + \alpha_{\text{T1}}(T_{\text{j,T1}} - \min\{T_{\text{j,T1}}\}) \quad (6.22)$$

$$c_4 = (v_{\text{cap}} - \min\{v_{\text{cap}}\}) + \alpha_{\text{cap}} \cdot (\max\{\overline{P}_{\text{l,cap}}\} - \overline{P}_{\text{l,cap}}) + \alpha_{\text{D2}}(T_{\text{j,D2}} - \min\{T_{\text{j,D2}}\}) \quad (6.23)$$

As demonstrated in Fig. 6.52 both the semiconductor temperatures as well as the capacitor losses have been optimized.

6.5.2 BC-MMC

For the BC-MMC it is advantageous to combine the thermal management of the semiconductor devices by the optimized mixed NLM switching sequences with the SM selection based on the capacitor voltages and the capacitor losses. As demonstrated in Fig. 6.53 the thermal behavior of the semiconductors and the capacitors have been optimized, as well and can be used for an economical design, overload capability and reliable operation.
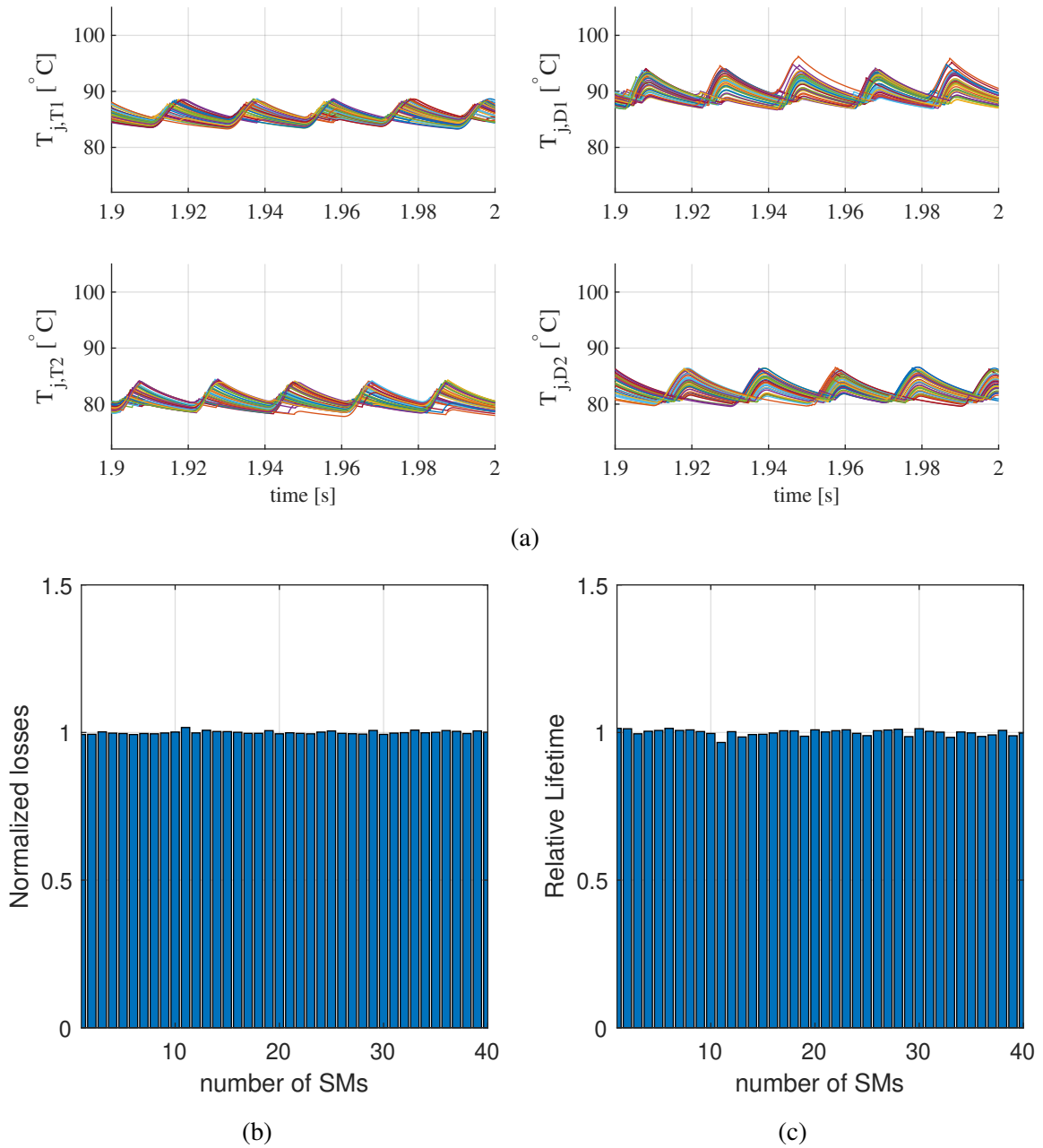
Figure 6.52: Combined thermal management for semiconductor devices and capacitor storages ($\alpha = 50$, $\alpha_{\mathrm{cap}} = 0.5$) for the CC-MMC (STATCOM, $Q_{\mathrm{g}} = 30\,\mathrm{Mvar}$): (a) Junction temperatures of semiconductors. (b) Normalized losses and relative lifetimes of capacitor storages.
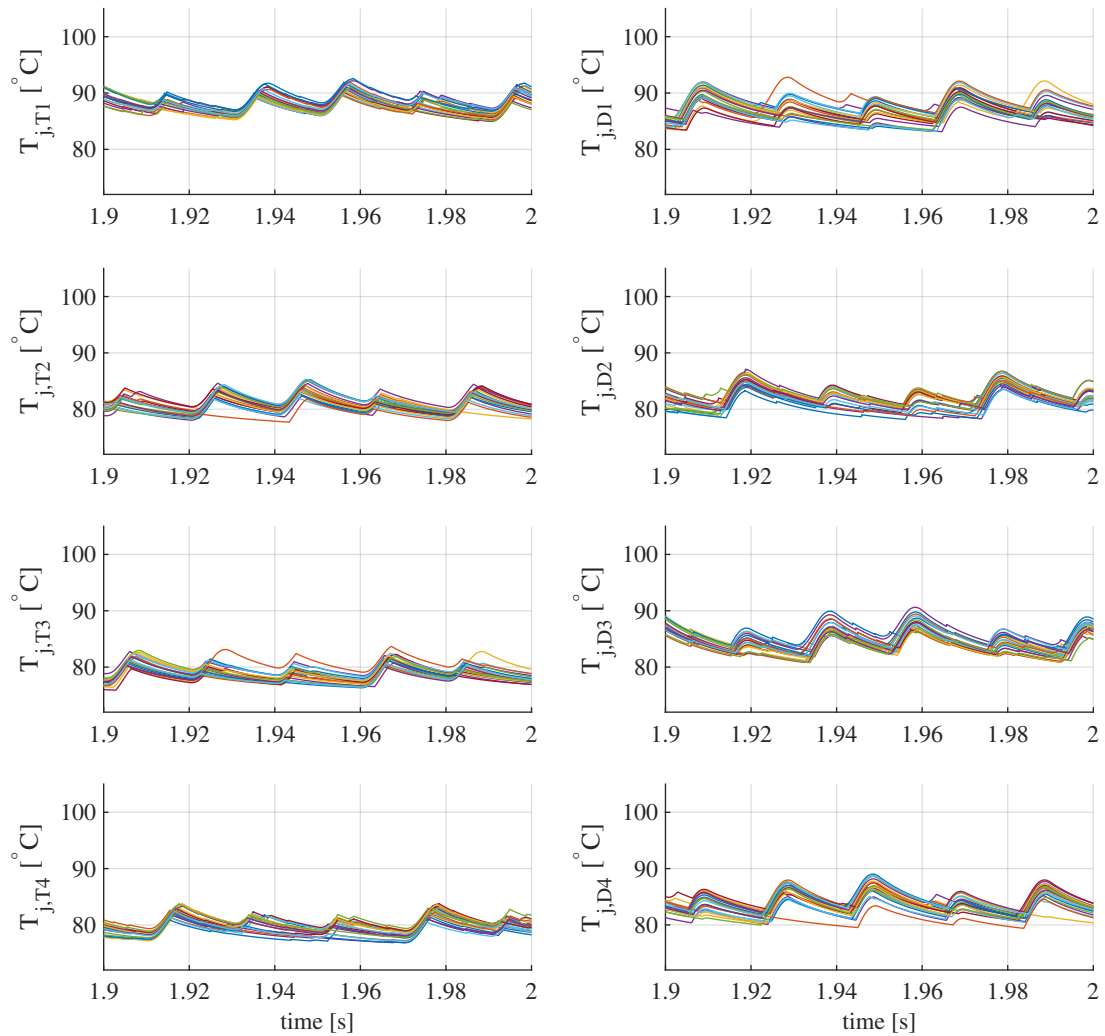
(a)
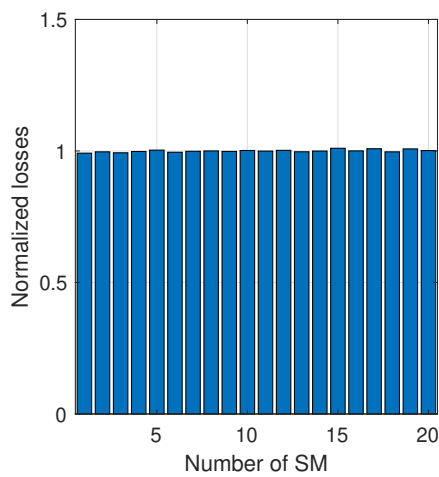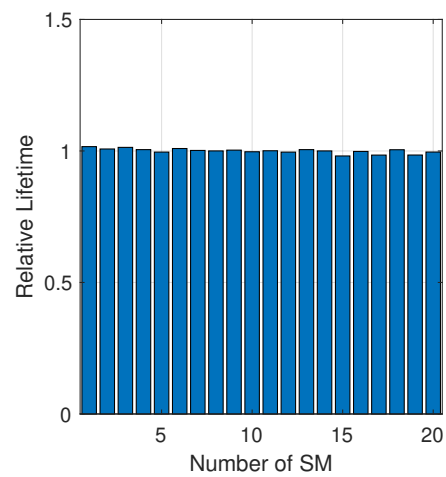
(b)   (c)

Figure 6.53: Combined thermal management for semiconductor devices and capacitor stor-
ages ($\alpha_{\mathrm{cap}} = 0.5$) for the CC-MMC (STATCOM, $Q_{\mathrm{g}} = 30\,\mathrm{Mvar}$): (a) Junction
temperatures of semiconductors. (b) Normalized losses and relative lifetimes of
capacitor storages.

6.6 Summary and Conclusions of the Section

A thermal management for the MMC has been introduced in this chapter, taking profit from the huge number of available redundant switching states for multi-objective optimization. The introduced approaches are not only taking into account the capacitor voltages of each SM but also the most relevant strain parameters of all semiconductor devices and capacitor storages. For the thermal management of the semiconductor devices two independent approaches have been introduced for the CC-MMC and for the BC-MMC. For the CC-MMC the thermal stress is shifted between the upper and lower semiconductor devices in each CC-SM by adopting the CVB algorithms by multi-objective cost functions for profiting from the highly redundant switching states in each MMC arm. Instead for the BC-MMC the thermal management is optimizing the modulation sequences to shift the thermal stress by the redundant switching states in each single BC-SM.

The extensive potential of the introduced approaches has been demonstrated for a MV STATCOM application as well as for an HVDC application. The maximum semiconductor temperatures have been reduced by up to 5 K in each single SM. Furthermore, thermal cycles have been reduced by up to 22 K (80 %) and fast strenuous temperature changes have been eliminated without affecting the overall system performance. The capacitor voltages are well balanced and the efficiency kept constant. It has been demonstrated that the achieved thermal optimizations cannot only be used for a more efficient design of all SMs but also to provide overload capability during normal or grid fault operation of up to 20 % at limited junction temperatures and strongly reduced thermal cycles. The expected semiconductor lifetimes have been approximately doubled at nominal power, enabling less semiconductor failures and extended maintenance intervals.

In addition to this, an own thermal management approach for the capacitor storages has been introduced, taking into account the averaged power losses, being directly linked to the temperatures and expected lifetimes. The capacitor losses have been perfectly balanced independent from parameter variations for both the CC-MMC and the BC-MMC. In this way, also the expected relative lifetimes have been equalized for enhanced reliability and service intervals. For an effective thermal management and high reliability of all crucial components the thermal management of the semiconductors and of the capacitors have been combined. In this way, the thermal stress of all SMs have been improved, enabling an economical design, overload capability and long component lifetimes without affecting the overall performance of the system. For real-time condition monitoring the modeling of power losses and temperatures have been introduced as well and the use of additional sensors can be completely avoided.

For practical evaluation and flexible cycling tests a universal experimental bench has been developed and introduced. By the presented experimental bench, the testing of huge MMC systems with hundreds or thousands of semiconductor devices can be avoided which would be neither practical nor economical. Instead, the mission profiles can be adopted to the different SMs and the practical evaluation and condition monitoring becomes even possible for HVDC applications as demonstrated. Both the electrical behavior and the temperature

distributions even on the semiconductor chips are monitored and recorded. The introduced experimental bench enables cycling tests of existing and future MMC systems for design optimizations as well as for improved temperature and lifetime modeling. Furthermore, testing of SMs under severe conditions as during fault or overload conditions and the detection of thermal hotspots becomes possible at high safety and limited costs.

7 Summary, Conclusion and Future Research

7.1 Summary and Conclusion

In this work modular power converters have been proposed for integration of high-power applications into the electric grid. They especially profit from their high modularity, multi-level waveform generation and high scalability to different power levels. A main potential for modular power converters has been identified in the proper use of the high number of available switching states, providing a high potential for reducing both, investment and operational costs of the converter systems. Based on the knowledge in terms of modular power converters, its controllability and reliability, the detailed behavior of huge converter systems have been investigated. Based on the provided analysis different approaches and algorithms have been proposed for multi-objective optimization by optimized modulation techniques and the introduced thermal management for highly efficient and highly reliable systems at very high power quality.

In Chapter 2 suitable inverter topologies for high-power applications have been reviewed for LV connection to a step-up transformer and for direct connection to the MV and HV grid. For LV connection the three-level NPC inverter has been identified as the preferred solution due to multilevel generation and increased blocking capability. Instead, for direct MV and HV connection the MMC has been selected, being scalable to different power levels. A wide variety for wind energy, STATCOM, DC transmission and grid impedance analysis have been considered and presented for further optimization.

Suitable multilevel modulation techniques have been investigated in Chapter 3 for both the three-level NPC inverter and the MMC. For the MMC the NLM has been identified as the preferred choice for highly efficient operation and suitable waveform generation. The NLM has been investigated for both the CC-MMC and the BC-MMC. Based on a deep analysis suitable switching patterns have been derived for a minimum number of commutations and taking into account the redundant switching states of the BC-SMs. For the application of parallel NPC inverters the well-established PD-PWM has been identified as the best choice for minimum harmonic distortion. However, this choice is not valid anymore for interleaved NPC inverters with a common DC link where the APOD-PWM has been introduced as the preferred modulation technique since circulating currents between both inverters has been strongly reduced at a comparable power quality.

In Chapter 4 one wind energy application and one grid impedance analyzer have been investigated based on parallel NPC inverters for LV connection to classical step-up transformers. The considered MV grid analyzer is a new and unique application, being able to inject monofrequent currents in a broad frequency range. The design process for the practical realization and the performance has been elaborated. Both applied systems have been optimized by interleaving modulation, achieving very low switching frequencies and a very small filter design. For very high powers the connection of NPC inverters reaches its limits because the

LV currents become huge. Therefore, especially for higher powers direct connection to the MV or HV grid can be seen as beneficial.

For direct connection to the MV and HV grid the MMC has been investigated and optimized in Chapter 5 for a STATCOM application and for DC transmission systems. For deep analysis, each single SM has been modeled, taking into account up to 150 SMs per arm. Both the electrical behavior of the CC-MMC and the BC-MMC for STATCOM have been investigated and compared from system level down to component level. It has been demonstrated that the capacitor storage sizes can be decreased a lot by the BC-MMC compared to the well-established CC-MMC. For all systems the NLM has been applied and fundamental switching frequencies have been achieved even for MV applications without additional AC filters. As an additional feature active power filtering capability has been implemented and investigated, properly generating currents up to 1000 kHz where the use of fast-switching PWM techniques also has been avoided.

In Chapter 6 a thermal management for the MMC has been introduced for further optimization just by the use of redundant switching states. Different algorithms have been developed for both the CC-MMC and the BC-MMC to minimize and to equalize the thermal stress within each semiconductor device and each capacitor. For the thermal management both the modulation and the CVB for SM selection can be optimized. For the semiconductor devices the modulation switching sequences have been optimized for the BC-MMC to profit from the redundant switching states in each SM. Instead for the CC-MMC the CVB has been optimized to also take into account the thermal stress of the semiconductor devices. Furthermore, the SM selection has been optimized for both MMC configurations to equalize the capacitor stress among all SMs.

By the introduced thermal management, the temperatures, thermal cycles and fast temperature changes have been significantly reduced just by software without any need for additional sensors. It has been demonstrated that the achieved optimizations can be exploited for a more economical design, significant overload capability and strongly increased lifetimes of the components. All the presented algorithms do not affect the system performance or efficiency of the system.

For experimental validation an experimental bench has been developed and introduced to emulate and monitor the behavior of single modular building blocks under reasonable, economical, safe and flexible conditions. The system can be used not only for SM emulation, thermal and lifetime modeling but also for testing under severe conditions, e.g. during faults or overload conditions. In Chapter 6 the experimental bench has been exemplary used for the evaluation and validation of an HVDC system with 150 SMs in one arm. Both the electrical and the thermal behavior have been recorded. Temperature hotpots and thermal cycles have been identified and optimized by thermal management algorithms.

7.2 Research Contribution

Contribution in the field of high-power applications

- One unique medium voltage grid impedance analyzer has been developed, being able to cover frequencies up to 10 kHz.

- Overload capability and active power filtering capability have been achieved for conventional STATCOM applications by control optimizations.

- An experimental bench has been developed and realized for flexible and safe testing of modular building blocks at a reasonable effort, which has been demonstrated for a high voltage application as a study case.

Contributions in the field of parallel NPC inverters

- A general design approach has been developed to provide high powers within a wide frequency range, e.g. applicable for grid analyzers and active power filters.

- The common-mode voltages and the circulating currents between parallel NPC inverters with common DC connection have been strongly reduced by proposing the APOD-PWM instead of the PD-PWM.

Contributions in the field of the MMC

- The MMC has been modeled for a flexible number of half-bridge (chopper-cells) and full-bridge (bridge-cells) submodules, taking into account the electrical and thermal behavior of each single component.

- Detailed comparison has been provided for both submodule configurations, highlighting the high potential for a more economical design by the latter one.

- Fundamental switching modulation techniques have been implemented with both submodule topologies for full-scaled system.

- Thermal management approaches based on redundant SM selection have been introduced for the MMC for an economical design and long service times without affecting the system performance and having opened a highly regarded new research field.

- Several algorithms have been introduced for the thermal management of the MMC with half-bridge (chopper-cells) and full-bridge (bridge-cells) submodules, taking into account not only the semiconductor devices but also the capacitor storages.

7.3 Future Research

Modular power inverters provide high potential for advanced control in renewable energy systems, STATCOM applications and transmission solutions at highly efficient and highly reliable operation. For these purposes, the thesis has proposed new strategies and concepts for improved modulation and thermal management approaches.

The following research topics are proposed for potential future research:

- The proposed and realized MV grid impedance analyzer is able to strongly extend the amount of available data for the MV grid. A second version of the MV grid impedance analyzer could be realized based on new insights, optimizing the frequency range and the required current injection for a tailored grid excitation. Furthermore, the system could be further optimized by direct connection to the MV grid to avoid high voltage drops and the usage of bulky transformers. With the help of wide-band gap devices a more compact design and higher switching frequencies could be achieved to minimize the pollution of the grid which would be particularly beneficial for possible commercialization.

- The applied modulation techniques for modular power inverters could be further optimized, e.g. by discontinuous modulation, space vector modulation or hysteresis bands, allowing higher degrees of freedoms for multi-objective optimization. Further potential can be also exploited by model predictive control, taking into account the future behavior of the system.

- For the thermal management of the MMC expected component lifetimes could be taken into account as control parameters. Condition monitoring could be applied by using advanced methods for the detection of the collector-emitter voltages (semiconductors) or impedance spectroscopy (energy storages). In addition, further stress parameters can be taken into account for evaluating the degradation processes, e.g. the humidity for offshore applications. Thermal cycling can be applied by the experimental bench to optimize the temperature and lifetime models. The SM selection could be further optimized by artificial intelligence and reinforced learning approaches.

- For the design of multilevel inverters WBG devices provide future potential. SiC MOSFET technology potentially enables significantly higher blocking voltages, lower conduction losses at partial load and strongly reduced switching energies. Accordingly, the number of cascaded semiconductor devices could be reduced to achieve a specific grid voltage level. Furthermore, power inverters with limited number of voltage levels could profit from high switching frequencies to achieve high power qualities and very small filters, even for harmonic injection. For the MMC the application of low-switching modulation techniques could be avoided to limit the variations in the capacitor voltages and in the semiconductor temperatures by the modulator itself.

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11 Curriculum Vitae

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