Accurate Numerical Modelling of MV and HV Resistive Dividers

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Accurate Numerical Modelling of MVand HV Resistive Dividers

M. Zucca, M. Modarres, D. Giordano, and G. Crotti

***Abstract* — An effective computational tool for the simulation and design of voltage dividers has been realized. It takes advantage from a finite element procedure for the accurate computation of the divider stray capacitances. These latter are then the input of a circuit solver procedure based on the modified node potential technique, which provides the divider frequency response. Furthermore, a test divider has been set up for the purpose of the tool validation. A very good agreement has been found between measured and computed results.**

This paper highlights that a correct representation of the resistors is necessary in the FEM model, during the computation of the stray parameters. This issue has been clarified for the first time in this paper. In addition, a comparison between FEM and BEM methods has been carried out before the implementation of the numerical code, stating the superior effectiveness of FEM.

The computational tool has been finally tested on a real voltage divider. Good results have been found in terms of computational accuracy. Limited discrepancies between measured and computed results have been found up to 10 kHz, being 5.7 % for the scale factor and less than 24 mrad for the phase errors.

***Index Terms*— Boundary element analysis, finite element analysis, numerical simulation, voltage divider, voltage measurement.**

I. Introduction

The continuous increase of the electrical energy produced by small and distributed generation plants from renewable sources, directly connected to the medium voltage (MV) distribution grid, requires reliable and continuous managing of the MV network. To this end, a widespread monitoring of the electrical quantities in a much greater number of nodes than required in the past should be ensured [1]. Moreover, the liberalization of the energy market in many countries has increased the importance of the accurate estimation of energy flows in the grid [2] and the monitoring of the power quality parameters.

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Voltage/current transducers have to be used to correctly scale the values of the measured quantities to levels compatible with those of measuring instruments. Following the evolution of the MV grid, good performances in terms of linearity and frequency response become a more stringent requirement [3]-[4]-[5] for these devices. This scenario gives rise to two different scientific approaches: the development of techniques to improve the performances of already installed inductive voltage and current measurement transformers [6]-[7] or the development of new voltage and current transducers able to match good metrological performances, with reduced dimensions and cost [8]-[9].

The new architecture of “smart” substations no longer requires the use of transducers with output power able to feed the protection or measurement devices [10]-[11]. This allows the use of devices to attenuate the high voltage and current, such as resistive/capacitive dividers and optical sensors, for the voltage attenuation and Rogowski coils and resistive shunts for the current measurement.

The paper focuses the attention on MV resistive voltage dividers, although the results here presented can be extended to capacitive/resistive and to HV dividers. The frequency response and the accuracy of a voltage divider (VD) strongly depend on parasitic parameters and, in particular, on stray capacitances. The stray capacitive couplings of the divider components are determined by the VD geometry and significantly degrade its frequency performances. A suitable design of the divider can increase its linearity and the flatness of its frequency response. To this end, a specific tool, which allows the accurate calculation of stray parameters and the evaluation of their effect on the resulting frequency response, would strongly facilitate the geometry optimization in the design phase.

In an actual VD several stray capacitive couplings occur, such as those between conductors, resistor bodies, and between the conductors and the resistor bodies. However, it is not a common approach to fully calculate such stray capacitances when simulating a VD [12]-[13]-[14]-[15]. For example, in [16] the capacitances in the HV arm are estimated starting from the tuned LV capacitance and the 2-D FEM simulation is done to choose the better shield minimizing the effect of stray capacitances. The work [17] approximates an estimate constant value for stray capacitances between resistors and between resistor and the electrode. In [18] the parameters of the stray-capacitance equivalent circuit are chosen in such a way that, with all resistive and inductive elements of the divider removed; the total input capacitance of the equivalent circuit is equal to the input capacitance of the divider. So, the circuit components are not considered in the

model. In [19] an HV resistive divider made of five 200 kV modules is surrounded by a capacitive path, which acts as a shield. A 3D FEM modeling approach is utilized to determine the optimal capacitive grading that minimizes the response time of the system. Capacitors are modeled but nothing is said about the resistor modeling. In other cases, arrangements for the reduction of stray capacitance effects are proposed following experimental verifications [20].

An effective computational tool for the simulation and design of voltage dividers is presented in this paper. It allows the computation of the frequency performance of the divider, from a circuital model including the calculated stray parameters. The stray capacitive couplings are numerically computed through a three dimensional (3D) FEM approach, starting from the divider geometry. An increase of the simulation accuracy is enabled by the much higher level of detail in the evaluation of the stray couplings, if compared with other approaches, as shown by the validation of the tool carried out by comparison with dividers of known geometry.

After a brief description of the numerical tool, a comparison between FEM and BEM methods is carried out before the implementation of the numerical code. The model is then validated by making use of a test set-up specifically developed. In particular, the influence of the resistor bodies and their modeling on the accuracy of the results in terms of the envisaged frequency response of the VD is investigated. Finally, the proposed approach is applied to the simulation of the frequency behavior of an actual 20 kV resin insulated VD, which confirms how the modelling of the resistor surface is of crucial importance for the accuracy level of the simulation.

II. NUMERICAL TOOL

The output of the proposed numerical tool is the frequency behavior of the scale factor K and phase error $\Delta\varphi$ of a VD. These two parameters define the metrological performance of a transducer being

$$K = \frac{U_p}{U_s} \qquad \Delta\varphi = \varphi_s - \varphi_p \tag{1}$$

where U_s and φ_s are the magnitude and phase of the secondary voltage while U_p and φ_p identify the primary voltage phasor.

The numerical tool is constituted by two modules. In the first one, the stray capacitive couplings between the electrodes, or in general between the conductive parts of the divider, are computed. The outcomes of such a module are input to the second one, which deals with the solution of the equivalent electrical circuit of the VD.

As a preliminary analysis, an investigation between the effectiveness of the two most common numerical techniques: Finite Element and Boundary Element methods is carried out. The results are shown and discussed in the following subsections.

A. Finite Element and Boundary Element Approach

The finite element approach here considered is a standard 3D approach, where the unknown is the electric scalar potential ϕ defined as $\mathbf{E} = -\nabla\phi$. The divergence of the electric flux density D is linked to the charge density ρ through the well-known Poisson equation. The governing law of the electrostatic field is

$$-\nabla\cdot(\varepsilon\cdot\nabla\phi) = \rho \tag{2}$$

where ε is the dielectric permittivity. This paper takes advantage of the implementation of eqn. (2) through the commercial well known and validated FEM code Opera 3D, by Cobham. Conversely, the implementation of the code BEM done at INRIM, by means of the code Sally 3D, is considered.

The BEM approach originates from the scalar form of the Green theorem applied to a volume V having boundary Ω, which is

$$\int_V (\psi\cdot\nabla^2\phi - \phi\cdot\nabla^2\psi)\,\mathrm{dv} = \int_\Omega (\psi\frac{\partial\phi}{\partial n} - \phi\frac{\partial\psi}{\partial n})\cdot\,\mathrm{ds} \tag{3}$$

where ψ is the Green scalar function defined as $\psi(\mathrm{P},\mathrm{P}') = \frac{1}{4\pi r}$, being r the distance between the computational point P and the source point P'.

It is easy to verify that the Laplacian of the Green function is null and the following equation can be obtained as

$$\zeta\ \phi(\mathrm{P}) = \int_{\Omega'} \left(\psi\ \nabla\phi\cdot\mathbf{n} - \phi\ \nabla\psi\cdot\mathbf{n}\right)\mathrm{ds} + \int_V \frac{\rho}{\varepsilon}\ \psi\ \mathrm{dv} \tag{4}$$

where the coefficient ζ is equal to 0.5 on the boundary Ω and is 1 inside the volume V. Eqn. (4) gives the potential in the computational point by introducing the continuity conditions between the media (a) and (b), these last divided by surface Ω,

$$\phi^{(a)} = \phi^{(b)}; \qquad \varepsilon^{(a)}\left\{\nabla\phi^{(a)}\cdot\mathbf{n}^{(a)}\right\} = -\varepsilon^{(b)}\left\{\nabla\phi^{(b)}\cdot\mathbf{n}^{(b)}\right\} \tag{5}$$

For each *i-th* discretization element four unknowns are identified, $\phi_i^{(a)}$, $\phi_i^{(b)}$, $(\nabla\phi_i^{(a)}\cdot\mathbf{n}_i^{(a)})$ and $(\nabla\phi_i^{(b)}\cdot\mathbf{n}_i^{(b)})$, which reduce to two by applying eqn. (5). More details can be found in [21].

B. Stray capacitance matrix

The computation of the stray capacitance network can be carried out starting from the electrode voltages or from the electrode potentials. In the first case, within n+1 electrodes/conductors one of them must be chosen as a reference. In this case, the direct computation of the so called "circuital matrix" is performed, as specified at the end of this subsection. In the second case, no reference conductor/electrode is selected and the capacitance matrix of

the system is the so called "generalized capacitance matrix" (6).

$$\begin{bmatrix} q_1 \\ \vdots \\ q_{n+1} \end{bmatrix} = \begin{pmatrix} \mathcal{C}_{11} & \mathcal{C}_{12}\cdots & \mathcal{C}_{1,n+1} \\ \vdots & \ddots & \vdots \\ \mathcal{C}_{n+1,1} & \mathcal{C}_{n+1,2}\cdots & \mathcal{C}_{n+1,n+1} \end{pmatrix} \cdot \begin{bmatrix} \phi_1 \\ \vdots \\ \phi_{n+1} \end{bmatrix} \tag{6}$$

$\mathcal{C}_{ij}$ represents the generalized capacitance, ϕ_i and q_i are the potential and the charge of the *i-th* electrode respectively. In the FEM computation, the zero potential can be assigned to the far boundary elements, using Dirichlet boundary conditions. In the case of BEM, the boundary condition is implicit. In both cases, the computation of the generalized capacitance matrix is done by rows. Assigned a unitary potential to the *i-th* electrode and zero to the others, the capacitance $\mathcal{C}_{ij}$ is computed through the integral

$$q_j = \mathcal{C}_{ij} = \int_{\Omega j} \mathbf{D}\cdot\mathbf{n}\cdot ds \quad \begin{cases} \text{being: } \phi_i=1 \text{ and } \phi_j\big|_{j\neq i}=0; \\ \quad i=1, 2 ..., n+1 \\ \textit{and } \phi_{boun}=0 \text{ at the boundary} \end{cases} \tag{7}$$

where Ω_j is the surface of the electrode j.

The generalized matrix cannot be directly used for the circuit solution. A circuital matrix is needed and the transformation from the generalized capacitance matrix to the circuital matrix can be done, without loss of generality, by the choice of one conductor/electrode as a reference electrode with zero potential. By choosing the *n*+1 conductor as a reference the terms of the circuital matrix can be computed as

$$C_{ij} = \mathcal{C}_{ij} - \frac{\left(\sum_{k=1}^{n+1} \mathcal{C}_{ik}\right)\cdot\left(\sum_{m=1}^{n+1} \mathcal{C}_{mj}\right)}{\sum \mathcal{C}} \tag{8}$$

where the circuital matrix is

$$\begin{bmatrix} q_1 \\ \vdots \\ q_n \end{bmatrix} = \begin{pmatrix} C_{11} & C_{12}\cdots & C_{1,n} \\ \vdots & \ddots & \vdots \\ C_{n,1} & C_{n,2}\cdots & C_{n,n} \end{pmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \tag{9}$$

and

$$V_j = \phi_j - \phi_{n+1} \tag{10}$$

According to [22] the circuital matrix (9) can be directly computed as follows. When $i = j$ the equation (11) will be applied, while the equation (12) will be considered when $i \neq j$.

$$q_i = \sum_{j=1}^{n} C_{ij} = \int_{\Omega j} \mathbf{D}\cdot\mathbf{n}\cdot ds$$

$$\begin{cases} \text{being: } V_i=1 \text{ and } V_j\big|_{j\neq i}=0; \quad i=1, 2 ..., n \\ \quad \textit{and } V_{boun} \text{ floating at the boundary} \end{cases} \tag{11}$$

Table I
COMPARISON BETWEEN FEM AND BEM FOR TWO PARALLEL PLATES

	3D FEM Circuital matrix	3D FEM General matrix	3D BEM
Circuital (*) capacitance [pF]	147.0	147.1 using (8)	171.5 using (8)
General cap. term C_{11}=C_{22} [pF]	-	150.4	175.8
General cap. term C_{12}= C_{21} [pF]	-	143.8	167.2
Discretization elements	965798	965798	14808

(*) The result of the circuital capacitance from the analytical formula is 141.7 pF

$$q_j = -C_{ij} = \int_{\Omega j} \mathbf{D}\cdot\mathbf{n}\cdot ds$$

$$\begin{cases} \text{being: } V_i=1 \text{ and } V_j\big|_{j\neq i}=0; \quad i=1, 2 ..., n \\ \quad \textit{and } V_{boun} \text{ floating at the boundary} \end{cases} \tag{12}$$

In both cases the condition at the boundary is equivalent to floating potential. The result is presented in (13), which is consistent with eqn. (9).

$$\begin{bmatrix} q_1 \\ \vdots \\ q_n \end{bmatrix} = \begin{pmatrix} \sum_{j=1}^{n} C_{1j} & -C_{12}\cdots & -C_{1,n} \\ \vdots & \ddots & \vdots \\ -C_{n,1} & -C_{n,2}\cdots & \sum_{j=1}^{n} C_{nj} \end{pmatrix} \cdot \begin{bmatrix} V_1 \\ \vdots \\ V_n \end{bmatrix} \tag{13}$$

C. FEM and BEM simulation results

To compare the computational accuracy of the two methods, a simple case having an analytical solution has been chosen. It consists of two parallel planes as shown in Fig. 1, where the analytical solution is available. In this case, the ratio of the plate surface *S* to the distance *d* is set to 1600 cm, so that the circuital capacitance of the system is close to the analytical value $C = \varepsilon \cdot S/d$, where ε is the air permittivity.

As evidenced by the results in Table I, the BEM approach uses a number of elements that is nearly two orders of magnitude lower than FEM, for the same mesh density of the surfaces, but shows a greater discrepancy with respect to the analytical solution, with a greater deviation compared to the

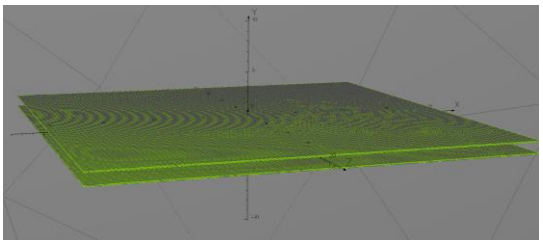


Fig. 1. 3D FEM model of the parallel plate capacitor. Only the mesh of the plates and the far boundary surface are visible. The plates are 1 cm far from each other and each side is 40 cm.

one of the FEM approach. To this reason, the FEM circuital approach is implemented in the tool.

D. Electrical network solution of VD

The second module of the numerical tool aims at solving the circuital network that simulates the voltage divider. The high voltage arm is subdivided into elementary cells series connected. Each cell represents a high voltage element. It is constituted by two nodes and two or three branches, depending on its resistive or resistive-capacitive nature. For each high voltage element the stray parameters can be introduced (internal stray capacitances of the resistors, internal stray inductance and internal equivalent series resistance of the capacitors). The low voltage arm is simply represented by an equivalent parallel RC dipole. The electrical circuit that has to be solved is made of passive dipoles and a voltage source [23]. Because of the presence of an ideal voltage source, which cannot be substituted by a Norton equivalent dipole, the modified nodal approach [24] is implemented. It is written in the frequency domain using Matlab™. The modified nodal approach requires the substitution of the pure voltage source with ideal current source of unknown amplitude. A projection matrix is introduced to extrapolate the unknown currents from the array which contains all the branch currents (known and unknown). The algebraic system, for a graph with N_n nodes and N_b branches has the following form:

$$\begin{bmatrix} [\mathbf{AYA}^t] & [-\mathbf{AT}^t] \\ [-\mathbf{TA}] & [0] \end{bmatrix} \cdot \begin{Bmatrix} [V_u] \\ [I_u] \end{Bmatrix} = \begin{Bmatrix} \mathbf{A}I_k \\ V_k \end{Bmatrix} \qquad (14)$$

where $\mathbf{A}[N_n,N_b]$ is the incident matrix describing the network topology, $\mathbf{Y}[N_b,N_b]$ is a diagonal matrix containing the branch admittances, and $\mathbf{T}[N_b,1]$ is the projection matrix. V_u and I_u are the unknown nodal potential and current source arrays respectively, while I_k and V_k are the known terms. In this specific case, the network does not have known current sources, thus the term $[\mathbf{A}I_k]$ is a zero array and the arrays V_k and I_u are, actually, scalar quantities. The first quantity is the applied voltage and the second one is the unknown current source, which replaces the supply source.

The incident matrix is built in three steps. In the first one the incident sub-matrix which describes the circuital topology of a elementary high voltage cell is replied on the diagonal of the matrix **A** as many times as the number of high voltage cells. Then M columns are added, where M is the number of stray capacitive couplings among divider electrodes (number of upper triangular part of capacitance matrix defined in (15)). Finally, two branches simulating the RC low voltage equivalent dipole are introduced by adding the last two columns to **A**. This approach allows the automatic building of the incident matrix associated with a divider of arbitrary structure.

III. Model Validation and Resistor Body Role

To validate the computational tool a test resistive VD has been set up. The analysis focuses on the frequency response of the device. To predict such a response, the equivalent network of the VD is solved, containing stray capacitance and circuital components, as described in the previous section. The frequency response of the VD equivalent circuit is compared with the K and $\Delta\varphi$ measurements carried out on the test device.

A. Characteristics of the VD and modeling approaches

A sketch of the low voltage test VD is shown in Fig. 2. It consists of six resistors and seven conductors (electrodes), the latter of which connected to ground. The high voltage arm is constituted by four non-inductive 10 MΩ, 10 kV resistors, while the low voltage arm has two 2 kΩ resistors, with a consequent rated scale factor of 10001. Two plastic transparent and parallel insulation plates, acting as a support for resistors and electrodes, are evident in Fig. 3(i). Two metallic plates are placed at the top and bottom of the VD.

To investigate the effect of including resistors in the calculation of parasitic parameters, three configurations have been considered:

- **case #a -** stray parameters computed considering only electrodes (Fig. 3(ii));
- **case #b -** stray parameters computed including the resistors (Fig. 3(iii)). Each electrode and each resistor are considered as separate elements in the FEM stray parameter computation, while in the circuit representation the resistor is split into two parts;
- **case #c -** stray parameters computed including the resistors, each of them divided into two parts (Fig. 3(iv)), where each resistor part contributes to the calculation of the parasitic capacitances of the contiguous electrode. Each electrode plus a half resistor is considered as one element of the FEM stray parameter computation, while in the circuit representation the resistor is considered as a whole.

In case #a and #c the circuital network has seven nodes, which correspond to the seven electrode potentials. The circuital network is built around these nodes. In case #b, the capacitance network is more complex, since the resistors are equivalent to six additional nodes. The value of each resistor is divided by two in the electric circuit solving program and each parasitic capacitance due to resistors is considered connected in the middle as shown in Fig. 4.

To complete the investigation a further case has been

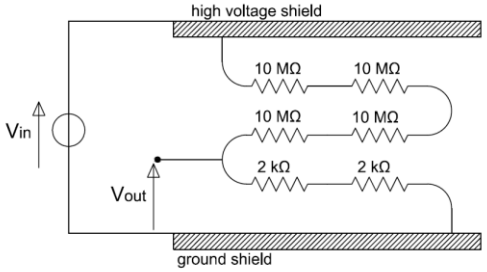
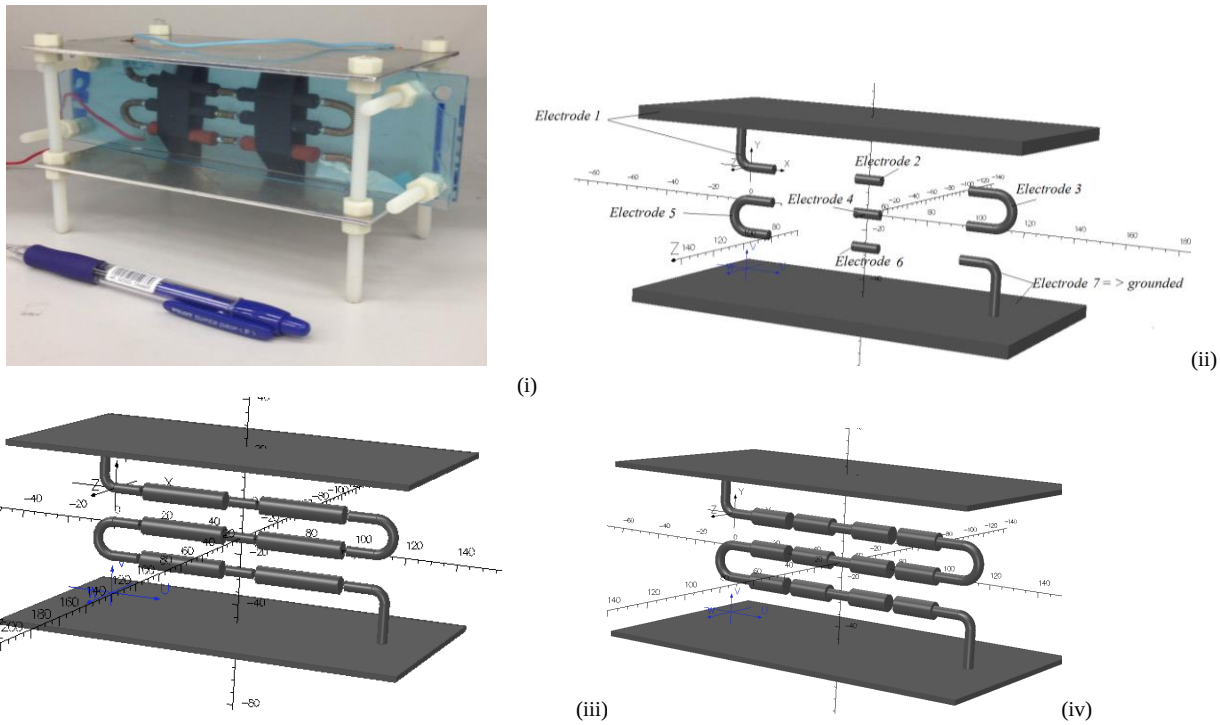


Fig. 2. Sketch of the test divider.



- Fig. 3. (i) Picture of the test divider. Geometric model of the test divider: (ii) only electrodes, iii) electrodes with entire resistor bodies, and (iv) electrodes with split resistor bodies.

considered being

- **case #d** – as the case #c, but including the dielectric plates.

B. Experimental characterization of the VD

The frequency behavior of the scale factor and phase error are obtained by measuring the output signal of the device under test and the applied voltage. The signals are digitized by two Agilent 3458 multimeters (AMM), configured for DCV digitizing and synchronized by an external trigger (Fig. 5). Thanks to the different selectable ranges, signals whose amplitude differs up to five orders of magnitude can be acquired. To evaluate the sinusoidal parameters (amplitude a, phase φ and offset component c) of each signal [9] a four-parameter nonlinear fit algorithm is used, whose function is

$$f(t) = a \cdot \sin(2\pi f \cdot t + \varphi) + c \qquad (15)$$

The frequency characterization is carried out supplying the divider with a stable 50 V voltage by means of a calibrator. The supply and measurement chain is remotely controlled. A Python program manages the supply and the acquisition systems and sets frequency sweep for the measurement of the divider scale factor and phase error. Because of the low pass filter of different cut-off frequency introduced by the digitizers, a correction on the measured phase error has to be applied. The selected digitizer voltage ranges are 100 mV and 100 V for the output and input voltages, respectively. Therefore, the measured cut-off frequency of digitizers are 58 kHz and 30 kHz, respectively [25]. By a first order model of the two filters, a correction factor is deduced and applied to the measured divider phase error.

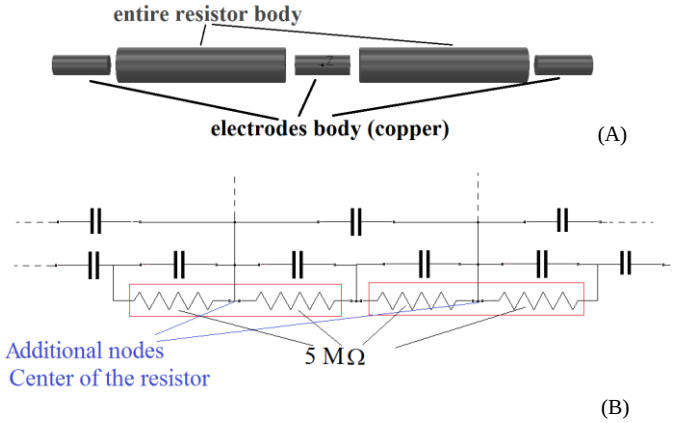


Fig. 4. Simulation of the case #b - (A) some resistors and electrodes in FEM model (B) part of the equivalent electric circuit with stray capacitances .

C. Validation results and discussion

The validation results are shown in Fig. 6, which shows a quite good agreement between measurements and computed results in the case #d up to 10 kHz. The deviations versus frequency of computed results from the measured values are shown in Table II, where

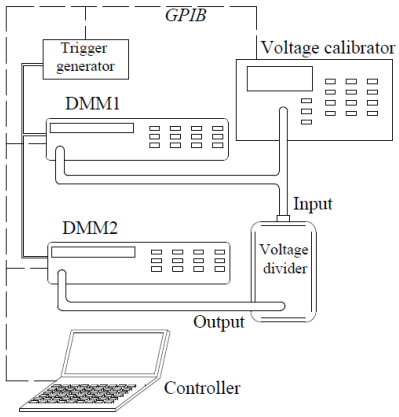


Fig. 5. Experimental set-up for the measurement of the resistive VD frequency response.

$$\varepsilon_K\% = \frac{K_{meas} - K_{comp}}{K_{meas}} \cdot 100 \quad (16)$$

and

$$\varepsilon_{\Delta\varphi} = \Delta\varphi_{meas} - \Delta\varphi_{comp} \quad (17)$$

being K_{meas} and K_{comp} the measured and computed scale factors respectively, while $\Delta\varphi_{meas}$ and $\Delta\varphi_{comp}$ are the measured and the computed phase errors.

It is worth to underline, how ε_K% is lower than 0.2% up to 1 kHz, reaching 4% at 10 kHz. Disregarding the stray capacitance due to the dielectric plates (case #c) worsen the results, as clearly shown by the dashed-dot-dot curves in Fig. 6 and by the Table II data. The relative deviation of computed scale factor from the measured values rises up to 4 % at 1 kHz and ~21% at 10 kHz. When the resistors are not properly modelled, as in case #b, where they are considered as an entire body, or in the cases #a, where they are not considered at all, the limits in the computation of the stray capacitances considerably affects the computed frequency response of the VD. In these cases, the computed results differ from the measured ones several percent at 1 kHz and 151% at 10 kHz.

The validation tests confirm the capabilities of the tool to reproduce the VD behaviour, highlighting the need for a detailed inclusion of dielectrics and all circuital components in the FEM model, to get accurate results in the range of frequencies where the stray couplings become significant.

IV. VALIDATION OF THE TOOL ON AN ACTUAL 20 kV VD

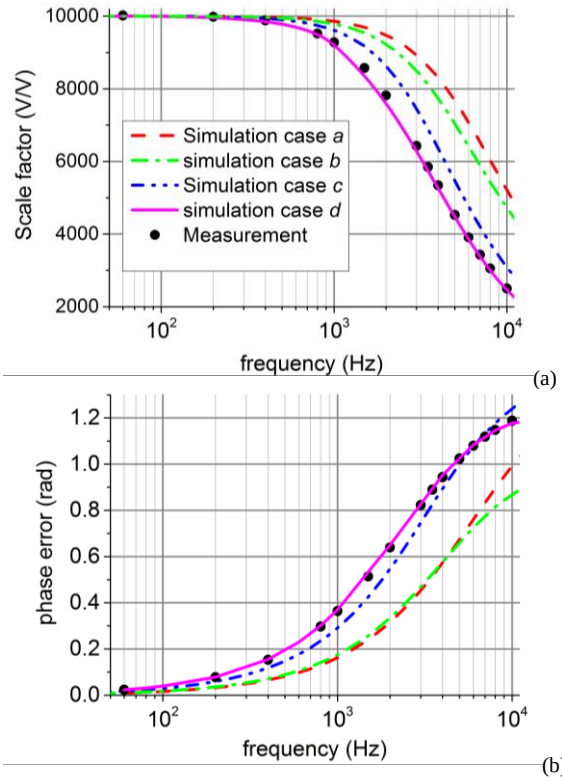


Fig. 6. Results of the test VD. a) Scale factor and b) phase error of measured and computed results in different conditions.

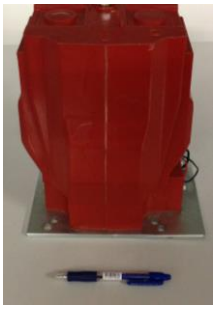
Table II
VD VALIDATION TEST: DEVIATIONS OF COMPUTED VALUES FROM THE MEASURED ONES FOR THE SCALE FACTOR AND THE PHASE ERROR.

	Case #a		Case #b		Case #c		Case #d	
f [kHz]	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)	ε_K %	$\varepsilon_{\Delta\varphi}$ (mrad)
0.06	-0.2	-18	-0.2	-12	-0.2	-6	-0.2	+ 1
0.4	1	-114	0.8	-79	0.5	-34	-0.1	-2
0.8	5	-217	4	-150	2	-62	-0.1	-4
1	8	-264	6	-181	4	-73	-0.2	-6
2	29	-430	18	-291	10	-92	-0.8	-10
5	107	-410	54	-338	20	-25	-2	+ 5
10	151	-115	85.5	-288	21	-55	-4	-10

In this section, the validated modelling procedure is applied to the 20 kV/2 V resin insulated, resistive VD shown in Fig. 7(a), developed for 50 Hz measurements and protection.

The resistors are arranged in a circular configuration; their layout is shown in Fig. 7 (b). The geometry of the VD created in the FEM pre-processor, as shown in Fig. 7(b), includes halved modelled resistor bodies and also takes into account the insulation material properties.

The output of FEM gives a 17×17 capacitance matrix, as there are 17 electrodes excluding the divider bottom plate, which is grounded. The capacitance matrix is the input for the Matlab™ program that solves the electric circuit including the resistors. The measured and computed scale factor and phase


a)

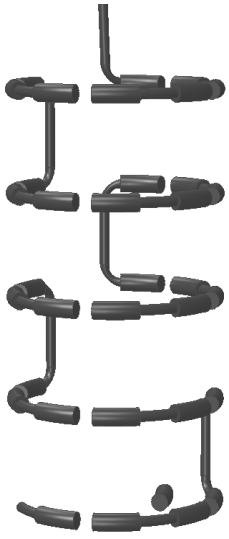

(b)

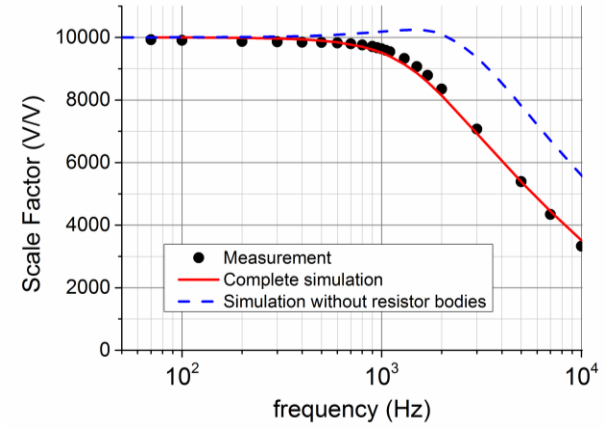
Fig.7. Structure of the 20 kV VD. a) sealed with insulation; b) the FEM model (here without insulation).

Table III
DISCREPANCIES BETWEEN MEASURED AND COMPUTED VALUES OF THE SCALE FACTOR AND PHASE ERROR OF THE 20 kV VD .

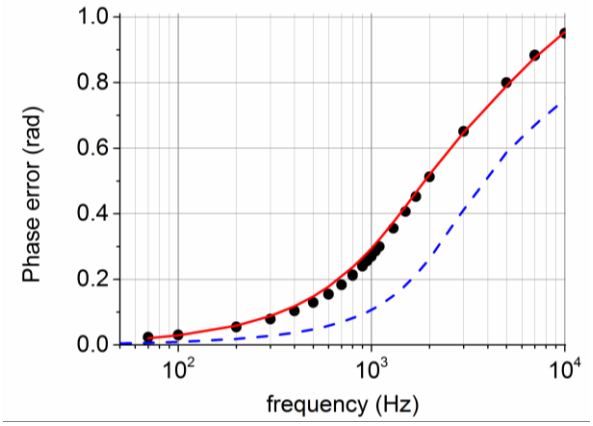
	Complete simulation	
f [Hz]	ε_K %	$\varepsilon_{\Delta\varphi}$ *(mrad)*
70	-0.8	3
400	-0.9	-14
800	0.6	-24
1000	1.3	-24
2000	2.5	-7
5000	0.1	10
7000	-2.2	8
10000	-5.7	4

error behaviours of the VD are shown in Fig. 8. Concerning simulations, two cases are considered. In the first one the resistor bodies are modelled in the FEM computation (complete simulation) and are neglected in the second one.

A good agreement between measured and computed results is also found for this divider in the complete simulation. This experiment confirms that the simulation accuracy strongly decreases when the resistor bodies are not included in the FEM simulation. In the complete simulation the maximum relative discrepancies between measured and computed values, in the frequency range up to 10 kHz, are limited to 5.7% for the scale factor and to 24 mrad for the phase error (Table III).



(a)



(b)

Fig. 8. Results of the 20 kV VD. a) Scale factor and b) phase error of measured and computed results. The dashed curves are obtained without considering the resistor bodies in the computation of the stray capacitances.

V. Conclusion

This paper proposes an effective tool for the simulation and design of resistive voltage dividers. By suitable modelling of the stray capacitances, the tool can be applied to the design of other transducers such as resistive-capacitive or pure capacitive dividers.

The tool implementing FEM analysis for the evaluation of the stray capacitive couplings, has proved the importance of including the resistor body in the FEM computation of the parasitic parameters. An effective solution has been demonstrated that considers the resistor split in two parts, with each part associated with the contiguous electrode. An incomplete modelling or the omission of the resistors may lead to errors higher than 150% when considering the device frequency response.

The results of the tests carried out on an actual 20 kV VD, show a computation accuracy within 5.7% for the scale factor, and 24 mrad for the phase errors up to 10 kHz.

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