Charge density increase in submonolayer organic field-effect transistors

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Interface confinement plays a central role in charge carrier accumulation and transport along the channel of organic field-effect transistors. Understanding the relevant interfacial interactions that affect the energy landscape experienced by carriers in the channel is of fundamental interest. Here we investigate charge transport in the submonolayer regime of pentacene transistors in which confinement arises due to the finite size of the interconnected semiconducting islands. *In situ* real-time electrical characterization is used to monitor the formation and evolution of the accumulation layer at the very early stages of growth. The morphology of the confining interfaces is controlled by growth conditions and pentacene coverage. Charge transport occurs when percolation pathways connecting source and drain electrodes are formed at a critical coverage. The displacement current across the oxide/semiconductor interface is observed starting from the onset of percolation (0.69 monolayer coverage). The analysis of the characteristics shows that already the submonolayer film fully screens the gate field and accumulates higher charge carrier density as compared to the monolayer film. We propose an electrostatic model to correlate the charge density to the characteristic length scale of the submonolayer film and the thickness of the dielectric layer. This explains charge mobility and threshold voltage of thin-film transistors in the submonolayer regime.

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I. INTRODUCTION

Confining interfaces play a crucial role for charge transport in organic field-effect transistors (OFETs). In OFETs a conducting channel is formed by the accumulation of charge carriers in the field of the gate electrode [1]. The strong electrostatic attraction of the carriers towards the gate confines the charge density to a thin accumulation layer extending a few nanometers from the dielectric interface into the thin film. Confinement of the charge density also arises from the finite thickness of the semiconductor layer in the case of ultrathin films or due to a limited lateral size of the semiconducting film caused for example by lithographic patterning, incomplete film formation, or domain boundaries. The impact of confining interfaces on the charge distribution and on transport properties of the organic semiconductor is of fundamental and technological interest. Nanoscale spatial confinement has been exploited to optimize electronic properties in organic thin film transistors [2] for applications in large area electronics [3,4], wearable electronics [5], and chemical and biological sensing [6]. Two confinement effects have been investigated. First, confining interfaces influence on polymorph selection and guide crystallization processes during the fabrication process, thus their control is needed for the optimization of semiconductor morphology aimed to direct charge transfer along the channel length [7,8]. Second, confinement at length scales in the order of the carrier localization changes the density of states and the transport properties [9].

In OFET a third effect has to be considered when transport in confined channels is studied: Lateral confinement impacts the capacitive coupling between the semiconductor and the gate electrode since it can induce the bending of field lines in the dielectric layer. A detailed understanding of the effect is necessary to obtain the correct charge density and to analyze transport properties in the transistor channel.

Several ways to fabricate organic transistor devices with nanoscale spatial confinement exist [10]. Single molecular layer transport is achieved with self-assembled monolayer (ML) transistors in which the semiconducting moiety is grafted to the dielectric surface by means of a linker [11–15]. Confinement in the direction parallel to the dielectric interface is also achieved by high-vacuum evaporation techniques of semiconductor molecules to form ultrathin films. The control of layer thickness by such techniques is below a single molecular layer [2,16]. Temperature dependent measurements have demonstrated that charge transport in these ultrathin films is indeed two-dimensional (2D) [9]. Lateral confinement of organic semiconductors is achieved by solution-based processes exploiting masks [17], patterned stamps [8,18], and self-organization at phase boundaries [19]. The length scales of the lateral patterns largely exceed the localization length of charge carriers in organic semiconductors. As a consequence, the confining interface can impact charge transfer only indirectly by influencing the morphology and the alignment of semiconducting polymer chains or crystallization processes of semiconductor molecules.

Transistors based on molecular ultrathin films allow further options to systematically study the effect of coverage on transport [17]: Below one ML thickness, the gate dielectric substrate is only partially covered, and lateral confinement arises due to the finite size of the semiconducting islands. A transistor current is measured if the islands interconnect to form a percolated network. A detailed analysis of self-assembled monolayer field-effect transistors (SAMFETs) led to the conclusion that the scaling relation between conductivity

and channel length could be fully explained by arguments based on 2D island percolation and the assumption that transport is independent of island size; thus effects on charge transport due to lateral confinement were excluded [13].

The reported studies on charge transport in laterally confined systems assumed a carrier density in the accumulation layer that is independent of coverage [8,11–13]. This assumption holds when the typical lateral spacing between features exceeds largely the thickness of the dielectric. In this regime the transversal electric field can be treated as homogeneous. If this is not the case, bending of the electric field in the dielectric has to be taken into account and corrections have to be introduced for the calculation of transport properties. Submonolayer OFETs represent a model system to study lateral confinement since the morphology can be systematically varied by growth conditions and coverage.

In this paper we investigate charge accumulation and transport in submonolayer pentacene transistors grown and characterized *in situ* in high vacuum [2,17,19]. We measure displacement currents to characterize the formation of the accumulation layer and the charge density [20,21]. The latter is shown to be dependent on coverage in the submonolayer regime and to exhibit a maximum when coverage exceeds the percolation threshold. Our findings are explained with an analytical electrostatic model. The knowledge of the charge density allows us to extract the carrier mobility in the submonolayer regime and to study transport close to the threshold of 2D percolation. Our results elucidate the critical role of microelectrostatics in laterally confined OFETs.

II. EXPERIMENTAL

Experiments were performed in a homebuilt high vacuum chamber [2] featuring a sample holder with electrical contacts to simultaneously measure currents in three independent transistors by using Keithley B2612 source measure units. Pentacene (Sigma Aldrich) was evaporated at a rate of 0.7 nm/min through a shadow mask exposing an area $A_0 = 0.104\,\mathrm{cm}^2$ of uncovered dielectric surface. The thickness of the growing film was monitored by a calibrated quartz microbalance. Test patterns with a common gate made of an n-type doped Si-wafer consisting of a 200 nm thick layer of thermal oxide were used. Their specific capacitance $c_{ox} = 17.3\,\mathrm{nF/cm}^2$. On top of the oxide layer, 80 nm high Au electrodes with a 2 nm Cr adhesion layer were patterned by photolithography. The electrodes define four transistors with channel lengths L of 20 μm and 40 μm and widths W of 11 200 μm and 22 400 μm, respectively. The test patterns were cleaned using a standard process with acetone, piranha solution, and hydrogen fluoride solution (2%). The extensive cleaning procedure was found to be crucial to avoid contact resistance effects (see below). The oxide surface was then functionalized with hexamethyldilazane (HMDS) by thermal evaporation on the cleaned surface. During pentacene growth, transfer characteristics were acquired by sweeping the gate potential V_{SG} from 20 to −20 V in a closed loop and keeping the drain potential at $V_{SD} = -20\,\mathrm{V}$. A fast sweep rate was applied to achieve a transfer measurement every 3 s. An alternating voltage ramp was used for the measurements of the displacement currents, as discussed below. Atomic force microscopy (AFM; Smena liquid head, NT-MDT, Moscow, Russia) was performed in intermittent contact mode on samples *ex situ*.

III. RESULTS AND DISCUSSION

The evolution of the transistor current I_D as measured at $V_{SG} = V_{SD} = -20\,\mathrm{V}$ during the growth of the pentacene layer is shown in Fig. 1(a). Percolation of the semiconducting film is marked by a sharp transition at a nominal layer thickness of $\Theta_C = 0.69\,\mathrm{ML}$ followed by orders of magnitude rise in the current. Upon completion of the first ML, the current increase slows down substantially, reflecting the layer-by-layer growth mode of pentacene thin films [22]. A second decrease of slope sets in when the second ML is completed. At roughly three MLs' thickness, the transistor current is saturated, demonstrating the strong spatial confinement of the carrier accumulation zone to the first two to three MLs [23]. This finding is consistent with the results reported earlier [2] and suggests that the HMDS passivation effectively decreases the defect concentration at the silicon oxide surface thus making the first ML as the one driving most of the current [24,25]. Fast sampling of I-V curves allows us to acquire transfer characteristics during film growth, maintaining the same sampling frequency as the single current measurements

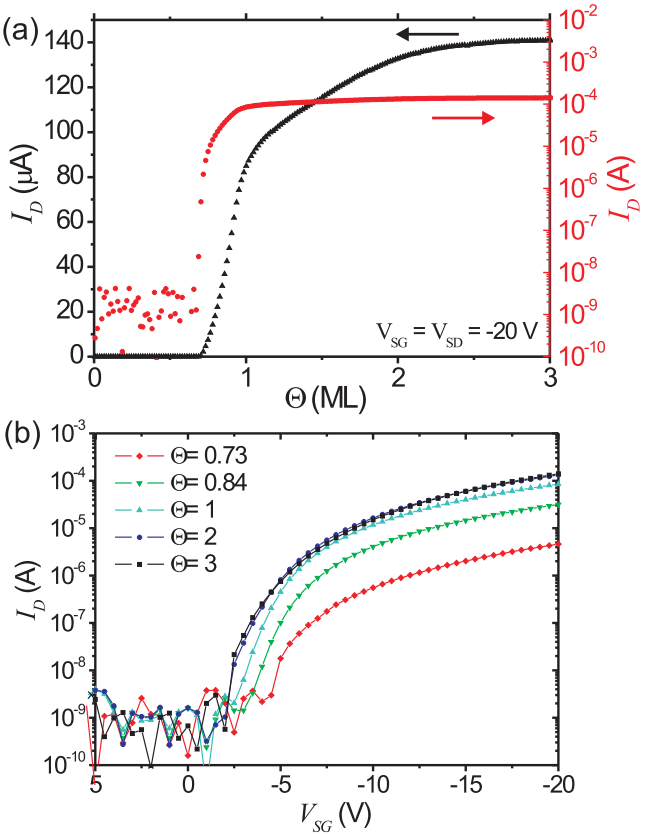

FIG. 1. (Color online) *In situ* growth and electrical characterization of pentacene transistor: (a) drain current I_D at $V_{SG} = V_{SD} = -20\,\mathrm{V}$ as a function of nominal layer thickness Θ; (b) examples for transfer curves at various Θ acquired at $V_{SD} = -20\,\mathrm{V}$. Each point in plot (a) corresponds to a full transfer characterization as shown in (b).

depicted in Fig. 1(a). Representative I-V curves are shown in Fig. 1(b). During the growth of the first two MLs, the shape of the transfer curves and their characteristic parameters such as pinch-off voltage, threshold voltage, and mobility are in constant evolution. In order to analyze these curves quantitatively and to extract the relevant transport parameters, it is necessary to quantify the amount of charge that accumulates in the semiconductor due to field effect. However, the usual approximation of a planar capacitor geometry in which the capacitance is calculated from the dimensions of the oxide layer does not hold in the submonolayer regime.

In order to measure the capacitance and carrier accumulation during the growth of the pentacene layer, we apply a triangular waveform to the potential V_{SG} and sample the displacement current I_G [20,21]. The source and drain electrodes were grounded to avoid any longitudinal gradient in the charge distribution within the semiconducting film. In order to achieve fast sampling during pentacene growth, we apply a negative offset potential to ascertain operation in the accumulation regime of the p-type semiconductor, thus avoiding slow carrier injection or extraction processes from a depleted channel [20].

Details of the V_{SG} sweep and the I_G acquired from a device with 3 ML pentacene coverage are shown in Fig. 2(a). The data allow us to calculate the capacitances of the layer stacks forming two capacitors connected in parallel, as depicted schematically in Fig. 2(b). The first stack contains the gold contacts, insulator, and common gate and is denoted C_{Au}. The second stack regards the area that is not covered by gold and contains the pentacene layer, insulator, and common gate and is referred to as $C_{SC}(\Theta)$ since it depends on coverage Θ. The following equation is used to extract the capacitances during the voltage sweep:

$$I_G = [C_{Au} + C_{SC}(\Theta)]\frac{dV_{SG}}{dt}. \quad (1)$$

We note that the capacitance containing the semiconducting layer can be further separated into two capacitances connected in series $C_{SC}(\Theta) = C_{OX}C_{Pen}/(C_{OX} + C_{Pen})$, which contain the contribution from the insulating oxide (C_{OX}) and the contribution from the pentacene layer C_{Pen} due to the spatial extension of the charge accumulation layer in the direction normal to the interface. However, the latter is typically neglected as $C_{OX} \ll C_{Pen}$ [20]. Figure 2(c) shows the *in situ* measured displacement current as a function of Θ. In the initial phase, the displacement current results from the capacitance that is formed between gold electrodes and the common gate and exhibits a characteristic pattern of positive and negative currents. At the percolation threshold of the semiconducting film, this pattern is perturbed. As the semiconductor percolates, the accumulation layer forms, and charges enter the semiconductor resulting in a positive background peak of the displacement current. The superimposed variations of I_G are due to the continuously swept V_{SG}. After percolation the stable pattern of charging and discharging currents returns with larger amplitudes due to the increased capacitance.

The resulting values of C_{SC} are plotted in Fig. 3(a). Before percolation, carriers cannot enter into the semiconducting film, and $C_{SC}(\Theta < \Theta_C) = 0$. At percolation at $\Theta_C = 0.69$, a sharp increase in C_{SC} occurs to reach almost immediately the maximum capacitance as determined by the oxide dielectric ($c_{SC} = C_{SC}/A_0 = 17.3\,\mathrm{nF/cm^2}$), which is reached upon completion of the first ML. Above 1 ML, the capacitance remains constant, thus revealing that spatial confinement orthogonal to the interface has only a minor impact on the charge density of the accumulation layer. This finding is in agreement with the small Debye length scale of 1–2 nm reported for organic semiconductors [26] and confirms the usual approximation $C_{OX} \ll C_{Pen}$. The initial sharp increase in C_{SC} demonstrates that already at the onset of percolation enough charges enter the semiconducting film to screen completely the gate field. This happens even if the dielectric surface is not completely covered by the semiconductor.

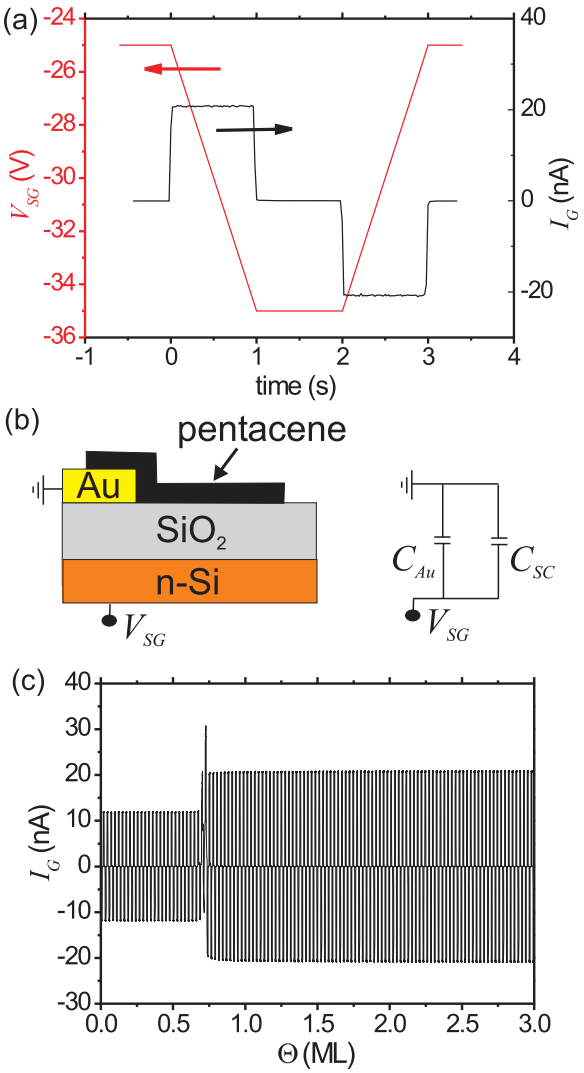

FIG. 2. (Color online) Measurement of carrier accumulation in pentacene thin-film transistors: (a) potential waveform applied to V_{SG} and resulting displacement current I_G at 3 ML thickness;(b) schematic diagram showing the measured capacitor and equivalent circuit; (c) displacement current measured during growth of pentacene film with a deposition rate of 0.47 ML/min applying continuously the described waveform. The displacement current before pentacene percolation ($\Theta = 0.69$ ML) results from the capacitance formed by gold source and drain electrodes.

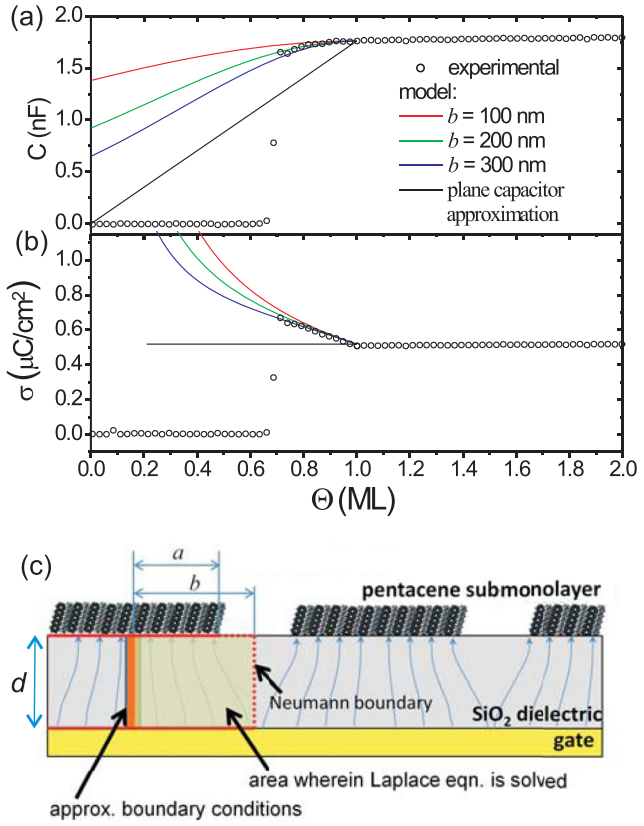

FIG. 3. (Color online) Capacitance C (a) and surface charge density σ (b) at $V_{SG} = 30\,\mathrm{V}$ in the semiconducting film during growth as extracted from the displacement current measurements; (c) development of electrostatic model describing capacitance and charge density as a function of coverage in the submonolayer regime.

In order to rationalize the observed screening already at submonolayer coverage, we derive a microelectrostatic model of the capacitive coupling between interconnected semiconducting islands and the gate electrode [Fig. 3(c)]. Submonolayer pentacene films were investigated by AFM to extract the geometric parameters describing the film morphology. Figures 4(a) and 4(b) show the topography of two films obtained before and after percolation of semiconducting islands. Both images show a distribution of islands of varying lateral size and shape. The typical island height corresponds to a single pentacene ML. The characteristic length scale for island spacing is obtained by analyzing the radial height-autocorrelation function as plotted in Fig. 4(c). At both coverages, the minimum at $b = 195\,\mathrm{nm}$ is equated to half of the interisland spacing. The value is close to the thickness of the gate dielectric $d = 200\,\mathrm{nm}$. As a consequence, the field lines exiting the dielectric bend slightly to re-enter in the pentacene-covered islands [Fig. 3(c)]. We model this behavior by means of a continuum electrostatic model that calculates the flux between the gate electrode and one half of a pentacene island by applying the conformal mapping technique to the 2D Laplace equation [27,28]. The periodic structure considered in the model is highlighted in green in Fig. 3(c). Its 2D geometry is described by the parameters b, d, and a, the latter describing the island extension. In the 2D model, we calculate an effective value for the island extension from the experimental coverage by $a = b\Theta$. As a final result, we obtain an analytic expression [Eq. (A1)] describing the capacitance $C_{SC}(\Theta, b)$ as a function of the experimentally accessible geometric parameters. Figure 3(a) compares the theoretical results for the capacitance with the experimental findings. Using the observed island spacing of $b \approx 200\,\mathrm{nm}$, we obtain a good fit of the data despite the model's simplifications. The model allows us to compare the impact of island spacing b on capacitance. Smaller b (equal to smaller characteristic feature size at constant coverage) leads to a reduction of the bending of field lines until they become straight and capacitance becomes independent on coverage. Instead, increasing b leads to an increase of the bending of field lines parting from uncovered areas. At very large island spacing ($b > 100\,d$), the contribution of bent field lines can be neglected, and the plane capacitor approximation, in which only areas covered by a semiconductor are considered, holds. As a consequence, the capacitance scales with the area covered by the semiconductor.

Charge transport through the transistor channel is governed by the surface charge density σ in the semiconductor. Knowing that $C_{SC}(\Theta)$, we calculate σ as a function of Θ by using $\sigma(\Theta) = C_{SC}(\Theta)V_{SG}/A_P$, where $A_P = \Theta A_0$ at $\Theta < 1\,\mathrm{ML}$ denotes the area covered by pentacene. A_0 is determined by the shadow-mask and gold electrode layout; here it amounts to $A_0 = 0.104\,\mathrm{cm}^2$. The result at $V_{SG} = 30\,\mathrm{V}$ is plotted in Fig. 3(b). A maximum in σ is observed close to the percolation threshold. With increasing coverage, σ drops as the total constant charge distributes over an increasing area. At $\Theta > 1\,\mathrm{ML}$, stability in σ is reached. This finding shows two

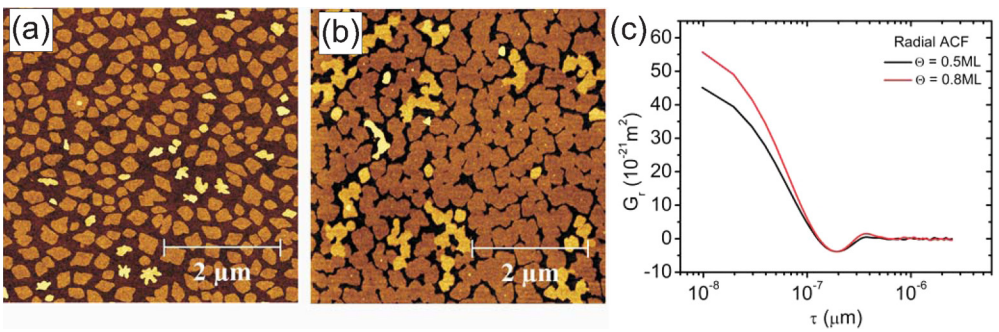

FIG. 4. (Color online) Morphology of submonolayer pentacene thin films: AFM topography at 0.5 ML (a) and 0.8 ML (b) coverage and corresponding height radial autocorrelation function (ACF) in (c) showing a characteristic minima at 195 nm.

competing effects that influence σ in the submonolayer regime. On one hand, σ is reduced due to the partial coverage, which leads to a small decrease in C_{SC} as field lines in the dielectric are bent. On the other hand, σ rises as the accumulated charges become concentrated in the submonolayer-covered area. The latter effect outperforms the former due to the close island spacing in the pentacene film, and a maximum in σ is obtained close to the percolation threshold.

With the knowledge of $C_{SC}(\Theta)$, the transistor parameters such as mobility μ and threshold voltage V_t can be calculated from the transfer characteristics acquired during growth. The findings show that in the submonolayer regime, a correction term has to be introduced to account for the increased carrier density due to lateral confinement in the incomplete ML. The correction can be readily introduced into the standard equations for current thin film transistors [23],

$$I_D = W[\sigma(x) - \sigma_t]\mu E(x), \tag{2}$$

where W is the width of the transistor channel, σ_t defines the charge trap density, and μ defines the charge mobility. Then, the term in brackets becomes

$$\sigma(x) - \sigma_t = \frac{C_{SC}(\Theta)}{\Theta A_0}(V_{SG} - V_t - V(x)) \quad \text{for} \quad \Theta < 1\,\text{ML}, \tag{3}$$

with V_t being the threshold voltage. In order to analyze the acquired transfer characteristics in saturation regime ($V_{SD} > V_{SG} - V_t$), we integrate Eq. (2) to obtain

$$I_D = \frac{W}{2L}\frac{C_{SC}(\Theta)}{\Theta A_0}(V_{SG} - V_t)^2\,\mu, \tag{4}$$

where L is the channel length. Fitting Eq. (4) to our dataset results in mobility μ and threshold voltage V_t as a function of Θ, as depicted in Fig. 5 for two transistors of different channel length L. At the onset of percolation, several orders of magnitude increase in mobility exhibiting a power law behavior $\mu \propto (\Theta - \Theta_C)^t$. Here we find a percolation threshold of $\Theta_C = 0.69$ and a critical exponent of $t = 1.8 \pm 0.1$. The charge mobility follows the shape of the current increase, as discussed above, with characteristic kinks at $\Theta = 1$ and 2 ML. The large increase in mobility during the growth of the first ML demonstrates its particular relevance for transistor performance in the present case. For the growth conditions chosen here, almost 60% of the final mobility is attained after the formation of the first ML. The addition of more than three MLs does not further improve performance or can even lead to a deterioration of properties [16]. As saturation mobility, we obtain $\mu = 0.15 \pm 0.04\,\text{cm}^2/\text{Vs}$ at $\Theta = 3$ ML. Transistors with different channel length yield within the experimental uncertainty identical behavior of mobility vs coverage. This finding allows us to exclude a strong role of contact effects in the observed phenomena, as reported elsewhere [17]. The calculated threshold voltage V_t is shown in Fig. 5(b). It starts right at percolation with a strongly negative value of $V_t = -15$ V but drops immediately to stabilize at $\Theta = 0.8$ ML at a low value of around $V_t = -4$ V. Larger variations at coverages >0.8 ML have been observed in studies that investigated threshold as a function of semiconductor thickness [16,17]. In general, the threshold voltage is closely related to the semiconductor/dielectric interface. Here, the oxide surface is functionalized by HMDS to cover polar hydroxyl groups that could give rise to hole traps and related variations in threshold voltage. We associate the small variations in threshold voltage observed in our experiments at $\Theta > 0.8$ ML with the apolar nature of the HMDS-modified silicon oxide surface. Several mechanisms can account for the very negative threshold voltage observed at the onset of percolation ($\Theta < 0.8$ ML). From percolation theory it follows that at this stage, the transport is dominated by a single or very few bottlenecks that allow the transfer of current from one percolated subnetwork to another. The density of states and the presence of trap states in these bottlenecks are likely to be distinguished from the rest of the conducting network, thus offering a possible explanation for the strong variation in threshold when the bottlenecks are substituted by wider connections between islands at larger coverage.

Further insight into transport in the submonolayer regime can be provided by comparing the values from the power-law fit of mobility to values from standard models of percolation theory [29]. In the initial phase of the ML, pentacene islands start to grow from nucleation sites that are almost randomly distributed over the surface. Percolation of randomly positioned objects is described in the literature by continuum models. The percolation threshold depends largely on the shape and anisotropy of the percolating objects. Close to the

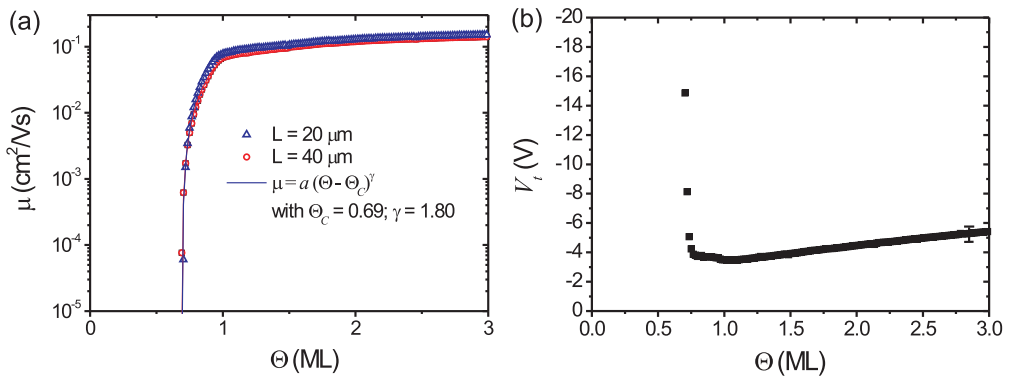

FIG. 5. (Color online) Mobility μ (a) and threshold voltage V_t (b) calculated from transfer characteristics acquired during growth of pentacene semiconducting layer at $V_{SG} = -20$ V and $V_{SD} = -20$ V. Correction for the increased charge density in the submonolayer regime has been included. Mobility values as extracted from two transistors of different channel length L are shown.

observed value of $\Theta_C = 0.69$ is the percolation threshold of randomly positioned discs ($\Theta_{C,\mathrm{disc}} = 0.67$) [30] indicating a circular shape of the percolating pentacene islands. Several theoretical studies investigated the dependence of the critical exponent t of the electrical conductivity in systems composed of resistors and insulators (here corresponding to pentacene and bare dielectric), which are interconnected to form a resistor network [29]. Again the value of t depends on the dimensionality of the system and on the lattice geometry. Reported exponent values fall in the range of $t_{2D} \sim 1.3$ and $t_{3D} \sim 1.8$. Although for pentacene, the layer-by-layer growth defines 2D percolation, the experimental finding of $t = 1.8$ for the percolation of the conducting pathway deviates, and the exponent is larger and closer to the three-dimensional (3D) behavior. The increase in exponent results in a reduced slope in mobility at $\Theta = \Theta_C$. We postulate two possible causes for the nonideality. (i) Small deviations from the ideal layer-by-layer growth mode slow down the formation of additional conducting pathways at the initial percolation stage as material is used to form a second ML. Evidence for small deviations from layer-by-layer growth can be seen in the AFM topography, as depicted in Fig. 4(b), where some pentacene islands already contain the second ML. (ii) The percolating resistor network model assumes constant local conductivity of the segments. For the pentacene film, the local mobility is likely to be influenced by the morphology changes during the growth. In fact, Fig. 5(a) shows that the mobility continues to rise also after the completion of the first ML, clearly demonstrating the relevance of other factors in addition to the geometric one.

IV. CONCLUSIONS

In this paper we investigated carrier accumulation and transport in submonolayer pentacene transistors. In this model system, charge transport is laterally confined within islands forming a percolating network. We show that the geometry of the network determines not only the percolation threshold and the critical exponent but also the density of charge carriers created by field effect. The latter effect was characterized in detail by displacement current measurements *in situ* during the formation of the semiconducting layer and by an analytical electrostatic model. Due to the nanostructured geometry with a characteristic island spacing in the range of or smaller than the thickness of the dielectric, the gate field gets completely screened, and field lines are only slightly bent in the dielectric. As a consequence, the capacitance governing carrier accumulation becomes almost independent of coverage once the percolation threshold is exceeded. The effect leads to an increase in charge density in partially covered films. The experimentally determined capacitance allows us to analyze transfer characteristics acquired in the submonolayer regime and to extract the mobility. The findings are of general relevance for partially covered thin-film transistors where the plane capacitor model is not applicable due to nanoscale lateral confinement.

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APPENDIX

To derive closed-form equations, we consider a 2D structure as shown in Fig. 3(c). The island size in the 2D model is described by the geometric parameters b and a, whereas the thickness of the dielectric enters with parameter d. The experimental coverage enters into the model via $a = b\Theta$. Within this periodic structure, the conformal mapping technique is applied to a two-corner structure (highlighted in green) to keep mathematics manageable. Figure 6(a) shows this structure in complex plane z. The gate electrode is defined between points 2 and 4, and the pentacene island between points 5 and 6. At the symmetry line within the gap (line between points 2 and 3), the Neumann boundary is applied. Along the symmetry line in the center of the pentacene island, the line connecting points 4 and 6, a Neumann boundary is approximated by extending both the top and bottom electrodes infinitely to point 1. This approximation holds if the influence of the fringing fields from the corner of the pentacene island upon the line between points 5 and 6 can be neglected, resulting in a nearly homogeneous field in this area. In the model structure, this is the case for a thickness d of the oxide, which is less than the length of the pentacene islands. The two-corner structure is mapped upon the upper half of a complex plane w [Fig. 6(b)]. Following the Schwarz-Christoffel transformation [27], the derivative of the mapping function is given by

$$\frac{dz}{dw} = -\frac{d}{\pi}\frac{1}{\sqrt{u+1}\sqrt{u-u_3}}.$$

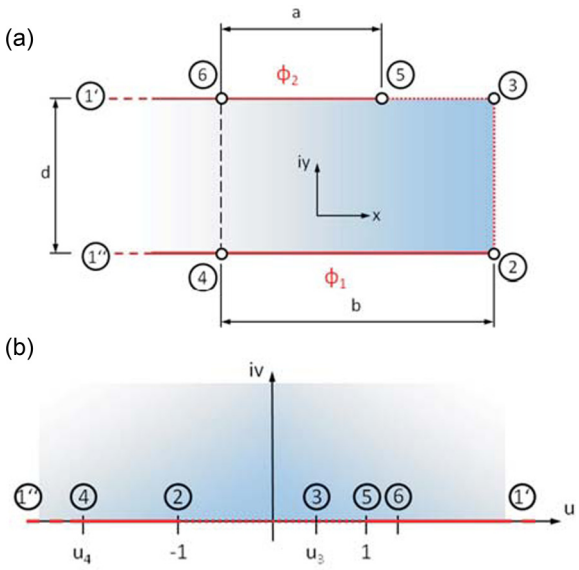

FIG. 6. (Color online) Conformal mapping technique applied to submonolayer pentacene film: The two-corner structure in complex plane z wherein Laplace equation is analytically solved is shown in (a). The area of interest is mapped upon the upper half in plane w (b).

Its integration yields [28]

$$z = f(w) = -\frac{2d}{\pi}\log(\sqrt{w+1}+\sqrt{w-u_3}) + D,$$

where the integration constant D defines the origin in z plane.

In w plane, the boundary of the mapped region lies along the real axis. Points 2 and 5 are mapped upon $w=-1$ and $w=+1$, respectively. Parameter u_3 can be derived by equating the distance between points 3 and 5 in z plane to the difference $b-a$ and results in

$$u_3 = \frac{2}{\cosh^2\left(\frac{\pi(a-b)}{2d}\right)} - 1.$$

Applying a potential Φ_1 between points $1''$ and 2 and a potential Φ_2 between points 5 and $1'$, the complex potential solution in the w plane reads [4]

$$P(w) = \Phi(w) + i\,\Xi(w) = \Phi_2 + i\frac{\Phi_2-\Phi_1}{\pi}\text{arccosh(w)}.$$

The integral dielectric flux, leaving in plane z the bottom electrode between points 2 and 4, is given by the difference of the imaginary parts of the complex potential at the corresponding points in plane w

$$\int_{2\to4} \vec{D}\,d\vec{z} = \epsilon_{ox}(\Xi(u_4) - \Xi(-1))$$
$$= \epsilon_{ox}\,\frac{\Phi_2-\Phi_1}{\pi}(\text{arccosh}(u_4) - \text{arccosh}(-1)).$$

By solving the equation $f(-1) - f(u_4) = b$ for u_4, one obtains

$$u_4 = u_3 - (1+u_3)\cosh^2\left(\frac{\pi b}{2d}\right).$$

Finally the capacitance between gate electrodes and pentacene film of total area A can easily be calculated from

$$C = A\frac{\epsilon_{ox}}{b\,\pi}(\text{arccosh}(u_4) - \text{arccosh}(-1)). \quad \text{(A1)}$$

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