A 868MHz CMOS RF-DC Power Converter With -17dBm Input Power Sensitivity and Efficiency Higher Than 40% Over 14dB Input Power Range

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***Abstract*—In this paper we present a novel CMOS RF-DC converter circuit, operating at 868MHz, for RFID and remote powering applications. The novel reconfigurable architecture of the converter allows the circuit to operate over a very wide input power range with very high efficiency compared with previous art works. Prototypes realized in STM 0.130µm CMOS technology provide a regulated output voltage ~2V with a -17dBm input power sensitivity. The circuit efficiency, higher than 40% over a 14dB input power range, peaks at 60%.**

I. INTRODUCTION

RF remote powering is a charming solution for the power supply of ultra-low power applications like WSN and active RFID tags. The improvement of the sensitivity and the efficiency of the RF-DC power converter is crucial for this alternative power supply technique, which requires to deal with i) the very low power available at far-end locations, and ii) the unpredictable variations of available power, which typically depends on several factors like the distance from the power source, the transmission media, the antenna orientation, etc.

Unfortunately, circuit solutions presented in literature aimed only at maximizing the circuit efficiency at a given input power level [1-2], while neglecting the issues related to input power variations, that strongly penalize the output power and the circuit efficiency, which is an appropriate metric to evaluate circuit performances. In addition, the converter output voltage is typically controlled by linear regulators which leads to a further efficiency drop [3].

In this scenario, the aim of this paper is to propose a novel RF-DC converter architecture, operating in the 868MHz ISM band, which allows maximizing the circuit efficiency over a very wide range of RF input power thanks to its reconfigurable architecture. In addition, the novel converter integrates a smart voltage regulator which allows generating a regulated DC output voltage, and start operating at very low input power.

The paper is organized as follows. Section II describes the proposed circuit architecture. Section III discusses experimental results. Section IV concludes the paper.

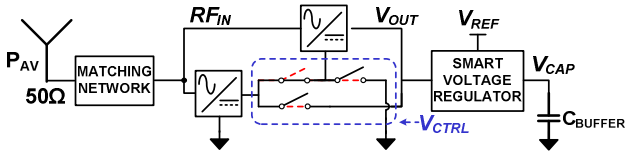

Fig. 1. Block diagram of the proposed RF-DC converter, comprised of a matching network, 2 identical rectifier sections (2-stage Dickson charge pump) , and a smart voltage regulator.

II. THE PROPOSED CONVERTER ARCHITECTURE

The simplified block diagram of the proposed circuit architecture is shown in Fig. 1. The RF-DC CMOS power converter is typically comprised of some standard building blocks: the matching network (MN), which maximizes the power transfer from the antenna through the chain; the voltage rectifier/multiplier; the energy storage device, i.e. a capacitor or rechargeable battery; the voltage regulator.

The novelty of the converter circuit solution we propose is represented by the reconfigurable topology devised for the rectifier, which allows maximizing the sensitivity and efficiency of the converter over a very wide ultra-low power range, and the integrated Smart Voltage Regulator (SVR), which provides a DC regulated output voltage, making the rectifier working at constant voltage for maximum efficiency.

The modular voltage rectifier is comprised of two identical section, i.e. a classical 2-stages Dickson charge pump [4], which can be connected in series or parallel in order to reconfigure the number of stages of the rectifier, as illustrated in Fig. 1. As described in the following, reconfiguring the voltage rectifier according to the input power level benefits twice the circuit performances: i) it allows to improve the sensitivity of the converter, allowing the circuit to operate over a wide input power range, ii) it maximizes the circuit efficiency.

A. Reconfigurable RF-DC Converter

The voltage rectifier has been optimized for maximum efficiency through a procedure which allows determining the optimum transistor width (W) and number of stages (*ns*) of the rectifier, minimizing the power losses of both the voltage rectifier and the matching network [5]. Isolated n-MOS and p-

MOS transistors are adopted for the clamp and the rectifying section of every stage of the voltage rectifier. They avoid the threshold voltage increase due to the body effect, further increasing the circuit efficiency. The drawback of this solution is related to the lower p-MOS transconductance, which needs to be compensated by adopting an higher p-MOS transistor width. This, in turn, increases the parasitic capacitance, that degrades the MN efficiency, as described in the following.

As shown in Fig. 2, the number of stages of the rectifier are reconfigured through the M_A, M_B and M_C transistors: when the control logic signal V_{CTRL} (which can be either generated on chip or provided from the outside) is low (high), the two sections of the rectifier are connected in series (parallel), and therefore the 4-stages (2-stages) configuration is adopted. Such transistors connect DC voltage points, and they has been designed with proper MOSFET width minimizing the power losses due to ON resistance and leakage current. Furthermore, this modular topology can be easily extended to a larger number of stages.

B. *Smart Voltage Regulator*

The SVR block is used to keep the converter output voltage V_{OUT} constant at the reference voltage V_{REF}, see Fig.2. This compensates the unpredictable variations of the input power, making the rectifier working more efficiently independently of the input power.

The operation of the SVR relies on the current-mirror-like branch comprised of M_{F2} and M_{F3}, which keeps constant the M_{F1} gate voltage. Thus, the V_{OUT} increase (decrease) induced by the input power P_{AV} increase (decrease) leads to an higher (lower) $|V_{GS}|$ of M_{F1}, which increases (decreases) the DC output current I_{OUT}, thus counteracting the V_{OUT} variation. For the correct SVR operation, M_{F1} has to be operated in saturation: this means that $V_{CAP} < V_{OUT} - V_{OVMF1}$, where V_{OVMF1} is the M_{F1} overdrive voltage and V_{CAP} is the voltage drop on C_{BUFFER}, which is the charge-storage off-chip capacitor charged by I_{OUT}. I_{OUT} depends on the available input power, and it is proportional to the energy stored into C_{BUFFER}.

C. *Matching Network*

The matching network (MN) plays a crucial role in improving the sensitivity and the efficiency of the RF-DC converter because of the very low power levels involved. The choice of the best MN topology depends on the voltage rectifier input impedance, which is represented by the parallel of the resistance R_{IN} and the capacitance C_{IN}. R_{IN} and C_{IN} are calculated in cyclostationary conditions from the fundamental components of the voltage and current at the rectifier input [6]. After some mathematical simplification, R_{IN} and C_{IN} can be expressed as shown in (1) and (2) respectively.

$$R_{IN} \approx \frac{V_{OUT} + 2 \cdot ns \cdot \left(V_{TH} + \sqrt{2 I_{OUT} / \left(k_N W_N + k_P W_P \right)} \right)}{8 \cdot ns^2 \cdot I_{OUT}} \quad (1)$$

$$C_{IN} \approx \left[\left(C_{GS0\text{-}N} + C_{SB0\text{-}N} \right) \cdot W_N + \left(C_{GS0\text{-}P} + C_{SB0\text{-}P} \right) W_P \right] nt/2 \quad (2)$$

where V_{TH} is the threshold voltage; k_N (k_P) is the n-MOS (p-MOS) transconductance factor; $C_{GS0\text{-}N}$ ($C_{GS0\text{-}P}$) and $C_{SB0\text{-}N}$ ($C_{SB0\text{-}P}$) are the n-MOS (p-MOS) gate-source and source-bulk capacitances per unit-length, respectively; W_P (W_N) is the p-MOS (n-MOS) transistor; *nt* is the number of diode-connected transistors of the rectifier; *ns* is the number of stages.

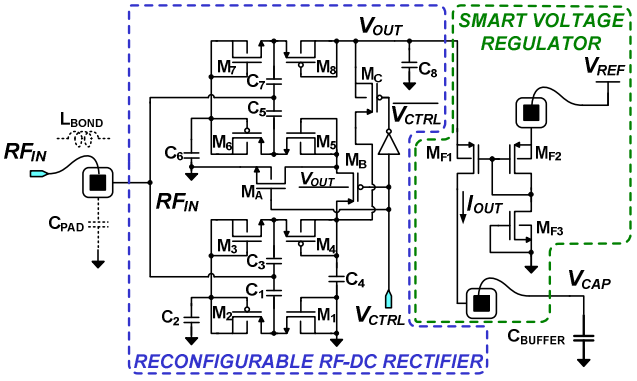

Fig. 2. Circuit schematic of the reconfigurable RF-DC rectifier and the smart voltage regulator blocks.

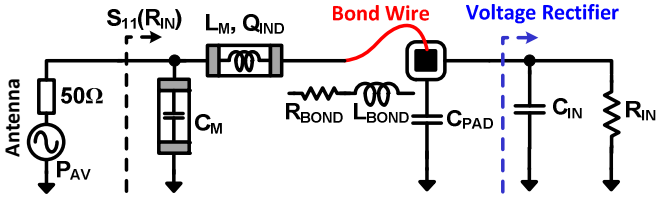

Fig. 3. Matching network π-topology: R_{IN} and C_{IN} represent the real and imaginary components of the voltage rectifier input impedance; C_{PAD} is the pad parasitic capacitance; L_{BOND} and R_{BOND} are the bond wire parasitic inductance and resistance, respectively; C_M is the external matching capacitance; L_M the external matching inductance with quality factor Q_{IND}; $S_{11}(R_{IN})$ is the reflection coefficient at the 50Ω antenna output which depends on R_{IN}.

R_{IN} depends on the number of stages, *ns*, the bias point of the diode-connected transistors (i.e. I_{OUT}) and the MOSFET parameters. R_{IN} depends also on the voltage rectifier DC output resistance $R_{OUT} = V_{OUT} / I_{OUT}$, thus accounting for the power flowing into the voltage rectifier. In particular, R_{IN} decreases when the available input power increases, as V_{OUT} is kept constant by the SVR while I_{OUT} rises. C_{IN} depends on the MOSFET capacitances and the total number of transistors in the voltage rectifier.

As shown in Fig. 3, among the different MN topologies a classic π-topology [5] has been chosen to match the 50Ω antenna impedance to the input impedance of the voltage rectifier. This topology allows to constructively exploit the IC parasitic due to the pad capacitance, C_{PAD}, and the bond wires parasitic inductance and resistance, i.e. L_{BOND} and R_{BOND}, respectively. Furthermore, the π-topology MN allows both maximizing the power transfer through the chain and boosting the signal amplitude, thus improving the overall circuit efficiency.

The operation of the smart voltage regulator, which modulates I_{OUT} in order to keep $V_{OUT} \approx V_{REF}$, changes R_{IN}, which decreases at high P_{AV}, moving the circuit operation further away from the optimum power matching conditions.

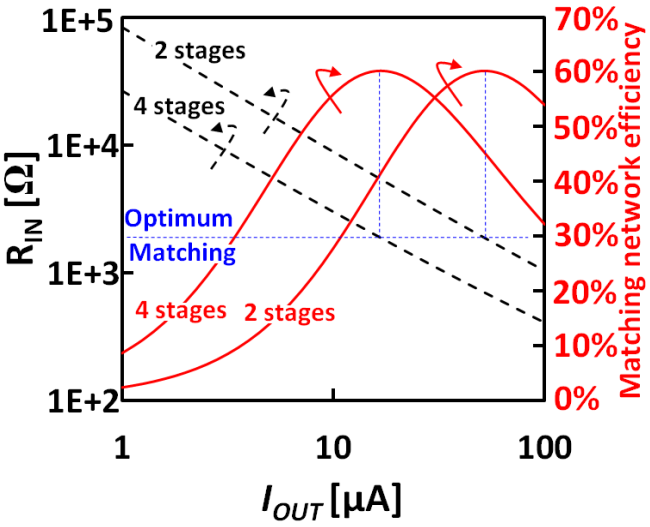

Fig. 4. The simulated voltage rectifier input resistance R_{IN} and the π-topology MN efficiency are plotted versus the rectifier DC output current for either a 2-stages and a 4-stages voltage rectifier.

This reduces significantly the maximum power which can be adsorbed from the antenna. Moreover, the R_{IN} variation affects also the MN ohmic losses, that are related to R_{BOND} and to the quality factor Q_{IND} of the external matching inductor L_M. The MN efficiency, η_{MN}, that includes both mismatch and ohmic losses is given by (3).

$$\eta_{MN} = \eta_{OHM} \cdot \left(1 - |S_{11}(R_{IN})|^2\right)$$
$$\eta_{OHM} \approx \frac{1}{1 + \frac{R_{BOND}}{R_{IN}}\left(1+Q^2\right) + \frac{Q}{Q_{IND}}} \qquad (3)$$
$$Q = 2\pi f \cdot R_{IN} \cdot C_{IN}$$

where f is the RF signal frequency; Q the MN quality factor; η_{OHM} the MN efficiency degradation due to ohmic losses; $S_{11}(R_{IN})$ is the reflection coefficient at the 50Ω antenna output, which depends on R_{IN}. It is worth pointing out that increasing C_{IN}, i.e. the transistor width, lowers the MN efficiency, thus limiting the maximum rectifier transistors width.

The MN efficiency dependence on R_{IN} limits the maximum P_{AV} range where the converter can work efficiently. In the converter circuit we propose, this strong limit which affects the functioning of any converter is overcame by adopting the reconfigurable rectifier topology shown in Fig. 2, which allows compensating the R_{IN} reduction at high P_{AV} by properly adjusting the number of stages. This allows achieving optimum matching conditions at two different power levels, significantly extending the P_{AV} range where the circuit can work efficiently with a standard (not reconfigurable) matching network topology.

The effectiveness of the proposed solution is demonstrated in Fig. 4, which shows the voltage rectifier input resistance and the MN efficiency simulated on a 2- and 4-stages voltage rectifier circuits at various DC output current, i.e. power levels. Since C_{IN} does not depend on *ns* (it depends only on the total number of transistors), changing *ns* from 2 to 4 allows matching the voltage rectifier input impedance at different I_{OUT}, i.e. power levels. This is crucial in order to extend the P_{AV} range where the circuit can operate efficiently.

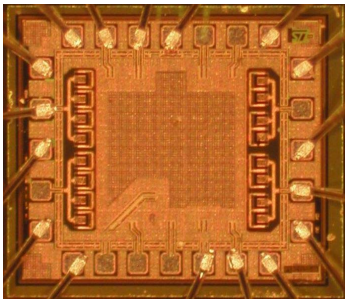

Fig. 5. Microphotograph of the CMOS converter.

Besides improving the MN performance, reconfiguring the voltage rectifier allows also to maximize the efficiency of the rectifier itself over a larger P_{AV} range. In fact, increasing the number of stages allows reducing the losses related to the transistor leakage current, which are more detrimental at low P_{AV}. On the other hand, reducing the number of stages lowers the losses due to the MOSFET on resistance, that penalize the converter efficiency at high P_{AV}, i.e. when an high I_{OUT} flows through the transistors. For these reasons, the optimization of the converter requires to reduce the number of stages with the P_{AV} increase, which can be achieved through the reconfiguration topology proposed in this paper.

III. Experimental Results

Figure 5 shows the realized prototype fabricated in STM 0.13μm with an area occupation of 550 x 400 μm. For the characterization, the chip has mounted on a PCB implementing the off-chip part of the matching network comprised of the matching inductance L_M=33nH (with Q_{IND}=35) and the matching capacitance C_M=4.7pF. Measurements are performed through Agilent RF Source N5181A, considering an insertion loss of 1.5dB for interconnections and cables.

Figure 6 shows the output voltage measured at different P_{AV}, which is maintained around V_{REF}=2V for the wide 20 dB P_{AV} range. The converter starts working at P_{AV}=-17dBm, thus demonstrating a very high sensitivity. Figure 7 shows the converter efficiency, calculated as the ratio between the output power and the RF available input power. The efficiency peak at 60% while remaining above the 40% over a 14dB P_{AV} range, proving the effectiveness of the proposed reconfigurable architecture to widening the operation input power range.

Figure 8 shows the reflection coefficient, S_{11}, measured with Agilent 5071c Network Analyzer at different available RF input powers. As expected, such measurements confirm that the 2-stages and the 4-stages rectifier are matched at different P_{AV} values. It is also important to underline that matching the input impedance at two different P_{AV} values does not necessarily mean to achieve the same efficiency for these two power levels. In fact, the ohmic losses in both the matching network and the voltage rectifier degrade differently the whole converter efficiency.

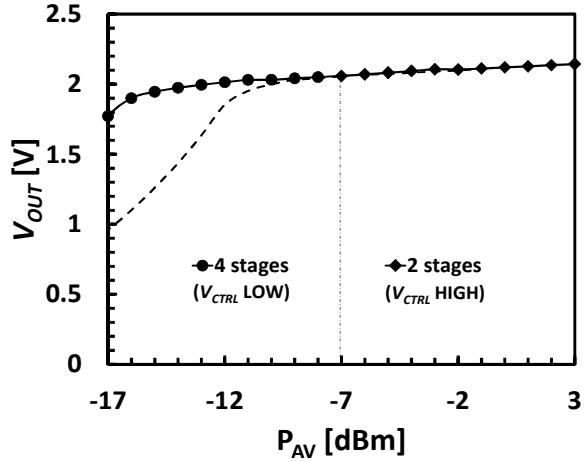

Fig. 6. Output voltage measured at different available input power.

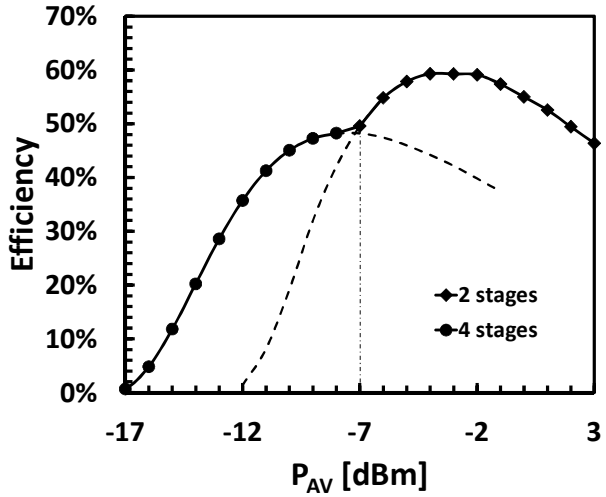

Fig. 7. Efficiency measured at different available input power.

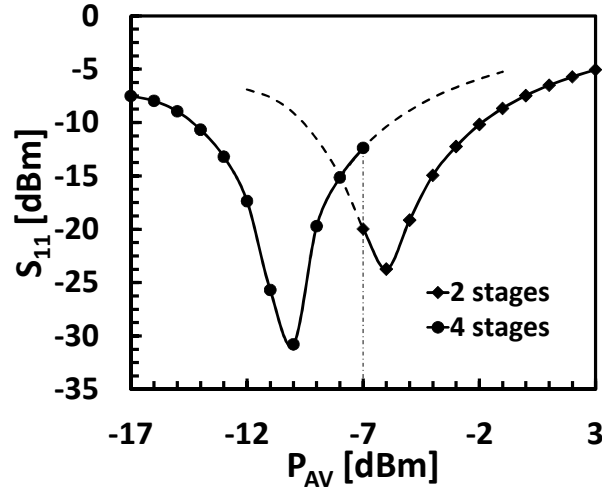

Fig. 8. Reflection coefficient (S_{11}) measured at different available input power

Table I reports the performance metrics, i.e. the maximum efficiency and sensitivity measured on circuit prototypes and reported for prior art works. It is worth noting that the converter circuit we propose shows by far the highest peak efficiency, even though it is fabricated in a standard CMOS technology.

TABLE I

Ref.	Min. RF Power @ V_{OUT}	Peak Efficiency	Technology
This work	**-17dBm@2V**	**60%**	**CMOS 0.13µm**
[3]	-14.7dBm @1.5V	15.76%	CMOS 0.35µm
[7]	-22.6dBm@ 2V (not regulated)	30% (estimated)	CMOS 0.25µm (Floating gate)
[8]	-17.8dBm @ 1.5V	28%	CMOS 0.5µm (Schottky diodes)
[9]	-14dBm @1.5V	11%	CMOS 0.3µm

IV. CONCLUSIONS

In this paper we presented a novel reconfigurable RF-DC conversion circuit that shows a very high efficiency, which peaks at 60%, remaining above 40% over a 14dB range of available input power. The circuit operation is based on a novel smart voltage regulator and a reconfigurable voltage rectifier/multiplier circuit, which compensates the power losses due to input impedance mismatch occurring at different input power levels. The modular topology of the voltage rectifier can be easily extended by increasing the number of reconfigurable stages.

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