

Power Optimization in Johnson Counter through Clock Gating with Static Energy Recovery Logic

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Abstract :- In the latest designs of VLSI, power dissipation is the main charge to take care. The dependency on micro electronics is rising as the size of chip is being compact & also the systems with minimal power are being prioritized. The computer systems are comprised of sequential circuitries & this is the reason that designs having minimal power absorption gave gained priority. In this document, we have suggested a schema on minimal power of Johnson Counter by employing a clock gating system & pass transistors in D flip flop. By making few judgements on power in SPICE, it is presumed that he suggested system design leads to minimal power decandence & has simple interlinking in contrast to the complicated traditional designs. In this document we put the outcomes of power in contrast in four methods that are TG ADCL i.e. Adiabatic Dynamic CMOS Logic, TG QSERL i.e. Quai static energy recovery logic, TG normal & TG split level pulse. Power has risen too high in TG ADCL, TG QSERL & TG normal.

Keywords—clock gating; Johnson Counter; low power VLSI design; power dissipation; sequential circuit

I. INTRODUCTION

A ring counter is considered to be a token that possess register with shifts in circular manner. The outcome generated by the shift register present at the previous node is taken to be as the input for the proceeding one. The significant distances provided beneath are hamming distances of two tokens described as, over beck & counter of Johnson.

- Counter for beck over = 2
- Counter of Johnson = 1

There are mainly two categories considered for tokens applied in ring:

- Counter for beck over = 2
- Counter of Johnson = 1

II. COUNTER OF JOHNSON

There are three names counter of Mobius, counter of Aoebas & counter of a ring are given to this. It links the outcome & input of last & the commencing registers respectively & create a stream of 1's & 0's surrounding the ring.

1. Counter of Johnson (4-BITS)

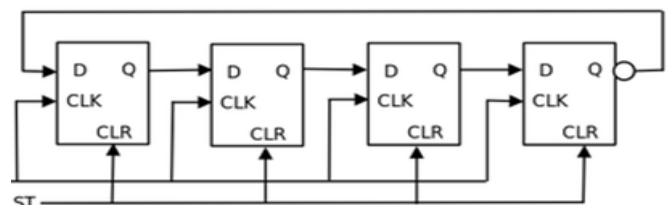


Figure 1.1:- Counter of Johnson

It is to be noted that counters of Johnson can be formulated by reversing the signal Q from the register of shift located at the extremity before providing an input D to the commencing register.

Activate the flip flop by pressing the Green Reset button. The reset button also functions as swith to on & off.

Press the Red CLK button & look at the variations in the outcomes generated by flip flops. This is a fugitive switch which resembles to a door bell. The clock of flip flop D has an edge in the raising direction of input CLK.

As an illustration: As per the behaviour of Q Q₀ – Preceding to the raised edge of CLK, it is accounted as value of input D. As the raised edge of CLK takes place, Q₁ is allocated to last observed value of Q₀.

The count is 6 of a Counter of Johnson comprised of 3 flip

flops.

III. PREVIOUS WORK

In every digitally formed system, counters are taken to be as the main constituent. The counters based on time that have constant & fast nature are cardinally required in designs of VLSI with high speed & also in variegated software's of the system of measurements & communication. The various circuitries like dividers & formulators of frequency, counters with high speed in which counters are implemented & are considered as the main formulating elements. Along with them the counters of time featured on counting on up down, presentation of outcome of radix-2 binary & loading of values is needed.

The circuitry that generates some distinctive compound outcomes with respect to the number of pulses provided as input is termed as Counter. The modulus term defines the number of distinctive outcomes generated by the counter. It is the need of the processes undergoing at a high frequency that each FF of a counter in synchronous state should be triggered at the same instant to avoid any type of flaws encountered. There are two differentiations in a counter which is synchronized in contrast to ripple counter though they both are alike: The implementation of pulses of clock to every single FF with some extra gates putted in that assures that the FFs toggle in a fine manner. The superiority that the counter that is synchronous state possess over the one in asynchronous state is there is no chance for the occurrence of any interruption while the transition of state is ongoing as a single clock synchronize all inputs & so the variations occur in flip flops while the counters that are in asynchronous state, a total delay is calculated by summing up all the delays in propagation. In the present industry of electronics, the main focus is on the absorption of minimal power. The requirement to minimize the absorption of power has drawn the attention along with the area & performance. Also it has become the main focus of the research field in large integrated VLSI circuits. Almost every product consumes some battery even in idle position. Such devices levy high limitations on the decadence of power. Thus deduction in absorption of power enhances the life of battery. Thus the designs that will expend minimal power have become a dare as no significant evolution is seen in field of battery. There are two forms in which power is expended in a circuitry, that are Dynamic & Static power.

The power in dynamic state is comprised of power in short circuiting & switching in a capacitive manner. Whereas the power in static state is comprised of the power decedent because of the currents leaked. CMOS is considered as the leading field for integration of VLSI at an extensive scale. With the advancements in the circuitry of VLSI, there is

enhancement in technology & integration & thus resulting in the clocks possessing very high speed.

The exemption of power is raised due to the high speed of clocks, raised integration level & scaling of technology. Flip flops are the elements formulated on the sensitivity of time which puts a large impact on speed of circuitry & decadence of power in system. The absorption of power by clock is almost 60% of the total power of a chip. Thus the extreme step of segregation of network of clock expends around 90% of the power. There are in standard four sources of decadence of power in digital circuitries constituted on CMOS which are static, short circuit, switching & leakage of power. In the circuitries which are dynamic, the decadence of power while the signal is switched is dominant. To optimize the area & absorption of power, the pass transistors flip flop with D inputs with gated clocks are ployed. Gating of clocks is considered as one of the famous methodologies ployed in several circuits which are in synchronised state, for deduction in decadence of power.

In order to prune the tree of clocks, more logics are implemented in the circuit by gating of clocks which intend to save the power. The removal of clocks from the circuit deactivates some sections of the circuit thus not allowing them to switch in the different states. The states that vary continuously absorb extra power. The absorption of power becomes almost negligible when no switching of states occurs & thus the current indulged from the leakage are induced in it. The look ahead path of states covers the gap in between modules that are being counted & the states that are assumed to be over flowed. The latches of DFF which are pipelined divides the modules that are counted into small segments of 2-bits each. In the similar way the path of look ahead is segmented & thus furnishes the accurately estimated states that overflow for all the stages that are counted. Thus the state of count is activated as all the DFFs that are pipelined are initiated on the side of clock, which is assessed by the states of counts that are less signified. This support of path of look ahead of states & path of counting to each other activates each module of count that is initiated simultaneously. The most firm application of latch of trigger on the side is constituted in pass transistor & invertors. When the state of clock is equal to zero, & also when the transistor of loop of PMOS is switched on, the invertors which are linked to each other are in state of memory. The other invertors that are linked functions in an opposite direction, & the function of reset is accumulated by the straight connection with the ground of slave & master by making use of devices constituted on NMOS technology.

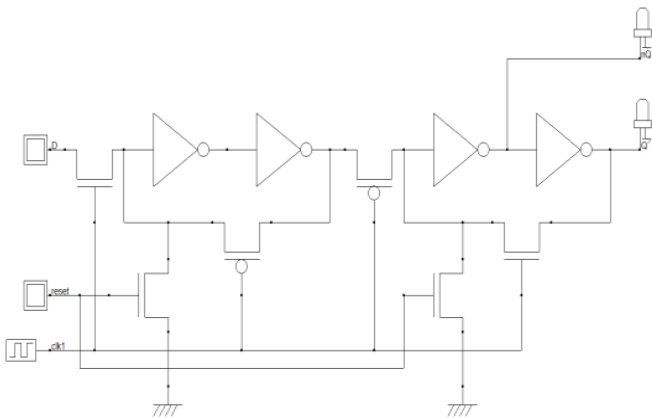


Fig 1.2: Using pass transistors in schema of D flip flop

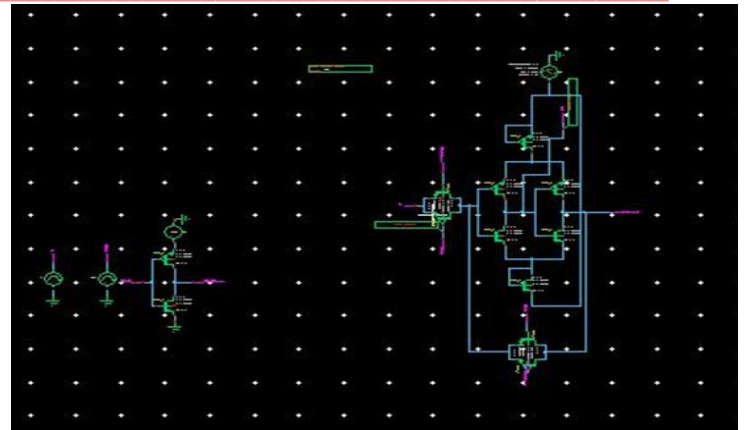


Fig 1.3 :- TG ADCL along the D flip flop

IV. PROBLEM STATEMENT

As mentioned, the outcomes of power are put in contrast in four terminologies that are TG normal, TG ADCL, TG QSERL & pulse of level of TG split. More power is dissipated in TG ADCL, QSERL & normal.

V. CONTER OF JOHNSON & D FLIP FLOP BY MAKING USE OF ADCL

Kaishita et al formulates a new theory by making some changes in the thesis of Mizunuma & Takahashi and which were formed on logics of ADCL. The two circuitries were distinguished by the position of diode that performs function of rectification. There is a significant decrease in the quantity of diodes in ADCL designs & circuits formulated on logics. By making use of a supply of clock in triangle & sinusoidal form, a system with minimal energy is obtained. In order to regulate the flow of charge, two diodes that functions for rectification are deployed on the path of discharging & charging. By making use of MOSFET as a diode, both drain & gate are limited of mosfet. As the diode ployed in the circuit of logistics, with a decrease of potential & so decadence of energy takes place with resistance in devices on MOS& so decadence of energy takes place as there is a drop of potential in the source & drain of the Mosfet's threshold voltage. Later on, by making use of clock in which power fluctuation is less, the decadence of energy will be minimal when the resistance of MOS equipments in activated. The waver representation of logical circuitry of ADCL, 2nd row visualize the input provided to inverter & 3rd row presents clock of power.

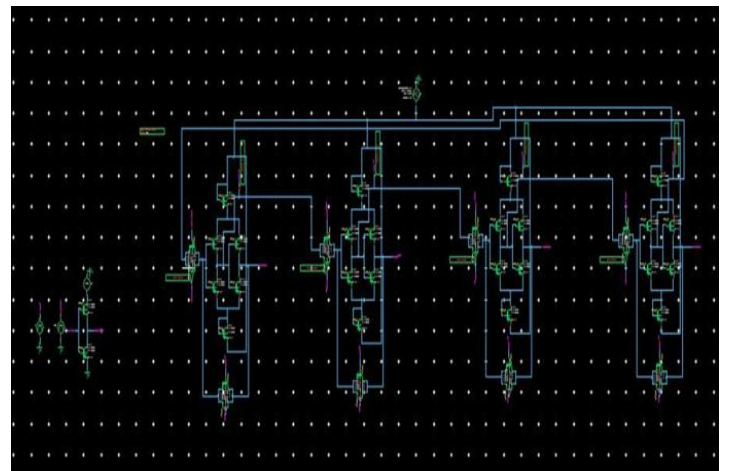


Fig 1.4 :- ADCL along the counter of Johnson counter

VI. TG QSERL ALONG THE COUNTER OF JOHNSON

The logics of CMOS & QSERL are similar to much extent. Diodes that are located on the top node of tree of p-mos will support the way of charging. On the other hand, diode located at the bottom of the nmos tree regulates the way of discharging. The alternate phases of cascaded gates are deployed. The complementary phases of sinusoidal clock clk & clk bar are deployed. The first & last gates are in evaluation & hold phase respectively. While compared to adiabatic logic of dynamic state, QSERL is static. The mosfet with minimal voltage replace the diodes of QSERL that regulates the ways of discharging & charging.

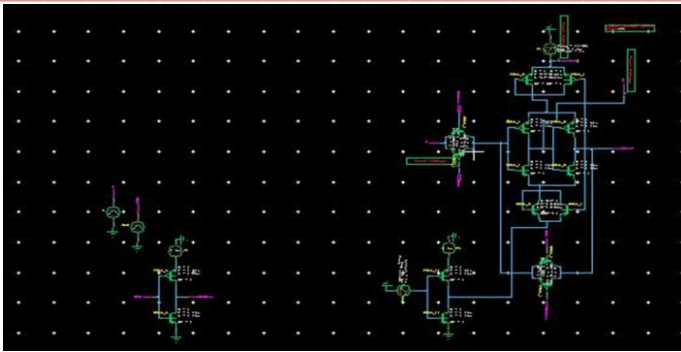


Fig 1.5 :- TG QSERL along the D flip flop

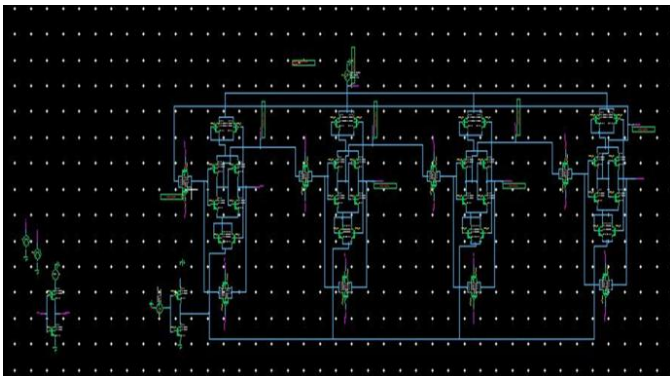


Fig 1.6:- TG QSERL along the counter of counter of Johnson

VII. PROPOSED METHODOLOGY

In order to make the dissipation of power minimal in circuits lying in their synchronous state, gating of clocks is one of best approach considered so far. In order to prune the tree of clocks, more logics are implemented in the circuit by gating of clocks which intend to save the power. The removal of clocks from the circuit deactivates some sections of the circuit thus not allowing them to switch in the different states. The states that vary continuously absorb extra power. The absorption of power becomes almost negligible when no switching of states occurs & thus the current indulged from the leakage are induced in it.

The condition of gating of clocks makes use of situations activated to join the registers in & thus do clock gating. So in order to make the best use of gating of clocks & gain some advantage from it, it is highly recommended to invade these conditions of activations in the design. As a large quant of muxes are eliminated & replaced by the logics applied by gating of clocks, this process also preserves the power & die area. The standard representation of logics formulated by gating of clocks is ICG ie. Cohesive gating of clock, But since the logics will be retained in the form of a tree of clocks these logics may make some significant variations in the design of tree of clocks.

There are numerous ways to implement the logics of gating of clocks in the design:

Embedded into the code of RTL as by the activation policies that may be transformed by themselves into logic of gating of clocks by tools that are synthesized.

The designers of RTL invade the design by their own by invading the library specified as ICG cells that gate the clocks of particular registers.

By the automatic tools for gating of clocks, semi automaticity is invaded in the RTL. Either cells of ICG are invaded in to RTL or conditions for the activation are embedded into the code of RTL. This eventually provides optimization of gating of clock in a sequential manner.

Note: the re-evaluation of the variations of functions is needed to be done as there are variegated values accumulated in the registers, as an outcome by the intention of manipulations done in RTL for improvisation of gating in clocks.

The process to withdraw the conditions of activation to the elements of downward or upward stream in a sequential manner is termed as gating of clocks in a sequential manner & thus the extra registers can be gated by clock.

So, as per the explanation, the circuits which are asynchronous don't possess a clock.

To express the reaction of circuit of asynchronous state that are constituted on the basic probabilities on the dependence of data, this term is described the absolute gating of clocks. By the time the granularity attains zero value, on which the circuit in synchronous state is gated on, the absorption of power becomes equivalent to a circuit in asynchronous circuit. The logical transactions are produced only when the computations are performed actively.

The community of chips like OMAP3 accumulated with mobile phone assist variegated types of gating of clock. On one side gating of clocks can also be done manually by making use of driver software that activates or deactivates the clocks required by a controller retained at a neutral state, while on the other side the gating of clocks can also be performed automatically in which the hardware itself analyze the usage of clock & turn it off when it is not in use. These types of forms can communicate with each other & may become the part of a same segment. As an illustration the internal bus may use automated form of gating & thus it is made as off gate still it is required by DMA or CPU or else various accessories

For example, an internal bridge or bus might use automatic gating so that it is gated off until the CPU or a DMA engine

needs to use it, while several of the peripherals that are deployed on the bus may be gated off for permanent if they are not in use in any manner.

There is almost more than half of the power is absorbed by a tree of clocks.

The major constitutes of the power are listed as:

- 1) The power absorbed by the logics of combinational circuits where values fluctuates on each side of clock.
- 2) The flip flops that absorb power.
- 3) Power that is absorbed by the buffer of tree of clock in design.
- 4) It is a good approach in the design to deactivate the clock when it is not in use. The latest tools of EDA assist the clock gated which is automated. The look after the circuitries where it is possible to invade the gating of clock.

The functioning of gating of clocks formulated on RTL is on chosen set of flip flops which share a standard activated signal for controlling. To regulate the select on a mux that is linked to the port D of the inputs of flip flop or the activated pin of the flip flop that possess clock activation abilities, some conventional terminologies are ployed to accomplish this task. The circuitry with the gating of clock is regulated by making use of activated signal by gating of clock by RTL that is linked to the ports of clock of each flip flop having a standard term of activation. Thus all the flip flops will absorb the power approximately null by the application of gating of RTL clocks that is comprised in a set of flip flops that all have a standard activation terminology till this signal is in false state.

There are mainly two forms of gating of clock gating are present:

- 1) Latch on which gating of clocks is formulated
- 2) Latch that if free of gating of clocks

A. Latch Free Clock Gating

There is a standard OR or AND gate is ployed in the gating of clock that is not comprised of latches. In this scenario the outcome of clock that is gated can either be stopped before completion or may produce several pulses of clock if the activated signal goes to inactive state while the pulse of clock is undergoing the process. This is the main limitation of this form of gating for our proposed design of flip flop constituted on a solely ployed clock.

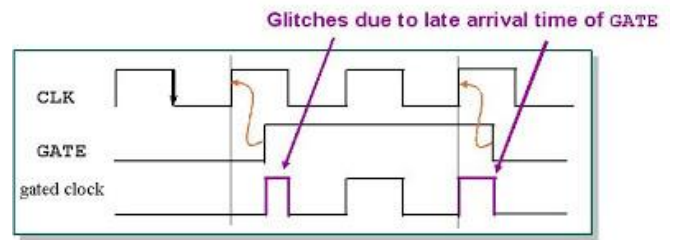
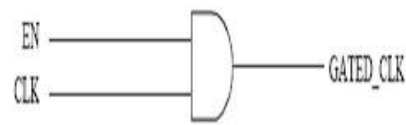


Fig 1.7:- Gating of clock free of latch

B. Gating Of Clock Constituted On Latch

A latch possessing sensitivity is summed up to this form of gating that retains the activation signal from the side of clock that is active to the side which is in inactive state. As the latch accumulates the position of the activation signal & retains it till the process of formulation of pulses of clock is completed, there is only need of activation signal to be in a stable state on the side of clock which is raised as similar to the conventional design of ungated clocks.

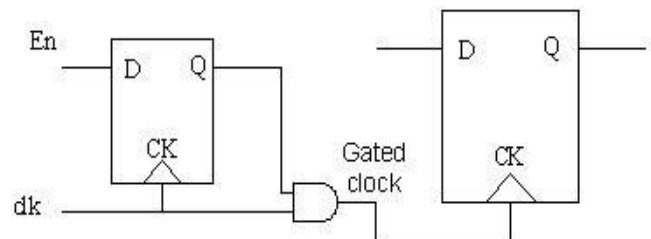


Fig 1.8:- gating of clocks constituted on latch

Some defined cells of gated clock are needed by the library whose tolls of synthesis make best use of them. The invasion in an automated manner by the tools of EDA along with the available that are gated by clocks proposes a simple methodology for low consumption of power. The superiority it possesses over the other technique is that no further changes are needed in it as per the definition of RTL.

n this type of simulation, we go through the impact that fall & rising time of counter of Johnson puts on the decadence of energy. A splintered level of pulse is deployed to eliminate any occurrence of mixed signals of outcome. The simulation that collates the decadence of energy of a splintered level of pulse with the ADCL & SERL will be implemented.

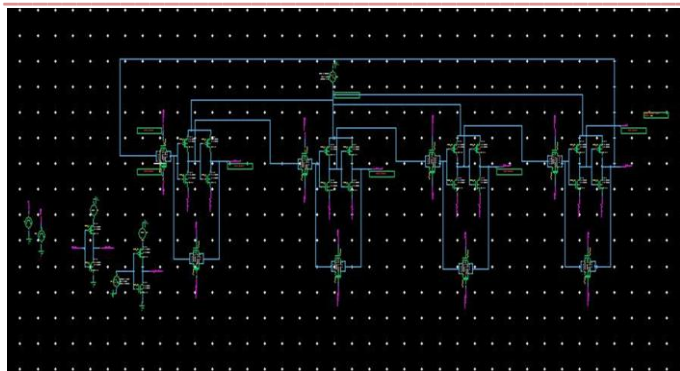


Fig 1.9 :- Counter of Johnson constituted in level of split of TG

VIII. RESULTS

A. TG ADCL Along The D Flip Flop

As per the design, whenever TG ADCL is implemented for a flip flop with input D, the outcome of power will be $7.493027e-007$ W.

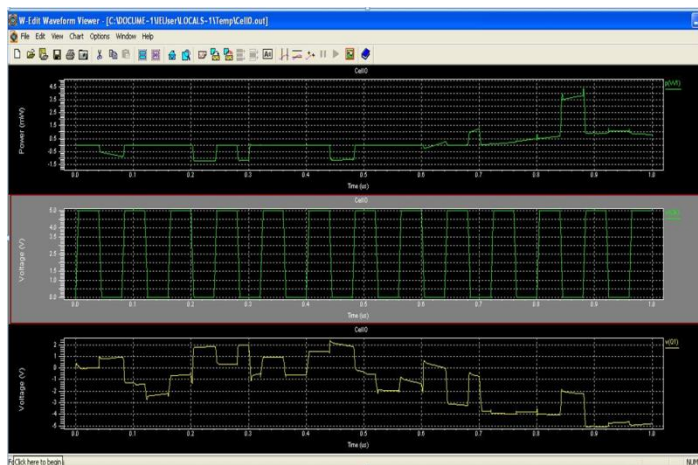


Fig 1.10 :- TG ADCL along the D Flip Flop

B. TG Normal Along The D Flip Flop

Here for a flip flop D, a standard TG is implemented. The power generated as an outcome will be $7.787218e-007$ W.

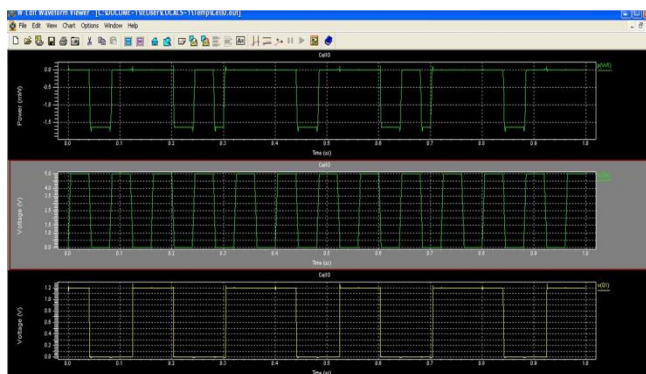


fig 1.11 :- TG NORMAL Along the D Flip Flop

C.TG QSERL along with D FLIP FLOP

Here for a flip flop with an input D, a TG QSERL is implemented. The power of outcome obtained is $8.344963e-007$ W.

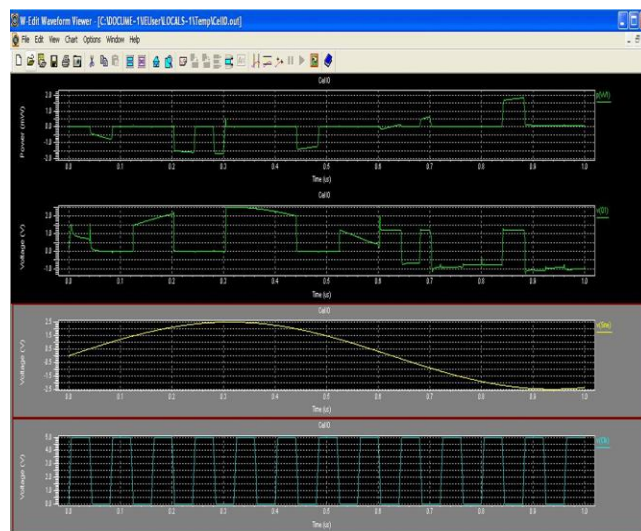


fig 1.12 :- TG QSERL along the D FLIP FLOP

D. TG Level of SPLIT Along The D Flip Flop

Here for a flip flop with input D, diversified level of D is implemented. The power of outcome obtained is $7.508064e-007$ W.

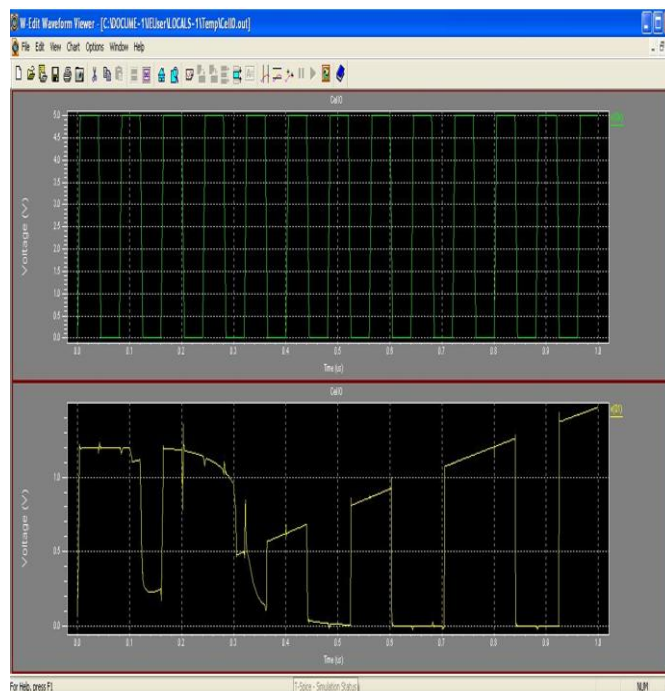


Fig 1.13 :- TG level of split along D Flip Flop

E. TG ADCL along the COUNTER of JOHNSON

Here a diversified level of TG for Johnson Counter along with the TG ADCL is implemented. The power of outcome obtained is 1.096218e-006 W.

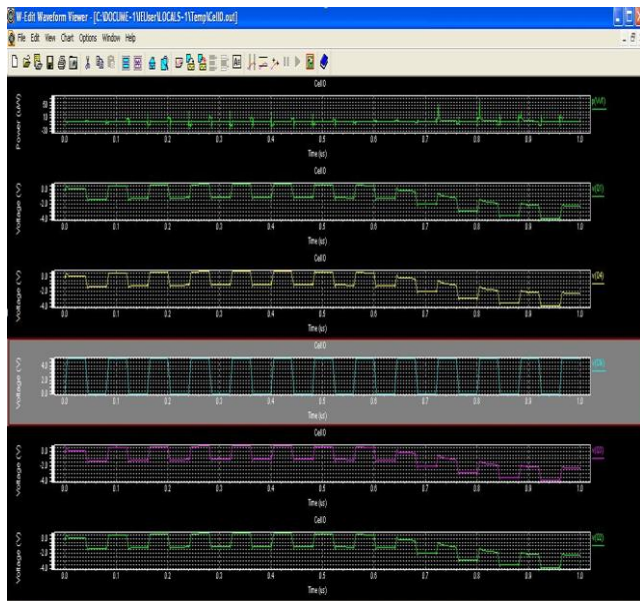


Fig 1.14:- TG ADCL along the Counter of Johnson

F. TG QSERL along the Counter of Johnson

Here a diversified level of TG for Johnson Counter along with the TG ADCL is implemented. The power of outcome obtained is 1.292338e-006 W.

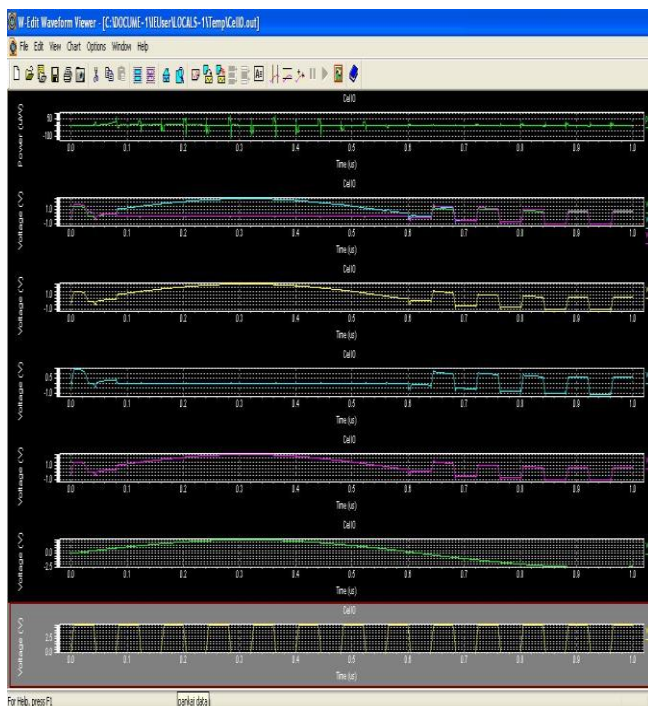


Fig 1.15:- Tg Qserl along the Counter of Johnson

G. Pulse Of Split Level Of Counter Of Johnson

Here a diversified level of TG for Johnson Counter along with the clock gating & split level of TG is implemented. The power of outcome obtained is 1.028622e-006 W.

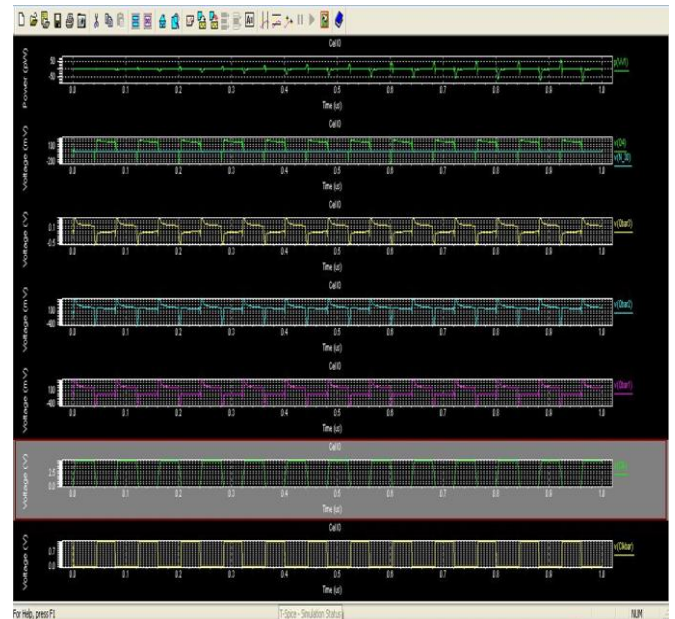


Fig 1.16:- Gating of clock & split level of TG along the Counter of Johnson

Circuit name	POWER(VV2)
D Flip Flop with TG ADCL	7.493027e-007 watts
D Flip Flop with TG Normal	7.787218e-007 watts
D Flip Flop with TG QSERL	8.344963e-007 watts
D Flip Flop with TG split level	7.508064e-007 watts
Johnson Counter with TG ADCL	1.096218e-006 watts
Johnson Counter with TG QSERL	1.292338e-006 watts
Johnson Counter with TG Split Level Pulse(Proposed circuit)	1.028622e-006 watts

Table 1.2:- table of comparison

IX. CONCLUSION AND FUTURE SCOPE

To assess the decadence of power in the design, the simulations of SPICE are performed in each segment. Our main concern is the decadence in the current in circuit that is due to transition of clock. Also for the basic traditional design an assessment of the power is also run in form of simulations.

Though decadence in power because of gating of clock is brought down by approximately %, thus taking into account the whole system as well with the system of gating of clock, it is observed that the decrease in decadence of power is at most 21% putting in contrast to counter of Johnson along with the decadence of power QSERL system. It signifies that occurrence in power decadence in more by this system of gating in clock. Though the system designed by us works in accordance with the power ahead of the traditional designs proposed earlier.

With furtherance, GDI method can be implemented to enhance the power performance. By deduction of the length of channel the delay occurring in the system can be minimized.

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