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Advanced Shift Register Design Using PSDRM Reversible Logic

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***Abstract*—** Reversible logic is one of the most important issues at the moment, with the different areas like low power CMOS devices, quantum computing, nanotechnology, cryptography, optical computing, DNA Computing, digital signal processing (DSP) etc. This can be achieved using reversible logic. The main purpose for designing reversible logic is to minimize cost and throughput. Reversible logic considered as a computing model in which there is one-to-one scaling between their input and output. Power distribution is considered as one of the most important aspects while designing circuit. Reversible logic has become an encouraging technology in low power circuit design. That's because back logic uses only very less power, thus resulting in reduced power dissipation.

In this report, we proposed a new reversible gate, and with the help of this gate we have designed our asserted D flip-flop by using the two reversible gates i.e. by using Fredkin and Feynman Gate. The proposed design is better in terms of the average power consumed, number of gates and garbage output than existing.

In Shift Register, we introduce a reversible D flip-flop by using FRG and FG gate in the place of existing D flip-flop which used Sayem Gate. The asserted design consumes less energy compare to traditional circuitry. Here we use Pseudo expressions (PSDRM). By using this technology there is an improvement in the factors, such as number of transistors, garbage output, quantum cost and power.

Keywords- *Reversible logic, reversible logic gates, low power VLSI, quantum computing, garbage output, quantum cost.*

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I. INTRODUCTION

Now days, reversible computing has emerged as a fast growing technology. The main reason for this is the tremendous increasing demands of the devices that have lower power. R. Landauer in the early 1960s demonstrated that losing of information in the process of execution in the form of bit cause loss of energy. Loss of information occurs when the input vector is not uniquely recovered from the output vector. According to Rolf Landauer's [1] principle the loss of each bit of information generates KTln2 Joules of energy. The K here represents the Boltzmann's constant whose value is $1.3806505\times10^{-23}m^2kg^{-2}k^{-1}$(joule/kelvin^{-1}) and the absolute temperature T at which operation is carried out. The generated heat due to information loss is quiet a very small at room temperature but when the information bit is very high as in the case of high computation work the generated heat is very large so that it affects the performance of the device. This cause the reduction of the lifetime of the device, Latter in 1973s C. H. Bennett showed that KTln2 energy dissipation problem can be avoided if the system allows the reproduction of the input vector from observed output vectors. In simple language if the circuit is made of reversible logic gate. The number of bit erased during the computation process is directly related to the amount of heat generated. Reversibility in computing implies that no information about computational states may

Ever lost, hence we may recover an earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. Computing systems give off heat when voltage levels change from positive to negative i.e. bits from zero to one. Most of the energy needed to make that change is given off in the form of heat rather than changing voltages to new levels. Reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. Many researchers are working in this field, very few work has been done in the field like sequential reversible circuit. According to Moore's law, on every 18 months the number of transistor will be double. Therefore the conservation of energy is must need of modern devices. The current irreversible circuit consumes lot of energy and therefore cause of reduce the lifetime of the circuit. The solution is to develop a new technology that enables extremely low power consumption and dissipation of heat is also very low.

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1.1 REVERSIBLE LOGIC GATES

A reversible logic gate is an n-input n-output logical device with one-to-one mapping. In reversible logic gate the input vector is uniquely recovered from the output vector and vice-versa. Suppose I_V is the input vector where $I_v = (I_1j, I_{2J}, I_{3J}\ldots\ldots I_{k\text{-}1J}, I_{kJ})$ and O_v is the output vector where $O_v = (O_1j, O_{2J}, O_{3J}\ldots Ok_{\text{-}1J}, O_{kj})$, then as per definition for every j I_v O_v. This serves to focus the outputs from the inputs; furthermore the inputs can be particularly recuperated from the outputs. On the other hand direct fan-out is not permitted in reversible circuit as one–to-many idea is not reversible. The problem of fan-out in reversible circuits is accomplished by utilizing additional gates. A reversible circuit ought to be designed by utilizing least number of reversible logic gates. From the perspective of reversible circuit design, there are numerous parameters for deciding the complexity and execution of circuits.

1. The total number (quantity) of reversible gates (n): the quantity of reversible gates which utilized as a part of circuit.

2. The total number of constant inputs used (CI): This alludes to the number of inputs that are to be kept up constant at either 0 or 1 so as to synthesize the given logical function.

3. The total number of garbage outputs (GO): This alludes to the quantity of unused outputs introduce in a reversible logic circuit. One can't maintain a strategic distance from the garbage outputs as these are exceptionally fundamental to accomplish reversibility.

Quantum cost (QC): This alludes to the expense of the circuit as far as the expense of a primitive gate. It is ascertained knowing the quantity of primitive reversible logic gates (1*1 or 2*2) needed to understand the circuit.

1.2 FEYNMAN GATE (FG)

Feynman Gate is 2*2 gates shown in figure 1.1. It has 1 quantum cost. It is also called CNOT

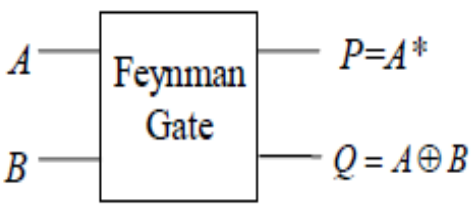

Figure 1.1:- (a) Block diagram of Feynman Gate

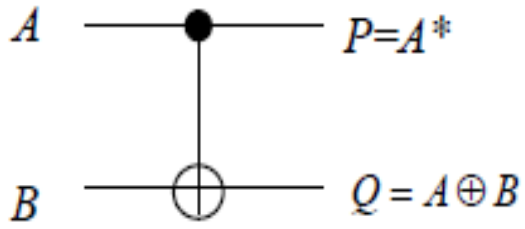

Figure 1.2:- (b) Quantum representation of Feynman Gate

I.e. Controlled NOT gate. An input vector is I_V (A,B) and an output vector is O_V(P,Q). And outputs are characterized by (P=A, Q = A XOR B). Quantum cost of FG is 1. FG may be utilized as copying gate (assigning B=0). Since a fan out isn't permitted in the reversible logic, this gate is valuable for duplication of the obliged outputs (assigning B=1).

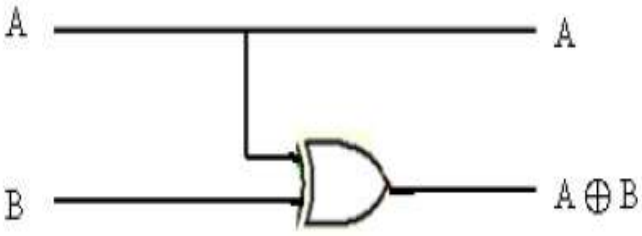

Figure 1.3:- Logic circuit of Feynman Gate

input		output	
A	**B**	**P**	**Q**
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1.1:- truth table of Feynman Gate

1.3 THE FREDKIN GATE (FRG) (ADDITIONALLY CSWAP-GATE

The Fredkin Gate is 3*3 gates. I_V = (A, B, C) are the input vector and O_V= (P, Q, R) are the output vector. The output O_V = (P=A, Q = $\bar{A}\,B \oplus A\bar{B}, \bar{A}\,C \oplus AB$). Computational circuit which is suitable for the reversible computing, concocted by Ed Fredkin. It is universal, which implies that any arithmetic or logical operation may be built altogether of the FRG. FRG is 3-bit gate which swaps last two bits if first ever bit is 1

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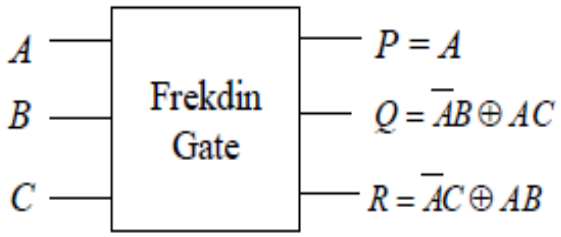

Figure 1.4:- (a) Block diagram of Fredkin gate

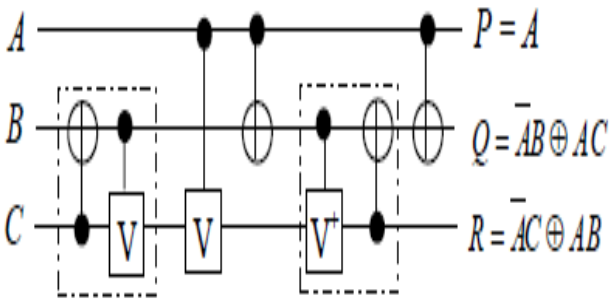

Figure 1.5:- (b) Quantum representation of Fredkin Gate

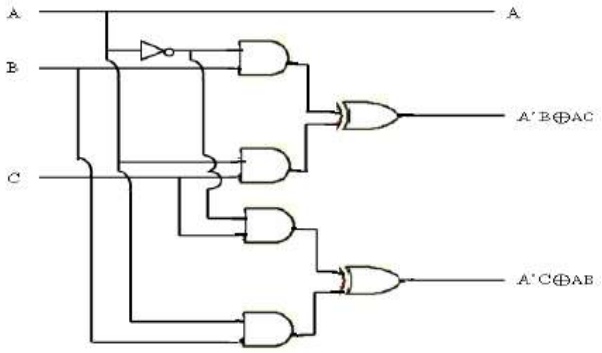

Figure 1.6:- Logic circuit of Fredkin Gate

TRUTH TABLE

INPUT			OUTPUT		
C	I1	I2	C	O1	O2
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Table 1.2:- Truth table of FRG Gate

The essential FRG is controlled swap gate which maps the three inputs (A, B, C) on to 3 outputs (P, Q, R). Input A is then mapped specifically to the P output. In the event that P=0, no swap is then performed, B maps to Q, and C maps to R. Something else, two types of outputs are then swapped, hence B maps to R, and C maps to Q. It's anything but difficult to see which particular circuit is a reversible, i.e. "fixes" itself when run in reverse. A summed up n×n Fredkin gate passes its first n-2 inputs unaltered to the comparing outputs, and the swaps its last two outputs if and if the first n-2 inputs are each of the 1. The FRG is reversible 3 bit gate which swaps last two bits if first bit is 1.

1.4 SAYEM GATE

Sayem Gate is a 4*4 gate having input vector I_V = (A, B, C, D) and the output vector O_V= (P, Q, R, S). The output are shown as

O_V= (P=A, Q=A'B⊕AC, R=A'B⊕AC⊕D, S=AB⊕A'C⊕D

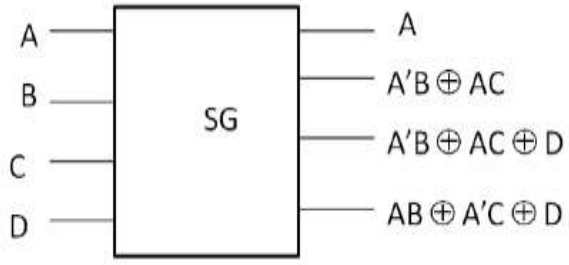

Figure 1.7:- Sayem Gate

A. REGISTERS

A registers is a group of flip-flops or binary cells setup in a linear fashion with their inputs and outputs which holds the binary information. It has two basic functions Data Storage and Data Movement. The flip-flops are connected in such a way that the data is shifted from one device to another when the circuit is active. Since a binary cell stores a bit of information, a n-bit register has n flip-flops and capable of storing any information of n-bits. A registers may have a combinational gates that perform some processing task of certain data. The registers have logic gates and flip-flops. The flip-flop store the binary information and gates control the transition of information to the registers. Unlike combinational logic sequential logic is not only offered by the present input rather than it also depends on the past history. In simple way we can say that sequential circuit remember past events. The simplest possible register is one that consists only flip-flops

B. SHIFT REGISTER

A shift register is a device which is capable of shifting binary information either to the left or to the right. This is in the same way as memory register is used to store information in binary forms. This stored data may be transfer from one address to some other address within the register with the help of shift register. So a flip-flops are

connected in the shift register such a fashion so that the input binary number into the shift register is shifted from one address to another and then shifted out finally. The Shift Register is some different category of logic circuit that are sequential whose usage can be for the accumulation of data or transferring it in the form of binary numbers that are referred as 0,1. The data that available is being loaded on inputs by this sequential appliance and then it is 'shifts' to its outcome one time in each clock cycle, hence its named as shift register. A general four bit shift register can be designed by using four D-flip-flop.

There are four possible ways to categorize the shift register—

- Serial-in to Serial-out (SISO):- in the siso inputs are provided serially from a single input line one by one bit and also the output is generated serially.
- Serial-in to Parallel-out (SIPO):- in the sipo input are provided serially i.e. one by one bit and output are taken simultaneously from all the flip-flops.
- Parallel-in to Serial-out (PISO):- in the piso the input data are provided or stored simultaneously. Outputs are drawn bit by bit i.e. serially.
- Parallel-in to parallel-out (PIPO):- in the pipo the input data and output data both are provide and drawn parallel manner.

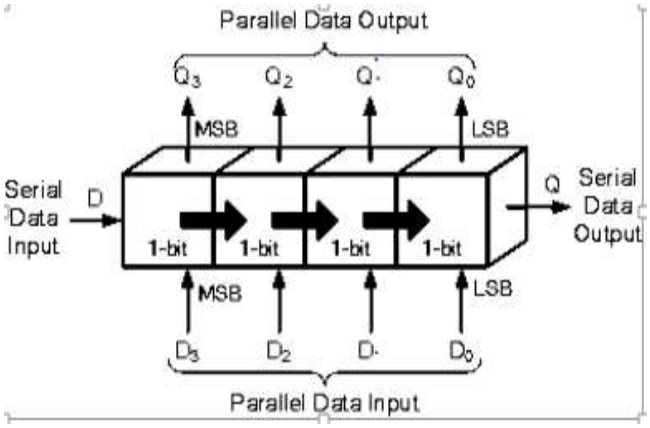

Figure 1.8:- Shift Resistors

II. LITERATURE REVIEW

In this section, detailed literature review done that aims to review the critical points of the current it works. Here the information collected on research and innovations carried out in the related technologies have been made. In this section you will highlight recent trends and innovations in the technology in question. Landauer [1] determined that the amount of energy dissipated by the loss of each bit information is at least kTln2 (where k is the Boltzmann constant that is 3 * 10 ^ 12 joules in the room temperature). During any calculation intermediate bits used to calculate the final result is lost, this loss of bits is the main reason for power dissipation. C. H. Bennett [2] in 1973 discovered that the power dissipation in any device can be zero or insignificant if the calculation is performed using reversible model. The theory was tested with the Turing machine which it is a model for the symbolic computation developed by Turing. Bennett also showed that the calculations they performed or irreversible classic machine can be performed with equal efficiency in the reversible machine. Based on the Previous research concept of reversibility was started in 1980. H R and M.K Venkatesha Bhagyalakshmi [3]. We discussed an overview of a multiplier and some of the reversible logic gates. A reversible logic door is an n-output n-input logic device with each other a mapping. This helps determine the outputs entries and entries can be only outputs recovered. Arunkumar P Chavan [4] proposed the pulse and unsigned multiplier detector. He also explained 4-Bit PISO reversible change log. Here the 4-bit shift registers synchronized FLOOR uses four reversible D flip-flops and four Fredkin Gates. Reversible Fredkin gate is used to develop a multiplier with enable signal. Similarly, a basic three reversible bit SIPO shift register can be constructed using three reversible clocked D flip-flops and two Feynman Gates. Praveen J and M N Shanmukaswamy [5] have new power reduction technique proposed LFSR using logic modified for VLSI circuit control. Is He explained that LFSR is a proposed technique targets to reduce energy consumption in the BIST. Energy consumption is reduced during the test a circuit under test (CUT) in two stages of testing. In initially, the control logic (CL) causes the clock change units idle for a period of registration time when the output of which is the same as above output and therefore reducing the switching flip- flop. In the second stage, LFSR reorders the test bit vectors exchanging its next and bit nearest neighbor. The ability of fault coverage is maintained Vector unchanged, but reduces the total
Hamming distance (THD) such that there is a reduction
In power while the operation is changed.

III. OBJECTIVE OF OUR WORK

In modern computing device we have packed more and more logic circuits into smaller and smaller volume and operate them at higher and higher clock frequency. This dissipates large amount of heat. These cause three problems.

- Generated Energy costs money.
- Portable devices exhaust their batteries.
- Overheating of devices.

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So, if we want to enhance the performance of the computing device we must continue to reduce the dissipated energy from each of the logic operation. Therefore an alternative method regarding this problem is the reversible logic. In the base paper a new D flip flop whose proficiency is indicated regarding number of gates, constant input and garbage output.

3.1 EXISTING DESIGN

3.2

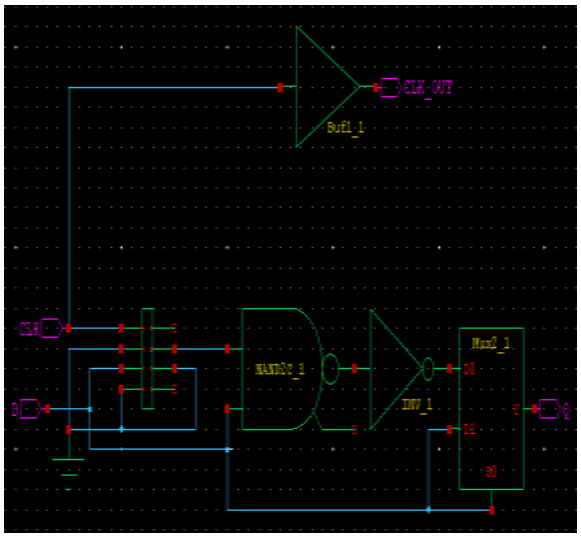

Figure 1.9:- Circuit design of existing D flip-flop

IV. PROPOSED WORK

In proposed design we substitute a new reversible logic gate called PSDRM logic gate in the place of D flip flop, which is used in the shift register. The proposed D flip flop design use only two reversible gate i.e. Feynman Gate and Fredkin Gate.

4.1 PROPOSED PSDRM DESIGN

In the PSDRM design, we have two inputs and two output. We simply utilize it at place of reversible logic gate. First the input is stopping by clock then one input part is going in buffer and one section is going in FRG Gates.

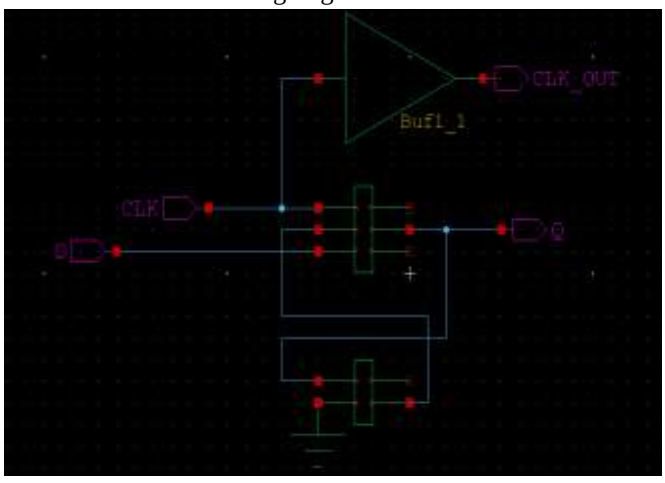

Figure 1.10:- circuit design of proposed reversible PSDRM D flip-flop

4.2 PROPOSED SISO BY PSDRM

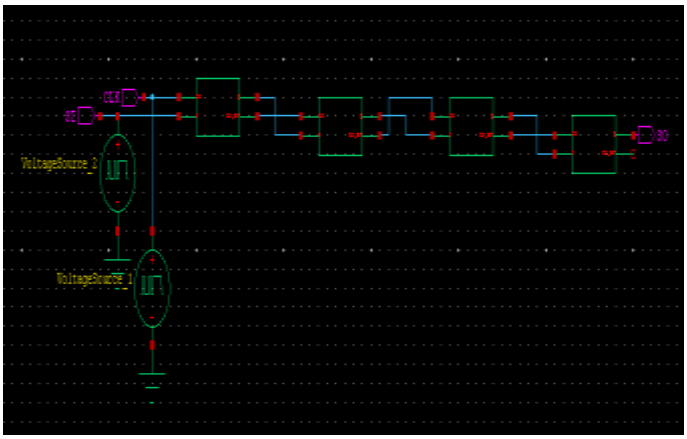

Figure 1.11:- circuit design proposed SISO by PSDRM

We have two input one is clk and SISO in, SISO out is an output. At the rising edge of clock the waveform are changing. As the rising edge will come the output value of the SISO get change.

4.3 PROPOSED PIPO BY PSDRM

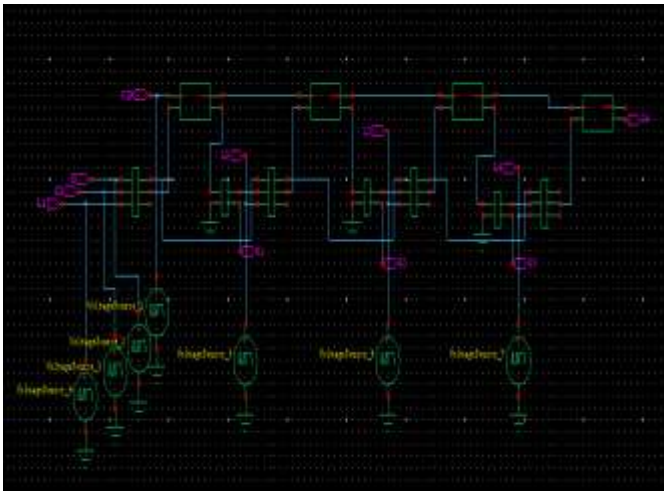

Figure 1.12:- circuit design of PIPO (Proposed)

We have 6 inputs for PIPO. These are clk (clock), enable (E), first input (L1), second input (L2), third input (L3), fourth input (L4). PIPO out is an output. At the rising edge of clock the waveform are changing. As the rising edge will come the output estimation of the PIPO get change.

PROPOSED PISO BY PSDRM

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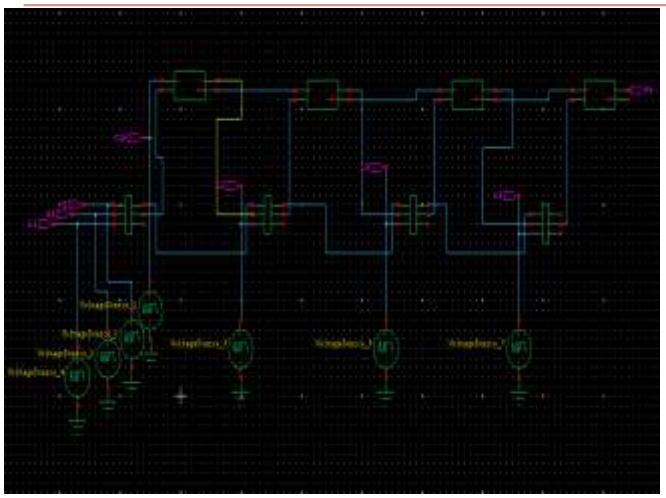

Figure 1.13:- PISO (proposed)

We have 5 inputs for PIPO. These are clk (clock), first input (L1), second input (L2), third input (L3), fourth input (L4). PISO out is an Output. At the rising edge of clock the waveform are changing. As the rising edge will come the output estimation of the PISO get change.

4.4 PROPOSED SIPO BY PSDRM

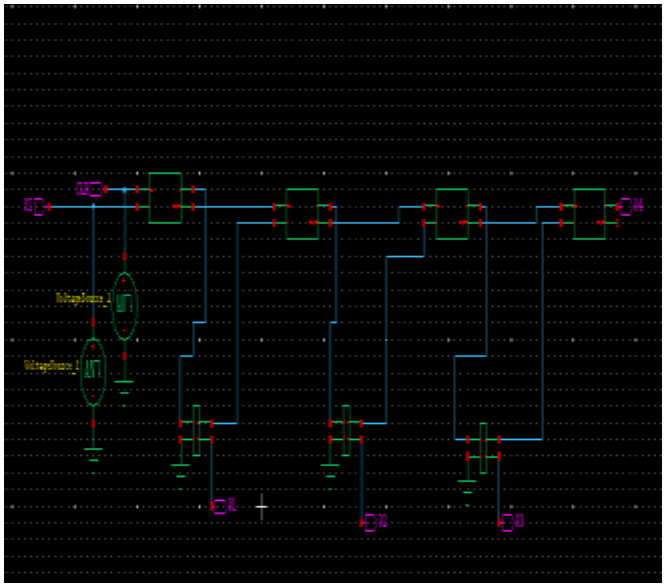

Figure 1.14:- SIPO (Proposed)

We have 2 inputs for SIPO. These are clk (clock), input (SI).four output first output (L1), second output (L2), third output (L3), fourth output (L4). At the rising edge of clock the waveform are changing. As the rising edge will come the output estimation of the SIPO get change.

V. IMPLEMENTATION AND RESULTS

5.1 SISO

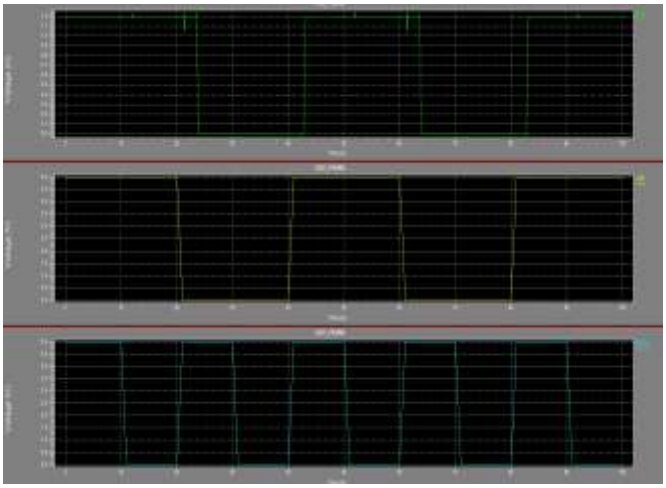

Figure 1.15:- Waveform of SISO

Power consumption results for existing (SISO) design	**Power consumption results for proposed (SISO) design**
Power Results vi from time 0 to 1e-007 Average power consumed -> 1.237301e-003 watts Max power 9.299949e-003 at time 1.17118e-008 Min power 3.093995e-007 at time 2.60551e-008	Power Results vi from time 0 to 1e-007 Average power consumed -> 3.985935e-004 watts Max power 6.918048e-003 at time 9.14931e-008 Min power 1.230782e-007 at time 7e-008

5.2 SIPO

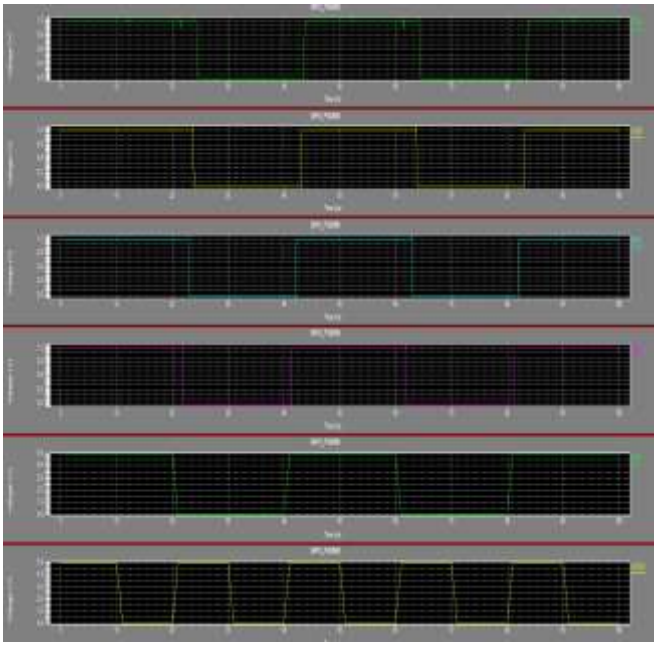

Figure 1.16:-Waveform of SIPO

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Power consumption results for existing (SIPO) design	Power consumption results for proposed (SIPO) design
Power Results vi from time 0 to 1e-007 Average power consumed -> 1.272417e-003 watts Max power 9.300387e-003 at time 1.17118e-008 Min power 3.602517e-007 at time 1.76761e-008	Power Results vi from time 0 to 1e-007 Average power consumed -> 4.316998e-004 watts Max power 6.913417e-003 at time 5.1493e-008 Min power 1.989400e-007 at time 0

5.3 PISO

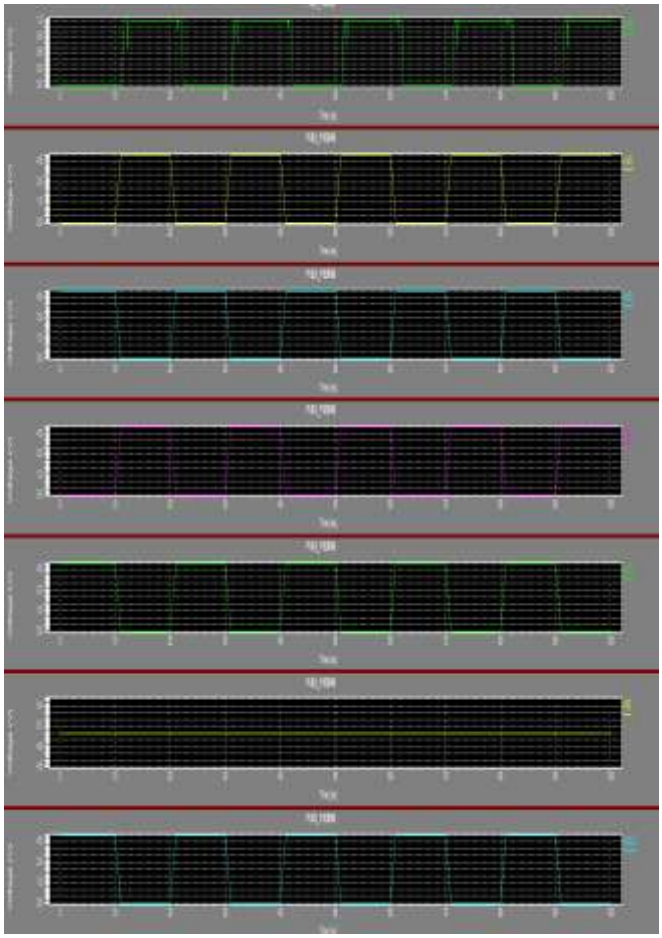

Figure 1.17:- waveform of PISO

Power consumption results for existing (PISO) design	Power consumption results for proposed (PISO) design
Power Results vi from time 0 to 1e-007 Average power consumed -> 1.424601e-003 watts Max power 1.073765e-002 at time 1.16949e-008 Min power 7.179393e-007 at time 4e-008	Power Results vi from time 0 to 1e-007 Average power consumed -> 8.057609e-004 watts Max power 8.556921e-003 at time 1.15135e-008 Min power 1.945659e-007 at time 1.64713e-008

5.4 PIPO

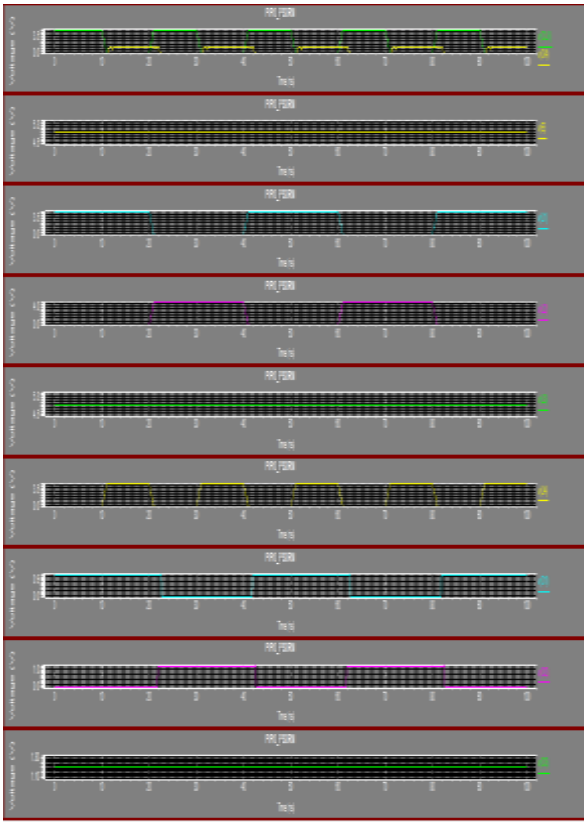

Figure 1.18:- PIPO waveform

Power consumption results for existing (PIPO) design	Power consumption results for proposed (PIPO) design
Power Results vi from time 0 to 1e-007 Average power consumed -> 1.713733e-003 watts Max power 1.082327e-002 at time 1.17161e-008 Min power 1.058192e-006 at time 3.94686e-008	Power Results vi from time 0 to 1e-007 Average power consumed -> 5.324304e-004 watts Max power 7.233520e-003 at time 7.14991e-008 Min power 1.924259e-007 at time 5.26263e-008

VI. CONCLUSION

Our proposed system Reversible computing has emerged as a fast growing technology in few decades. The circuits designed by using reversible logic are the base to develop modern quantum computers. Reversible logic gates are the elementary unit of modern computing technology. For low power computations this techniques are much efficient.

In our proposed method reversible PSDRM D flip-flop is used which is designed from Fredkin Gate and Feynman Gate. This proposed D flip-flop is implemented in 4 bit Shift Register. The proposed work is effective in comparison of average power consumption, number of garbage output and number of transistor used.

VII. POWER CONSUMPTION TABLE

	SISO		SIPO		PISO		PIPO	
	existing	proposed	existing	proposed	existing	proposed	existing	proposed
average power consumed	1.237301e-003 watts	3.985935e-004 watts	1.272417e-003 watts	4.316998e-004 watts	1.424601e-003 watts	8.056769e-004 watts	1.713733e-003 watts	5.324304e-004 watts
garbage output	8	8	12	3	8	8	12	8

VIII. COMPARISON TABLE OF TOTAL NODES AND DEVICES USED

	SISO		SIPO		PISO		PIPO	
	existing	proposed	existing	proposed	existing	proposed	existing	proposed
Total nodes	288	212	327	251	441	365	480	404
Total device	571	419	649	497	872	720	950	798
Active devices	568	416	646	494	864	712	942	790
Passive devices	0	0	0	0	0	0	0	0
Independent sources	3	3	3	3	8	8	8	8
Controlled sources	0	0	0	0	0	0	0	0

IX. FUTURE WORKS

If we talk about future scope than we can say that there are tremendous scopes for reversible logic. We can improve the circuit by designing more and more reversible logic gates. The lot of research is yet to be done in sequential circuit and the areas like-

- Modern quantum computer
- Biomolecular computations
- Medical devices
- Smart cards
- Smart tags
- DNA computing
- Computer graphics

X. REFERENCES

[1] R. Landauer, "Irreversibility and heat generation in the computing process," IBM Journal of Research and Development, vol. 5, pp. 183-191, 1961.

[2] C. H. Bennett, "Logical reversibility of computation," IBM Journal of Research and Development, vol. 17, no. 6, pp. 525-532, 1973.

[3] M. Haghparast and K. Navi, "A novel reversible BCD adder for nanotechnology based systems," American Journal of Applied Sciences, vol.5, no.3, pp. 282-288, 2008.

[4] NM Nayeem, Md. A Hossian, L Jamal and Hafiz Md. Hasan Babu "Efficient design of Shift Registers using Reversible Logic," Proceedings of International Conference on Signal Processing Systems, 2009.

[5] Abu Sadat Md. Sayem and Masashi Ueda, "Optimization of Reversible Sequential Circuits," Journal of Computing, vol.2, issue 6,\ pp. 208-214, 2010.

[6] J. E. Rice, "A New Look at Reversible Memory Elements," Proceedings of IEEE International Symposium on Circuits and Systems, 2006.

[7] H. Thapliyal and M. B. Srinivas, "A Beginning in the Reversible Logic Synthesis of Sequential Circuits," Proceedings of Military and Aerospace Programmable Logic Devices International Conference, 2005.

[8] H. M. H. Babu, M. R. Islam, S. M. A. Chowdhury and A. R. Chowdhury, "Synthesis of Full-adder Circuit Using Reversible Logic," Proceedings of 17th International Conference on VLSI Design

[9] M.H. Babu, M.R. Islam, A.R. Chowdhury, S.M.A. Chowdhury, "Reversible logic synthesis for minimization of full-adder circuit", IEEE Conference on Digital System Design 2003; 50-4.

[10] H.M.H. Babu, M.R. Islam, A.R. Chowdhury, .SM.A. Chowdhury, "Synthesis of full-adder circuit using reversible logic", 17th International Conference on VLSI Design 2004; 757-60.

[11] R. Feynman, Quantum Mechanical Computers, Optical News 1985; 11-20.

[12] T.Toffoli "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.

[13] E. Fredkin and E. Toffoli "Conservative Logic", International Journal of Theoretical Physics, 1983; 21: 219-53.

[14] A. Peres. "Reversible Logic and Quantum Computers", Physical Review, 1985; 3266-76.

[15] M. Haghparast,K. Navi," A Novel Reversible BCD Adder. For Nanotechnology Based Systems"; American Journal of Applied Sciences 5 (3): 282-288, 2008,ISSN 1546-9239.

[16] A. K. Biswas, M. M. Hasan, A.R. Chowdhury and H. M. H. Babu, Efficient Algorithms for Implementing Reversible Binary Coded Decimal Adders, *Microelectron. J*, 39(12):1693– 1703, 2008.