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Statistical Static Timing Analysis for Digital Circuitry

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***Abstract*—**This paper proposed the impact of variations on delay in CMOS technology of 32 nm. The magnitude of process variations have grown, there has been an increasing realization that traditional design methodologies both for analysis and optimization are no longer acceptable. The main objective of the project is that Statistical Static Timing Analysis method has the result closer to best method and less time consuming which is far more acceptable. So we consider Statistical Static timing Analysis is the best and acceptable method for timing analysis of digital Circuits. The variation in propagation delay is big concern. The proposed system considers the variations in the designing process and finds the propagation delay. This is compared with another method called as Monte Carlo method. Also the simulation time required for both the methods are considered.

Keywords*-Static Timing Analysis, Process Variations, Technology*

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I. INTRODUCTION

As CMOS technology scaling down to nanometer, process variations have been increased. The process variations change the transistor dimensions like length, width, thickness of oxide and threshold voltage. This results in variations in timing parameters which makes difficulty in performance count of digital circuits.

So it is necessary to characterize and control the parameter fluctuations to improve the performance. To calculate more accurate timing parameters and performance of the circuits, statistical static timing analysis (SSTA) is an important technique [1]. SSTA analyses circuit propagation delays statistically by considering process variations.

The variations described above can be classified as random variations or systematic variations. Random variations occur without regard to the locations and patterns of transistors within a chip; the variation in transistor threshold voltage, for example, is a random variation. Systematic variations, on the other hand, are related to the locations and patterns; some examples of these variations are exposure pattern variations and silicon‐surface flatness variations.

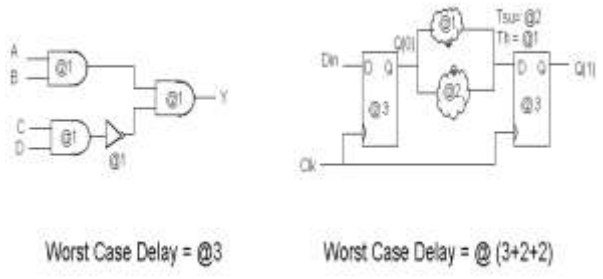

Figure 1. Delay count using conventional STA.

In the conventional methods static timing analysis (STA) is used, which uses corner based analysis shown in Figure 1. The corner values show best case and worst case delay of the circuit. By considering worst case designer predict the performance of the system.

This method is not considered to be accurate as the possible process variations are not considered. This method does not consider the process variations. With a case based STA analysis, it is therefore difficult to calculate actual timing distribution of a circuit. To overcome this difficulty SSTA is one of the new concepts. SSTA models process parameters such as gate length, width, oxide thickness and doping concentration as random variables and propagates these random variables through the circuit in topological fashion to calculate the performance of the system similar to the propagation in its deterministic counterpart.

As mention earlier conventional method is not accurate method. To overcome this, various methods are available to give accurate timing analysis. One of the most usable method that is Monte Carlo analysis, but this is very time consuming method. To overcome this researcher finds various algorithms, but some of them consider only one or few process parameter variation to decide operating speed. In this study, we propose a new algorithm that will consider all process variations and gives accurate operating speed of the circuit.

The main concept of SSTA is to statistically consider the random variations of WID in order to analyze circuit delay more accurately. The simplest method of statistical calculation is Monte Carlo simulation. However, the computation time of this method increases drastically according to the number of variation factors and the circuit scale. For this reason, Monte Carlo simulation is not practical for analyzing actual designs. Therefore, many researchers have studied the basic SSTA method, and many of their results have been reported, starting from about 2000. The basic SSTA method defines the random variations of the delay as random variables and calculates the probability density function (PDF) of circuit delay. The method saves computation time while producing results equivalent to those of Monte Carlo simulation.

VLSI Circuit design specifications

To design high speed VLSI circuit, the major three specifications are important first the operating speed of the circuit, second the power dissipation of the circuit and third

area required to fabricate a chip. Out of these three the first one i.e. operating speed of the circuit is most important and challenging one. To decide the operating speed of the circuit the designer must know all timing constraint of the circuit like propagation delay of each logic gate, clock to Q time, setup and hold time of the flip flop and interconnect delay. By using these timing constraints designer finds longest path delay. According to that the speed of the system will decide. If the circuit is small then this may not be a tough task. But for millions transistor integration this will be very tough and challenging task [8].

II. STATISTICAL STATIC TIMING ANALYSIS OF GATES

A. For NOT GATE

We will consider the two NOT gates connected in series i.e. first NOT gate is driving second NOT gate.

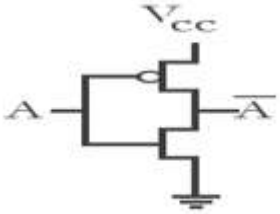

Figure 2. NOT Gate

To calculate the Statistical static timing analysis, we need to calculate the proportional delay (tp) of the NOT gate. In second invertor, capacitance is generated at the PMOS & NMOS transistors, we will call them as CP & CN respectively. Now, the first Invertor will be either charge or discharge the load capacitor CL.

Where CL = CP + CN. CL will be charged through PMOS of first invertor and CL will discharge through NMOS of first invertor.

Propagation delay for NOT gate is given by:

$T_P = (T_{PLH} + T_{PHL}) /2$ (1)

For charging the load capacitor CL,

$T_{PLH} = R_P \times C_L$ (2)

$R_P = V_{DD} / I_{DSP}$ (3)

For discharging the load capacitor CL,

$T_{PHL} = R_N \times C_L$ (4)

$R_N = V_{DD} / I_{DSP}$ (5)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ (6)

$I_{DS0} = (W_{eff} / L_{eff}) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ (7)

$\mu_{eff} = \mu_0 / [1+(V_{A+} V_C V_{BS}) \{V_{gsteff} +[2(V_{TH0} - V_{fb} - \phi_S)/T_{OXE}] E_V\}$ (8)

μ_0 is low field mobility which is 0.06 m^2/V for N channel & 0.025 m^2/V for P channel.

V_A is first order mobility degradation coefficient (10^{-15} m/v^2).

V_C is second order mobility degradation coefficient (0.045×10^{-15} m/v^2).

V_{FB} is flat band voltage and the value is (-1.0Volt).

V_{BS} is the voltage difference between bulk and source and by default it is 0V.

T_{OXE} is oxide thickness and the value is 2nm.

E_V is exponent for mobility degradation and the value is 1.67m^2/V for N channel and 1.0 m^2/V for P channel.

V_{gsteff} is a smoothing function to ensure continuity between subthreshold region and linear region.

$V_{gsteff} = \max \{ V_{off} [(n V_t \ln(1+ \exp (V_{gs} - V_{th}))/ (n V_t)]/[1+n \exp(-(V_{gs} - V_{th}))/ (n V_t)]\}$ (9)

N= 1+N Factor

N Factor is nearly close to 1. So N is close to 2.

ϕ_S is a surface potential.

$\phi_S = 0.4 + V_t \ln(NDEP/ni)$ (10)

NDEP is a Channel doping concentration for zero body bias.

Ni is an intrinsic carrier concentration for silicon.

From the above equations we can say that the propagation delay varies with the length (L), width (W), oxide thickness (T_{OXE}) and dopants (ni) in the MOSFET. Now in statistical static timing analysis, we will consider the varying values of these variables and calculate the propagation delay. Whereas the value of oxide thickness and dopants are having very less variation so we can neglect those variations and can consider them as constant. In this we will vary length from minimum value to maximum value keeping other variables constant. We will generate matrix of these values and solve it.

B. For NOR gate

The load capacitor (CL) will charge through PMOS N1 and N2 and load capacitor (CL) discharge through either N3 or N4. SO we need to design the PMOS and NMOS as per the requirement. R_{p1} and R_{p2} will come in series through load capacitor CL charges. So we need to take the value of R_{p1} and R_{p2} as

$R_p = R_{p1} + R_{p2}$ (11)

So to reduce the resistance $R_{p1 \text{ and}}$ Rp2 by half, we need to increase the width (W) by twice. So the charging time of load capacitor will be same. And for discharging the load capacitor through NMOS transistors the R_{N1} and R_{N2} are in parallel but it is not fix through which path it will discharge. So considering the worst condition we keep the width (W) as it is for NMOS transistors.

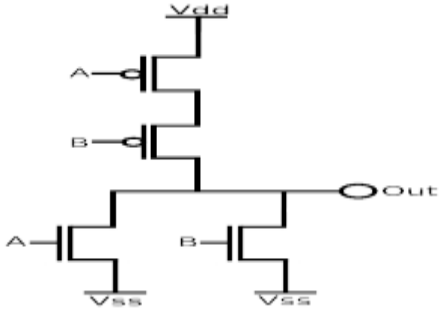

Figure 3. NOR Gate

Propagation delay for NOR gate is given by:

$T_P = (T_{PLH} + T_{PHL}) /2$ (12)

For charging the load capacitor CL,

$T_{PLH} = (R_{P1} + R_{P2}) \times C_L$ (13)

$R_{P1} = R_{P2} = V_{DD} / I_{DSP}$ (14)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ (15)

$I_{DS0} = (2 \times W_{eff} / L_{eff}) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ (16)

And for discharging the load capacitor CL,

$T_{NHL} = R_{N3} \times C_L$ or $R_{N4} \times C_L$ (17)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ (18)

$I_{DS0} = (W_{eff} / L_{eff}) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ (19)

C. For NAND gate

The Load capacitor (CL) will charge through the PMOS Resistor R_{p1} and R_{p2} but the two resistors are in parallel in NOT gate. So the resistance R_{p1} and R_{p2} needs to be double so that it will charge the CL till its limit. So we need to decrease the width (W) by half. And while discharging the load capacitor discharges through R_{N3} and R_{N4} of the NMOS transistors, here these R_{N3} and R_{N4} are in series. So again we need to lower these resistances by half so we need to increase the width (W) by twice.

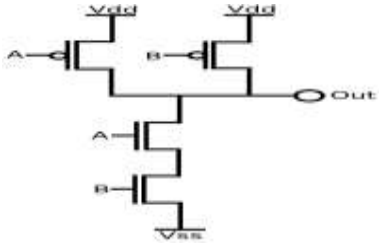

Figure 4. NAND Gate

Propagation delay for NAND gate is given by

$T_P = (T_{PLH} + T_{PHL}) /2$

For charging the load capacitor CL,

$T_{PLH} = R_{P1} \times C_L$ or $R_{P2} \times C_L$ (20)

And for discharging the load capacitor CL,

$T_{NHL} = (R_{N3} + R_{N4}) \times C_L$ (21)

$R_{N3} = R_{N4} = V_{DD} / I_{DSP}$ (22)

$I_{DSP} = I_{DS0} [1+(V_{ds} – V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ (23)

$I_{DS0} = (2 \times W_{eff} / L_{eff}) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ (24)

F For Ex-OR gate

Here the complication increases and ex-or gate is implemented using the two NOT gate s and three NAND gates. The CMOS structure of the same is as shown below,

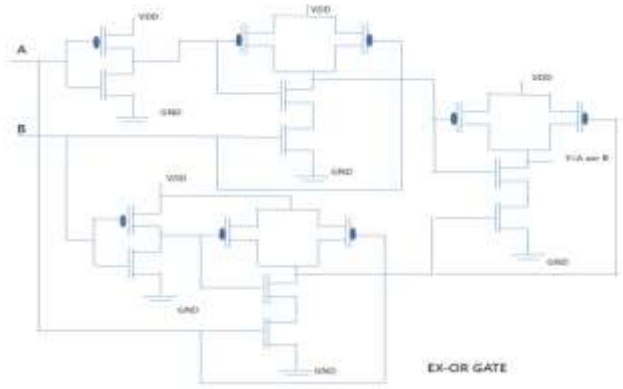

Figure 5. EX-OR Gate

E. For Half Adder

Half Adder is implemented using Ex-or Gate for carry output and NAND and NOT gate combination for Summing output.

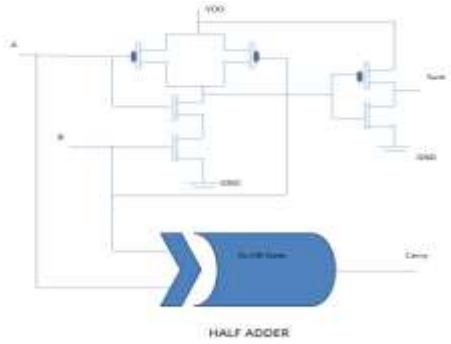

Figure 6. Half Adder

F. For Full Adder

Using two half adders and a combination of NOR gate and NOT gate is used for implementing the full adder. Here we know that the delay for summing output is less compared to carry output so considering only carry output we calculate the delay.

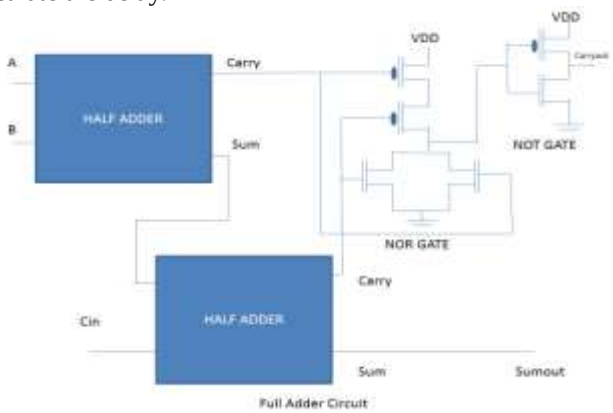

Figure 7. Full Adder

G. Experimental Result

Our method has been tested for the various cases and the results are compared with the Monte- Carlo analysis for 32 nm technology are found to be as follows, percentage error in mean for NOT gate is 1.6 %, for NOR gate is 0.21 %, for NAND gate is 0.42%, for EX-OR gate 0.283 %, for Sum of half adder % is 0.57% for carry of Half adder is 0.18% for full adder is 8.9%. and the percentage error in propagation delay time for NOT gate is 2.82 %, for NOR gate is 0.042 %, for NAND gate is 1.34 %, for EX-OR gate 3.2 %, for Sum of half adder % is 1.1% for carry of Half adder is 0.45% for full adder is 5.1%.In all cases the result are considered for variation up to 0 to 8%. From these result we can say that our result is closely matched with the Monte-Carlo analysis to the satisfactorily conditions.

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Table-1
For Mean of Digital Circuits

	Statistical Analysis	Monte-Carlo Analysis	% Error
Gate Type	**Mean**		
NOT Gate	3.68E-12	3.62E-12	1.60E+00
NOR Gate	4.61E-12	4.62E-12	2.16E-01
NAND Gate	2.83E-12	2.82E-12	4.29E-01
Ex-OR Gate	1.88E-11	1.87E-11	2.83E-01
Half Adder Sum	1.86E-11	1.87E-11	5.76E-01
Half Adder Carry	1.88E-11	1.87E-11	1.81E-01
Full Adder	2.68E-11	2.46E-11	8.93E+00

Table-2
For Standard Deviation of Digital Circuits

	Statistical Analysis	Monte-Carlo Analysis	% Error
Gate Type	**Standard Deviation**		
NOT Gate	2.08E-13	2.15E-13	3.30E+00
NOR Gate	2.14E-13	2.12E-13	9.63E-01
NAND Gate	1.26E-13	1.17E-13	7.34E+00
Ex-OR Gate	8.54E-13	8.56E-13	2.82E-01
Half Adder Sum	8.39E-13	8.56E-13	1.97E+00
Half Adder Carry	8.26E-13	8.56E-13	3.47E+00
Full Adder	2.08E-12	2.27E-12	8.46E+00

Table-3
For Propagation Delay of Digital Circuits

	Statistical Analysis	Monte-Carlo Analysis	% Error
Gate Type	**Propagation Delay**		
NOT Gate	4.12E-12	4.01E-12	2.82E+00
NOR Gate	5.00E-12	5.00E-12	4.20E-02
NAND Gate	3.07E-12	3.03E-12	1.34E+00
Ex-OR Gate	2.10E-11	2.03E-11	3.20E+00
Half Adder Sum	2.01E-11	2.03E-11	1.10E+00
Half Adder Carry	2.04E-11	2.03E-11	4.57E-01
Full Adder	3.02E-11	2.87E-11	5.01E+00

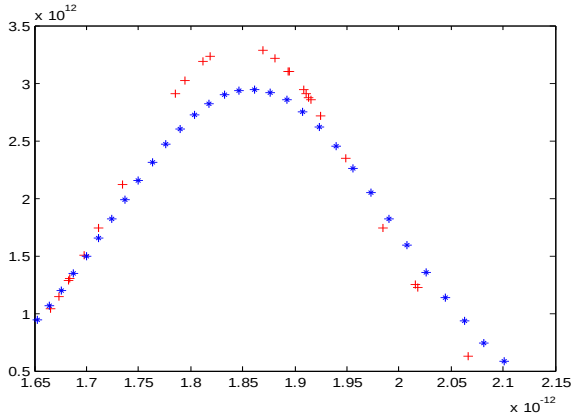

Figure 8. Probability Curve of NOT Gate (Probability Vs Delay).

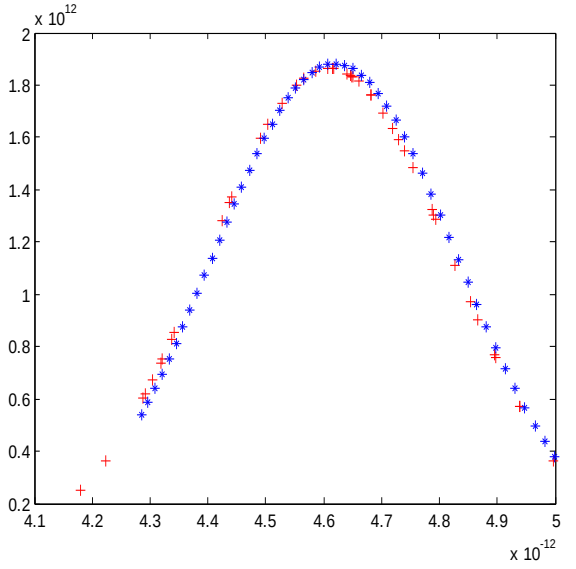

Figure 9. Probability Curve of NOR Gate (Probability Vs Delay).

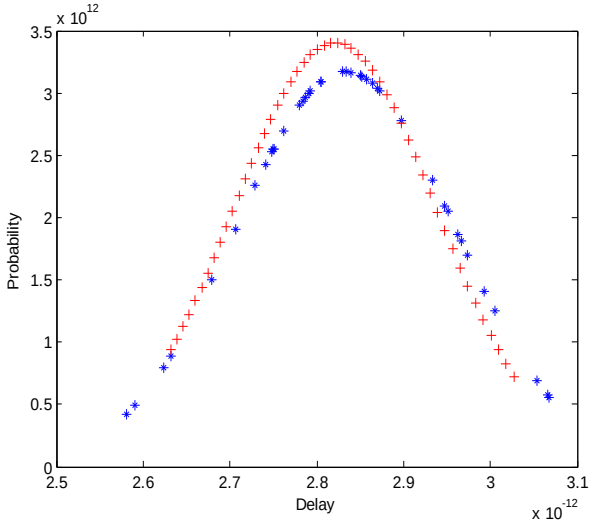

Figure 10. Probability Curve of NAND Gate (Probability Vs Delay)

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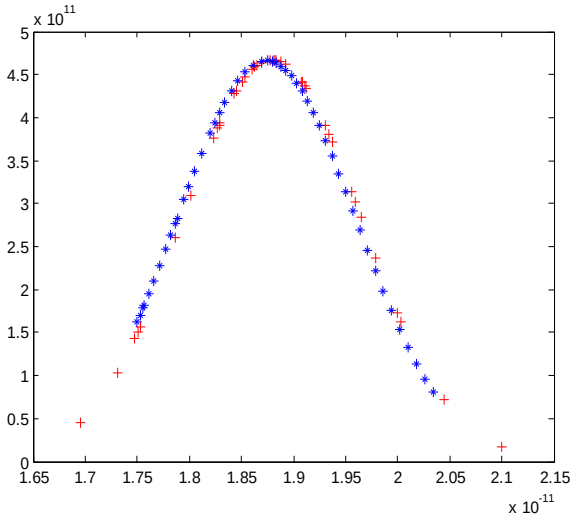

Figure 11. Probability Curve of EX-OR Gate (Probability Vs Delay)

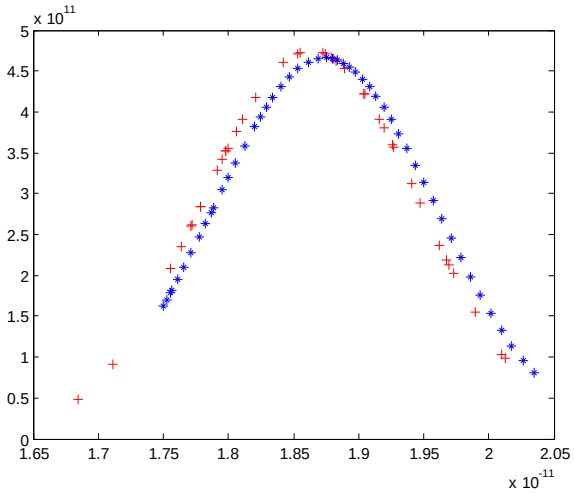

Figure 12. Probability Curve of Half Adder Sum (Probability Vs Delay)

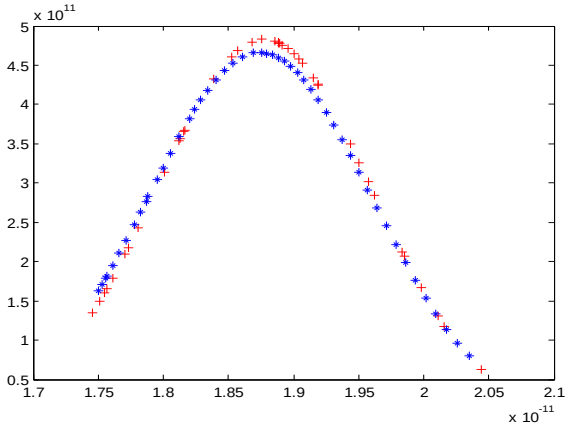

Figure 13. Probability Curve of Half Adder Carry (Probability Vs Delay)

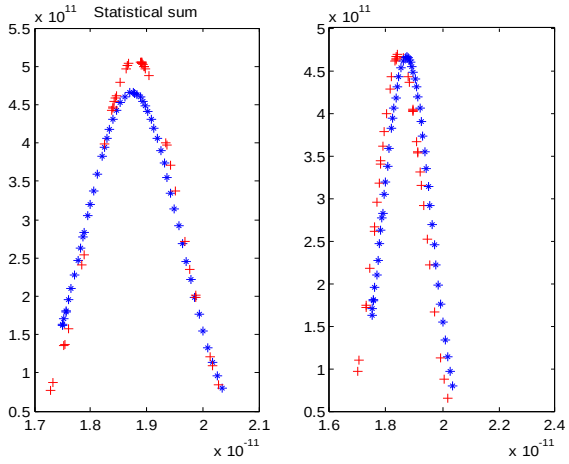

Figure 14. Probability Curve of Half Adder Sum & Carry (Probability Vs Delay)

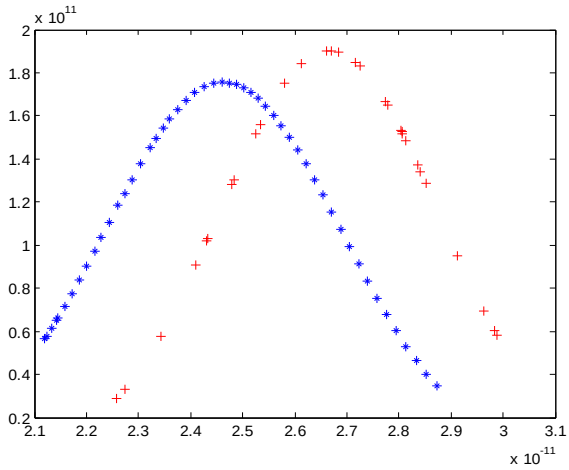

Figure 15. Probability Curve of Full Adder Carry (Probability Vs Delay)

III. CONCLUSIONS

We proposed Statistical Static Timing analysis for calculating the Mean, Standard Deviation and Propagation Delay of the Logical Circuits of 32nm technology and it reduces the execution time. We carried out the test results at various cases and the comparison of the proposed SSTA to the Monte-Carlo technique is done and the satisfactory results are obtained.

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