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HDL Design for Peta Hertz Clock based $2e^{31}$-1 Peta Bits Per Second (Pbps) PRBS Design for Ultra High Speed Applications/Products

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Abstract-The Design is mainly Intended for High Speed Random Frequency Carrier Wave Generator of Peta Bits Per Second P.b.p.s (Peta Bits Per Second) Data Rate $2e^{31}$-1 Tapped PRBS Pattern Sequence. The P.R.B.S is Designed by using L.F.S.R Linear Feed Back Shift Register & XOR Gate with Specific Tapping Points as per C.C.I.T.T I.T.U Standards. R.T.L Design Architecture Implemented by using V.H.D.L &/ Verilog H.D.L, Programming & Debugging Done by using Spartan III F.P.G.A Kit. Transmission done through this carrier frequency. Propagation Carrier Done either Serially / Parallel lines I/O.

Keywords: *C.C.I.T.T – Consulting Committee for International Telegraph & Telecom , I.T.U – International Telecom Unit, R.T.L- Register Transfer Level, L.F.S.R-Linear Feedback Shift Register, V.H.D.L- Very High Speed Integrated Circuit Hardware Description Language, P.R.B.S-Pseudo Random Binary Sequence. Verilog-Verification Logic.*

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1.0 INTRODUCTION

In Modern Hi-tech Communication Engineering world, High Speed based Portable Communication System Hardware & Software Products Came to the market, speed is an important factor and is in terms of Giga bits per second for all Hi-tech Real time Smart Computing Portable wireless Communication System Software products like Cloud Computing ,wireless Internet Data Packets Transceivers Computing, Tablets,Pocket Mobile Multimedia Systems, Note Book Computers, Wireless Routers,N.O.Cs,Network-Cards/Racks,Wi-Fi,GiFi,Wi-max,G.P.S,G.S.M,Q.C.D.M.ATranceivers.For that purpose ,I Designed Peta Bits Per Second, P.b.p.s High Speed P.R.B.S is Pseudo Random Binary Sequence Frequency Generators, Generate & Received Random Frequency Data in the form of Random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. P.R.B.S Generators, Receivers, Transceivers Designed for HiFi Wireless Internet Data Packets Computing and Cloud Computing etc. Transmission, Reception of Data is in the RANDOM Sense, This P.R.B.S Generator, Receiver is Designed for Identification property of Different Tapped P.R.B.S Sequences like 7,10,15,23,31 at a Clock carrier frequency speed of Pbps(Peta Bits Per Second) .The Length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, Wi-Fi, Gi-Fi, LTE, Wireless O.F.D.M.A , C.D.M.A,Q.C.D.M.A Computing, wireless internet computing, cloud computing etc because of Ultra High speed Communication Rate in terms Tbps. All these P.R.B.S L.F.S.R Sequences are designed by tapping different points according to I.T.U O.150,O.151,O.152 Standards. This P.R.B.S Design Consists of Multiplexer, PRBS Registers of different tapped sequence points, Clock Frequency Generators of Pbps Speed. The Advantages of these P.R.B.S Generators having In Built Checkers, Bit Error Rate Detection & Correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & C.R.C

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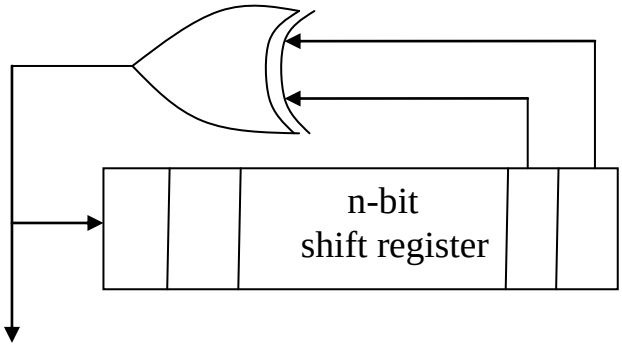

FIG[1]: Fibonacci (many-to-one) realization of LFSR with minimum number of taps and XOR gate in its feedback

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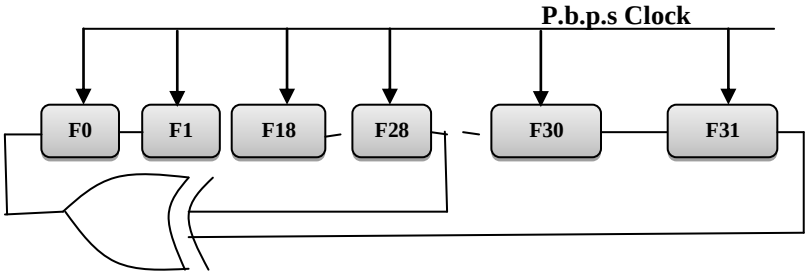
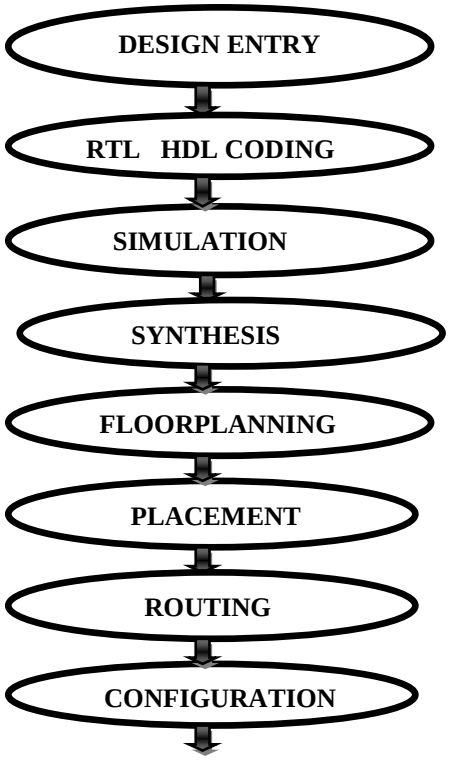
2.0 $2e^{31}$-1 P.b.p.s- PRBS Logic Design Architecture

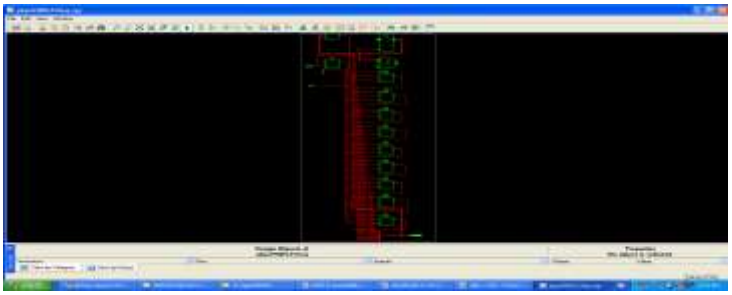


3.0 SOFTWARE – VLSI IC DESIGN FLOW

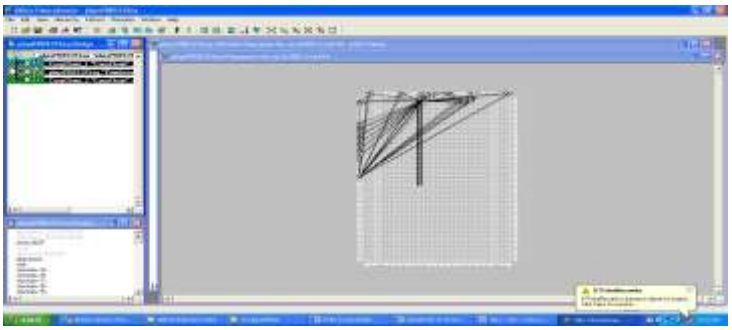


FIG[3]: VLSI Design Flow Chart

B. $2e^{31}$-1 P.b.p.s PRBS RTL Schematic

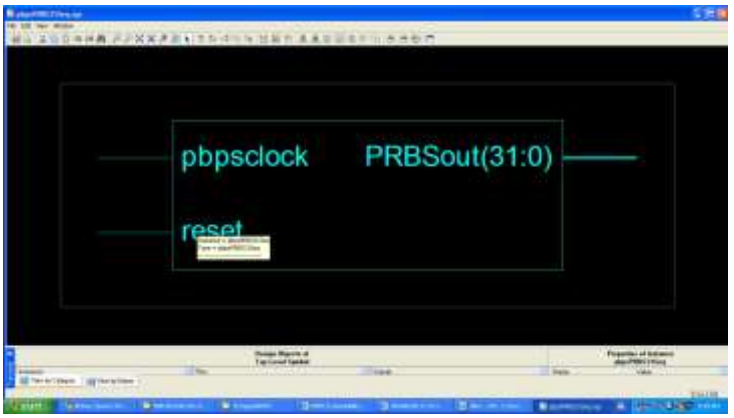


C. $2e^{31}$-1 P.b.p.s PRBS DESIGN PLACED Report



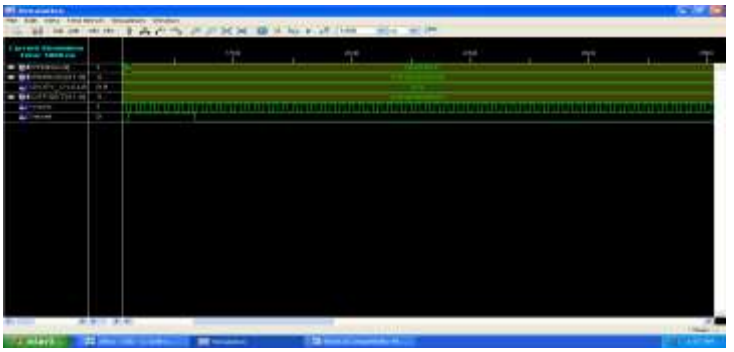
4.0 DESIGN FLOW REPORTS OF $2e^{31}$-1 Pbps PRBS DESIGN

A. $2e^{31}$-1 P.b.p.s PRBS DESIGN RTL BLOCK



D. $2e^{31}$-1 P.b.p.s PRBS DESIGN ROUTED Report

E . SIMULATION WAVE FORM RESULTS -$2e^{31}$-1 P.b.p.s PRBS



7.0 CONCLUSION

Designed High Speed Random Carrier Frequency Generator **$2e^{31}$-1 Pbps PRBS** for Ultra High Speed Wireless Communication Engineering Products

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