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Performance Analysis of CMOS Flip-flops

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Abstract- Low power has emerged in today's electronic industry. CMOS technology is best known for low power consumption, which makes the device more reliable, efficient & portable. This paper presents the comparative analysis of CMOS flip-flops for power & speed using analog simulation, and the results are discussed.

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I. INTRODUCTION

The power consumption of digital circuits are described by the clock signal. As we know that, the digital circuits are triggered by clock signal, which causes the signal transition. The power consumption in CMOS flip-flop is dominated by the dynamic power, which can be expressed as

$$P_{dynamic} = \sum \alpha\ f_c\ C\ Vdd^2$$

Where α is node transition factor. fc is the clock frequency, C is the node capacitances & Vdd is the supply voltage. The node transition factor α describes the effective number of voltage transition during one clock cycle .

The clock itself has α=1. a high value, so the clock is always expensive in power. Therefore clocked capacitances should be minimized in order to save power. An ordinary data signal can change once per clock cycle at maximum.

The main requirements of high performance flip-flop are high clock frequency, low power consumption & speed, supply voltage scalability. In this paper these parameters are analyzed for high performance flip flop .

II. DESIGN & OPERATION

CMOS flip-flops derived from a P-latch followed by an N-latch. Usually a CMOS flip-flop contains two latches a master and a slave. While the slave is not latched, master must be latched for both high and low output states and vice versa. CMOS flip-flops can be static or dynamic. Dynamic flip-flops are used to reduce the circuit complexity, increase the operating speed & lower power consumption.

a) **9-T Flip-Flop.**

9T is a positive edge triggered flip flop, which uses the P half latch as master & a standard PTSPC latch as slave. As the name denotes, it has 9 transistors in the basic unit.

The output Qb is isolated from the internal nodes whenever clock is equal to zero. The nodes y1 & y2 are the precharged nodes of the master & slave respectively.

When the clock =0,D=0; MP1,MP2,MP3 turned On. The nodes y1 & y2 charged to Vdd. Hence output Qb is in low s When the clock=1, D=0; the nodes y1 &y2 are discharged to GND through MN1,MN2, this makes MP4 be ON. Hence the output Qb is become High.

Similarly when clock=1,D=1; MP2 is OFF then node y1 & y2 are in charged state .Hence output Qb is become low.

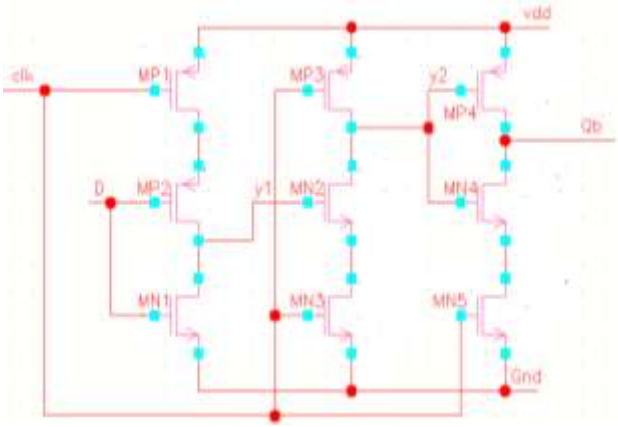

Figure 1: 9-T Circuit diagram

b) DSTC Flip-Flop

DSTC stands for Dynamic Single Transistor Clocked flip flop. DSTC flip flop is designed using p DSTC master and an n DSTC slave.

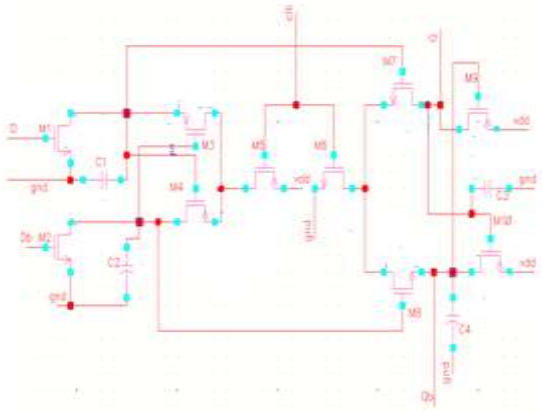

Figure 2: DSTC Circuit diagram

When clock=0, D=0;Db=1.

Master: m5 is ON ,m1 is off, m2 is ON, then C2 charged to vdd.

Slave: M6 is OFF, input to m7 is 0 & m8 is 1 that makes Q=0,Qb=1. Hence slave retains the current state.
D=0 is the non transparent input to slave.
When D=1, Db=0;Q is held at logic 1. But this doesn't change the output of the slave. Thus it is proved that slave is latched at clk=0.

When clk=1,

For master:

M5 is off. When D=0, Db=1; D=1, Db=0; Q is 0 and Qb is 1 making the master latched. Q remains at 1 Qb discharges to 0.

For slave

m10 is ON. When inputs to slave are 0 and 1, then Q=0 and Qb=1 and vice versa. Hence the slave is transparent for clk=1.

c) SSTC Flip-Flop:

SSTC is the static version of DSTC flip flop. In DSTC the inputs change until the clock was high. To overcome this, SSTC flip flop was designed. It is designed using a modified p SSTC master and an n SSTC latch. It has two clocked transistors, making it an efficient for very low power consumptions.

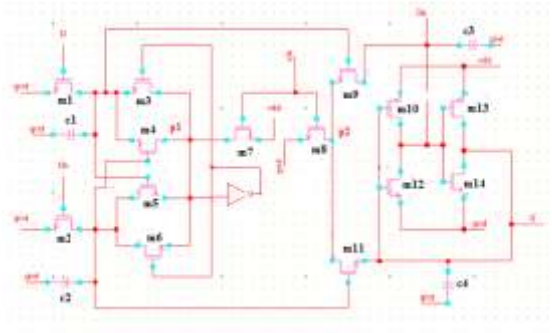

Figure 3: SSTC Circuit diagram

For master:

When Clk=0, M7 is ON and there is a path from Vdd to node p1.The inverter output is 0. Therefore input to M3 and M4 are given a 0 and are cutoff. Node P1 is at logic 1. **D=0, Db=1**

M2 is turned ON. Input 0 is given to transistor M4, turning it ON. Since node P1 is held at logic 1, there is a path from Vdd, charging the capacitance c3 to 1.Therefore Q=0.From the operation of the n-SSTC, when clk=0, D=X(0/1) there is no direct connection to ground. Hence the output will be the current state.

clk=1, transistor M7 is turned OFF and there is no path from Vdd to P1. Therefore P1=0, inverter output is logic 1. M4 and M5 are given to 1. Hence are turned ON.

D=0/1, Db=1/0

The master retains the current state output. In other words master is latched and slave is transparent.

For slave:

When clk=1, D=0 Db=1

In this case transistor M10 is ON then the load capacitor c4 gets discharged. i.e, Q=0. Hence M12 is turned ON charging the load capacitance c3=1. This is because of the cross coupled inverter.

d) STSL Flip-flop

STSL is a Self timed slave latch. It is a static flip-flop based on self timed slave latch& it has 3 clocked transistors.

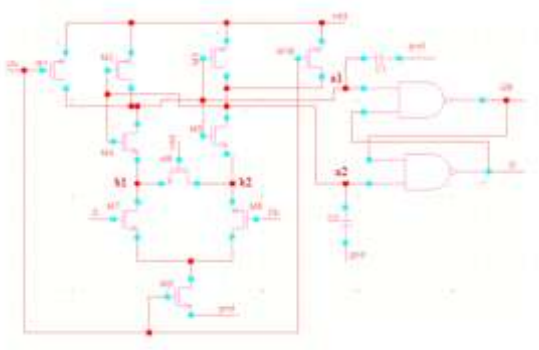

Figure 4: SSTL Circuit diagram

The circuit diagram of STSL flip flop consists of Master and Slave. Slave is the sub circuit of the STSL flip flop. i.e. made of two NAND gates. In the master part, transistors M1,M9 and M10 are the clocked transistors and 'a1'and 'a2' are the intermediate nodes and 'b1' and 'b2' are the nodes at transistor M6 and c1and c2 are the capacitors at the nodes 'a1'and 'a2'respectively. The transistor M6 is always ON to keep the same potential at both the nodes 'b1' and 'b2'. When clk=0, the intermediate nodes 'a' are precharged high (capacitors c1 and c2) making the output set-reset stage keep its previous value. When clk=1 and d=1, transistors M1 and M10 are cutoff, transistor M7 is ON and M8 is OFF. Transistors M2, M4 and transistors M3, M5 acts as cross coupled inverters. Since M7 is ON and M8 is OFF, the node 'b1' is high, the node 'b2' is low and the corresponding node 'a2' is low. The precharged value of 'a1' is given to M3 and M10. Now M5 is connected to Gnd since M9 is OFF. Hence output Q=1 and Qb=0.

Similarly works when clk=1 and d=0 and therefore output Q=0 and Qb=1.Based on the input to M8 and M7, the inverter which drives faster to Gnd dominants. The cross coupled inverters prevents new input data from propagating to nodes 'a1' and 'a2' and transistors either M8 or M7 which was not active initially is now OFF and therefore not active until next precharge. The valid data on nodes 'a1' and 'a2' is finally propagating to output, as the low value will reset the output stage.

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III. PERFORMANCE ANALYSIS

Low power, high speed are the main parameters for high performance Flip flop .

Low power consumption includes reduction of supply voltage, reduction of load capacitance. The reduction of supply voltage leads to an increase of delay.

IV. SIMULATION:

Simulation at lower level of design abstraction offers better accuracy at the expense of increased computer resources. SPICE attains excellent accuracy. The most useful mode for digital IC power analysis is transient Analysis.

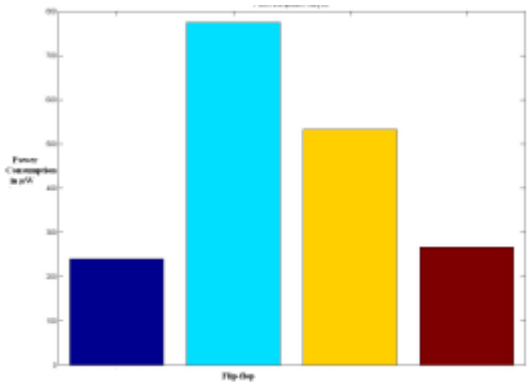

Figure 5: Power consumption analysis

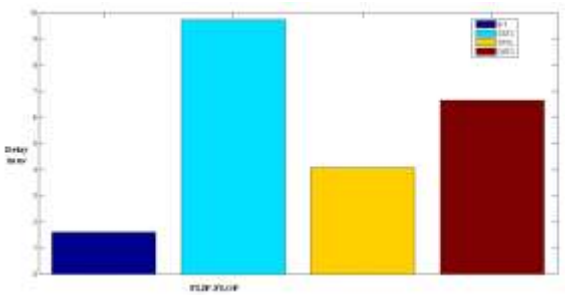

Figure 6: Delay analysis

Each circuit was simulated in SPICE and power consumption & delay are recorded.

In figure 5 & 6 shows the simulation results from 9T, DSTC, SSTC, STSL flip-flops, where all have complementary outputs. Here 9T has the lowest power consumption & less delay. SSTC has the maximum power consumption & high delay. DSTC has reasonable power consumption & more delay. STSL has the higher power consumption & reasonable delay.

V. RESULTS & DISCUSSION

SSTC has max average power consumption in the flip flop family. The range of power consumption is 774 µW.

9T has the least delay among the CMOS flip flops and hence is the fastest among the flip flops.

For Vdd=3V α=0.5

Flip-flop	Power consumption	Delay
9T	240 µW	1.60 ns
DSTC	267.2 µW	6.65 ns
SSTC	774.12 µW	9.73 ns
STSL	532 µW	4.07 ns

VI. CONCLUSION

The power consumption of CMOS flip-flops dependent on the clock, supply voltage & the activity factor. A reduction of any one of these is beneficial to achieve low power consumption. CMOS circuits are suitable for good speed & low power. In this analysis their in no correlation between power & speed. Finally we can conclude that ,it is necessary to combine low power & high speed.

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