International Journal on Recent and Innovation Trends in Computing and Communication
Volume: 3 Issue: 6

ISSN: 2321-8169
3849 - 3852

Performance Analysis of CMOS and FinFET based 16-Bit Barrel Shifter

Bharti Midha[1]
1Research scholar, ECE Department, JCDM College of Engineering, Sirsa

Manish Mehta[2]
HOD, ECE Department, JCDM College of Engineering, Sirsa

Abstract:- A barrel shifter shifts 'n' number of bits in one cycle. Barrel shifter can perform the following functions: shift left logical, shift left arithmetic, rotate left, shift right logical, shift right arithmetic and rotate right. The design of the barrel shifter is purely MUX based will improve its efficiency if Mux consumes less power. The MUX based SLC barrel shifter circuits are designed using Tanner EDA tools. Fin-type field-effect transistors (FinFETs) are promising substitutes for bulk CMOS in nano - scale circuits. This paper compares the performance of barrel shifter using two different technologies on the basis of power consumption, time delay and power delay product

Keywords: *FinFET , Barrel Shifter, MUX, SG mode, LP mode ,IG mode, SLC*

*****

I. INTRODUCTION

A barrel shifter is a digital circuit that can shift a data word by a specified number of bits in one clock cycle. It can be implemented as a sequence of multiplexers (mux.), and in such an implementation the output of one mux is connected to the input of the next mux in a way that depends on the shift distance. Barrel shifters, are commonly found in both digital signal processors and general-purpose processors. The power consumed by MUX trees is quite significant and cannot be ignored. Thus, to minimize power dissipation of MUX trees MUX should be designed using nano scale technology. Multiplexers are digital circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of select lines . In this paper barrel shifter is designed using 2:1 mux. FinFETs [3] are double-gate transistors which are the rival of CMOS. In FinFET two gates can either be shorted for higher performance or independently controlled for lower leakage or reduced transistor count. This new technology gives us power delay trade off.

II. BARREL SHIFTERS

A barrel shifter [4] has n data inputs, n data outputs and a set of selected inputs that specify the no. of bits shifted. The connections between multiplexers specify the type of shift (logical, arithmetic or circular - circular shift is usually designated rotation), the direction of the shift (left or right), and the amount of shift (from 0 to n - 1). Different type of shifting operations performed using barrel shifter:

SRL - Shift right logical: performs m-bit right shift and sets the upper m bits to zeros.

SRA - Shift right arithmetic: performs m-bit right shift and sets the upper m bits to the most significant bit to implement sign extension.

SRC - Shift right circular: performs m-bit right shift and sets the upper m bits to the lower bits of the input.

SLL - Shift left logical: performs m-bit left shift and sets the lower m bits to zeros.

SLA - Shift left arithmetic: performs m-bit left shift and sets the lower m bits to zeros. The sign bit is set to In-1.

SLC - Shift left circular: performs m-bit left shift and sets the lower m bits of the output to the higher bits of the input.

Barrel shifter is designed using Multiplexers. Barrel shifter design is for natural size like (2,4,16) .This project is done on 16 bit barrel shifter which can Shift left circular input. Four select lines are used as it is 16 bit barrel shifter i.e. S0, S1, S3, S4. Basically barrel shifter is used with logical left shift operation which is controlled by select inputs. Select lines are used to specify the amount of shift only, For example, consider a 4 bit barrel shifter, with input A, B, C, and D. The shifter can cycle through the order of bit ABCD i.e. it can shift all output through three positions.

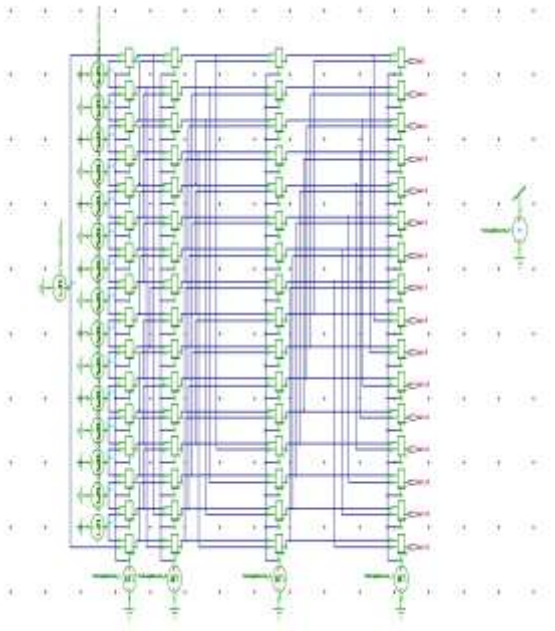

Figure 1. 16 bit SLC Barrel Shifter

 ISSN: 2321-8169
3849 - 3852

III. FinFET

Small channel MOSFETs shows short-channel behavior and have high leakage current. Multigate field-effect transistors (FETs) overcome these problems because of tighter control of the channel potential by multiple gates wrapped around the body. The FinFET device structure consists of a silicon fin surrounded by shorted or independent gates on either side of the fin, typically on a silicon-on-insulator substrate. The efficiency of each new technology is measured in terms of power consumption, area and delay. FinFETs (fin-type field-effect transistors), an emerging transistor technology that is likely to supplement or supplant bulk CMOS (complementary metal-oxide-semiconductor) at 22-nm and beyond, offer interesting delay–power tradeoffs. Both CMOS logic and pass transistor logic were developed for conventional NMOS and PMOS transistor so teir performance is not so good at short channels. In FinFET the NMOS in CMOS technology is replaced with NFinFET and PMOS with PFinFET, then, both gates of FinFET are shorted together. By using this approach, we can design a FinFET version of a CMOS logic circuit or a pass transistor logic circuit that retains the same functionalities as the MOSFET version. Presence of multiple gates in FinFET provides better circuit performances and reduces leakage current through effective suppression of short-channel effect and near-ideal subthreshold swing .

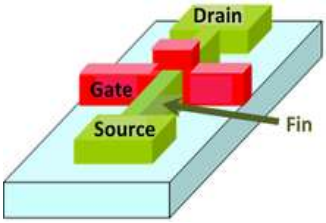

Figure 2. Basic structure of FinFET

Double-gate (DG) FinFETs are broadly classified into two types, namely, shorted gate (SG) and independent gate(IG) FinFETs. SG behaves like a three-terminal MOSFET because it has both the gates (front and back) connected each other, whereas the IG has two independent gates.

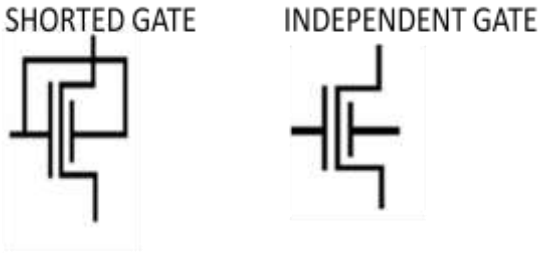

Figure 3. Types of FinFET

The FinFET [6] is the most attractive choice among the double gate device architectures due to the self-alignment of the two gates and the fabrication compatibility of the FinFETs with the existing standard CMOS fabrication process. Both short-gate and independent-gate FinFETs have been successfully fabricated. A fabrication process is described in [18] for implementing the short gate and independent-gate FinFETs on the same die. In [3] and [5], the independent-gate FinFETs are utilized to reduce the number of transistors required for implementing specific logic functions as compared to the standard circuits with shorted gate FinFETs. In addition to the area savings, significant speed enhancement is reported due to the reduced parasitic capacitance and the lower transistor stack heights with the independent gate FinFET circuits as compared to the circuits with shorted gate FinFETs. The power consumption is also reduced due to the lower parasitic capacitance of the simplified circuit topologies with the independent-gate FinFETs.

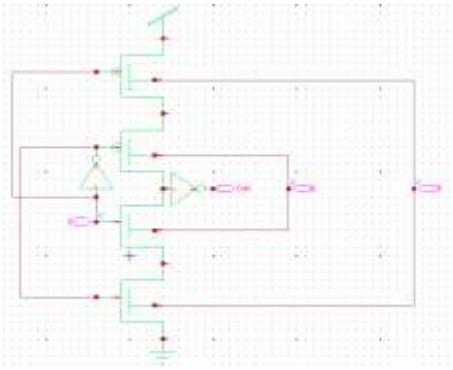

Figure 4. MUX using FinFET

IV. SIMULATION RESULT

The designs are simulated in TSPICE using 22nm and 45nm FinFET [6] technology and CMOS technology. The fig 5 shows the transient analysis of 2X1 MUX and fig 6 shows the transient analysis of 16-bit barrel shifter for input 1011111101101100.

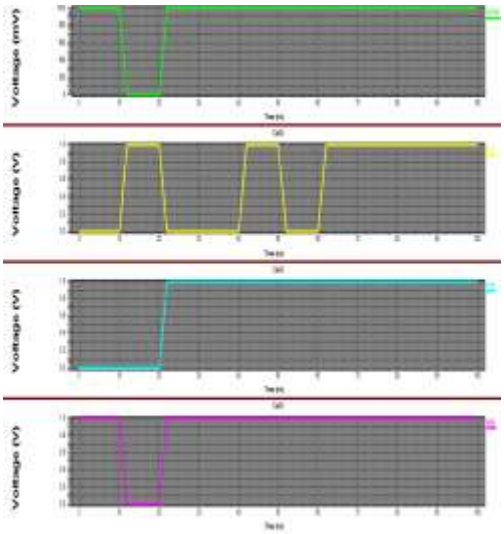

Figure. 5. Transient analysis 2:1 mux

ISSN: 2321-8169
3849 - 3852

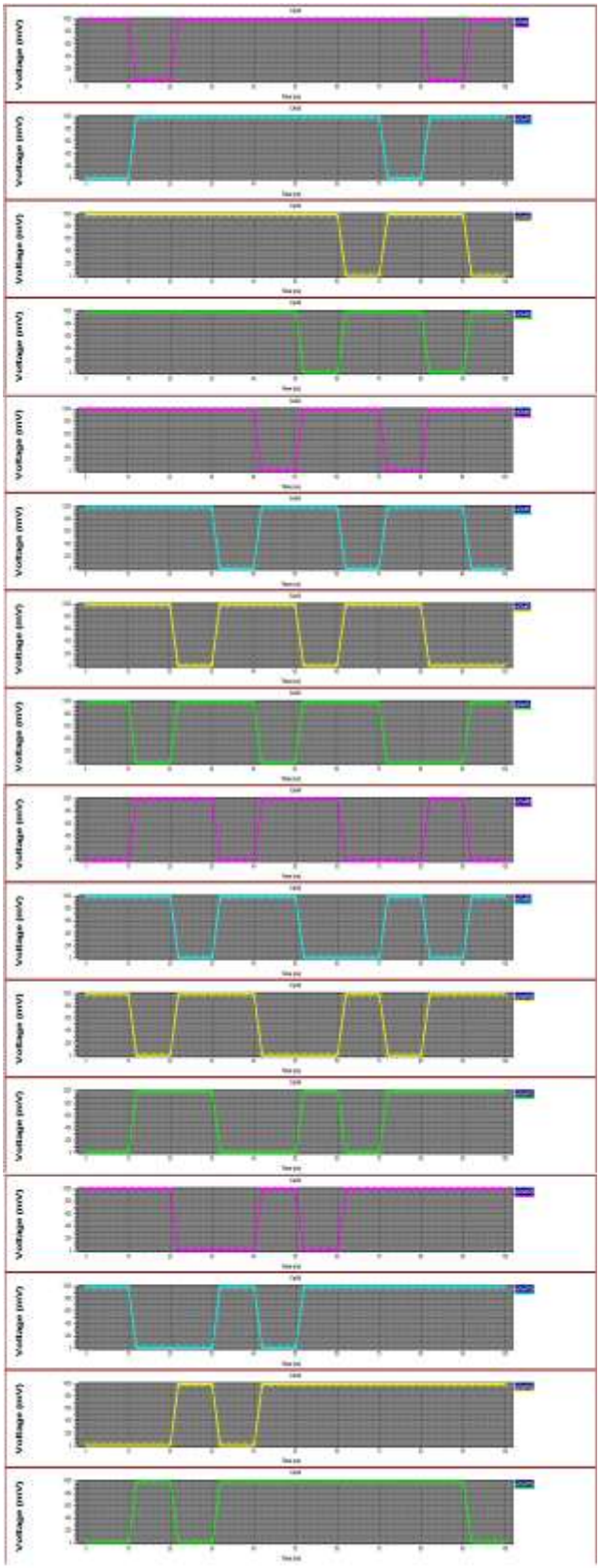

Figure. 6. Transient analysis of 16 bit barrel shifter

Table 1. Performance analysis of 2:1MUX using CMOS technology

Technology	Average Power (W)	Time delay (S)	PDP
22nm	1.0797e-006	0.3542e-011	0.3135e-017
45nm	3.8956e-006	2.4577e-011	9.57422e-017

Table 2. Performance analysis of 16 bit Barrel Shifter using CMOS technology

Technology	Average Power (W)	22nm	PDP
22nm	1.1081e-004	3.1530e-011	3.4938e-015
45nm	1.1213e-004	3.6427e-011	4.0845e-015

Table 3. Performance analysis of MUX using FinFET technology

Technology	Average Power (W)	Time delay (S)	PDP
22nm	0.51406e-006	1.2123e-011	0.6232e-017
45nm	1.2682e-006	3.6941e-011	4.6848e-017

Table 4.Performance analysis of 16 bit Barrel Shifter using FinFET technology

Technology	Average Power (W)	Time delay (S)	PDP
22nm	2.1146e-005	5.6719e-011	1.19938e-015
45nm	3.2353e-005	6.9636e-011	2.25293e-015

V. CONCLUSION

In SLC Barrel shifter the bits are rotated in such a way that LSB becomes MSB and other bits are shifted to left hand side depending on the value of selected inputs. The proposed Mux using FinFET technology is used in Barrel Shifter which consumes less power and have more delay as compare to CMOS technology .FinFET seems to be good

substitute of CMOS in terms of power consumption. In FinFET based barrel shifter 80% of power consumption is reduced on the cost of 60% increase in delay. With the reduction of technology power consumption reduces because when we reduces the technology, its length and width are also reduces by factor s. In FinFET value of parasitic capacitance is small, so its switching time is fast as compare to CMOS. It is clear from table 2 and 4 FinFETs have more PDP as compared to CMOS.

VI. REFERENCE

[1] J. Maria Jenifer and Dr. Pukhraj Vaya "FinFET based 8- bit arithmetic unit for leakage reduction",IJESC, july 2014
[2] Sourindra Chaudhuri and Niraj K. Jha "FinFET logic circuit optimization with different FinFET styles: lower power possible at higher supply voltage" ,IEEE International Conference on VLSI Design,2014
[3] Ajay N. Bhoj and Niraj K. Jha"Design of logic gates and flipflops in high performance FinFET technology" IEEE transaction on vlsi , vol. 21 ,no. 11 , november2013
[4] Shweta Chawla, Ramanand Harijan and Harpal singh "Design low power 32-bit barrel shifter using efficient charge recovery logic" IEEE,2013
[5] Y. Yang, and N. K. Jha "FinPrin: Analysis and optimization of FinFET logic circuits under PVT variations," in Proc. Int. Conf. VLSI Design, pp. 350-355, Jan. 2013.
[6] Rinu Pappachan, V.Vijayakumar, T.Ravi, V.Kannan" Design and analysis of a 4-bit low power barrel shifter in 20nm finfet technology",IJES,2013
[7] Vaibhav Neema, Pratibha Gupta" Design strategy for barrel shifter using Mux at 180nm technology node",IJSME,july 2013.
[8] Ch. Srigowri and M.Srihari "VLSI Design of Low Power Reversible 8-bit Barrel Shifter" ,IJTEL,vol.2,no.6, December 2013.
[9] Prateek Mishra, Anish Muttreja and Niraj.K.Jha; et. al "FinFET Circuit Design",springer
[10] O.Anjaneyulu,T.Pradeep and C.V.Krishna Reddy "Design and implementation of reversible logic based bidirectional barrel shifter" IEEE-ICSE2012 Proc., 2012.
[11] Mahalingam.P.R, Shimmi Asokan "Adapting barrel shifter at compilation level for efficient implementation of multiplications"IEEE international conference on advances in computing and communications , 2012
[12] K.Nehru, A.Shanmugam. Dr., G. Darmila Themozhi "Design of Low Power ALU Using 8T FA and PTL Based MMUX Circuits" IEEE-International Conference On Advances In Engineering, Science And Management (ICAESM-2012) March 30,31,2012
[13] Abhijit Asati1and Chandrashekhar "VLSI Implementation of a High Performance Barrel Shifter Architecture using Three Different Logic Design Styles" International Journal of Recent Trends in Engineering, Vol 2, No. 7, November 2009
[14] Prasad D Khandekar, Dr. Mrs. Shaila Subbaraman, Venkat Raman Vinjamoori "Quasi-Adiabatic 2X2 Barrel Shifter" IEEE, Fourth International Conference on Industrial and Information Systems, ICIIS 2009, 28 - 31 December 2009, Sri Lanka
[15] Ms. G.L. Madhumati , Dr. M. Madhavilatha , and Mr. K. Ramakoteswara Rao" Power and delay analysis of a 2-to-1 multiplexer implemented in multiple logic styles for multiplexer-based decoder in flash ADC" International Journal of Recent Trends in Engineering, Vol. 1, No. 4, May 2009 .
[16] Sherif A. Tawfik and Volkan Kursun," Low-Power and Compact Sequential Circuits With Independent-Gate FinFETs" IEEE transactions on electron devices, vol. 55, no. 1, january 2008.
[17] Prasad D Khandekar, Dr. Mrs. Shaila Subbaraman, Venkat Raman Vinjamoori "Low Power 2:1 MUX for Barrel Shifter"IEEE first international conference on emerging trends in engineering and technology,2008.
[18] Y. Liu et al., "Cointegration of high-performance tied-gate three-terminal FinFETs and variable threshold-voltage independent-gate four-terminal FinFETs with asymmetric gate-oxide thicknesses," IEEE Electron Device Lett., vol. 28, no. 6, pp. 517–519, Jun. 2007.
[19] M.-H. Chiang et al., "Novel high-density low-power logic circuit techniques using DG devices," IEEE Trans. Electron Devices, vol. 52, no. 10,pp. 2339–2342, Oct. 2005.
[20] Weimin Zhang , Jerry G. Fossum ,Leo Mathew and Yang Du "Physical insights regarding design and performance of independent gate FinFETs"IEE transactions on electron device,vol.52,no.10,oct 2005
[21] Masoud Rostami and Kartik Mohanram "Novel dual-Vth independent-gate FinFET circuits"
[22] http://en.wikipedia.org