# Statistical Static Timing Analysis for Performance of Logic Gates

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***Abstract***—In the recent nanotechnology, the variation in the gate propagation delay is the big concern. This paper proposes the new model for gate delay propagation using the Statistical Static Timing Analysis and the results of it are compared with another modelling called as Monte-Carlo analysis. The proposed model uses Statistical analysis to find accurate propagation delay of the logic gates with reduced simulation time for 16nm technology.

***Keywords***-*SSTA;Variations;Technology*

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## I. INTRODUCTION

As CMOS technology scaling down to nanometre, process variations have been increased. The process variations change the transistor dimensions like length, width, thickness of oxide and threshold voltage. This results in variations in timing parameters which makes difficulty in performance count of digital circuits.

So it is necessary to characterize and control the parameter fluctuations to improve the performance. To calculate more accurate timing parameters and performance of the circuits, statistical static timing analysis (SSTA) is an important technique [1]. SSTA analyses circuit propagation delays statistically by considering process variations.[1][3]

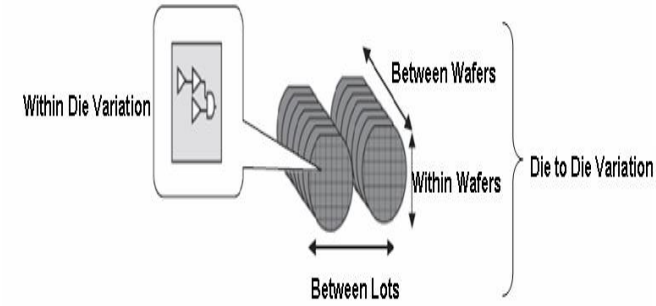


Figure 1. Within die and die to die variation [8]

The variations may occur within chip or one chip to another chip shown in Fig 1. The variations within chip called intra die variation and the variations from chip to chip, wafer to wafer and one lot of wafers to another lot of wafers are called inter die variations. Intra die variations are caused by process gradients over the wafer during manufacturing. Global or random parameter variations are divided into two types such as extrinsic variations and intrinsic variations. Fluctuations of effective channel length, doping concentrations and oxide thickness caused by extrinsic equipment are considered to be extrinsic variations. The intrinsic variations are due to random fluctuations in channel dopant number, oxide charge, interface charge, etc.

In the conventional methods static timing analysis (STA) is used, which uses corner based analysis shown in Figure 2.[1] The corner values show best case and worst case delay of the circuit. By considering worst case designer predict the performance of the system.

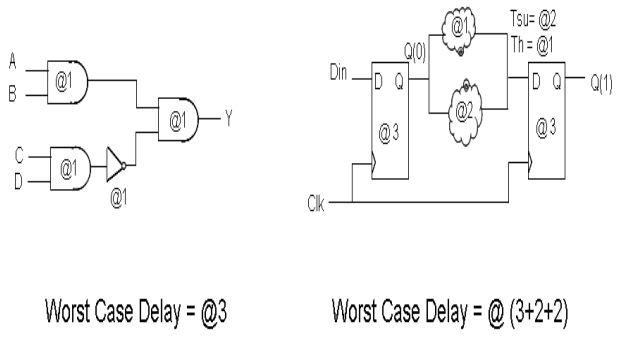


Figure 2. Delay count using conventional STA [8]

This method is not considered to be accurate as the possible process variations are not considered. This method does not consider the process variations. With a case based STA analysis, it is therefore difficult to calculate actual timing distribution of a circuit. To overcome this difficulty SSTA is one of the new concepts. SSTA models process parameters such as gate length, width, oxide thickness and doping concentration as random variables and propagates these random variables through the circuit in topological fashion to calculate the performance of the system similar to the propagation in its deterministic counterpart.

As mention earlier conventional method is not accurate method. To overcome this, various methods are available to give accurate timing analysis. One of the most usable method that is Monte Carlo analysis, but this is very time consuming method. To overcome this researcher finds various algorithms, but some of them consider only one or few process parameter variation to decide operating speed. In this study, we propose a new algorithm that will consider all process variations and gives accurate operating speed of the circuit.

### *A. VLSI Circuit design specifications*

To design high speed VLSI circuit, the major three specifications are important first the operating speed of the circuit, second the power dissipation of the circuit and third area required to fabricate a chip. Out of these three the first one i.e. operating speed of the circuit is most important and

challenging one. To decide the operating speed of the circuit the designer must know all timing constraint of the circuit like propagation delay of each logic gate, clock to Q time, setup and hold time of the flip flop and interconnect delay. By using these timing constraints designer finds longest path delay. According to that the speed of the system will decide. If the circuit is small then this may not be a tough task. But for millions transistor integration this will be very tough and challenging task.[8]

## II. STATISTICAL STATIC TIMING ANALYSIS OF GATES

### A. *For NOT Gate*

We will consider the two NOT gates connected in series i.e. first NOT gate is driving second NOT gate.

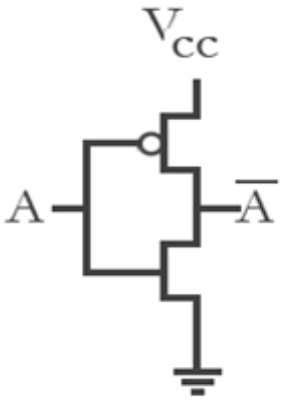


Figure 3. NOT Gate

To calculate the Statistical static timing analysis, we need to calculate the proportional delay (tp) of the NOT gate.

In second invertor, capacitance is generated at the PMOS & NMOS transistors, we will call them as CP & CN respectively. Now, the first Invertor will be either charge or discharge the load capacitor CL.

Where CL = CP + CN. CL will be charged through PMOS of first invertor and CL will discharge through NMOS of first invertor.

Propagation delay for NOT gate is given by:

$T_P = (T_{PLH} + T_{PHL}) /2$ Eq. (1)

For charging the load capacitor CL,

$T_{PLH} = R_P \times C_L$ Eq. (2)

$R_P = V_{DD} / I_{DSP}$ Eq.(3)

For discharging the load capacitor CL,

$T_{PHL} = R_N \times C_L$ Eq. (4)

$R_N = V_{DD} / I_{DSP}$ Eq. (5)

$I_{DSP} = I_{DS0} [1+(V_{ds} – V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ Eq. (6)[4]

$I_{DS0} = ( W_{eff} / L_{eff} ) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ Eq. (7)[4]

$\mu_{eff} = \mu_0/[1+(V_{A+} V_C V_{BS})\{V_{gsteff} +[2(V_{TH0} - V_{fb} - \phi_S)/T_{OXE} ] E_V\}$ Eq.(8)[4]

$\mu_0$ is low field mobility which is 0.06 $m^{2/}V$ for N channel & 0.025 $m^{2/}V$ for P channel

$V_A$ is first order mobility degradation coefficient ($10^{-15}$ $m/v^2$).

$V_C$ is second order mobility degradation coefficient ($0.045\times 10^{-15}$ $m/v^2$)

$V_{FB}$ is flat band voltage and the value is (-1.0Volt)

$V_{BS}$ is the voltage difference between bulk and source and by default it is 0V.

$T_{OXE}$ is oxide thickness and the value is 2nm.

$E_V$ is exponent for mobility degradation and the value is 1.67$m^{2/}V$ for N channel and 1.0 $m^{2/}V$ for P channel.

$V_{gsteff}$ is a smoothing function to ensure continuity between subthreshold region and linear region.

$V_{gsteff} = \max \{ V_{off} [(n V_t \ln(1+ \exp (V_{gs} – V_{th}))/ (n V_t)]/[1+n \exp(-(V_{gs} –V_{th}))/ (n V_t)]\}$ - -Eq. 9[4]

N= 1+N Factor

N Factor is nearly close to 1. So N is close to 2.

$\phi_S$ is a surface potential.

$\phi_S = 0.4 + V_t \ln(NDEP/ni)$ Eq. (10)

NDEP is a Channel doping concentration for zero body bias.

Ni is an intrinsic carrier concentration for silicon.

From the above equations we can say that the propagation delay varies with the length (L), width (W), oxide thickness ($T_{OXE}$) and dopants (ni) in the MOSFET. Now in statistical static timing analysis, we will consider the varying values of these variables and calculate the propagation delay. Whereas the value of oxide thickness and dopants are having very less variation so we can neglect those variations and can consider them as constant. In this we will vary length from minimum value to maximum value keeping other variables constant. We will generate matrix of these values and solve it.

### B. *For NOR gate*

The load capacitor (CL) will charge through PMOS N1 and N2 and load capacitor (CL) discharge through either N3 or N4. SO we need to design the PMOS and NMOS as per the requirement. $R_{p1}$ and $R_{p2}$ will come in series through load capacitor CL charges. So we need to take the value of $R_{p1}$ and $R_{p2}$ as

$R_p = R_{p1} + R_{p2}$ Eq. (11)

So to reduce the resistance $R_{p1}$ and $R_{p2}$ by half, we need to increase the width (W) by twice. So the charging time of load capacitor will be same. And for discharging the load capacitor through NMOS transistors the $R_{N1}$ and $R_{N2}$ are in parallel but it is not fix through which path it will discharge. So considering the worst condition we keep the width (W) as it is for NMOS transistors.

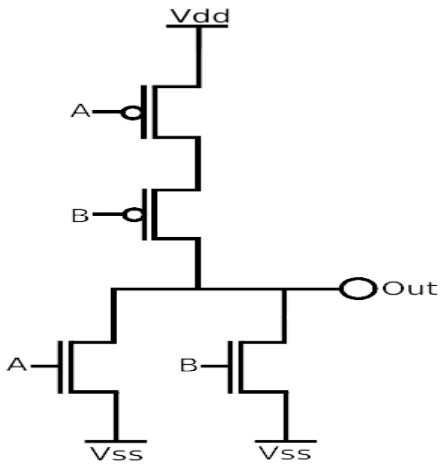


Figure 4. NOR Gate

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Propagation delay for NOR gate is given by:

$T_P = (T_{PLH} + T_{PHL}) /2$ Eq. (12)

For charging the load capacitor CL,

$T_{PLH} = (R_{P1} + R_{P2}) \times C_L$ Eq. (13)

$R_{P1} = R_{P2} = V_{DD} / I_{DSP}$ Eq. (14)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ Eq. (15)[4]

$I_{DS0} = ( 2 \times W_{eff} / L_{eff} ) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ Eq. (16)[4]

And for discharging the load capacitor CL,

$T_{NHL} = R_{N3} \times C_L$ or $R_{N4} \times C_L$ Eq. (17)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ Eq. (18)[4]

$I_{DS0} = ( W_{eff} / L_{eff} ) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ Eq. (19)[4]

### *C. For NAND gate*

The Load capacitor (CL) will charge through the PMOS Resistor $R_{p1}$ and $R_{p2}$ but the two resistors are in parallel in NOT gate. So the resistance $R_{p1}$ and $R_{p2}$ needs to be double so that it will charge the CL till its limit. So we need to decrease the width (W) by half. And while discharging the load capacitor discharges through $R_{N3}$ and $R_{N4}$ of the NMOS transistors, here these $R_{N3}$ and $R_{N4}$ are in series. So again we need to lower these resistances by half so we need to increase the width (W) by twice.

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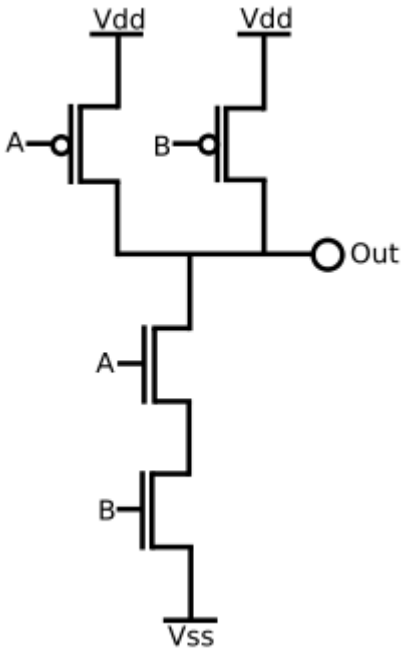


Figure 5. NAND Gate

Propagation delay for NAND gate is given by

$T_P = (T_{PLH} + T_{PHL}) /2$

For charging the load capacitor CL,

$T_{PLH} = R_{P1} \times C_L$ or $R_{P2} \times C_L$ Eq. (20)

And for discharging the load capacitor CL,

$T_{NHL} = (R_{N3} + R_{N4}) \times C_L$ Eq. (21)

$R_{N3} = R_{N4} = V_{DD} / I_{DSP}$ Eq. (22)

$I_{DSP} = I_{DS0} [1+(V_{ds} - V_{dseff}) / V_{ascbe}] [1+(1/ C_{clm}) \ln (V_{ASAT} + V_{Aclm}) / V_{ASAT}]$ Eq. (23)[4]

$I_{DS0} = (2 \times W_{eff} / L_{eff} ) \mu_{eff} (\varepsilon_0 \varepsilon_r / T_{OXE}) V_{gseff} [1- (A_{bulk} V_{dseff}) (V_{gsteff} +4V_t)] [(V_{dseff} / (1+ V_{dseff} / \varepsilon_{sat} L_{eff})]$ Eq. (24)

## III. EXPERIMENTAL RESULT

Our method has been tested for the various cases and the results are compared with the Monte- Carlo analysis for 16nm technology are found to be as follows, percentage error in mean for NOT gate is 0.018%, for NAND gate is 4.049% and for NOR gate is 4.834%. Whereas the percentage error in standard deviation for NOT gate is 11.083%, for NAND gate is 0.206% and for NOR gate is 7.008%, and the percentage error in propagation delay time for NOT gate is 0.205%, for NAND gate is 4.854% and for NOR gate is 0.327%. In all cases the result are considered for variation up to 0 to 10%. From these result we can say that our result is closely matched with the Monte-Carlo analysis to the satisfactorily conditions.

TABLE I. RESULT TABLE FOR MEAN

| Table Head | Mean | | |
|---|---|---|---|
| | *Statistical Analysis* | *Monte-Carlo Analysis* | *% Error* |
| Not Gate | 1.6354e-007 | 1.6351e-007 | 0.018% |
| Nor Gate | 2.3919e-007 | 2.2816e-007 | 4.834% |
| Nand Gate | 1.4904e-007 | 1.5533e-007 | 4.049% |

TABLE II. RESULT TABLE FOR STANDARD DEVIATION

| Table Head | Mean | | |
|---|---|---|---|
| | *Statistical Analysis* | *Monte-Carlo Analysis* | *% Error* |
| Not Gate | 8.9908e-009 | 8.0937e-009 | 11.083% |
| Nor Gate | 1.0854e-008 | 1.1672e-008 | 7.008% |
| Nand Gate | 8.1950e-009 | 8.1781e-009 | 0.206% |

TABLE III. RESULT TABLE FOR PROPAGATION DELAY

| Table Head | Mean | | |
|---|---|---|---|
| | *Statistical Analysis* | *Monte-Carlo Analysis* | *% Error* |
| Not Gate | 1.7954e-007 | 1.7991e-007 | 0.205% |
| Nor Gate | 2.3919e-007 | 2.3841e-007 | 0.327% |
| Nand Gate | 1.6364e-007 | 1.7199e-007 | 4.854% |

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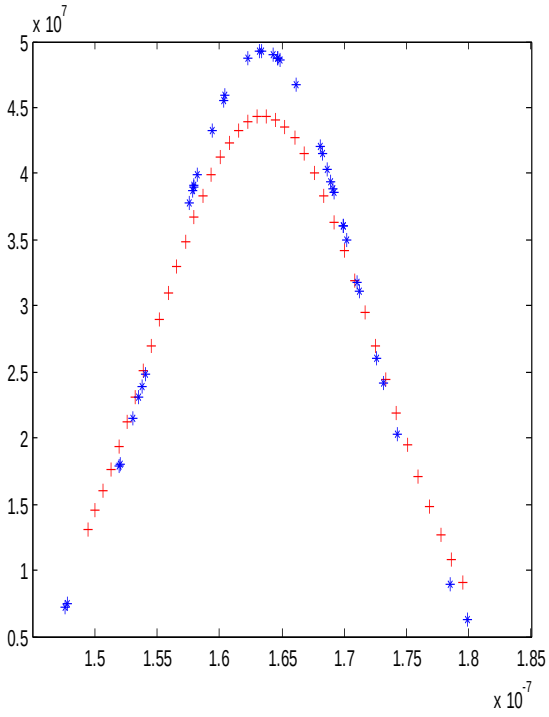


Figure 6 Probability Curve of NOT Gate (Probability Vs Length).

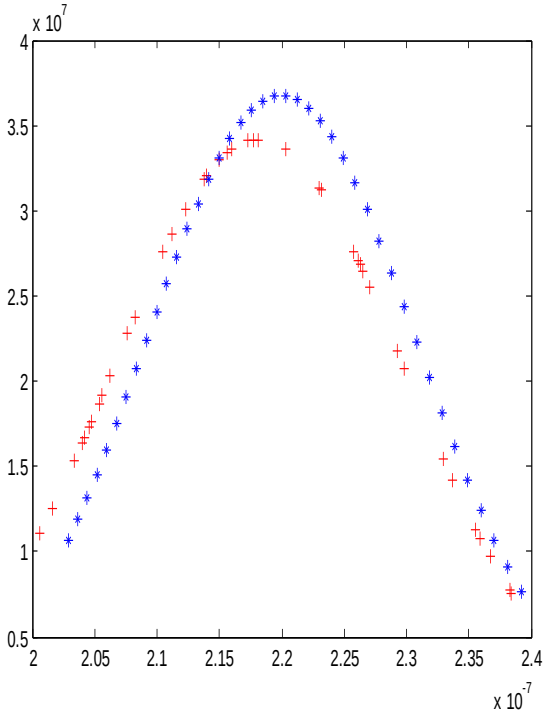


Figure 7 Probability Curve of NOR Gate (Probability Vs Length).

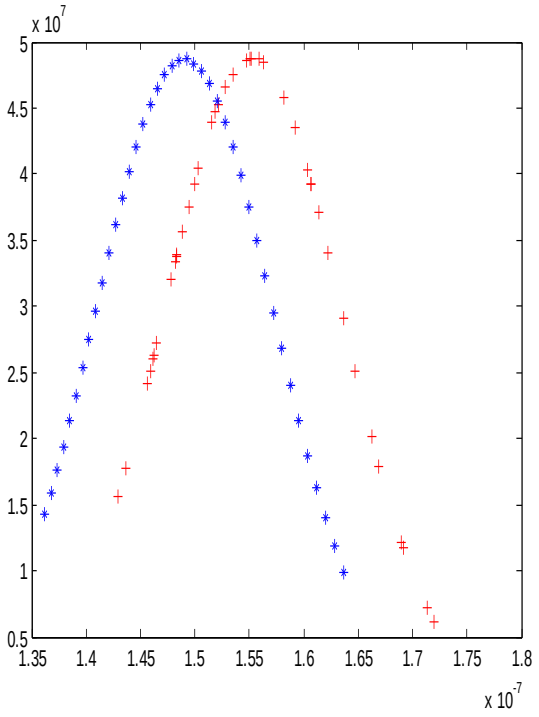


Figure 8 Probability Curve of NAND Gate (Probability Vs Length)

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