VHDL Implementation of Fastest Braun's Multiplier

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Abstract— Multiplication is an essential arithmetic operation for common Digital Signal Processing (DSP) applications, such as filtering and Fast Fourier Transform (FFT). To achieve high execution speed, parallel array multipliers are widely used. To decrease computational delay and improve resource utilization carry look-ahead adder circuit are use and Braun's-architectures multiplier is compared with its conventional architectural.

Keywords- *Braun's multipliers, carry look ahead adder, integrated circuit, central processing unit, gate delay, Xilinx*

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I. INTRODUCTION

Multiplication is an essential operation in Digital Signal Processing (DSP) applications. If the multiplicand is given be
A= an-1…a1a0 and multiplier B=bn-1…b1b0, then product P=P2nP2n 1P2n-2…P1P0 is given by

$$P = \sum_{i=0}^{n-1} \sum_{j=0}^{n-1} a_j \; b_j \, 2^{(i+j)}$$

Over the years the computational complexities of algorithms used in Digital Signal Processors (DSPs) have gradually increased. This requires a parallel array multiplier to meet the performance demands and a typical implementation of such an array multiplier is Braun design [1]. Multipliers consume most of the power in DSP computations. The unnecessary addition operation causes significant delay as well as power dissipation. This could be mitigated by employing Carry look ahead adder in place of ripple carry adder. Parallel processing and pipelining reducing delay. The objective of this study is to present a comparative study between the conventional multiplier and proposed multiplier.
In rest of the paper, section II explains Delay analysis of adder. Conventional and Proposed design of Braun's multiplier is presented in section III and IV followed by its performance and comparative analysis in section IV. Finally conclusions are made in section VI.

II. DELAY ANALYSIS OF ADDERS

A. *Half adder*

Assuming that all the different types of gates have same propagation delay, say T**.**
In half adder number of label of gate is one, hence propagation delay is one **T**.

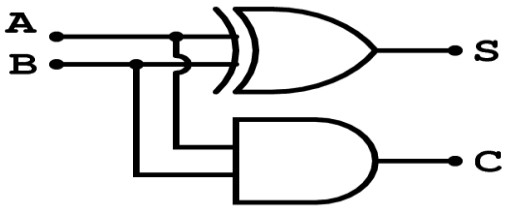

Fig . 1 Half adder

B. *Full adder*

From fig2 Full adder consists three label of gates. Hence propagation delay will be **3T**.

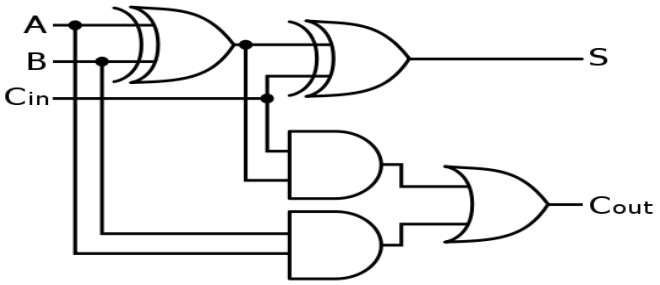

Fig. 2 Full adder

C. *Ripple carry adder*

Ripple carry adder is a very basic adder. The signal from the input to the output carry propagates through an AND and OR gate, which constitute two gate levels. If there are four full adders present in the circuit, the output carry would have 2 x 4 = 8 levels from C0 to C4,where CO and C4 are the input and output carry respectively.
The total delay time in this 4-bit adder would be the propagation time in one half adder (which is the first half adder) plus eight gate levels. so the total delay is **9T**.

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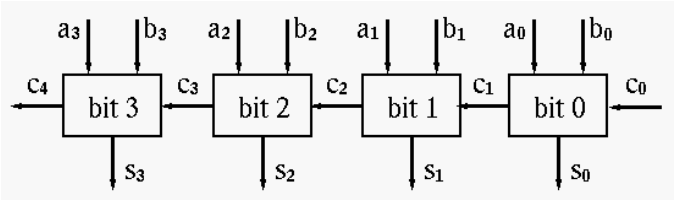


Fig. 3 Ripple carry adder

D. Carry look ahead adder

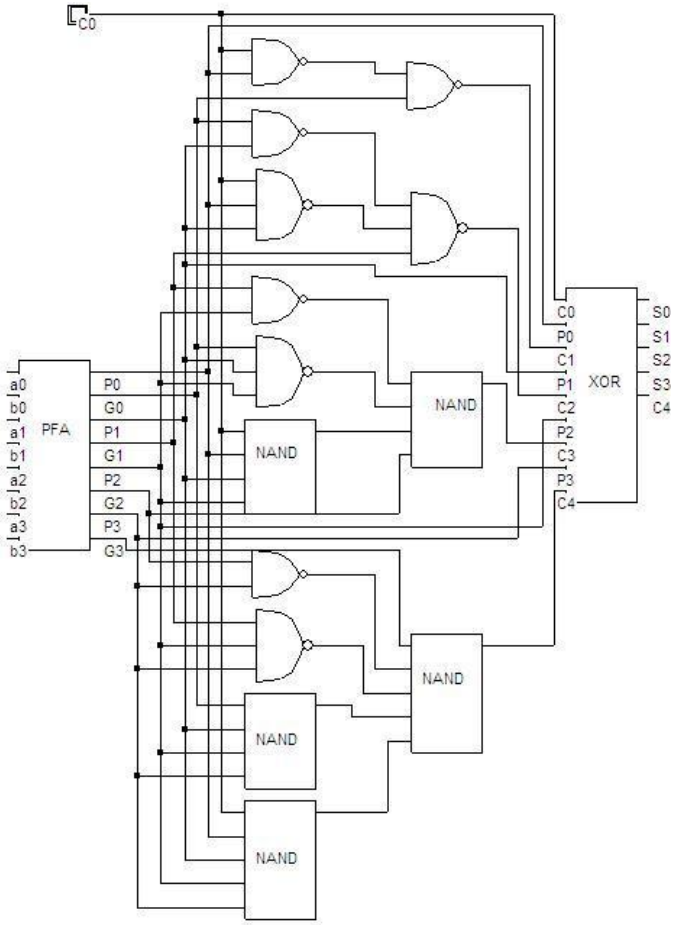


Fig. 4 Carry look ahead adder

The 4-bit carry look-ahead (CLA) adder consists of 3 levels of logic.

First level: Generates all the P & G signals. Four sets of P & G logic (each consists of an XOR gate and an AND gate). Output signals of this level (P's & G's) will be valid after 1T.

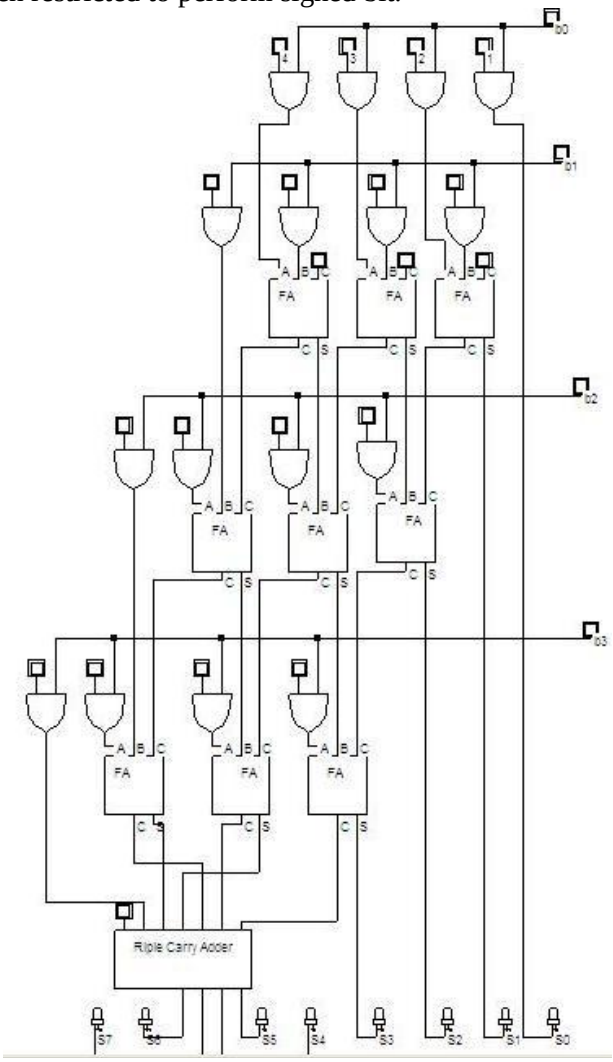
Second level: The Carry Look-Ahead (CLA) logic block which consists of four 2-level implementation logic circuits. It generates the carry signals (C_1, C_2, C_3, and C_4) as defined by the above expressions. Output signals of this level (C_1, C_2, C_3, and C_4) will be valid after 3T.

Third level: Four XOR gates which generate the sum signals $s_i = p_i$ XOR C_i. Output signals of this level (S_0 ,S_1 , S_2 and S_3) will be valid after 4T.

Thus, the 4 Sum signals (S_0 ,S_1 , S_2 and S_3) will all be valid after a total delay of **4T.**

III. CONVENTIONAL BRAUN'S MULTIPLIER

Conventional Braun's multiplier is a simple parallel multiplier called as carry save array multiplier. It has been restricted to perform signed bit.



FigNo.5 Braun's Multiplier with Ripple carry adder

The structure of conventional Braun's multiplier consists of array of AND gates and adders arranged in the form of iterative manner and no need of logic registers. This can be called as non – addictive multipliers.

Architecture:

An n*n bit Braun multiplier [1] & [7] is constructed with n (n-1) adders and n2 AND gates as shown in the fig.5 Where,

X: 4 bit multiplicand

Y: 4 bit multiplier

S: 8 bit product of X and Y

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The structure of the full adder can be realized using above figure.. Each of the products can be generated in parallel with the AND gates and Each partial product can be added with the sum of the partial product which has previously produced by using the row of the adders. Then the carry out will be shifted one bit to the left or right and then it is added to the sum which is generated by the first adder and the newly generated partial product. The shifting would carry out with the help of Carry Save Adder (CSA) and then the Ripple carry adder should be used for the final stage of the output of the circuit. Braun's multiplier performs well for the unsigned operands that are less than 16 bits in terms of power, speed and area. But it is the simple structure when it is compared to the other multipliers. The main disadvantage of this multiplier is that the potential susceptibility of Glitching problem due to the Ripple Carry Adder present in the last stage. The total delay depends on the delay of the Full Adder and also in the final adder in the last stages. From the above figure 5 we can calculate delay through finding the number of labels of logic gates. All Inputs a0a1a2a3b0b1b2b3, we can apply inputs signal in only one label, we know that all the full adder woks in three logic labels except last ripple carry adder .hence columns of three adders works in 3x3 labels, i.e. in total 9 labels. Last stages of ripple carry adder works in extra 9 labels as explained above. from the above fig. we can conclude that the Braun's multiplier using ripple carry adder is very slow in terms of its response time. The total stages to execute Braun's multiplier contains 19 labels, hence the total delay is **19 T.** and this amount of delay is quite large and hence a proposed method is introduced here to minimize the delay of Braun's multiplier**.**

IV. PROPOSED BRAUN MULTIPLIER

The Braun's Multiplier (fig. 5) which uses the ripple carry adder block adding the partial product of last stages. in the proposed method we have used the fast addition method i.e. carry look ahead adder so that we are reducing the number of labels so delay is also getting reduced. The fig. 6 which shows the proposed method of the Braun's multiplier. In the proposed method the number of labels of addition are reduced and due to this delay has been very less when compare to the conventional method. In proposed Braun's multiplier, we used carry look ahead adder in place of ripple carry adder. From the figure 6 we can calculate delay through finding number of labels of logic gate. All Inputs a0a1a2a3b0b1b2b3, we can apply inputs signal in only one label, we know that all the full adder woks in three logic labels except last carry look ahead adder .hence columns of three adders works in 3x3 labels ,i.e. in 9 labels. Last stages of carry look ahead adder works in extra 4 labels as explain above. The total stages to execute proposed Braun's multiplier contains 14 labels, hence delay is **14 T**.

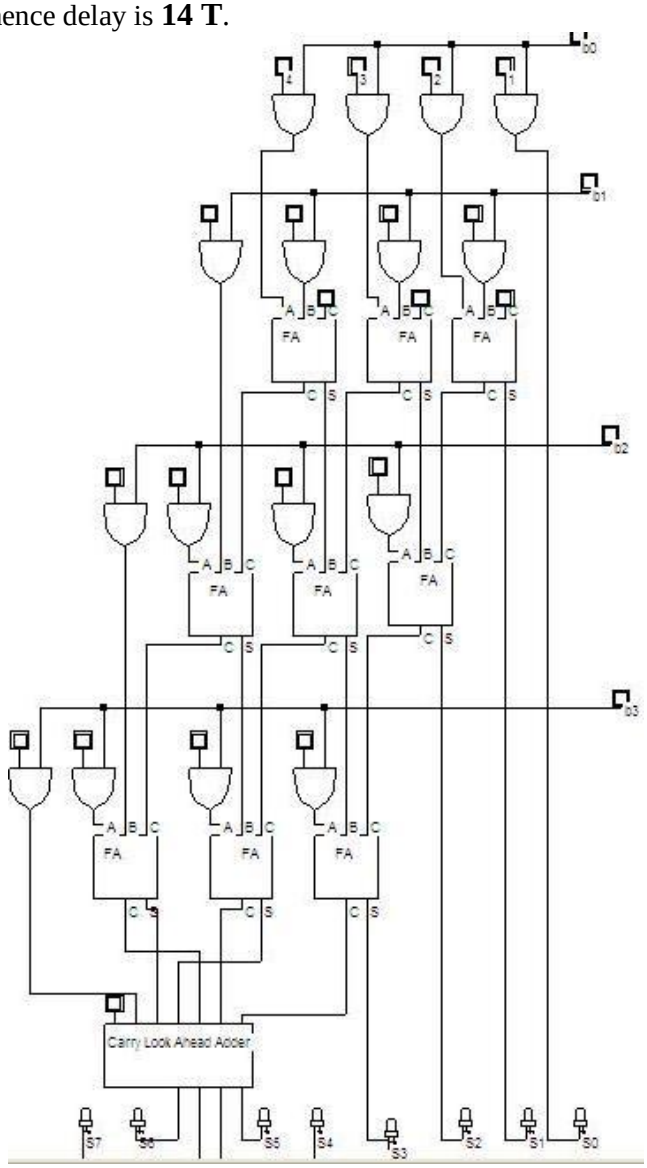

Fig. No. 6 Braun's Multiplier with carry look-ahead add

V.IMPLEMENTATION AND RESULTS

The simulation is carried on Xilinx and microwind .
Proposed work reduced the delay of Braun's multiplier to an great extend. In the proposed work carry look ahead circuit is used which reduces delay but increases circuit complexity, area and power consumption.
In conventional Braun's multiplier number of gate label is 19 as in fig 5 explain., where as in proposed Braun's multiplier number of gate label is 14 as explain in fig 6. Since more number of gate label adds delay at each level thus proposed Braun's multiplier cuts down much delay of the circuit .

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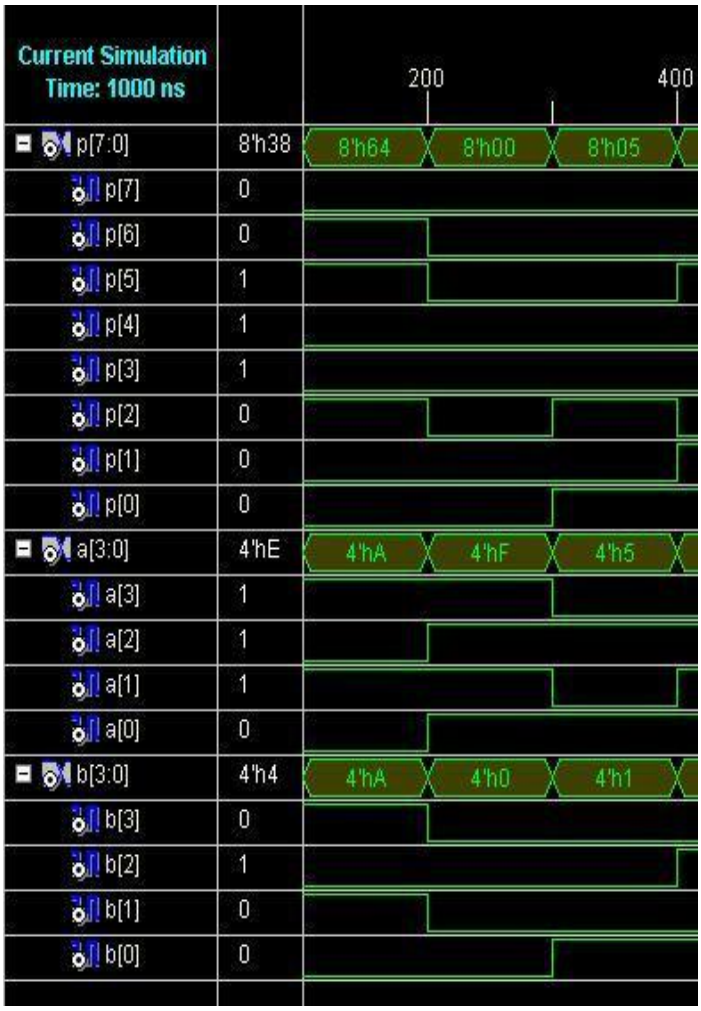
Figure 5 The simulated of time delay of Braun's Multiplier in the tool of Xilinx-ISE.



V. CONCLUSION

The proposed work in this paper shows that the Braun's Multiplier emerged as the fastest among the conventional multipliers. The circuit designed by using ClA has successfully reduced the delay upto 25%.The proposed multiplier circuit finds it application where the hardware requires quick response. The delay is reduced and hence the response of the circuit becomes superior by sacrificing some of its parameters such as area, power and circuit complexity. This is preferably used in Digital Signal Processing applications where the response of the circuit is given much importance than its cost.

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