USRP N210 FPGA Loop Back System

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Abstract—The USRP™ (Universal Software Radio Peripheral), provides users worldwide to address a broad range of research, industrial, academic and defense applications. The Universal Software Radio Peripheral is developed for RF application, and provides options for GPS Disciplined Synchronization, MIMO configurations and embedded systems. Ettus Research introduced number of USRPs with different FPGA in it. Different USRP have different FPGA but they have similar TX and RX chain in it. Day by day Ettus research provide USRP with large FPGA and FPGA codes open so that users can implement their own modules in FPGA and test it. This paper focused on USRP N210 having Xilinx Spartan 3A DSP FPGA. In USRP 1 they provide loopback system but in current USRP no loopback available. If loopback is available then user can test their module at two stage: 1) after ADC/DAC module and 2) after DDC/DUC module.
This paper describes the loopback system at two different stage: 1) after ADC/DAC and 2) after DDC/DUC in USRP N210 FPGA.

Keywords-*USRP N210, FPGA, ADC, DAC,DDC, DUC*

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I. INTRODUCTION

Universal Software Radio Peripheral is well known product in worldwide for developing prototypes of different system. USRP is perfect to test and verify the different protocols developed in laboratories[4]. Ettus research provides various type of USRP. Ettus research introduced a series of USRP for user as per their area of interest. It includes bus series(USRP B200/b210), network series (N200/N210), embedded series(E200/E210) . Different USRP have different FPGA small, medium, and large. The FPGA is different in different USRP but the receive and transmit chain inside it is same for all[6].

USRP can compatible with variety of daughterboard so the user can choose it as per their own requirement. The FPGA code for USRP is openly available and it's completely open source[6]. Due to those reason lots of research origination and institute use this to tess and verify their design on it. New USRP products provides large FPGA i.e USRP N210 have Xilinx Spartan 3A DSP so that user can develop their own custom module in USRP FPGA and test it[5]. To fulfill that requirement loopback system is required in USRP. USRP is controlled through host PC but in some place host PC can cause problem so we must remove it or we loopback data from FPGA of USRP.

USRP controlled through UHD driver, which can be installed in host PC. UHD is compatible with Linux, MAC and window OS.UHD provides API through which we can control as well as change the USRP parameters.

II. UNIVERSAL SOFTWARE RADIO PERIPHERAL (USRP N210)

Universal Software Radio Peripheral is software reconfigurable RF hardware from Ettus Research to build a digital communication system. The PC controls the USRP through the gigabit Ethernet cable[1].USRP is the hardware platform for SDR which is composed of programmable FPGA, analog to digital converter/ digital to analog converter, digital down converter/digital up convertor, dsp rx/tx chain and Ethernet port. It is designed to interface analog signal with the software. It takes an analog signal and interfaces it with SDR libraries, such as GNU-Radio, Simulink within Matlab, LabVIEW and UHD (Universal Hardware Driver).

Fig. 1: USRP N210 Front Panel

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USRP is basically a motherboard with FPGA. It has a daughterboard which has both transmitter (TX) and receiver (RX). The two onboard analog devices AD9777 capture the data; do decimation and interpolation tasks and filtering. Xilinx FPGA outputs stream of data into ZPU CPU . The ZPU accesses the interface between FPGA and LAN port so that we can transfer data into PC. Internal block diagram of USRP is shown in Fig. 2[1].

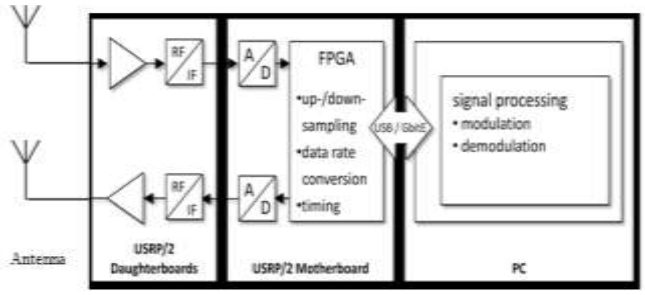

Fig. 2: USRP module block diagram [1]

A. Daughterboard

The USRP's motherboard can be interfaced with daughterboards or even with a custom RF front end. The daughterboards, available from Ettus research, have different specifications: bandwidth, power, and noise figure etc [2]. Daughterboards make it possible to use USRP in different frequency spectrums. This is because there are physical RF components needed to receive different frequency spectrum. On the motherboard there are four slots where one can plug up to 2 TX and 2 RX daughterboard. Each daughterboard slot has access to 2 of the 4-high speed AD/DA converters. It is also possible to use transceiver daughterboard to enable USRP to send and receive simultaneously [3].

B. Analog to Digital Converter (ADC)

ADC converter converts analog signal to digital. In USRP board there are dual 14-bit high-speed ADC with sampling rate of 100MS/s. In reality, it could digitize a band with wide width of 32 MHz [3]. The only problem is, it is not possible to receive signals with bandwidth larger than 32 MHz.

C. Digital to Analog Converter (DAC)

The DAC converts a digital constructed signal to analog. On transmitter side, there are dual high-speed 16-bit D to A converters. The DAC sampling rate is 400 MS/s[3].

D. Field Programmable Gate Array (FPGA)

FPGA (field programmable gate array) is a large resource of logic blocks and RAM block which provides high speed digital computation. FPGA help us to implement the real time application system. USRP contain an on-board FPGA, which provide all signal filtering of the RF signal. FPGA consists reconfigurable logic elements and switch matrix to route signal between them.

E. Internal component of USRP FPGA

The complete FPGA of the USRP can be divided into a different communication layer stack. Fig.3 defined a block diagram of internal component of FPGA in USRP N210. Different components of the FPGA in USRP N210 are Gigabit Ethernet at the physical layer interface, followed by the MAC layer having GEMAC, a packet router in the network layer, VITA 49 protocol or VITA chain in the transport layer and finally DSP chain at the application layer. The signal received from the RF front end panel is delivered to the MAC layer via Gigabit Ethernet. The GEMAC of the MAC layer is removed the MAC address of the data and the packet is delivered to the network layer for the routing purpose. The packet router in the network layer removed the IP address and routes the packet to CPU, DSP chain as well as the external controller. An aeMB processor is in FPGA of USRP having a wishbone-bus interface for all signals controlling elements. All signal and packet management is carried out by the CPU called ZPU.

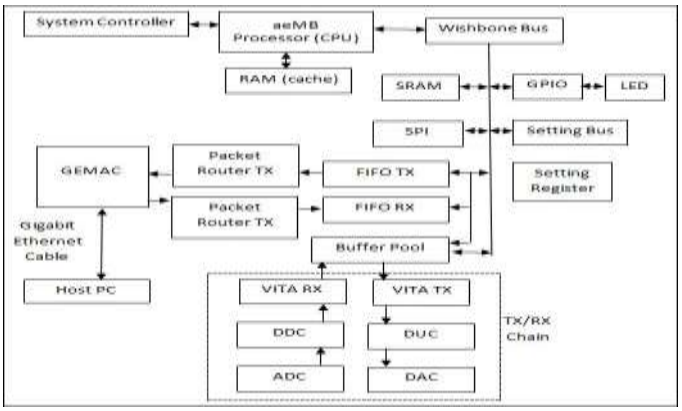

Fig. 3: Internal block diagram of USRP's FPGA

The external module interface to FPGA such as LED is done via the GPIO (general purpose input/output). The status of all six LEDs describe the information about receive, transmit, firmware and CPLD loaded, reference clock status and MIMO cable line status. The Daughter-boards are fixed onto the FPGA through the SPI (serial peripheral interface). The FPGA has a built-in SRAM to store the data. External memory card of 1GB is supporting in USRP N210. The soft-core processor ZPU in USRP N210 FPGA has a wishbone bus interface to fetch the data from the memory. DSP chain in the FPGA performs all the signal process like filtering and processing in digital and analog domain. DUC-DDC unit of TX/RX chain is used for frequency up-down conversion of the RF signal. Finally signal is pass-through DAC/ADC of Daughterboard.

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III. PROPOSED SYSTEM

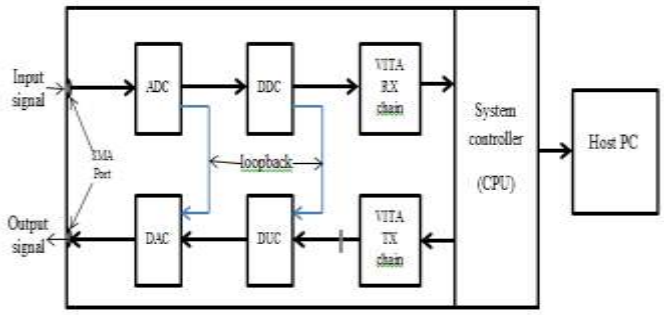

Fig. 4: proposed system for loopback in USRP N210

Fig. 4 describe the two loopback system combine. Here the basic Tx and Rx chain described. The received signal from Rx SMA port will travel through ADC to DDC and from DDC to VITA Rx chain and finally go to the device CPU. CPU controlled the received signal and transmit to the host PC in a proper format. They have two formats: UHD control protocol and VITA 49 protocol format. The host PC contains different kind of framework like GNU Radio, LabView. Host PC uses those framework to process received signal from USRP and send it back to the USRP to transmit in the air or over the wire. The transmission process is reverse of receive process.

After analysis the Rx and Tx path, there are total three possibility to do loopback into FPGA of USRP. Frist is after ADC turns the signal to the DAC directly. The output from ADC is 14 bit while input of DAC is 16 bit so we have to pad two bit in two output adc_a and adc_b and directly map to the DAC input. The second possibility is transmit signal to the DUC after doing DDC. The output of DDC is 32 bit sample and input of DUC also 32 bit sample so after DDC done, the 32 bit sample wired to the input of DUC. Third possibility is after VITA Rx chain but that is little bit difficult to understand. In above two possibility the inbuilt clock handle and in VITA chain the VITA time also came in picture.

I. EXPERIMENTAL SETUP AND RESULTS

Proposed system described the three possibility but here we did loopback by two different levels. For experimental setup used systems are USRP N210, signal generator, spectrum analyzer, desktop computer.

Fig. 5: experimental setup for loopback system

Fig. 5 is experimental setup in which USRP N210 is connected with desktop computer, signal generator, and spectrum analyzer. To change the FPGA code or functionality, ISE 12.2 in Linux is recommended by Ettus research. Once the FPGA code changed the FPGA image file have to generate using make command because USRP accept FPGA and firmware images(.bin). We developed two different FPGA image for two different loopback system and then test it. USRP accept only FPGA images so one way to test it functionality is describe here.

A. ADC to DAC loopback

In this experiment the FPGA functionality changed through change in FPGA code in that the output of ADC is directly connect to input of DAC under taking care of bit size. After that FPGA image generated and load in USRP N210 through UHD util. Once image file accepted successfully by USRP N210 the final testing can happen.

Fig. 6:ADC/DAC loopback in FPGA of USRP N210

For testing loopback system a signal generator connect to the Rx2 SMA port or USRP N210 from where a signal came into USRP FPGA. Signal generator preset to generate sine wave of frequency 93.00 Mhz at input -22.0 dBm because USRP N210 have maximum input is -10 dBm. The TX/RX port of USRP is connected to the spectrum analyzer. The

connection between computer and USRP is not require at this stage so it removed. As connected all port properly we can see that the output signal from USRP N210 in spectrum analyzer in channel 2 that sine wave come out from USRP N210. The USRP in not connected with host PC that means no command is given to USRP from host PC and same wave coming out which we gave to USRP N210. This proved that the loopback is done through ADC to DAC successfully.

B. DDC to DUC loopback

In this expirriment same prosedure follow as done in above expiriment the only difference is that change in FPGA code and then generate new FPGA image to load in USRP. Output of DDC is 32 bit sample which is directly given to the input of DUC.

Fig. 7: DDC to DUC loopback system

In this we use 91.00 Mhz and -26.7 dBm input and successfully loopback done.

II. CONCLUSION

By this experiment the loopback is possible in USRP N210 FPGA from two different stages. In first stage the signal is directly loopback from ADC in receive side to DAC in transmit side. In second experiment loopback is happen after DDU in receive side to DUC in transmit side. This will helpful for future use of loopback system where user want to use only ADC/DAC or ADC/DAC-DDC/DUC of USRP N210 and receive signal back from FPGA direct without sending signal into computer.

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