Analyze and Study the Impacts of Different Packages on Static and Dynamic IR Drop Analysis on Different Infineon Designs

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Abstract – Dynamic voltage drop depends on the switching activity of the logic compared to static IR drop, and hence it is a vector dependent concept. In this paper we have highlighted the methodology of extraction and modeling of package along with the chip-package static IR drop as well as dynamic IR drop analysis scenarios.A proper structured approach to analyze the impact of package parasitics onto the die is presented, with an emphasis to cover different corners in which IR analysis is impacted, and how it can be implemented in the design cycle. Finally, the impact of package on chip is studied by considering the histogram plots obtained from dynamic IR numbers. Later using all the numbers & plots impact of different packages on chip is realized.Results are from acquired from industrial designs in 65nm process related to the said topics.

Keywords- *IR drop analysis, Package modelling, Static IR drop, Dynamic IR drop, Package simulation*

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I. Introduction

Designing a good power network which is robust across multiple operating scenarios of a chip itself is a major challenge. The problem has magnified with the technology shrinking allowing more and more components, features and performance to be packed in a smaller area, from one node to another. The power distribution on a chip and package needs to ensure timing or reliability is not affected due to dynamic IR drop, caused by localized power demand and switching scenarios.Further, amongst today's devices power management techniques like are introduced which also have some effect over the design performance.[5]

This paper discusses the issues related to design closure and sign-off (timing, IR drop, EM, reliability etc.,) comprehending dynamic IR drop effects realistically. On one hand, the factors and scenarios that impact on dynamic voltage drop analysis on chip have to be removed, while on the other we must ensure that the methodology ensures good coverage of various silicon conditions along with design operating scenarios. We then discuss the methodology of extracting and modeling the package file which will be usually in package design tool supported format and highlight the various aspects that need to be taken care of, from the early stages of design implementation. We also demonstrate the systematic use of the modelled spice package sub circuit file in the power analysis environment. All the analysis, findings are based on design implementations of application processors for various devices. The designs include high frequency CPU cores, memory IPs and other analog macros. The numbers mentioned are from the analysis and/or from simulation.[5]

The structure of the paper is as follows. In section II,the methodology for extraction and modeling of package file using Package modelling tool is discussed along with the most common issues generally encountered during the package simulation. In section IIIthe commonly followed static and dynamic IR methodologies are highlighted with design results. In section IV then explains how we went about the power analysis on chip only and chip with different packages by using third party IR analysis tool. Section V shows the tabulation of results captured from designs along with and without different packages.

II. Methodology for package extraction & modeling.

A. Overview of packaging integrated chip.
In IC manufacturing process, integrated circuit packaging is the important step in semiconductor device fabrication, in which the tiny block of semiconducting material which is also called as die is encased in a supporting case that prevents physical damage and corrosion. The case, known as a "package", supports the electrical contacts which connect the device to a circuit board and also provides mechanical support for the chip.

For our analysis we have considered different packages like BGA, LQFP and QFP.Here in this paper we discuss about the extraction and modelling of these packages to generate a spice file which is later used for power analysis with the chip. The spice file provides the actual information about the package nets, layers and other components involved in it.

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B. Extraction and modelling of package.[2]

In this paper we discuss about steps involved in the extraction process and also issues encountered during extraction and modelling. The package is basically designed in Package design tool environment and the extraction is done using Package modelling tool.

Package modelling tool is ahigh performance q-static electromagnetic modelling tool for IC packaging and System in Package (SiP) designs etc.

With an advantage ofGUI and direct package design and layout database import functions, package designers and other engineers can efficiently build a physically robust and correct RLCK model for the entire package. With Package modelling tool, designers can quickly assess the electrical and physical performance of the package such as characteristic impedance, crosstalk and signal noise due to mutual capacitance and inductance, and power-ground inductance distribution over the chip. The designers can also get to know the package design weaknesses through the current distribution maps, as well as the RLC distributions by layers etc.This is one of the powerful tool for extraction which supports for different CAD tool interfaces like Package design tool (.sip, .brd, .mcmm), Gerber, Mentor Graphics MCM station, Zuken CR-5000 etc. For our analysis we have considered .sip file which is outcome of some package designer environment. At first basically the designer develops a package layout and runs a simulation on it just to make sure it does not contain any DRC or other geometry errors. Once it is done it will be saved in a .sip extension. We now use Package modelling tool along with some third party tool to extract and convert the .sip into .xfl format.

The third party tool used here is a Package modelling tool which is used as static extraction tool in the market that provides whole package RLC parasitic extractions. Design physical features such as wires,vias, solder balls and pads require a unified model to provide SPICE-level accuracy. In this tool fast model extraction technology is used for package extraction.Package modelling tool uses techniques like direct energy integration depending on the simulation results like electrical field (potential) or magnetic field (currents) to calculate and evaluate the model parameters. Package modelling tool provides a non-tedious way using GUI for package designers to build a multi-dimensional model. Its various options and pictures help designers with an interface to enter geometric, layer stack and material information, and automatically building the multi-dimensional model.

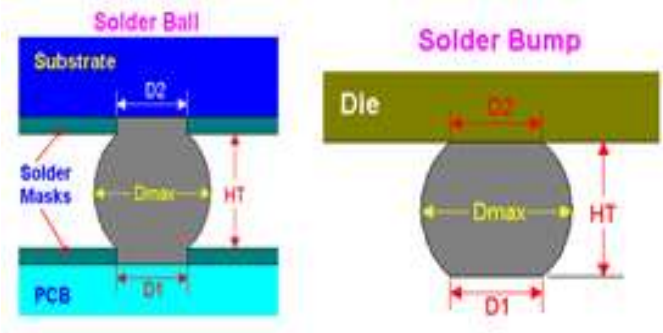

Fig1: Specifying technology parametersincludes bump/ball geometry) for package extraction.

Package modelling tool first builds completemulti-dimensional modeldepending on input design files. The building of multi-dimensional modelsis completely automatic. It then processes the static Maxwell equations and obtains electrical and magnetic fields of the multi-dimensional models. From the resulting fields, Package modelling tool extracts the RLC parasitic parameters and generates SPICE models, including H-SPICE compatible models for signal integrity simulations.

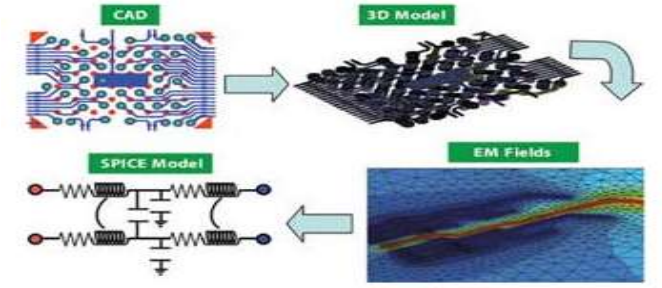

Fig2: Automated package modelling-from design geometry to SPICE model.

C. Port power and ground nets extraction [5].

With the robust automatic finite element mesh and grid generation engine, Package modelling tool can efficiently simulate complex power as well as ground nets. Geometric information such as holes in a plane, solder bumps, vias and solder balls are all modeled carefullysince smaller geometric things can affect the complete behaviors of a power net and ground net. Package modelling tool's allows one to assign port parameters and configurations using multi-port modules to extract its power and ground RLC parameters. Along with the generating RLC parasitic parameters, Package modelling tool gives power net and ground net voltage drop values

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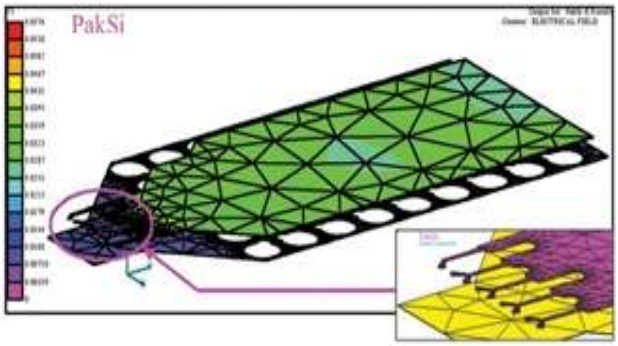

Fig3:Extracting power net and ground nets with multi-ports.

D.Challenges during extraction and modelling

Once the package simulation is done, we go for IR analysis tool compatible spice file and pad location file (Ploc) generation using third party utility. Here the chip ploc is used for providing die pad information and wideband spice (WBS) is generated from Package modelling tool.

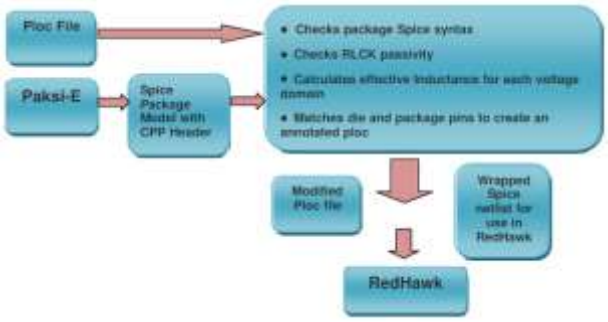

Fig4: Third party package compiler data flow

The data flow for compilation is shown above. The inputs are ploc file and wideband spice from paksi-E along with the CPP header. CPP is Chip Package Protocol which enables Package modelling tool to automatically align and connect to grouped pins. Later on third party utility performs different tasks like checking of package spice syntax, RLCK passivity checks, calculates effective inductance for each voltage domain and matches die-package pins to create an annotated ploc.

III. IR drop analysis methodology

A.Overview of Static IR dropandDynamic IR drop.

Static IR drop depends on average current through the net in the design. Whereas Dynamic IR drop is based on the activity profile of the logic cells, hence it is a vector dependent. Dynamic IR drop is based on the switching timeand is not much dependent on the clock period times. The Average current through any net depends usually on the time period, where dynamic IR drop depends upon the instantaneous current through one of the net which is higher while the cell is switching.

Static voltage drop sign-off was good for closure stage, since in previous technology nodes where most of the natural decap capacitance from the PDN and non-switching logic networks were available. Where Dynamic voltage drop is when largeamounts of circuitry switch at a time, causing high peak current demand. Thispeak current demand could be localized and could handle with the single clock cycle, and could also results in anvoltage drop that causes extratiming violations. Typically IR drop impact on clock distribution network causes timing that too hold-time violations while IR drop on data paths signal nets results in setup violations.

B. Methodology for data preparation.

For our analysis we have considered six different designs and LQFP, BGA and TQFPas packages.Third party tool is used for IR analysis which provides accurate results and IR simulations. At first the database is prepared in a setup file. The inputs to the third party tool are DEF, LEF, LIB, SPEF/DSPF, STA, APL, Ploc and TECH file.DEF is Design exchange format which basically consist of logical and physical connectivity between different blocks and instances in the design. LEF is library exchange format which has the information related to pin description and block or instance boundaries etc. LIB are the Synopsys liberty files which contains several electrical as well as logical properties of a celllike input and output pin properties, power distribution information on different power pins, cell internal energy and information related to functionality of a cell etc. SPEF is the standard parasitic exchange format which has RC values for each and every net in the design. Tech file consist of information on all interconnected layers along with layer stack up information and other limitations like EM, IR.

Ploc is the location information of all pads based on full chip floorplan. APL files contains current profile characteristics for each standard cell, decaps characterization for each cell etc. STA files contains timing information from primetime, for static analysis it provides transition times and frequency for instances and for dynamic analysis it provides switching windows.

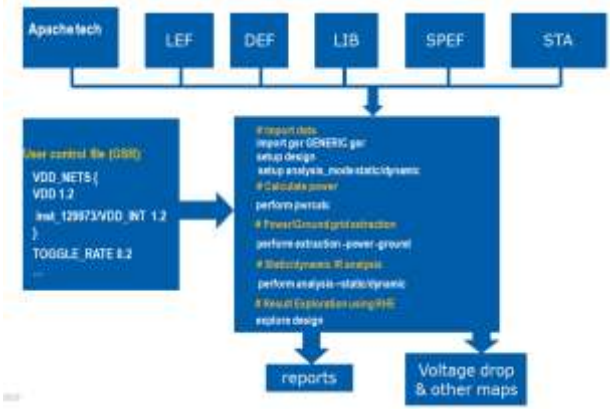

Fig 5: Inputs and outputs for IR flow.

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IV.Methodology and flow for with and without package Power analysis.

A. IR analysis flow using IR analysis tool.

Once the data is prepared we can always go ahead for IR/EM analysis. The first step is to basically consider only the chip and to carry out static and dynamic analysis i.e without package analysis. The results from the tool are evaluated by considering PG weekness, missing VIA, floating pins or many other parameters and if they seems to be good then the results are saved. Next step is to carry out the Static/Dynamic analysis with one of the package like LQFP/BGA. It is easy to add the spice file and ploc for package layout which is basically generated out of Package modelling tool into the setup file of IR analysis tool. Once this setup is prepared we can drive the third party tool with some tcl commands. Later the results are evaluated based on some parameters and graphs and saved. Similarly we can carry out analysis for any type of package as mentioned above.

The setps involved in analysis are shown in the below figure 6. At first the data is prepared, then it is imported into IR analysis environment here we can see the design layout. Later the power grid is extracted just to analyse each and every net. Power calculation is done through power stream which is integrated within the third party tool.

Fig6: Static/Dynamic IR Drop Analysis Flow.

Power/ground weakness are analysed to see any missing VIA or any other floating PG pads. Package parasitics are set with RLC values. Later on the requirement basis static or dynamic IR analysis is carried out. Then results are explored to see the overall scenario. The flow is shown in the above flowchart.

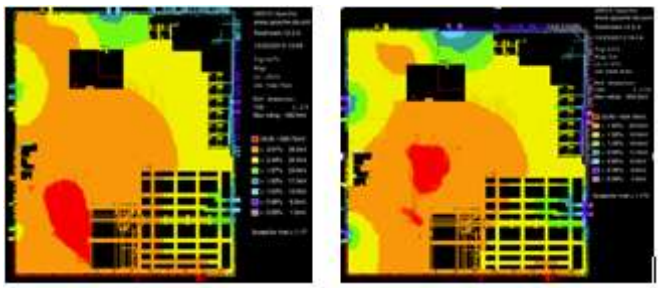

Fig7:static IR drop on VDD net with LQFP package and without package for Design-1

Now we can see the chip layout without and with package analysis. At first we did chip only analysis and later we added package spice file to it. The below picture shows how IR drop is occurred on selected net. Here we have considered VDD net, we can also see the ground bounce when we consider VSS net to generate the heat maps.Fig7 shows the static IR drop on VDD net with LQFP package and without i.e chip only for Design-1 design. Similarly the dynamic drop heat maps are also generated for the same design and package. Similarly we have considered 6 different designs and 2 types of packages to see the impact of package on these different designs.

DESIGN	PACKAGE	
Design-1	LQFP	BGA
Design-2	LQFP	BGA
Design-3	LQFP	BGA
Design-4	LQFP	BGA
Design-5	LQFP	BGA
Design-6	LQFP	BGA

Table1:List of design and package for analysis

The above said process is carried out for all the designs and packages. In order to see the package impact. we consider the effective vdd voltage on every instance obtained from dynamic IR report.

IV. Tabulation of results after analysis.

After the analysis is completed we can see the generated maps which clearly shows the impact on different regions with different colors. With these graphs we can analyse which pad is contributing more voltage drop. So now we have the results of dynamic analysis on with and without

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package spice sub-circuit. We can easily compare the effective vdd voltage appearing at each instance's power pin for both with and without package. The difference in voltage between with and without package analysis can be seen through a histogram plot which typically shows the number of instances falling on specified voltage range. From this graph we can see the differences clearly and the average IR drop for LQFP is found to be more than the BGA package. In the below figure we can see the histogram for Design-1 design. The first graph shows the impact of BGAon chip and second one is with theLQFP package.

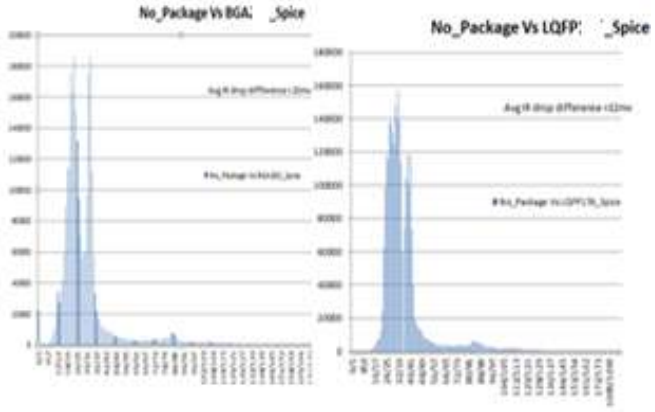

Fig 9: Histogram plots for Design-1 with BGA and LQFP package.

Similarly we can analyse the impact of these packages on different designs as mentioned above in the table 1. The summary of all the results recorded from the analysis is displayed in the table below.

DESIGN	Avg package IR drop difference between LQFP & BGA in %
Design-1	21.8%
Deisgn-2	48.2%
Design-3	42.8%
Design-4	22.2%
Design-5	17%

Table2: Results acquired from various designs.

The above table shows the average package IR drop of each package on different designs. The difference can also be studied using histogram plots, which shows the number of instances falling in exact IR drop range.

V. Conclusion

In this paper we have highlighted the steps and necessary ideas to extract and model the package completely. Also we can study impact of package parasitics like inductance and resistance on chip. Adding a package is just like adding extra resistance and inductance to the power and ground pins. BGA is shows less Package IR drop compared to LQFP. Since BGA offers less lead resistance than LQFP.Separate analysis should be carried out with BGA & LQFP in order to know the behavior at different corners.Along with the chip RLC, we can analyze the impact of Package RLC on the chip.Addition of package to the chip clearly implies addition of more parasitics and that could result in extra IR drop on chip.So the designer should be aware of the package IR drop contribution along with chip only drop.In order to know the RLC effects precisely, it is better to have separate analysis for all packages and IR drop analysis on package alone should be preferred.Package only IR drop analysis should be carried out by considering the chip current profiles in order to get realistic results.

Obviously there will be effects due to change in parasitics with the chip and we can also see some impact on chip performance. In order to minimize these effects decaps are spread all over the design. Necessary steps are involved in power distribution network design etc.

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