Design of Quaternary Arithmetic Unit in Standard CMOS

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Abstract— The multiple-valued logic (MVL) plays very important role in VLSI circuit design. The number of interconnections is reduced by using Quaternary logic than binary logic. In this paper we present the design of a prototype implementation and experimental results. Quaternary converter circuits are designed by using down literal circuits (DLC). Addition, Subtraction and multiplication i.e. arithmetic operations in Modulo-4 and in galois field logic are design and simulation results are shown in this paper by using Quaternary logic. Schematic of the design is done through S-SPICE. Simulation result is shown in Tspice. Tanner has created a software platform that is cost-effective and easy to use.

Keywords: *Down literal circuit, Multiple-valued logic, Quaternary logic, Modulo-n addition and multiplication*.

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I. INTRODUCTION

Interconnections are responsible delay, area and energy consumption in CMOS digital circuits. If we use Multiple-valued logic then it decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. The main characteristic of standard CMOS is timing and power. Quaternary look up table (LUT) designed using single voltage supply and employing only simple voltage mode statures is better than binary look up table (LUT). Since consuming 122 µW power and area efficient [1]. arithmetic logic unit (ALU) employed using quaternary logic by mapping binary LUT into the quaternary LUT using integrated linear circuits is more efficient than binary arithmetic logic unit (ALU) in term of area and speed required [2].circuits implanted in quaternary logic using voltage mode structures, by binary to quaternary mapping based on integer linear programming reduces transistor count by 27% and is power & cost effective[3]. The proposed adders are implemented in Multiple-Valued voltage-Mode Logic (MV-VML). In quaternary half adder, quaternary logic levels are first converted to binary and binary logic levels are used for the purpose of addition. Addition operation is performed with less number of gates and minimum depth of net [5]. Multi-valued logic (MVL) has matured to the point where four- valued logic is now part of commercially available VLSI IC's [6].

1. DOWN LITERAL CIRCUIT (DLC) Down literal circuit (DLC) is one of the most useful circuit element in multi-valued logic (MLV). The down literal circuit (DLC) can divide the multi-valued signal into a binary state at an arbitrary threshold. It consisting of variable threshold voltage by way of controlling only two bias voltages.

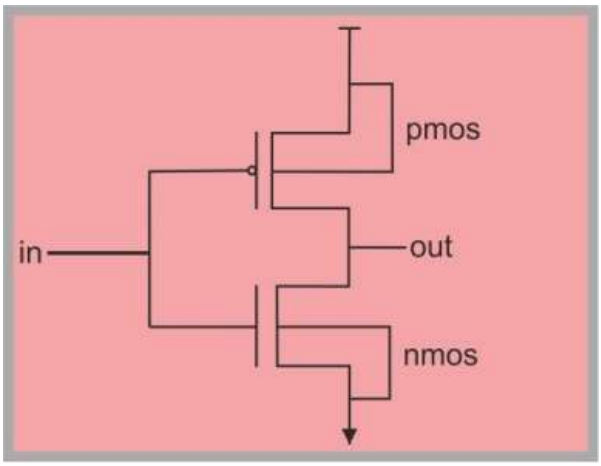

Figure 1: Circuit diagram for DLC

2. Modulo Arithmetic "Modulus" (abbreviated as "mod") is the Latin word for "remainder, residue" or more in "what is left after parts of the whole are taken". Thus, "modular" or "mod arithmetic" is really "remainder arithmetic". More precise: We are looking for the integer that occurs as a remainder (or the "left-over") when one integers is divided by another integer. We are familiar with "clock arithmetic." They subconsciously accept that 9 + 4 = 1, and 12 +12 = 12 in 12hr and that 12 + 12 = 0 in 24hr. in this paper we are using Modulo 4 arithmetic.

3. Galois fields are readily implementable with today's MVL technology .Galois field circuits are useful in many applications, from error correcting code encoders to cryptographic protection devices to interleaved memory controllers. Binary Galois field circuits have been investigated by many researchers All fields containing a finite number of elements must have the number of elements equal to a prime number (*p*) or some power of it (*pn*). Such fields are known as *Galois fields*. In this paper we are using GF (4).

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II. DESIGN OF QUATERNARY CONVERTER CIRCUITS

Depth of net means the largest number of gates in any path from input to output. The objective of optimization is to minimize depth of net and also to minimize number of gates needed. The reason for choosing these two objectives is that they will give very good properties when implemented in VLSI. When we minimizing number of gates will reduce the area and when we minimizing depth will give opportunity to use highest clock frequency.

2.1 Quaternary to binary converter (Q2B):

In Quaternary to binary converter, we use three down lateral circuits DLC D1, D2, D3 (each having different threshold voltage) and 2:1 multiplexer as shown in fig.2.As shown in fig.2 , Qin is the quaternary input for 3 DLC circuits. Q is changing from 0, 1, 2 and 3 then the binary outputs thus obtained will be in complemented form then we will required to pass output through inverters to get actual binary numbers i.e. B0 and B1. DLC are realized from basic CMOS inverter by changing the threshold voltages of pmos and nmos transistors.

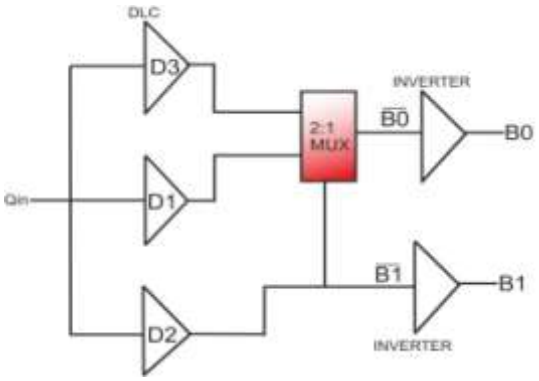
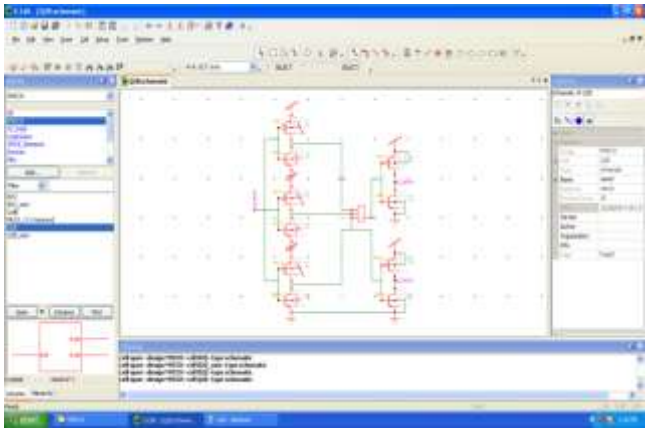
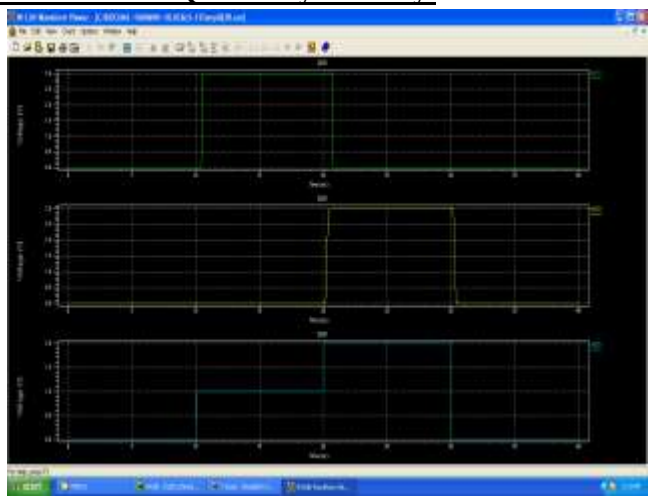


Figure 2: Quaternary to binary converter circuit

Schemetic for Quaternary to Binary:



Simulation 1 for Quaternary to Binary:



2.2 Binary to Quaternary converter (B2Q):

Figure 3 shows Binary to quaternary converter circuit. In two bit binary number LSB and MSB are given to DLC D1. Pmos1 = - 0.6 V, nmos1 = 0.6 V, pmos2 = - 1.2 V and nmos2 = 0.6 V are threshold voltages of transistor. Output of two inverters will provide quaternary number Qout. D1: V_{tp} = -2.2V and V_{tn} = 0.2V, D2: V_{tp} = -1.2V and V_{tn} = 1.2V, D3: V_{tp} = 0.2V and V_{tn} = 2.2V.

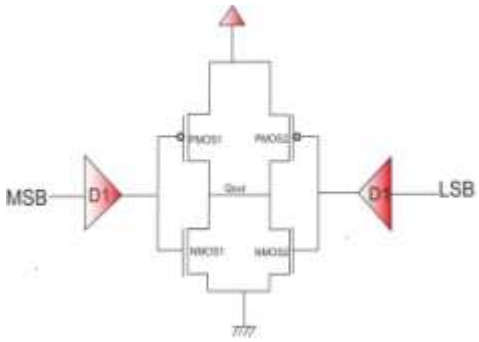
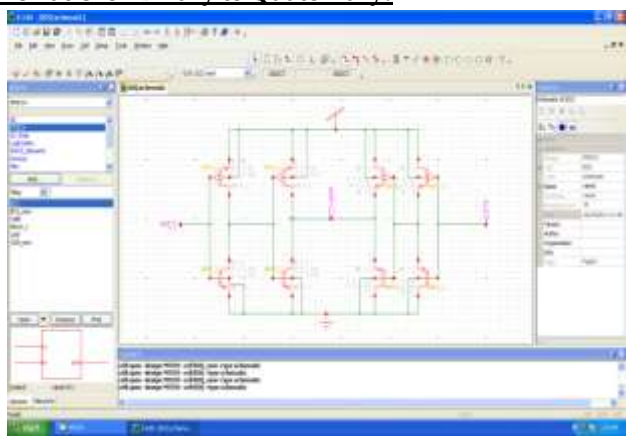


Figure 3: Binary to Quaternary converter circuit

Schematic for Binary to Quaternary:



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Simulation 2 for Binary to Quaternary:

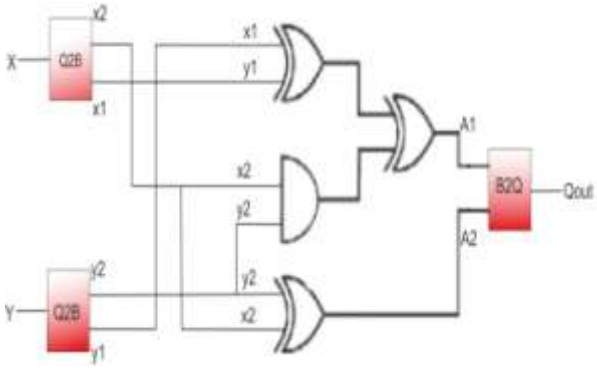


Fig.4 Logic Diagram for Modulo 4 Addition

III. MODULO-4 ARITHMETIC OPERATIONS

4.1. Modulo-4 addition and multiplication:

After quaternary to binary (Q2B) conversion the Modulo-4 addition and multiplication is take place. Consider, Quaternary inputs 0, 1, 2, 3 applying to the Q2B converter are represented as 00, 01, 10, and 11 respectively in binary. By taking objective of optimization in to consideration Modulo-4 addition and multiplication are performed. Truth table of Modulo-4 addition and multiplication are shown in table 3.

Suppose that, x_1 x_2 and y_1 y_2 be the binary representation of quaternary numbers X and Y which has to be added and multiplied.

Now suppose that, m_1 and m_2 denote the binary result of multiplying the binary numbers x_1 x_2 and y_1 y_2, and A_1 A_2 the result when adding them. We get output in binary form it is converted into Quaternary by using binary to quaternary converter (B2Q).

For addition:

$A_1 = (x_1 \oplus y_1) \oplus (x_2\ y_2)$ …… (1)

$A_2 = (x_2 \oplus y_2)$ …….. (2)

Here, M_1 and M_2 shows result when multiplying x_1 x_2 and y_1 y_2.

For multiplication:

$M_1 = (x_1\ y_2) \oplus (x_2\ y_1)$ …… (3)

$M_2 = x_2\ y_2$ ..... (4)

Logical diagram for addition shown in figure 4 and multiplication in modulo-4 are shown in figure 5. We can understood that depth of net is reduced to two and minimum number gates required are four as shown in fig.4 and 5.

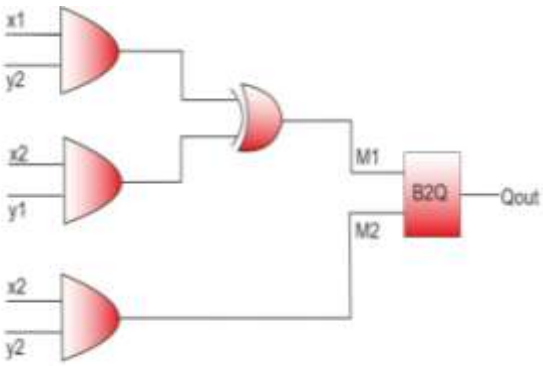
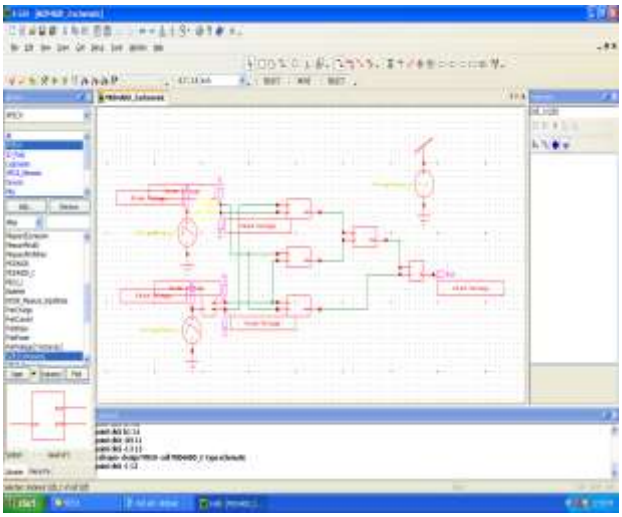


Fig.5 Logic Diagram for Modulo 4 Multiplication

Schematic for Modulo 4 addition:



x_1x_2

y_1y_2	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

Modulo-4 addition

x_1x_2

y_1y_2	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	0	2
3	0	3	2	1

Table 3 and 4: Tables for modulo-4 addition and multiplication

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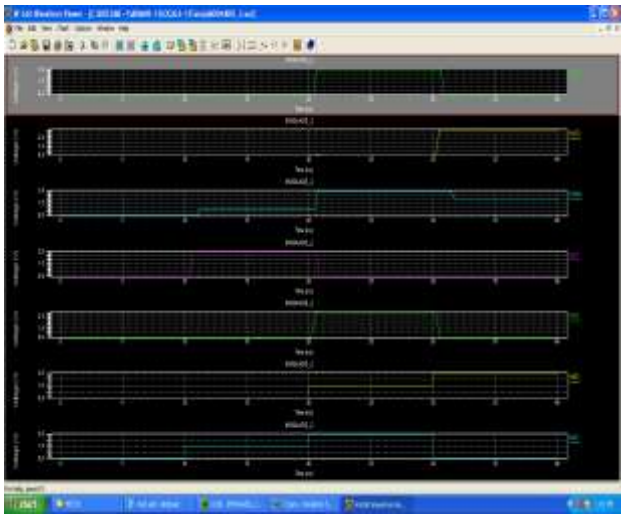
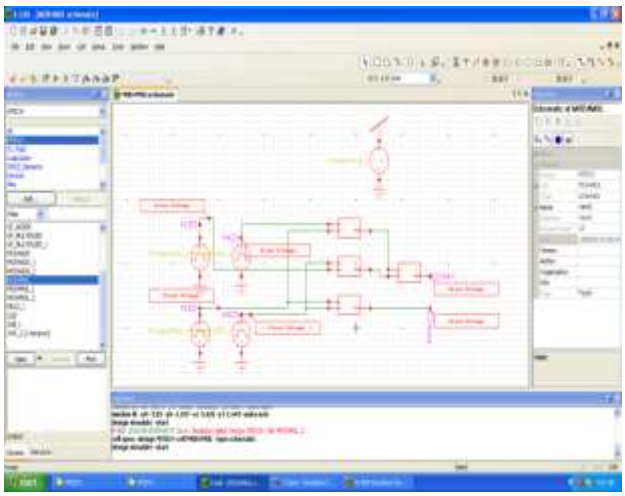
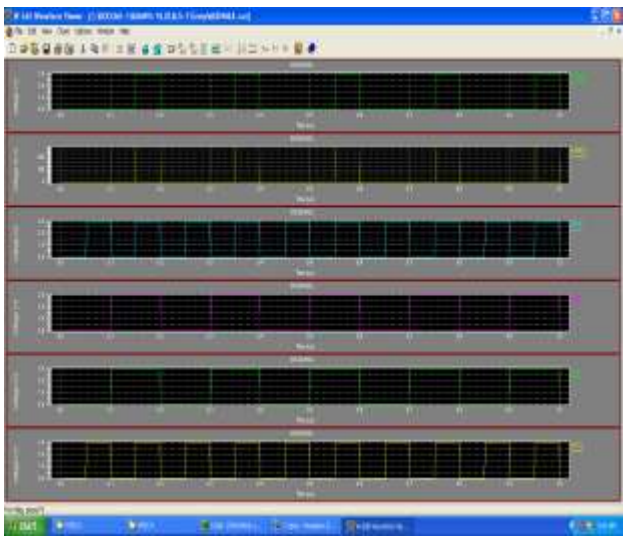
Simulation 3 for Modulo 4 addition:



Schematic for Modulo 4 multiplication:



Simulation 4 for Modulo 4 +Multiplication:



IV. Galois field addition and multiplication:

Fig.6 show two XOR gates input to these XOR gates are x_1 x_2 and y_1 y_2 which is binary representation of quaternary numbers. Galois addition table 5 is utilized in Karnaugh diagrams to induce minimum operate. The two bit results of addition between x_1x_2 and y_1y_2 shown by A_1 and A_2 square measure. $A_1=(x_1 \oplus y_1)$….(4),$A_2=(x_2 \oplus y_2)$…(5) equation shows that addition in GF (4) required solely 2 gates and depth of web is reduced to a minimum of one.

Y1Y2 \ X1X2	0	1	2	3
0	0	1	2	3
1	1	0	3	2
2	2	3	0	1
3	3	2	1	0

Table 5 : Addition for GF(4)

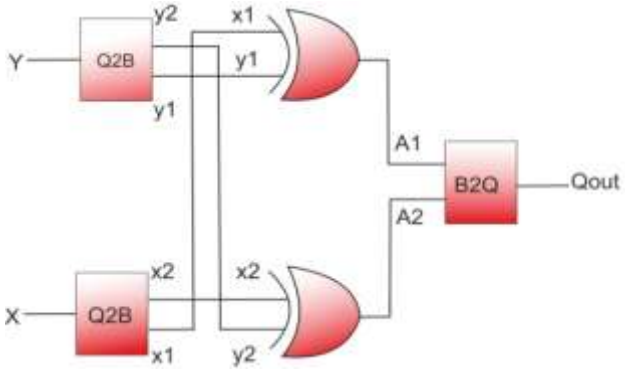
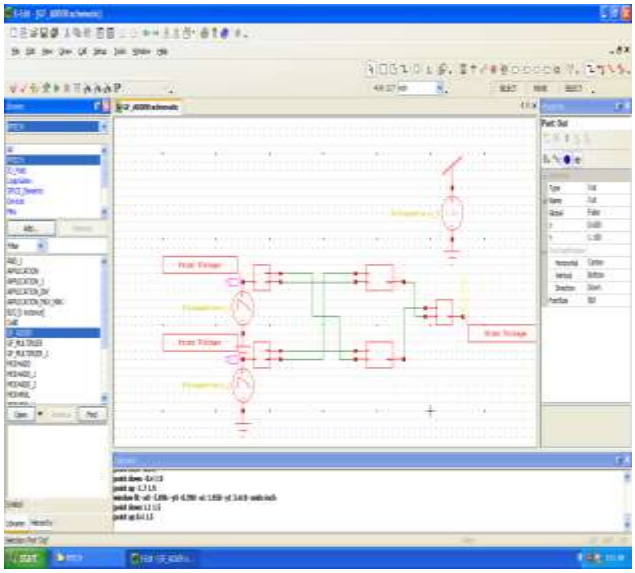


Fig.6: Logic diagram for GF addition

Schematic for Galois field addition:



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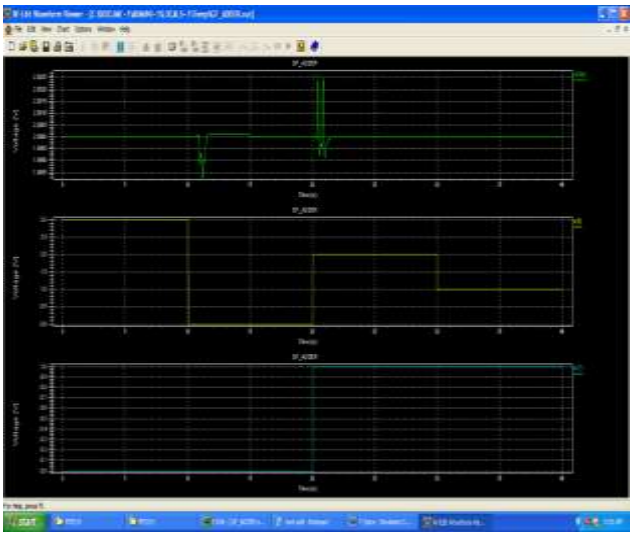
Simulation 5 for Modulo 4 addition:



	X			
Y	0	1	2	3
0	0	0	0	0
1	0	1	2	3
2	0	2	3	1
3	0	3	1	2

Table 6: Multiplication for GF (4)

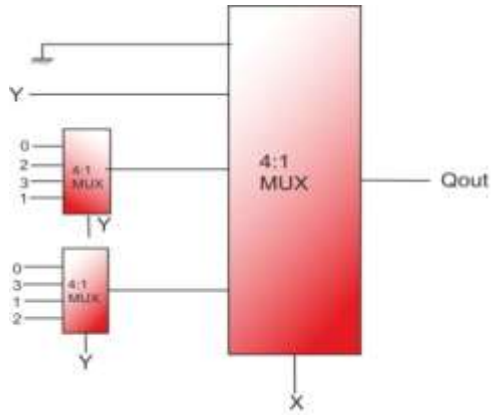
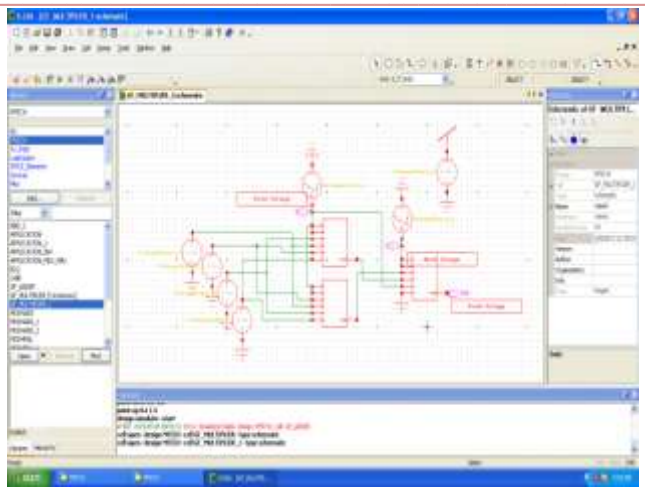


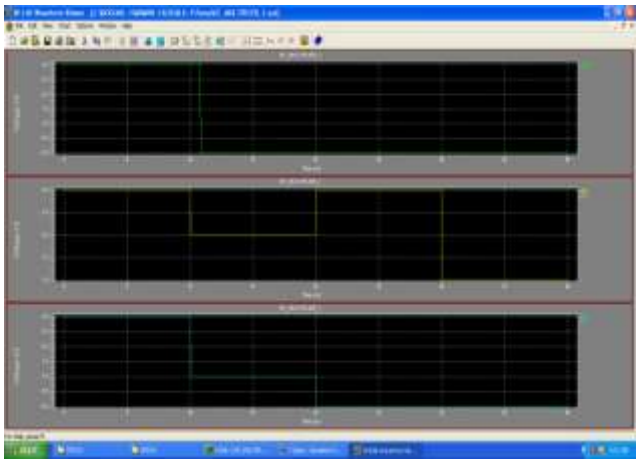
Figure 7: Logic diagram for multiplication in GF (4)

Fig 7 shows the Galois field multiplier factor circuit .During circuit, no would like of quaternary to binary and binary to quaternary conversion. Here, This circuit is that the combination of 3 4:1 mux. The output happy the Evariste Galois field multiplier factor table.

Schematic for Galois field multiplier



Simulation 6 for Galois field Multiplier:



V. Modulo-4 subtraction

Fig.8 shows logic diagram for modulo 4 subtraction y_1 y_2 is subtracted from x_1 x_2. Let, X is quaternary value of x_1 x_2 binary number and Y is Quaternary value for y_1 y_2 binary number then S=(X+4)-Y for X<Y.

Example: if X = 1and Y = 2 then 1 + 4 = 5 - 2= 3, table 7 shows subtraction of y_1 y_2 from x_1 x_2.

Suppose that, x_1 x_2 and y_1 y_2 be the binary representation of quaternary numbers then Subtraction take place.

Suppose that, S_1 and S_2 denote the binary result of subtracting the binary numbers x_1 x_2 and y_1 y_2.

$S_1 = (x_1 \oplus y_1) \oplus (x_2\ y_2)$….. (6)

$S_2 = (x_2 \oplus y_2)$ ……. (7)

	y_1y_2			
x_1 x_2	0	1	2	3
0	0	3	2	1
1	1	0	3	2
2	2	1	0	3
3	3	2	1	0

Table 7: Table for modulo-4 subtraction

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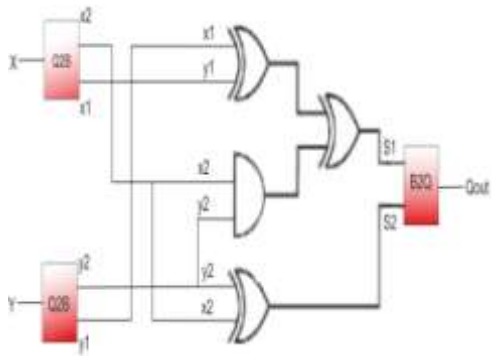
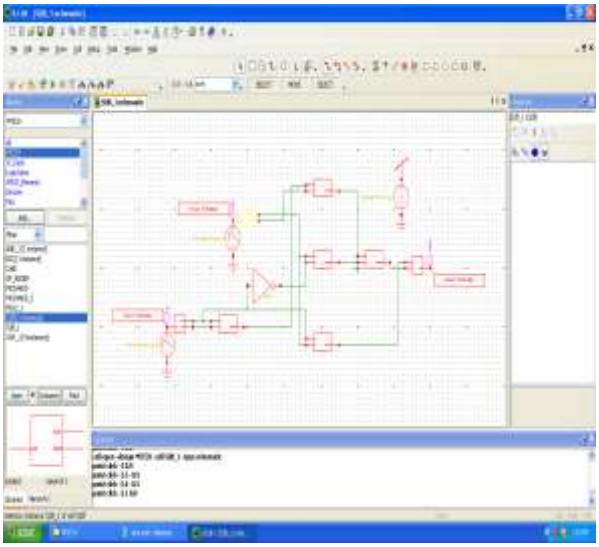
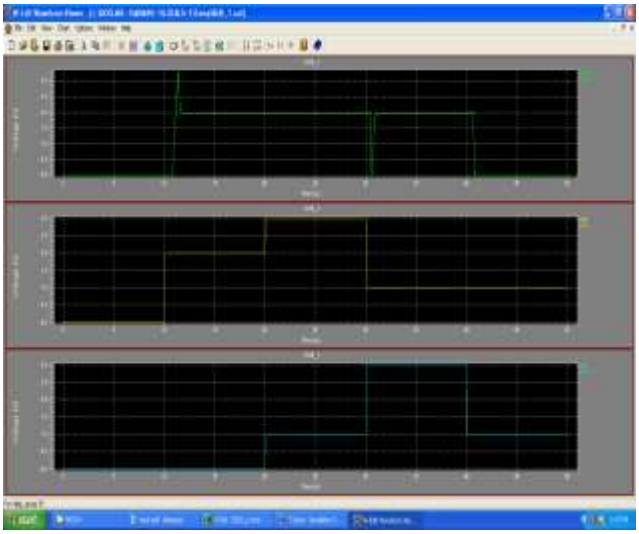


Figure 8: Logic diagram for modulo-4 subtraction

Schemetic for Modulo 4 Substraction:



Simulation 7 for Modulo 4 Subtraction:



VI. Galois field subtraction

Galois subtraction circuit is shown in figure 9. In this circuit, to introduce input and output in quaternary kind. 1st quaternary to binary circuit is connected to the input of the mathematician field subtraction circuit. As shown in fig.9 this circuit contains 2gates one is xor and another one is logic gate. This circuit contains less number of gate as compare to modulo- 4 subtractions . Because of This cut back the depth of interconnection. The output of mathematician field subtraction circuit connected to binary to quaternary converter, output is within the style of quaternary kind.

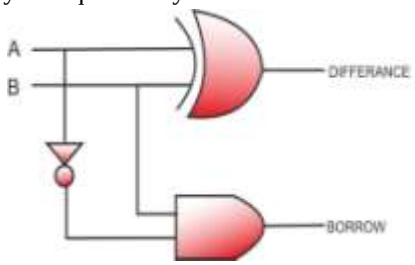
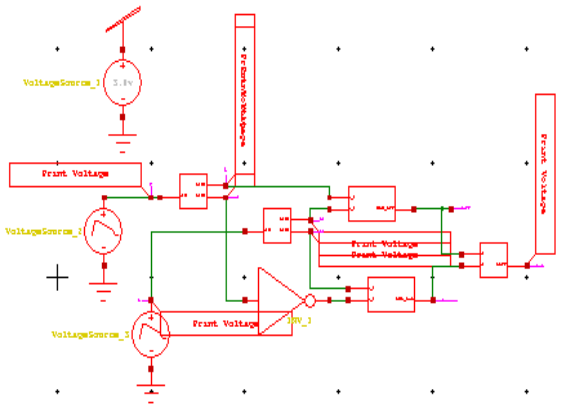
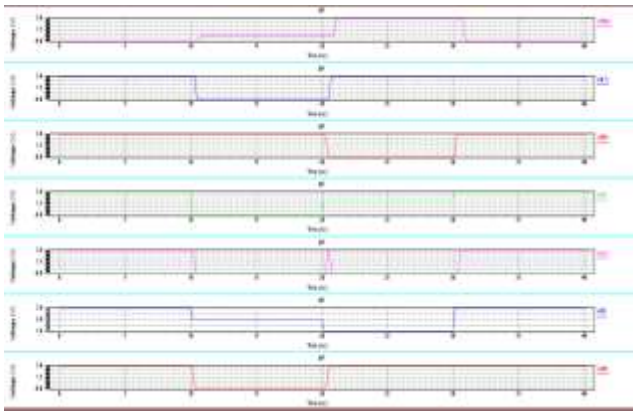


Fig 9**:** circuit diagram of Galois field subtractor

Schematic of Galois field subtraction



Simulation 8 for Galois field subtraction



VII. Result

Simulation result of quaternary to binary and binary to quaternary are shown in simulation 1 and simulation 2. Simulation results of Modulo-4 addition in simulation 3,

modulo-4 subtraction in simulation 7,modulo-4 multiplication in simulation 5 and Galois Field addition in simulation 4,Galois field subtraction in simulation 8 and Galois field multiplier in simulation 6. The below table 7 shows the comparison between modulo-4 and Galois field through power, no. of MOSFETs and current. In galois multiplier we use multiplexer which requires only 40 MOSFETs.

Table 7: Result

NAME	VOLTAGE	NO.OF MOSFET	POWER	CURRENT
MODULO ADDER	3V	94	845.91nW	281.33nA
GALOIS ADDER	3V	76	270.63nW	89.47nA
BINARY TO QUATERNARY	3V	8	420.90 nW	140.3032 nA
QUATERNARY TO BINARY	3V	22	210.89nW	70.2991n A
MODULO SUBTRACTOR	3V	108	1.0872uW	286.1056 nA
GALOIS SUBTRATOR	3V	72	845.8627n W	281.954n A
MODULO MULTIPLIER	3V	82	1.0872uW	286.1909 nA
GALOIS MULIPLIER	3V	40	9pW	3pA

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