Manisha Mankar Department of Electronics Engineering Priyadarshini College of Engineering Nagpur, Maharashtra,India manshree379@gmail.com

Dr.R.V Kshirsagar Department of Electronics Engineering Priyadarshini College of Engineering Nagpur, Maharashtra, India

Prof.M.V.Vyawahare Department of Electronics Engineering Priyadarshini College of Engineering Nagpur, Maharashtra, India

Abstract—Rijndael algorithm is an efficient cryptographic technique consist of different operations in iterative looping approach in order to minimize hardware consideration, with block size of 128 bit, lookup table implementation of S-box. It includes generation of ciphers for encryption and inverse ciphers for decryption by performing four rounds of transformations. This paper presents 192 bit key size cipher. Synthesizing and implementation of the VHDL code is carried out on Xilinx-Project Navigator ISE 14.5 software.

Keywords-Rijndael Algorithm, Key Expansion, Encryption, Decryption, Cryptography.

I. INTRODUCTION

Cryptography is the science of information security which has become very critical in modern computing system to secure data transmission and storage. The need for privacy has become a major priority as widespread use of personal communication devices. The exchange of digital data in cryptography results in different algorithm classified into two cryptographic mechanism: symmetric key in which same key is used for encryption and decryption which are fast and easier to implement than asymmetric key algorithm.

Rijndael algorithm to be introduced in Octomber 2000 replacing the DES algorithm. Rijndael is a symmetric byte oriented iterated block cipher that can process 128 bits using keys with length of 128,192,256 bits.

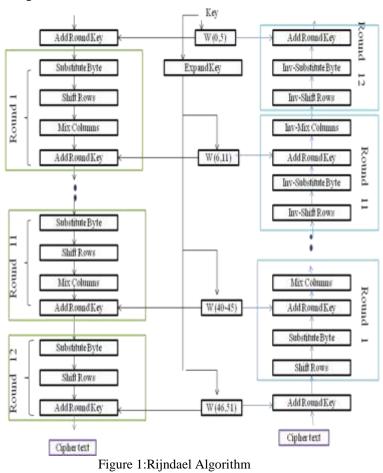
II. RIJNDAEL ALGORITHM

Rijndael algorithm composed of three main parts: Cipher, Inverse Cipher and Key expansion. Cipher converts data in a coded form called Cipher text and inverse cipher converts data back into its original form called plaintext. Key expansion generates a key schedule used in cipher and inverse cipher procedure and composed of specific number of rounds. Number of rounds is dependent on the key length. Rijndael algorithm specifies three encryption: 128 bit, 192 bit, 256 bit. Number of rounds Nr based on key length of Nk words. Nb is constant for all versions.

	J		
Туре	Key Length	Block Size	Number of Rounds
	(Nk words)	(Nb words)	(Nr)
128 Bit	4	4	10
192 Bit	6	4	12
256 Bit	8	4	14

In cipher and inverse cipher, round function is composed of four different byte oriented transformations-Sub Byte, Shift Rows, mix column and Add round key.

Encryption and Decryption process for 192 bit key shown in figure 1.





The data / plaintext will first XOR with initial key and basic round operation repeated Nr-1 times.Nr depends on the key length. Last round will execute only three functions.

A. Subbyte and Inverse Subbyte

In this, each input byte of the state matrix is independently replaced by another byte from look-up table called S-box is replaced with its multiplicative inverse in GF (2^8) with the element $\{00\}$ being mapped onto itself ,followed by affine transformation over GF (2^8) .For decryption ,inverse S-box is obtained by applying inverse affine transformation followed by multiplicative inversion in GF (2^8) shown in figure 2.

S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}				S' _{0,2}	
S _{1,0}	S _{1,1}	S _{1,2}	S _{1,3}	<i>Sbox</i>	S' _{1,0}	S' _{1,1}	S' _{1,2}	S' _{1,3}
S _{2,0}	S _{2,1}	S _{2,2}	S _{2,3}		S' _{2,0}	S' _{2,1}	S' _{2,2}	S' _{2,3}
S _{3,0}	S _{3,1}	S _{3,2}	S _{3,3}		S' _{3,0}	S' _{3,1}	S' _{3,2}	S' _{3,3}

Figure 2: Subbyte Transformation

	-	1	1	2	4	5	î	7	ŝ	ş.	1	4	1	ŧ	4	1		4	ĩ	1	4	1	3	1	ŧ	1	ž.	1	ì.	t.	1	ŧ.	1
1	5	12	IJ	1	2	8	8	C.	12	Ð.	Ŧ	3	ł.	1	a	3	\$	5	ā	ŝ	ő	Ħ	35	if.	慧	1	4	đ	強		\$	17	1
t	5	5	ġ.	ñ.	Ŧ	3	4	R	1	4	É	Ť	k	\$	1	0	1	8	4	3	¢	ħ	8	t	17	族	8	羽	4	я	ŧ	4	1
2	ŝ	ŧ		3	5	5	ŧ	c.	3	ś		fl	1	5	3	5	1	54	h	91	T.	ń	tî.	'n.	M	=	4	8	Ób	4	8	4	1
1	ġ.	ıî.	21	ġ.	5	×.	×.	ŝ	Į.	2	8	2		3	2	3	1	2	à	4	ī	3	19	31	Ц.	76	2	ú.	\$	2	â	11	1
L.	8	5	3	a,	3	12	3	£	2	3	8	ы	3	8	Z	8	4	72	1	ŧ	şi	Æ	督	1	1í	5	şi	x	=	x	藝	10	
5	-	1	1	18	T.	R	11		塘	4	ž	з	41	2	3	đ	1	ŧ	π	46	5	ŧ	ai.	15	#	5	ī	÷	Ŧ	#	22	生	1
£.	6	ŧ	31	4	4	ы	3	E	15	5	1	7	5	2		2	é	98	đ	4	1	*	x	£	a:	ft	64	58	3	*	ŧs	£	1
	8	0	4	Ŧ	÷.	3	3	8	×	*		21	15	Ŧ	5	\$	1	a	1	2	ŧ	#	3	ġ	u.	4	đ	=		a	2	34	
	4	8	13		3	5	4	9	#	8	2	N	8	2	1	3	ŧ	з	圭	11	4		ŧ	±	41	÷	t	ŧ		t	ţz	Ħ	
Į.	6	2	1	*	17	3	-	H	45			-11	8	3	3	10	ŝ	×	τ	11	72	ø	zi	Б	£i	ŵ	8	iř	Ħ	k	ā	ź	ŀ
i	2	-	1	6	8	a.	1	÷	4	6	2	53	2	10	el.	7	1	67	fi	7	7	1ź	Ø	5	8	6	质	权	Qe.	3	3	10	
L	-	8	17	8	8	6	4	11	-	1	-	-	ž	à		8	b.	Ŕ	Ŧ	ħ	4	đ	Ŕ.	ħ	32	5	#	5	ħ	π	ίΰ.	31	
	-	-	*		10	-	-	~					~	-	-	-	¢	1	α	4	3	IJ	17	\$	П	拉	₫	古	5	Π	8	=	
1	2	1	3	2	N	1	H	08	2	đ.	R.	1	+2	¥.	8	à	6	ij	2	3	đ	3	15	4	ħ.	ы	é	h	¥	8	8	x	ŀ
5	ų,	2	Ħ.	荀	4	Ð	f	ł	8	ž	Ŧ	15	Æ	2	1	2		10	4	3	4		ь	б	10	4	10	=	2	ä	5	2	l
	¢	1	9	悠	蔷	ŝ	ŝ.		h	1	Ŧ	ŧ	19	5	2	f	1	-	à	-	-	-	-	-	H	-	-	-		-	-		÷
F	à.	ţ,	21	2	÷.	1	ę.	-	4	15	à	Ŧ	Ń	8	ġ.	\$	f	+	4		n.	-	11	4	-	4	2	148	-	4	4	4	L

Figure 3: Rijndael S-box and inverse S-box

B. Shift Row and Inverse Shift Row

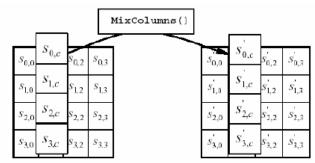
It is a cyclic shift operation, each row is repeated cyclically to the to the left using 0,1,2,3 byte offset for encryption as shown in figure 4, while for decryption to the right.

S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}	S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}
S _{1,0}	S _{1,1}	S _{1,2}	S _{1,3}	S _{1,1}	S _{1,2}	S _{1,3}	S _{1,0}
S _{2,0}	S _{2,1}	S _{2,2}	S _{2,3}	S _{2,2}	S _{2,3}	S _{2,0}	S _{2,1}
S _{3,0}	S _{3,1}	S _{3,2}	S _{3,3}	S _{3,3}	S _{3,0}	S _{3,1}	S _{3,2}

Figure 4: Rijndael Shift Row Operation

C. Mix Column and Inverse Mix Column

In this transformation, each column of the state matrix is multiplied by a constraint fix matrix is shown in figure 5, for i = 0, 1, 2, 3 respectively.



$$\begin{split} S'_{0,c} &= (\{02\}.S_{0,c}) \: Ex\text{-or} \; (\{03\}.S_{1,c} \;) \: Ex\text{-or} \; S_{2,c} \: Ex\text{-or} \; S_{3,c} \\ s'_{1,c} &= S_{0,c} \: Ex\text{-or} \; (\{02\}.S_{1,c} \;) \: Ex\text{-or} (\{03\}.S_{2,c} \;) \: Ex\text{-or} \; S_{3,c} \\ s'_{2,c} &= S_{0,c} \: Ex\text{-or} \; S_{1,c} \: Ex\text{-or} \; (\{02\}.S_{2,c} \;) \: Ex\text{-or} \; (\{03\}. \: S_{3,c} \;) \\ s'_{3,c} &= (\{03\}.S_{0,c} \;) \: Ex\text{-or} \; S_{1,c} \: Ex\text{-or} \; S_{2,c} \: Ex\text{-or} \; (\{02\}. \: S_{3,c} \;) \end{split}$$

Similarly for decryption we compute inverse mix column by multiplying each column of state matrix by constant fix matrix.

 $S_{0,c}^{*} = (\{0e\}, S_{0,c}) \text{ Ex-or } (\{0b\}, S_{1,c}) \text{ Ex-or } (\{0d\}, S_{2,c}) \\ \text{Ex-or } (\{09\}, S_{3,c}) \\ S_{1,c}^{*} = (\{09\}, S_{0,c}) \text{ Ex-or } (\{0e\}, S_{1,c}) \text{ Ex-or } (\{0b\}, S_{2,c}) \\ \text{Ex-or } (\{0d\}, S_{3,c}) \\ S_{2,c}^{*} = (\{0d\}, S_{0,c}) \text{ Ex-or } (\{09\}, S_{1,c}) \text{ Ex-or } (\{0e\}, S_{2,c}) \\ \text{Ex-or } (\{0b\}, S_{3,c}) \\ S_{3,c}^{*} = (\{0b\}, S_{0,c}) \text{ Ex-or } (\{0d\}, S_{1,c}) \text{ Ex-or } (\{09\}, S_{2,c}) \\ \text{Ex-or } (\{0e\}, S_{3,c}) \\ S_{3,c}^{*} = (\{0e\}, S_{3,c}) \\ \text{Ex-or } (\{0e\},$

Mix Columns		S _{0,0}	S _{0,1}	S _{0,2}	S _{0,3}
]	$\mathbf{S}_{1,0}$	$\mathbf{S}_{1,1}$	$\mathbf{S}_{1,2}$	S _{1,3}
		S _{2,0}	S _{2,1}	S _{2,2}	S _{2,3}
		S _{3,0}	S _{3,1}	S _{3,2}	S _{3,3}

Figure 5: Rijndael Mix-column

D. Add Round Key

The output of mix column is XOR-ed with corresponding Round Sub key derived from user key. The Add round key step is same for encryption and decryption.

in ₀	in ₄	in ₈	in ₁₂
in ₁	in ₅	in ₉	in ₁₃
in ₂	in ₆	in ₁₀	in ₁₄
in ₃	in ₇	in ₁₁	in ₁₅

Input Byte

	K _{0,0}	K _{0,1}	K _{0,2}	K _{0,3}	K _{0,4}	K ₀₅
Round keys	K _{1,0}	K _{1,1}	K _{1,2}	K _{1,3}	K _{1,4}	K _{1,5}
	K _{2,0}	K _{2,1}	K _{2,2}	K _{2,3}	K _{2,4}	K _{2,5}
	K _{3,0}	K _{3,1}	K _{3,2}	K _{3,3}	K _{3,4}	K _{3,5}
		•	Ĵ			
Output Bytes	out ₀	out ₄	out ₈	out ₁₂		
	out ₁	out ₅	out ₉	out ₁₃		
	0ut ₂	out ₆	out ₁₀	out ₁₄		
	out ₃	out ₇	out ₁₁	out ₁₅		

Figure 6: Rijndael Add Round key

E. key expansion

The AES key expansion algorithm takes as input a 6-word key and produces a linear array of 52 words. Each word contains 32 bytes which means each subkey is 192 bits long.

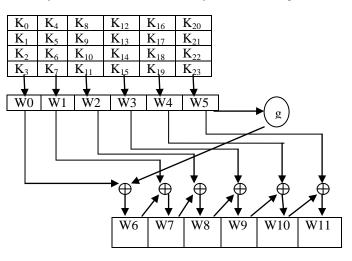


Figure 7: Rijndael key Expansion

III. RIJNDAEL IMPL.EMENTATION

Rijndael algorithm is implemented using VHDL coding in Xilinx ISE 14.5 .Algorithm is tested by block size. 128 bits. only one block data is encrypted at a time, the number of clock cycle necessary to encrypt a single block of data is equal to number of cipher rounds. Cipher feedback is used in encryption and decryption process.

IV.SIMULATION RESULTS

A) Encryption Process Rijndael block length/Plaintext = 128 bits (Nb=4) Key length = 192 bits (Nk = 6) No. of rounds = 12 (Nr = 12) Plaintext:

00112233445566778899aabbccddeeff Key: 000102030405060708090a0b0c0d0e0f1011121314151617 Cipher text:

dda97ca4864cdfe06eaf70a0ec0d7191

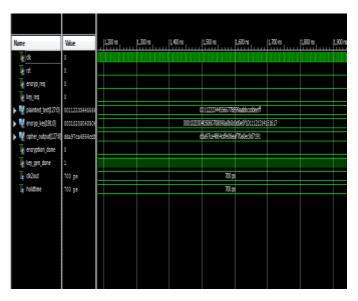


Figure 8: waveforms of Encryption process



Figure 9: RTL Schematic of Encryption process

B) Decryption Process Rijndael block length/Plaintext = 128 bits (Nb=4) Key length = 192 bits (Nk = 6) No. of rounds = 12 (Nr = 12) Input/Cipher text: dda97ca4864cdfe06eaf70a0ec0d7191 Key: 000102030405060708090a0b0c0d0e0f1011121314151617 Plaintext: 00112233445566778899aabbccddeeff

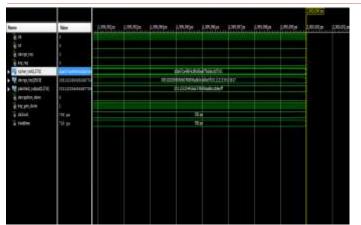


Figure 10: waveforms of Decryption process

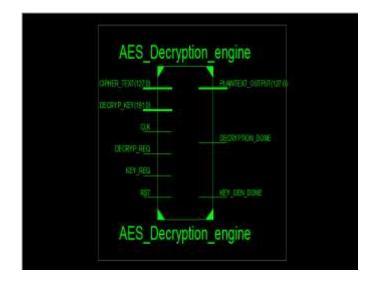


Figure 11: RTL Schematic of Decryption process

V.CONCLUSION

Rijndael Algorithm is an iterative symmetric block cipher that can process data blocks of 128 bits and key lengths of 128,192,256 bits. In this paper, 128 bit block and 192 bit key is used.VHDL code is developed and results are verified using Xilinx ISE 14.5 Simulator both for encryption and decryption process.

REFERENCES

- Bin Liu, Student Member, IEEE, and Bevan M. Baas, Senior Member, IEEE; "Parallel AES Encryption Engines for Many-Core Processor Arrays", IEEE TRANSACTIONS ON COMPUTERS, VOL. 62, NO. 3, MARCH 2013
- [2] Kamalika Datta, Vishal Shrivastav, Indranil Sengupta, Hafizur Rahaman "Reversible Logic Implementation of AES Algorithm"8th international conference on design & technology Integrated systems in nanoscale era,978-1-4673-6040-1/13/\$31.00,2013 IEEE.
- [3] N.Anitha Christy and P.Karthigaikumar "FPGA implementation of AES algorithm using Composite Field Arithmetic"International conference on devices circuits and systems,978-1-4577-1546-4/12/\$26.00,2012 IEEE
- Hong Trang;Nguyen Van Loi;"An efficient FPGA implementation of the advanced Encryption Standard algorithm"978-1-4673-0309-5/12,2012,IEEE.
- [5] Nabihah Ahmad, N.; Hasan, R.; Jubadi, W.M; "Design of AES S-Box using combinational logic optimization", IEEE Symposium on Industrial Electronics & Applications (ISIEA), pp. 696-699, 31.00,2010 IEEE.
- [6] Marcelo Barcelos, Ricardo Reis "An IP of an Advanced Encryption Standard For Altera Devices", IEEE Symposium on Integrated circuits and systems Design (SBCCI'02)0-7695-1807-9/02, 2002, IEEE.
- [7] Hrushikesh S.Deshpand, Kailash J.Karande, Altaaf O.Mulani "Efficient Implementation Of AES Algorithm on FPGA" International Conference on Communication and Signal Processing, April 3_5,2014, IEEE.
- [8] Girish Kumar P,Mahesh Kumar "Implementation of AES algorithm using verilog"International Journal of VLSI and Embedded Systems,vol-4,Article 05090;june 2013.
- [9] Hrushikesh S.Deshpand, Kailash J.Karande, Altaaf O.Mulani "Efficient Implementation Of AES Algorithm on FPGA" Progress In Science in Engineering Reaserch Journal ,PISER 11,vol.02,ISSN 2347-6680 (E),2014.
- [10] Vijaya Kumar.B, T.Thammi Reddy "Fpga Implementation of High speed AES Algorithm For Improving The System Computing speed" International Jouranal of Computer trends and Technology(IJCTT)-VOLUME 4 Issue 9-Sep 2013.
- [11] J. Nechvatal et.al., Report on the development of Advanced Encryption Standard, NIST Publication, Oct,2000.
- [12] J. Daemen and V Rijmen, "AES Proposal:Rijndael", AES Algorithm Submission, September 3, 1999.
- [13] National Institute of Standards and Technology (NIST), Data Encryption Standard (DES), National Technical Information Service, Spring field, VA 22161, Oct. 1999.
- [14] N Radhika, Obili Ramesh, Priyadarshini, "Design and Verification of Area-Optimized AES Based on FPGA using verilog HDL"International Journal of Engineering Trends and Technology-volume 4 Issue9-Sep 2013.