

A Survey on Interlaken Protocol for Network Applications

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Abstract— As technology evolves the need of high speed, high-bandwidth and reliable interface is a prime requirement of any system. As a result of such needs CISCO systems comes up with a solution under the name of “Interlaken”. Interlaken is an interconnect protocol optimized for high-bandwidth and reliable packet transfer. It is a narrow, high-speed channelized chip-to-chip interface, which takes advantages of two dominant high-speed chip-to-chip interface protocols for networking applications such as XAUI(Roman numeral X, meaning ten, and the initials of "Attachment Unit Interface") and SPI4.2 (System packet Interface level 4, phase 2). It works as an interface between 1st and 2nd layer of OSI model, i.e. PHY layer and DATA LINK layer devices.

Keywords- Interlake; XAUI; SPI4.2; SerDes; FR4; SONET.

I. INTRODUCTION

The continuous growing demand for high-speed and reliable interfaces has been a driving force in the development of new designs of interconnects to support intense need of high-speed communication technology. As a by-product of this need numerous protocols were proposed and developed. Here is a short review of evolution.

Components with gigabit-scale throughput traditionally have data buses running about 100Mbps per pin. Differential signaling technology has increased this bandwidth almost ten times, to about 800Mbps per pin pair, which enables components with throughput on the order of 10Gbps. New serial technology with clock and data recovery has increased band width another ten times to about 6Gbps per pin pair, which enables components with multiple of 10Gbps streams.

Fig. 1 shows the graph of technology evolution and its maximum speed achievement.

The Interlaken protocol is created to take advantage of this latest technology for a high-speed, robust, versatile interface for packet transfer between components within communication systems [2].

There are two dominant high-speed chip-to-chip interface protocols for networking applications XAUI and SPI4.2. In the following sections brief information regarding these dominant protocols are given.

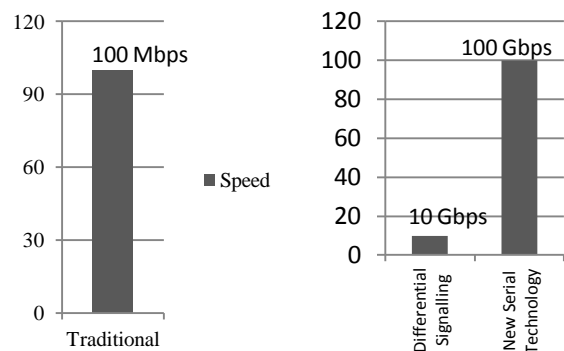


Fig. 1. Technology Evolution

II. DOMINANT HIGH-SPEED PROTOCOLS

[1] SPI4.2 (System packet Interface level 4, phase 2)

It is published by the Optical Internetworking Forum in 2003 and designed to be used in systems that supports OC-192/SONET (Synchronous Optical Networking) interfaces and is sometimes used in 10 Gigabit Ethernet based systems.

According to [3], System Packet Interface 4 Phase 2 (SPI4.2) is a protocol used for data transfer between link layer and physical layer. It is an interface for packet and cell transfer between a physical (PHY) layer device and a link layer device, for aggregate bandwidths of OC192 ATM and Packet over SONET (POS), as well as for 10 Gb/s Ethernet applications.

SPI 4.2 is a packet based high speed protocol. Its basic function is to intelligently multiplex the data coming from

link layer, to the SPI 4.2 bus. The receiver is an intelligent de-multiplexer that de-multiplexes the data coming from the SPI 4.2 bus into the respective port's FIFO.

The input to the transmitter is 64bitdata at 155.50 MHz rate. The output on SPI 4.2 bus is 311 MHz DDR 16bitdata. Hence the input data rates are matching with the output data rates for the transmitter design / architecture.

Following are some highlighting points of SPI4.2 [3]:

- Point-to-Point connection (i.e. between single PHY & single Link Layer device),
- Support for 256 ports,
- Transmit & receive data path is 16 bit,
- Channelization, programmable burst size & per-channel backpressure,

[2] XAUI(Zowie)

XAUI, the 10 Gigabit Attachment Unit Interface, is a technical innovation that dramatically improves & simplify the routing of electrical interconnections. It is developed by IEEE 802.3ae 10 Gigabit Ethernet Task Force. And it delivers 10 Gb/s of data throughput using four differential signal pairs in each direction. XAUI is a standard for extending the XGMII (10 Gigabit Media Independent Interface) between the MAC and PHY layer of 10 Gigabit Ethernet (10GbE). XAUI is pronounced "zowie", a concatenation of the Roman numeral X, meaning ten, and the initials of "Attachment Unit Interface"[4].

XGMII provides a 10 Gb/s pipeline, the separate transmission of clock and data coupled with the timing requirement to latch data on both the rising and falling edges of the clock results in significant challenge in routing the bus more than the recommended short distance of 7 cm. For this reason, chip-to-chip, board-to-board and chip-to-optical module applications are not practical with this interface. Consequently, the XGMII bus puts many limitations on the number of ports that may be implemented on a system line card.

To overcome these issues, 10 Gigabit Ethernet Task Force developed the XAUI interface. XAUI is a full duplex interface that uses four self-clocked serial differential links in each direction to achieve 10 Gb/s data throughput. Each serial link operates at 3.125 Gb/s to accommodate both data and the overhead associated with 8B/10B coding.

Following are some highlighting points of XAUI interface:

- It is a narrow 4-lane interface, offers long reach,
- Independent transmit and receive data paths,
- Differential signaling with low voltage swing,
- Utilization of 8b/10b encoding,

- It suits a variety of implementations like FR4 on PCB, backplanes & cables,
- As a packet-based interface it lacks channelization & flow control.

Interlaken is targeted to achieve advantages of these two dominant chip-to-chip interface protocols for networking application.

III. INTERLAKEN PROTOCOL

A. Design Goals

Following are the design goals taken into consideration while designing Interlaken Protocol.

1) *Bandwidth Range*: Interlaken should not have specific upper limit. It is primarily targeted for 10Gbps to 100Gbps connections.

2) *Scalability*: The scalability in the case of Interlaken is achieved by its ability to run over a varying number of lanes. The following two parameters determine the connection bandwidth:

a) *Number of serial lanes in the interface*[2]: The effective bandwidth of Interlaken protocol corresponds to the number of lanes on which it is working. And the number of lanes can vary according to the availability of the system. For example, an eight-lane interface can carry twice the payload of a four-lane interface running at the same per-lane speed, as shown in Fig. 2

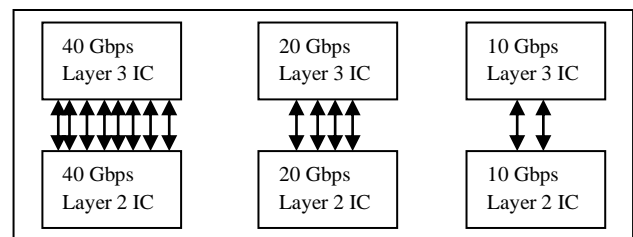


Fig. 2 Effective Bandwidth Scales with the Number of Lanes [2]

b) *Frequency of each lane*[2]: Since bandwidth can be increased by either adding more lanes or by increasing the bit rate per lane, Interlaken is a very scalable interface. For example, as shown in Fig. 3, an IC with a capacity of 40 Gbps can connect to other 40 Gbps ICs using eight lanes, to 20 Gbps ICs using four lanes and to 10 Gbps devices using two lanes. Thus, ICs of different capacities can be made to

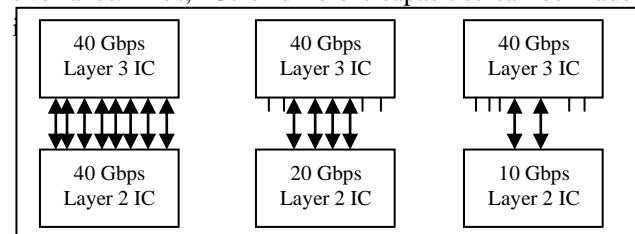


Fig. 3 Flexibility of Interlaken Allows ICs of Different Capacities to Connect [2]

3) *Flexibility*[2]: Interlaken should have ability to run over a varying number of lanes which will provide high flexibility in component interconnects. ICs with different capacities in a single physical interface can be split up into multiple lower-speed physical interfaces. For example, as shown in Fig. 4, eight physical lanes can be organized as a single 40 Gbps interface, two 20 Gbps interfaces, or four 10 Gbps interfaces.

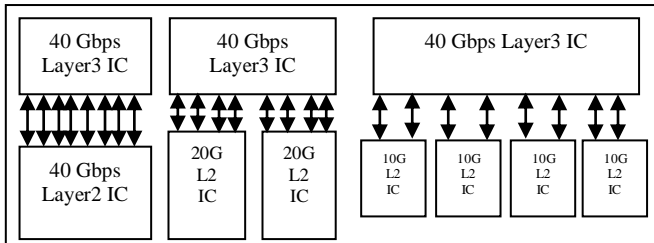


Fig. 4 Flexibility of Interlaken Allows Multiple Connection Options [2]

4) *Channelization*: As application varies the number of channels available for communication will vary. So to support varying number of channels Interlaken should have support to operate on different number of channels available for the particular application. This characteristic is known as channelization. For example, different channels can be used to carry traffic destined for separate physical ports, logical SONET channels, or traffic priority flows.

Interlaken is designed to natively support 256 channels, extendable up to 64 K channels, by using a dual-use channel-field extension that meets the requirements of most applications.

5) *Resiliency*: Resiliency in Interlaken protocol is maintained by the use of strong cyclic redundancy check (CRC) and technology known as scrambling. The health of each serial link is continuously and transparently monitored.

B. Basic Concept of Interlaken protocol

The basic structures which define the Interlaken protocol are, the Data Transmission Format and Meta Frame [1]. Data Transmission Format is transmitted over number of lanes available for communication and this is obtained by striping the main data frames to be transmitted. This striped data is called as burst. Each burst is bounded by two control words, one before and one after. Packet data is transmitted sequentially by means of one or more bursts.

The Meta frame is designed to carry control related information of the communication. It contains a set of four unique control words, which are defined to provide lane alignment, scrambler initialization, and clock compensation.

[3] Highlights of Interlaken Protocol

Interlaken is a narrow, high-speed channelized chip-to-chip interface. It is characterized by the following features:

- Support for 256 communications channels, or up to 64K with channel extension.
- A simple control word structure to delineate packets, similar in function to SPI4.2.
- A continuous Meta Frame of programmable frequency to guarantee lane alignment synchronizes the scrambler, perform clock compensation, and indicate lane health.
- Protocol independence from the number of SerDes lanes and SerDes rates.
- 64B/67B data encoding and scrambling.
- Performance that scales with the number of lanes.

IV. EXISTING WORK

Initially White Paper of Interlaken Technology was proposed by Cisco System Inc., Cortina Systems Inc., and Silicon Logic Engineering Inc. on 08 March 2007 [2]. Later numbers of revisions of Interlaken Protocol were released for example revision 1.1, revision 1.2 on 07 October 2008[1], etc. Implementation history of Interlaken Protocol is given in TABLE I [8].

TABLE I IMPLEMENTATION HISTORY

Serial No.	Corporation	Hard IP/Soft IP	Device
1	Xilinx Inc.	Hard IP	Virtex-5, Virtex-6, Virtex-7 & Kintex-7
2	Altera Corporation	Hard IP	Stratix-IV GX & Stratix-V GX
3	Rockfish Technology	Soft IP	-
4	Open-Silicon	Soft IP	-
5	Flowgic	Soft IP	-
6	Tamba Networks	Soft IP	-
7	Xelic Inc.	Soft IP	-
8	GDA Technologies	Soft IP	-
9	More Than IP	Soft IP	-
10	Smart DV	Soft IP	-
11	Achronix	Hard IP	Speedster22i

According to current market survey there are number of IPs of Interlaken Protocol are available as depicted in Table I. The feature of these available IPs are discussed in the following few paragraphs.

1) Xilinx Inc.: Xilinx hard IPs of Interlaken Protocol are included in their FPGAs such as Virtex-5, Virtex-6 & Virtex-7 are based on Sarance Technologies intellectual property [5].

Xilinx's device Kintex Ultra Scale KU040 FPGAs which supports Interlaken Protocol IP is currently in volume production which is implemented using 20nm technology.

These ICs will be available in the estimated one year time to market [16].

2) Altera Corporation: A Hard IP of Interlaken protocol developed by Altera Corporation implements Interlaken Protocol Specification 1.2. And it comes with Stratix-IV GX & Stratix-V GX devices [6].

3) Rockfish Technology: A soft IP of Interlaken Protocol developed by Rockfish Technology supports all the extensions published [7].

4) Open Silicon: Interlaken IP of Open Silicon is build on the channelization feature of SIP 4.2 and number of I/O pins are reduces by using high-speed SerDes technology of XAUI [8].

5) Flowgic: An efficient implementation of Interlaken Protocol Specification 1.2 is Flowgic Interlaken IP core. The advantages of this core are such as low gate count, customization options, etc.[9]

6) Tambe Network: Tamba Networks comes up with a configurable Interlaken IP which can support Interlaken Protocol Specification 1.2 and Interlaken Look-Aside Protocol Specification 1.1.[10]

7) Xelic Inc.: Xelic Inc’s Interlaken core (XCI4FIC) supports both segment mode and packet mode of transmission. And it is also configurable number of lanes [11].

8) GDA Technologies: GDA Technology is currently working on development of Interlaken IP and its functional verification [12].

9) More Than IP: More Than IP’s Interlaken IP supports Interlaken Specification 1.2 and implements a programmable number of SerDes lanes from 4 to 24 [13].

10) Smart DV: Smart DV developed a Verification IP of Interlaken Protocol which supports all the specifications and can work with Systemverilog, Vera, SystemC, etc.[14]

11) Achronix: Achronix has developed a Hard IP of Interlaken Protocol which comes with the Speedster22i device which is designed using Interlaken Specification 1.2.[15]

The characteristics of various IPs of Interlaken Protocol is summarized and compared in TABLE II

TABLE II SUMMARY OF CHARACTERISTICS OF VARIOUS IPS FROM VARIOUS ORGANIZATIONS

Parameter Organisation	Each Lane Operating At	Number of Channel Support	Full packet mode/Segment mode	Set/Reset Scrambler	SerDes width	Devices Supports
FLOWGIC	10.3125Gbps	256	yes/yes	yes	32bit	-
Tamba Network	9.375Gbps	32	Yes/-	-	-	stratix 4,5 virtex6,7
Altera 50G Interlaken MegaCore	6.25Gbps	8	yes/yes	-	-	stratix 5
Open Silicon	3.125Gbps to 25Gbps	1 to 48	yes/yes	-	8, 10, 16, 20, 32, 40, or 64 bits	-
More Than IP	10.3125Gbps	4 to 24 in steps of 4	yes/yes	-	-	stratix 5
Smart DV	-	-	-	configurable	8,10,16,20,32,	-
Achronix	10.3125Gbps	256	yes/yes	-	-	Speedster22i
Xelic	-	256	yes/yes	-	-	-

V. CONCLUSION

According to the survey, if we compare the available interconnect protocols and Interlaken Protocol, Interlaken offers many advantages in scalability, reduced pin count, and data integrity. Numerous IPs are developed based on various definitions and various characteristics as mentioned in TABLE II. It is applicable for wide range of application because of channelization, scalability and flexibility. As there

are number of IP cores available it is easy and cost effective to adopt new technology. Because of these remarking advantages Interlaken will be the obvious choice for next-generation communications equipment.

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