HDL Implementation of Vending Machine by KCPSM3 Processor

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Abstract:- The objective here to design vending machine controller which accepts money as input in any sequence and delivers the required product when the required amount has deposited and it also gives back the change. Here the additional facility is provided for our users. It is possible to withdraw the user deposited money in between if the customer wishes to pressing a specified button PUSH button.

Keywords:- verilog HDL kcpsm3,Xlinx simulator software

I. INTRODUCTION

A vending machine is a machine that provides different items even diamonds and platinum Jewellery to the customers, after the vendee credits the money into the machine. This process would get not be consume time at all. The machine would get all the details on screen. It is necessary to make the system as more reliable with efficient algorithm so the microprocessor controlled vending machine was would be replaced by the FPGA because previous one is inefficient compared with the FPGA. For the processing we have made an attempt to vend products of different products with price. The machine will able to give the change back depends on the amount of money deposited by user. This has the feature of the cancellation of the product and gives money back.

II. DESIGN OBJECTIVES

To design the reliable vending machine the required features are

- 1. Sell three types of products and accept two types of coins (Re2, Re5)
- 2. Give the change after successful trade
- 3. Return the change if the trade fails
- 4. Small in size and acceptable power consumption.

BLOCK DIAGRAM OF VENDING MACHINE

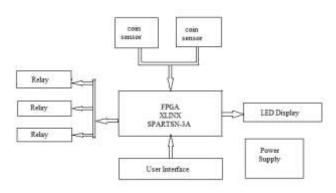


Fig. block diagram of vending machine

The machine can accept coins of two rupees and five rupees in any possible sequence. There is a coin slot which is connected to FPGA. User interface used coins dispense and product dispense. Relay is control the product dispatch. The programs has written on KCPSM3 processor and download into the Spartan-3A kit by using ELBERT configuration for selecting product and coin sum, balance and it will be displayed on LCD.

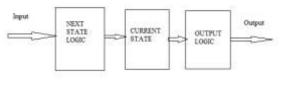
FINITE STATE MACHINE

A sequential circuit can be converted into a state machine using state diagram. In a state machine the circuit output is defined in a set of states. There is a state register to hold sate of a machine and the next state logic to decode the next state. There are two types of state machines.

- 1. MOORE
- 2. MEALY

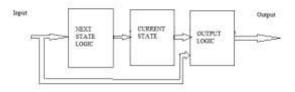
MOORE MACHINE

In this the output state is totally depends on the present state.



MEALY MACHINE

In the output depends on input as well as present state.



COIN DESCRIMINATOR

When the coin is inserted into slot, it falls vertically and first hits an anvil, rolling down a short ramp about few centimeters. The sensors are located along this path, and their signals have to be pressed to decide the coin is good or not before it reaches the ramp, where the coin is driven to the storage or return to the customer. The role of the sensor is to measure the physical properties of the coin, such as dimensions, conductivity, permeability etc., here dimension is measured directly all others are measured indirectly.

BLOCK DIAGRAM FOR COIN DESCRIMINATOR

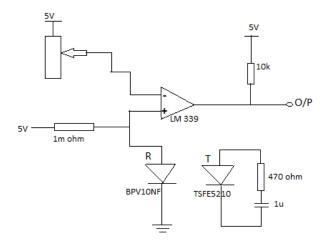


Fig. circuit for coin discriminator

RELAY

Relay is designed to control the load the load maybe motor or any other type. The operation can be controlled by OFF/ON of the relay. These OFF/ON conditions based on Q1 & Q2 transistors in the circuit. Relay connected to the collector terminal of Q2 transistor. Relay is am electronic device which has 3 pins. They are COMMON, NORMALLY OPEN (NO), NORMALLY CLOSE (NC).

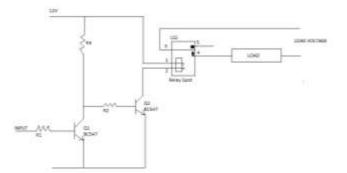


Fig. circuit diagram for RELAY

The relay common pin is connected to the supply. The **NO** pin connected to load. When the high pulse signal given to

Q1 transistor which will be conducting and shorts the collector and emitter terminal. Then zero signal will given to the Q2 transistor which will make relay OFF.

The low pulse is given to the transistor Q1, transistor Q1 turned OFF. Now the 12V is given to the base of transistor Q2 so the transistor conducting and the relay turned ON. Hence the common terminal and NO terminal of relay are shorted. Now load gets supply voltage through relay.

- **COM** -moving part of switch
- NC com connected to this when relay is off
- NC com connected to this when relay is on

KCPSM3 PROCESSOR

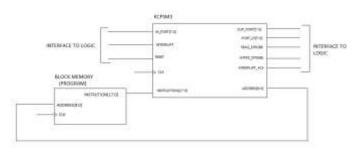


Fig. KCPSM3 PROCESSOR

KCPSM3 is a very 8 bit microcontroller primarily for SPARTAN 3 devices. It is non time critical state machine hence it is the name of (K) constant coded programmable state machine. One most exciting feature of this KCPSM3 is totally embedded into the device and requires no external support. Although it could be used for processing of data. It is most likely to be employed in applications requiring a complex.

Xilinx - Spartan -3A FPGA

USB interface provides the easy and faster configuration download to the on board SPI Flash. ELEBERT features a stable clock source which is delivered from on board configuration controller. ELEBERT incorporates LED'S and switches for a curious user to get started. This is the world's lowest cost I/O optimized FPGA's. the advance feature in this include unique device DNA serial number, support for 26 I/O standards, enhanced multi booth capability, dual power management modes and dynamic input delay.

Xilinx is driving the multiple domain-optimized platforms for highly efficient and optimal design solutions, instead of forcing inefficient, one size fits all solutions on significantly varying application requirements.

III. DESIGN METHODOLOGY

At initial state of the machine the RESET button is pressed, then the machine will be ready for the user to select his/her product. The machine can accept only two types of coins (Rs 2, Rs 5). For example the user selects Rs 2 as input, the machine will firstly check whether the product is available or not. When the desired amount is inserted the machine will go to the product state and will delivered at the product output. If product is not available in the machine the machine control unit will get reset automatically. And this has the additional feature of withdrawing the request if the user does not want to the product. When the cancel button is pressed then the inserted money will be returned to the user through the return output. The money count signal is used for calculating the total money inserted into the machine. If the money is inserted more than the product money the extra change will be return to the user.

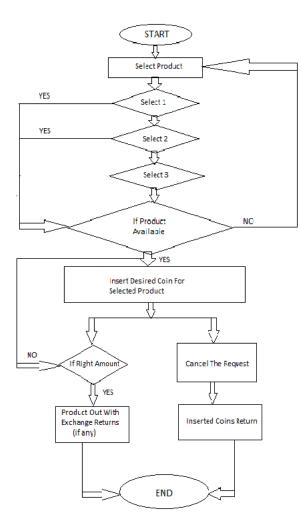


Fig. Design methodology

IV. RESULTS & ANALYSIS

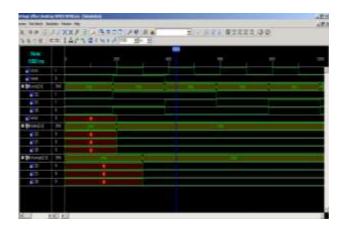


Fig. simulatation waveforms

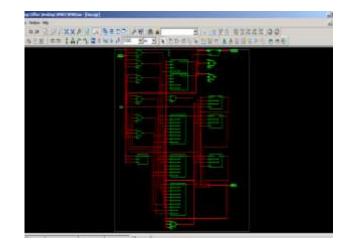


Fig. RTL Schematic diagram

V. CONCLUSION

Here we can observe that FPGA based vending machine will gives fast response, low power consumption and easy to use an ordinary person. Our result shows the FPGA based machine increases the efficiency and accuracy of vending machine and having the flexible algorithm and reliable for more number of products, and low cost compared with the micro processor based vending machine. And also we can monitor the vending machine by main frame computer.

REFERENCES

- [1] Ana Monga, Balwinder Singh, "Finite State Machine based vending machine controller with Auto Billing Features" in 2012 journal of VLSI Design & Communication Systems.
- [2] Shatrughan Modi, Dr. Seema Bawa, "Automated Coin Recognition System using ANN" in 2010

international	journal	of	Computer
Applications(0975-8887).			

- [3] Biplab Roy, and Biswarup Mukherjee, "Design of coffee vending machine using single electron devices" in 2010 International Symposium on electronic design of system pp-38-43.
- [4] K.P. Subramoney, Prof. G.P.Hancke," A Secure Web Service For Electronic Payment Vending in South Africa " in 2007 the Third International Conference on Web Services (ICWS), New York, USA, pp 1-9.
- [5] Muhammad Ali Qureshil, Abdhul Aziz1, Hafiz Faiz Rasool," Design and Implementation of Automatic Train Ticketing System Using Verilog HDL"@ ICCIT, pp-707-712.
- [6] Kaushal Mahesh Ambani, Harshil Mayur Gandhi, Priyank Jayesh Shan, "Automatic Ticket Vending Via Messaging Service(ATVMS)" in March 2012 International Journal of Computer Applications(0975-8887) volume 42 – No.17, pp-25-29.