Low power FIR filter design using Graph Based Algorithm

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Abstract:-Digital filters are a very important part of DSP. In fact, their efficient performance is one of the key reasons that DSP has become so popular. In this paper, we designed an FIR filter using graph based algorithm. Common Sub expression Elimination (CSE) algorithm has a drawback that, it defines the constant in number representation such as CSD (or) MSD, binary. But, when implementing Graph Based (GB) algorithm, it is not restricted to any number of representation of constant. By reducing the height of the tree structure, the numbers of adders are reduced. It reduces the area and power than existing one. The implementation of GB Algorithm is done by Verilog.

Keywords: *Finite Impulse Response (FIR) filtering, Common Sub expression Elimination (CSE) algorithm, Graph Based (GB) algorithm.*

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I. Introduction

Digital filter is the filter which arises due to its operation on discrete time signals.The term finite impulse response arises because the filter output is computed as a weighted, finite term sum, of past, present, and perhaps future values of the filter input, i.e.,

$$y[n]=\sum_{k=0}^{N} h[k]x[n-k] \text{----------(1)}$$

The implementation of FIR filter requires three basic building blocks-multiplication, addition and signal delay. We also need to be able to store filter coefficients in memory. In DSP system, multiplier must be fast and must have sufficient precision to support the desired application. If the multiplier is not fast, throughput gets affected. In an FIR filter additions are required in combinations with multiplications, hence DSP microprocessors feature multiply accumulate (MAC)units. Adders generally operate with just two input at a time. The unit delay provides a one sample signal delay. A sample value is stored in a memory slot for one sample clock cycle and then made available as an input to the next processing stage. An M-unit delay requires M-memory cells

An FIR filter of order N is characterized by N+1 coefficients and, in general, require N+1 multipliers and N two-input adders. Structures in which the multiplier coefficients are precisely the coefficients of the transfer function are called direct form structures.

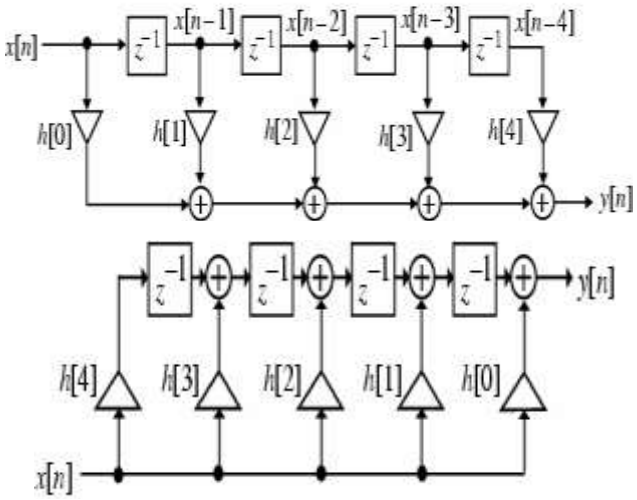


Fig.1 Direct Form Structure and Transpose form of direct structure

The transpose of the direct form structure shown earlier is indicated above. Both direct form structures are canonic with respect to delays.

The core of FIR filter design is the multiplication of a variable by a set of constants. The optimization of these multiplications can lead to improvements in various design parameters like area or power consumption. This problem is known as a multiple constant multiplication problem (MCM).

Graph based algorithms and common sub-expression elimination (CSE) technique are two methods to tackle the MCM problem. Multiplier free design of MCM is achieved with the help of shift and adds operation which shares the common sub operations using canonical signed digit (CSD)

coding and common sub expression elimination (CSE) to minimize the adder count of MCM. As a simple example, consider the constant multiplication 30914x.their decomposition in binary are listed as follows:

30914x=(111100011000010)binx=x<<14+x<<13+x<<7 +x<<11+x<<12+x<<6+x<<1.

II. COMMON SUB-EXPRESSION ELIMINATION (CSE)

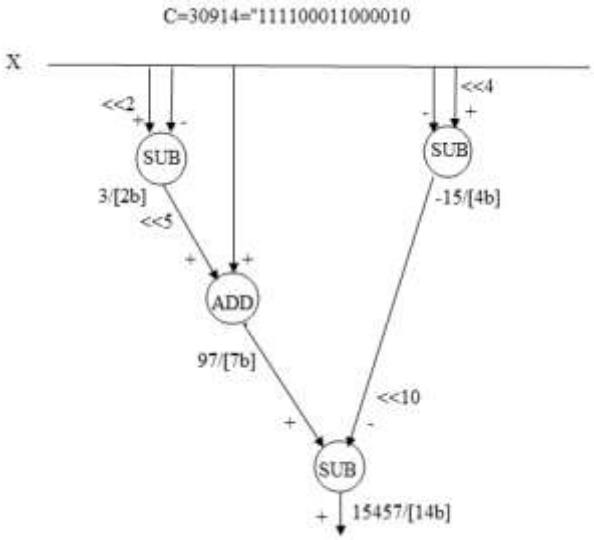


Fig.2 Common Sub-expression Elimination (CSE)

An algorithm for efficient solution for the multiple constant multiplication problems.

The idea of CSE can be demonstrated on a FIR filter design. The optimization procedure targets the minimization of the multiplier block area. After expressing the coefficients in a canonical signed digit (CSD) format in order to reduce the total number of nonzero bits(thus also the addition/subtractions necessary),an add shift expansion is performed. The goal of CSE is identify the bit patterns that are present in the coefficient set more than once. Since it is sufficient to implement the calculation of the multiple identical expressions only once, the resources necessary for these operations can be shared.

The CSE algorithm consists of four steps. First, all possible implementations of constants are extracted from the nonzero digits of the constants defined under a number representation: binary, CSD, or MSD. Then, the implementations of constants are represented in terms of a Boolean network. Third, the bit-level area optimization problem is formalized as a 0-1 ILP problem with a cost function to be minimized and a set of constraints to be satisfied. Finally, a set of operations that yields the minimum area solution is obtained using a generic 0-1 ILP solver.

III. GRAPH BASED (GB) ALGORITHM

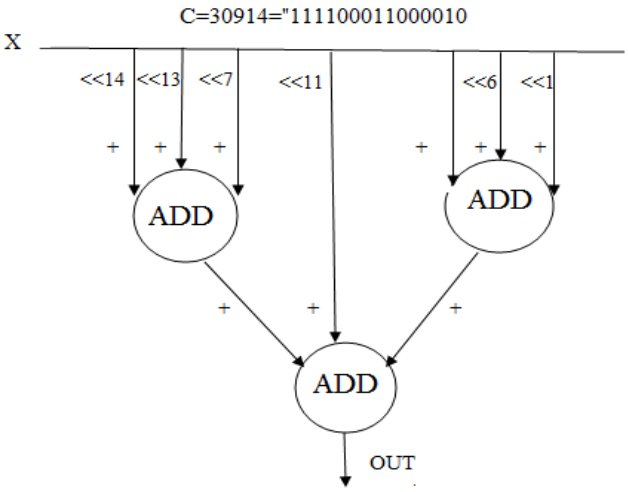
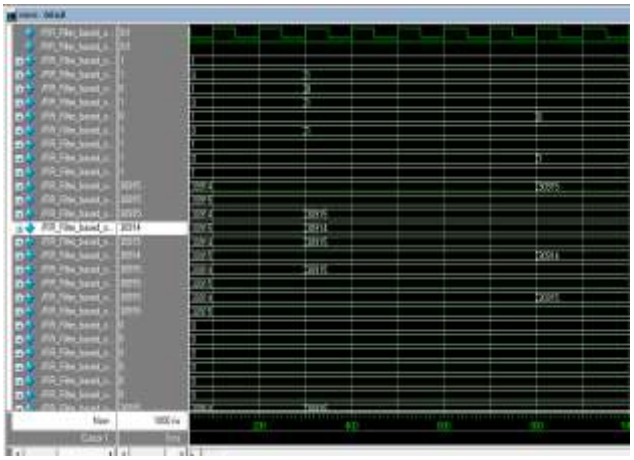


Fig .3.Graph Based Algorithm

The graph based algorithm which is introduced to reduce the addition in shift adds implementations of constant multiplications. These methods are not limited to any particular number representation and consider a large number of alternative implementations of a constant yielding better solution than the shift add implementation of constant multiplication.

IV. SIMULATION AND SYNTHESIS REPORT

We performed the simulation and synthesis of Common Sub expression Elimination (CSE) and Graph Based (GB) algorithm.



(a)

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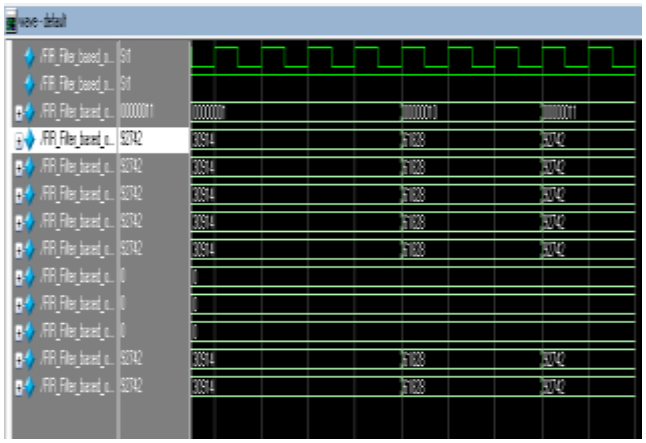
Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	124	26,624	1%
Number of 4 input LUTs	320	26,624	1%
Logic Distribution			
Number of occupied Slices	182	13,312	1%
Number of Slices containing only related logic	182	182	100%
Number of Slices containing unrelated logic	0	182	0%
Total Number of 4 input LUTs	354	26,624	1%
Number used as logic	320		
Number used as a route-thru	34		
Number of bonded IOBs	116	487	23%
IOB Flip Flops	2		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	4,401		
Additional JTAG gate count for IOBs	5,568		

(b)

Fig.4. Common Sub expression Elimination (CSE) algorithm. (a) FIR filter based on adder tree by CSE output waveform. (b) Synthesis result for area.



(a)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	55	7,168	1%
Number of 4 input LUTs	107	7,168	1%
Logic Distribution			
Number of occupied Slices	58	3,584	1%
Number of Slices containing only related logic	58	58	100%
Number of Slices containing unrelated logic	0	58	0%
Total Number of 4 input LUTs	114	7,168	1%
Number used as logic	107		
Number used as a route-thru	7		
Number of bonded IOBs	31	141	21%
IOB Flip Flops	5		
Number of GCLKs	1	8	12%
Total equivalent gate count for design	1,636		
Additional JTAG gate count for IOBs	1,488		

(b)

Fig 5.Graph Based (GB) algorithm. (a) FIR filter based on adder tree by GB output waveform. (b) Synthesis result for area.

TABLE

Comparison between area and power using Common Sub expression Elimination (CSE) and Graph Based (GB) algorithm.

Parameters	**CSE**	**GB**
Delay	20.360ns	19.849ns
Number of slices	124	55

V. CONCLUSION

Graph based algorithm provides a significant changes in the method of shift and add operation, thereby height of tree structure is reduced. Thus in our paper, by the implementation of graph based algorithm, the area is maximum reduced, and the power is also reduced.

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