Design and Simulation of Multiplexer using Josephson junction using OrCAD Capture

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***Abstract*—** The work presented here is a summary of the result obtained when Multiplexer was simulated using simulator: OrCAD Capture 16.5. The Multiplexer is made using the universal logic gates formed by Josephson junction. This allows us to focus our attention on solely the output characteristics and related results derived from the Multiplexer. We begin by describing formation of universal gates and more. We conclude by stating the output characteristics are in match with the multiplexer.

***Keywords*—** *Mux, OrCAD, PSpice, Simulation, NOR Gate, Josephson Junction.*

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I. INTRODUCTION

In our advent into the world of circuit simulation, we have chosen to taken up a subject, which is in the center of many important developments in the modern world. Electronics has seen its boundaries extended with the addition of simulation capabilities. It is our intent to contribute, in our own small way, to this growing pool of knowledge.

Using a simulation technique allows one to analyze electronic circuit's large scale – subject to available computing power. There are a huge number of simulation tools available. In this case study, we focus on OrCAD.

The paper goes on to describe formation of universal NOR gate and Multiplexer obtain using the former made gates. Section 2 describes OrCAD in its various features and its relevance with the electronic simulation space. Section 3 lists out the simulation setup used, and describe the different hardware and software parameters of the simulation workbench. Section 4 and 5 analyze the results obtained, while drawing some conclusions. Finally, the paper end with a look at future steps in the direction and list of works referenced which were helpful in guiding us in our work.

II. OrCAD

A. Introduction

For design and process of documentation of electrical and electronic circuits OrCAD Capture acts as one of the most widely used tool in present world. It provides schematic design solutions for the electrical and electronic circuits. It is easy to learn, design and processing of circuits are really fast which makes it more useful.

Electric and electronic circuit design in today's world require much more than merely obtaining the interconnect knowledge, constructing components or parts or generating net-lists for final developed product and to obtain a significant reduction in project cost and time. Also, improvements in product manufacture and quality are prime concerns which can be easily achieved by using this tool. Tool allows the re-use of circuit design maintaining all the relationships of signal and circuit intact.

It offers services for designing a new analog or mixed-signal circuit, modifying a previously designed circuit, improving the existing model circuits, floor-planning, routing, net-listing and use of different components to improve circuit performance.

It has other tools in support for various activities use. For example:

1. OrCAD PSpice – Used for electrical and electronic circuit simulations.

2. OrCAD CIS (Component Information System) for choosing and selecting more efficient components for optimizing and improving the quality and reliability of the the circuit designed.

B. Schematic Editor

It is highly sophisticated tool which includes all necessary functions and features to fasten up the process of design and building of the electrical and electronic circuits. It can be used to design circuits ranging from simpler designs to complex ones.

C. *Productivity and ease of Use*

In terms of the productivity and ease of use is far away better than its competitive products. It serves a highly recommended tool which has various features and functionalities which are essential for a better design of circuit. As discussed in previous section it supports the design reuse. Also, provides easy way to designers for interconnecting the various components used in design

It has in-built auto-wire feature which enables designers to interconnect the components automatically thus proves beneficial in terms of reducing the time required to connect these components.

To improve the visibility of components and wires, coloring is possible. The major advantage is felt once we use design reuse in larger circuits where connections between components are needed accurate and should be done throughout the circuit design.

D. *Design reuse*

OrCAD capture supports design re-use which is effective in both circuit design time improves the quality of circuit.

Using pre-verified design reduces the efforts needed to design a new circuit also maintain the good quality in the present design.

You may reuse a design of a simple power supply, small components to big designs like memory circuit (or) designs having multiple input and output ports.

E. *PSpice Simulation*

The OrCAD tool has a supporting tool PSpice for analog and mixed signal circuit simulation. It reduces the efforts made by designer by avoid re-designing the same circuit on PSpice. Hence, reducing the time. It directly takes the circuit from OrCAD capture and allows simulation on PSpice. Desginers can test their circuit in terms of real-working environment conditions. Thus, allowing to maintaining the quality of the design. It also provides the generation of net-list for the component used.

Designers can really explore the circuit schematic and its signal flow.

OrCAD Capture with use of tool OrCAD PCB SI enables designers to perform the exploration on circuit creation and connection, signal analysis and provide the constraint to circuit just at circuit design entry.

It has Electrical CSet i.e. Electrical Constant Set to assist all of the features and available as a part of complete constructed and how components are connected in schematic database.

III. SIMULATION SETUP

We choose to execute the simulation of the circuits so as to understand and study the various effects of the circuits.

TABLE I
THE HARDWARE/SOFTWARE SETUP

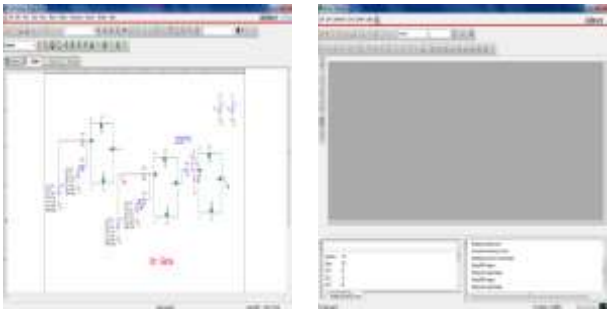
Operating System	Microsoft Windows 7 Home Premium
Processor	Intel Core i3 – 2.40 GHz – 4 Processes
Memory	4GB
Simulated using	1. OrCAD Capture 16.5 2. PSpice AD

Over the course of the many simulations that led to the final ones presented here, we understood that OrCAD Capture is a highly resource intensive simulation package.

Once we gained enough confidence over our circuit model and general proficiency over logic gates implementation by using Josephson Junctions, we moved further to simulate the Multiplexer formed by the logic circuits made earlier. The run configuration we designed allowed us to use the multiple Josephson Junctions available on our design.

We must admit that our software configuration with respect to the real world conditions are fairly limiting. We intended to simulate the Multiplexers using logic gates.

Figure 1 denotes the screenshot while simulating the basic logic gates design. Also for this purposes we have to configure the simulation profiles of the circuit.



1.a 1.b

Figure 1.a – 1.b: OR Logic Gate made using Josephson Junctions; (B) Simulation of (A) in PSpice AD

Figures 1.a & 1.b are illustrations using a computer screenshot taken during the simulation.

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Figure 2 denotes the simulation profiles configurations being used during simulation.

Figure 2: Simulation Profile Settings

IV. RESULTS

A. *Design of NOR Gate*

Figure 3 shows the universal logic gate NOR gate formed using the Josephson Junction.

The input a receives the two inputs in form of pulses and the output out can be seen as in figure.

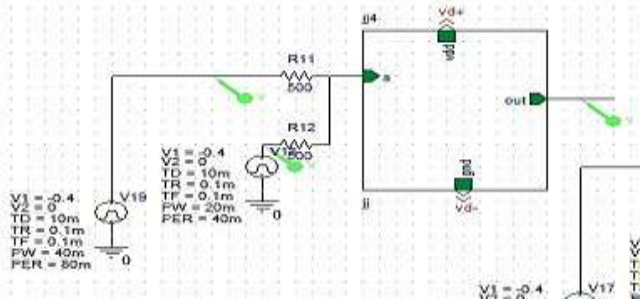

Figure 3: The Design of NOR gate.

The behavior of circuit can be inferred as NOR gate as the output waveform satisfies the logic of NOR gate. The Table II shows the values of NOR gate and its equivalent Boolean logic.

The Boolean logic for NOR gate is

$$Out = \overline{(A + B)}$$

It can be observed from the table that the output is HIGH only if both the inputs are LOW and output is LOW when either of the input is HIGH.

TABLE II
TRUTH TABLE OF NOR GATE

Inputs		Output
A	**B**	**Out**
0	0	1
0	1	0
1	0	0
1	1	0

B. *Simulation Output of NOR Gate*

The below figure 4 shows the simulation outputs for the NOR gate formed using the Josephson junctions.

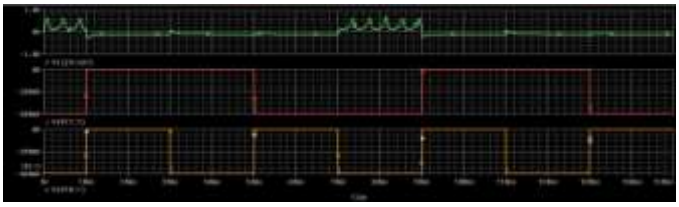

Figure 4: The Output of NOR gate.

C. *Design of MUX*

Figure 5 shows the Mux formed using the Josephson Junction.

The input a receives the two inputs in form of pulses and the output out can be seen as in figure 5.

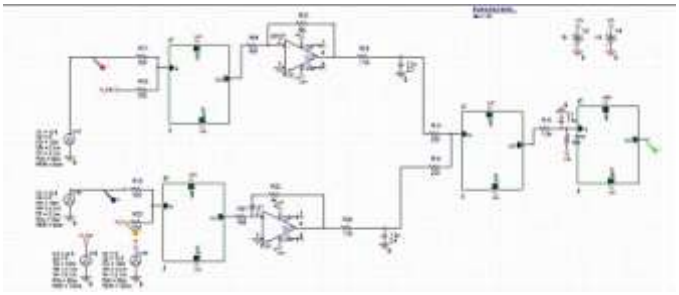

Figure 5: The Design of 2:1 Mux.

The behavior of circuit can be inferred as Multiplexer as the output waveform satisfies the logic of multiplexer. The Table III shows the values of multiplexer and its equivalent Boolean logic is mentioned below.

The Boolean logic for multiplexer is Out = S.A2 + $\overline{S}$. A1

It can be observed from the table that the output corresponds to A1 only if S is LOW and when S is High output corresponds to A2.

TABLE III
TRUTH TABLE OF 2:1 MUX

Inputs			Output
S	A1	A2	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

D. Simulation Output of 2:1 Mux

The below figure 6 shows the simulation outputs for the MUX formed using the Josephson junctions.

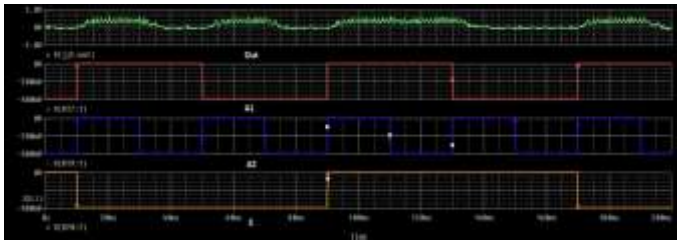

Figure 6: The Output of 2:1 Mux.

That concludes the different parameters we wished to discuss as a part of this paper. We believe that the presented parameters are critical in the evaluation and discussion of any set of digital circuits. We shall now go on to draw out some conclusions on the next section.

V. CONCLUSION

In the previous section, we have made and evaluated the universal NOR gate and 2:1 Mux. Simulation parameters were recorded for them and output graphs were shown.

In conclusion, we believe that Multiplexer has been successfully made as output graph was in accordance to the truth-table.

REFERENCES

[1] B. D. Josephson, "Possible new effects in superconductive tunneling," Phys. Lett., Vol. 1, pp. 251–253, July 1962. P.W. Anderson, "How Josephson discovered his effect," Phys. Today, Vol. 23, pp. 23–29, November 1970.

[2] P. W. Anderson and J. M. Rowell, "Probable observation of the Josephson superconducting tunneling effect," Phys.Rev. Lett., Vol. 10, pp. 230–232, 15 March 1963.

[3] R. P. Feynman, R. B. Leighton, and M. Sands, The Feynman Lectures on Physics, Vol. III, Reading, Massachusetts: Addison-Wesley, 1965, pp. 21–14. A more detailed treatment is given by B. D. Josephson, "Weakly coupled superconductors,"in Superconductivity, Vol. I (R. D. Parks, Ed.). New York: Marcel Dekker, 1969.

[4] H. Ohta, "A self-consistent model of the Josephson junction," in SQUID, Superconducting Quantum Interference Devices and Their Applications (H. D. Hahlbohm and H. Lübbig, Eds.). Berlin and New York: Walter de Gruyter, 1977, pp. 35–50.

[5] M. Tinkham, Introduction to Superconductivity, 2nd ed. New York: McGraw-Hill, 1996, p. 198.

[6] V. Ambegaokar and A. Baratoff, "Tunneling between superconductors," Phys. Rev. Lett., Vol. 11, p. 104, 15 July 1963 (Erratum of Phys. Rev. Lett., Vol. 10, pp. 486–491, 1 June 1963).

[7] M. Fiske, "Temperature and magnetic field dependences of the Josephson tunneling current," Rev. Mod. Phys., Vol. 36, pp. 221–222, January 1964.

[8] T. A. Fulton and D. E. McCumber, "dc Josephson effect for strong-coupling superconductors," Phys. Rev., Vol. 175, pp. 585–586, 10 November 1968. R.E. Harris, R. C. Dynes, and D. M. Ginzberg, "Strong-coupling correction to the jump in the quasiparticle current of a superconducting tunnel junction," Phys. Rev. B., Vol. 14, pp. 993-995, August 1976.

[9] E. Riedel, "Zum Tunneleffekt bei Supraleitern im Mikrowellenfeld," Z. Naturforsch., Vol. 19a, pp. 1634–1635, 15 December 1964.

[10] C. A. Hamilton, "Frequency dependence of the Josephson current," Phys. Rev. B., Vol. 5, pp. 912–913, 1 February 1972.

[11] P. G. de Gennes, "Boundary effects in superconductors," Rev. Mod. Phys., Vol. 36, pp. 225–237, January 1964

[12] S. Benz, "Superconductor-normal-superconductor junctions for programmable voltage standards," Appl. Phys. Lett., Vol. 68, pp. 3171–3173, May 1996.

[13] K. A. Delin and A. W. Kleinsasser, "Stationary properties of high critical temperature proximity effect Josephson junctions," Superconductor Science and Tech., Vol. 9, pp. 227–269, April 1996.

[14] R. Gross, L. Alff, A. Beck, O. M. Froehlich, D. Koelle, and A. Marx, "Physics and technology of high temperature superconducting Josephson junctions," IEEE Trans. Appl. Superconduct., Vol. 7, pp. 2929–2935, June 1997.

[15] K. K. Likharev, "Superconducting weak links," Rev. Mod. Phys., Vol. 51, pp. 101–159, January 1979.

[16] M. Yu. Kupriyanov and V. K. Lukichev, "The influence of the proximity effect in the electrodes on

ISSN: 2321-8169
968 - 972

the stationary properties of S-N-S Josephson structures," Sov. J. Low Temp. Phys., Vol. 8, pp. 526–529, October 1982.

[17] J. Seto and T. Van Duzer, "Theory and measurements on lead-tellurium-lead supercurrent junctions," in Low Temperature Physics — LT 13, Vol. 3 (K. D. Timmerhouse, W. J. O'Sullivan, and E. F. Hammel, Eds.). New York: Plenum Press, 1974.

[18] D. Dimois, P. Chaudhari, J. Mannhart, and F. K. LeGoues, "Orientation dependence of grain boundary critical currents in YBaCuO7 crystals," Phys. Rev. Lett., Vol. 61, pp. 219–333, 11 July 1988

[19] M. Maezawa, M. Aoyagi, H. Nakagawa, I. Kurosawa, and S. Takada, "Specific capacitance of Nb/AlOx/Nb Josephson junctions with current densities in the range of 0.1–18 kA/cm2," Appl. Phys. Lett., Vol. 66, pp. 2134–2136, 17 April 1995.

[20] E. J. Tarte, G. A. Wagner, R. E. Somekh, F. J. Baudenbacher, P. Berghuis, and J. E. Evetts, "The capacitance of bicrystal Josephson junctions deposited on SiTiO3 substrates," IEEE Trans. Appl. Supercond., Vol. 7, pp. 3662–3669, June 1997.

[21] http://www.orcad.com/sites/orcad/files/resources/files/OrCAD_Capture_Final.pdf