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# Design and Performance Comparison of Average 8T SRAM with Existing 8T SRAM Cells

[1]Bini Joy, [2]Sathia Priya.M,[3]Akshaya.N [4]Ruth Anita Shirley.D

[1,2,3,4] PG Students/DEPT OF ECE, SNS College of Technology, Coimbatore, India

*akshayaa176@gmail.com,bini251990@gmail.com*

**Abstract :-**

This paper presents 8T SRAM cell by using various techniques. The conflicting design requirement of read versus write operation in a conventional 8T SRAM bit cell is eliminated using separate read/write access transistors The read stability and the write-ability can be optimized independently by optimizing the respective access transistor size. A new average-8T write/read decoupled SRAM architecture for low-power sub/near-threshold SRAM used in power-constraint applications such as biomedical implants and autonomous sensor nodes. The proposed architecture consists of several novel concepts in dealing with issues in sub/near-threshold SRAM including the differential and data-independent-leakage read port that facilitates robust and faster read operation Simulation result of 8T SRAM design using TANNER tool shows the reduction in total average power and delay.

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## I. INTRODUCTION

Static Random Access Memory (SRAM) occupies a significant portion of the total-die area and it is predicted that nearly 90% of the total die area would be occupied by on-chip cache memory in future nano scale technologies.Ultralow Voltage and low-power SRAM design is critical in embedded systems such as biomedical implants, self-powered wireless sensors, and energy harvesting devices in which battery life or input power is of main concern It is well-known that the best way to reduce the power in a digital circuit is to lower the supply voltage as it has quadratic impact on the power consumption. SRAM design remains challenging and becomes more interesting due to the rapid advancement of CMOS technologies and with increased demand of on-chip memory in the wireless implantable/wearable biomedical sensors. In modern high performance integrated circuits more than 40% of the total active mode energy is consumed due to leakage currents. The feature size of the transistor is scaled down the threshold voltages of MOSFETs have been reduced thereby increasing leakage power substantially. Leakage is the only source of energy consumption in an idle circuit .SRAM arrays are important sources of leakage since the majority of transistors are utilized for on-chip memory in today's high performance microprocessors and systems-on-chips

## II. SINGLE ENDED 8T SRAM CELL

A novel asymmetrical Write-assist cell virtual ground (VGND) biasing scheme is proposed to improve the RSNM, WM, and operation speed of single-ended 8 T SRAM. As shown in Fig.1, this technique is based on symmetrical cross-coupled inverters (M1-M4) and the isolation of Read and Write paths in single-ended 8 T SRAM cell. The separation of Read/Write paths is one of the common approaches to mitigate noise disturbance. The Read isolation port (M6 and M7) eliminates the Read disturbance. As such, the static noise margin in Read mode is the same as that in Standby mode, thus facilitating low voltage operation. The Read and Write operations share the same BL to reduce active BL switching power.

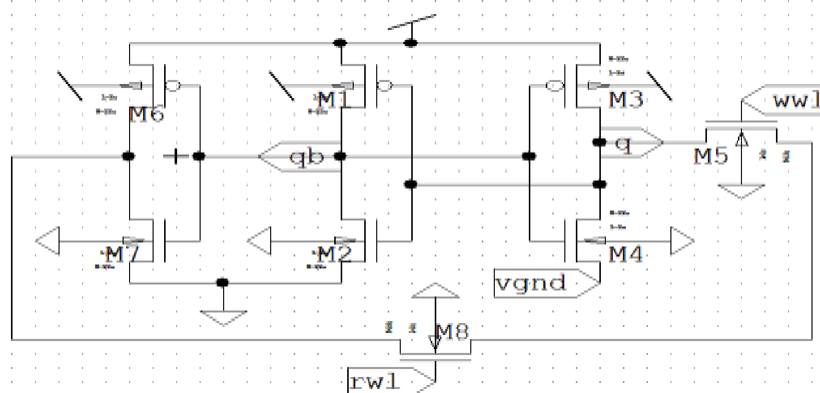


Figure 1 Single Ended 8T SRAM Cell

***Write* Operation**

The asymmetrical cell structure can improve the SNM without degrading Read/Write operation. The asymmetrical sizing technique is still limited to about 0.7 V supply voltage, because the driving capability of bit-line is reduced at lower supply voltage. The scheme mitigates the M4/M5 voltage dividing effect without increasing the threshold voltage of M2 and the trip voltage of the left inverter. Therefore, it is easier to turn on M2 to start the feedback process to flip the cell storage data.eration. In Write "0" mode, the access transistor M5 offers a strong "0" pull-down signal to flip the storage data. The Q node is pull down to change the state of the left inverter. Although the latch feedback loop is broken due to floating of the M4 source node, the Write "0" operation wouldn't be affected. Another commonly used metrics to characterize Write-ability is the Write "1" Margin (WM1). The Write "1" Margin for differential BL SRAM cell is defined as the highest voltage level of the low-going bit-line that can flip the cell.

***Read* Operation**

In Read operation, the RWL signal turns on pass-transistor M8, and the stored data is transferred through M6/M7 inverter and M8 to the bit-line as indicated in Fig.1 . The Read operation is executed by the static M6/M7 inverter buffer, so power dissipation can be reduced by not precharging the bit-lines The circuit consumes AC power only when the Read-out data changes.The bit-lines are precharged to "High". During Read operation, the precharge transistor and the half-selected cells along the selected bit-line pair form a configuration similar to multi-input dynamic NOR gate. The dynamic bit-line is sensitive to the leakage due to process variations because the cell leakage will degrade the Read margin. The static Read-out inverter offers a larger Read margin to mitigate the effect of process variation. If a design target is for area efficiency, not power efficiency and robustness by removing M6 from the proposed 8 T SRAM cell could be used to achieve high density, but BL precharge circuit should be used to make function work.

## III. DIFFERENTIAL SENSING READ WRITE 8T CELL

The differential sensing with read-disturb-free mechanism requires 10 transistors to form the bit-cell. In the proposed 1R/1W port 8T bitcell, the read-access transistor is shown as N1 in Figure 2 is shared across the bitcells of each row. Thus, the proposed scheme contains only 8 transistors per bitcell unlike the earlier 9T bitcell in which RWL access transistor is used for every bitcell. Moreover, the proposed 8T bitcell has dual port functionality unlike the single port functionality in earlier reported 9T bitcell .

***Read/Write* Stability**

In the conventional 8T SRAM bitcell access transistor and the pull-down transistor strengths need to be balanced for maintaining the read-stability across wide range of supply and process variations. Addition of separate read port in the proposed 8T bitcell results in read-disturb free operation improving the read-stability. The read-stability in the proposed 8T bitcell is same as the hold-mode stability. Separate write port in the proposed 8T bitcell allows upsizing write-access transistor widths compared to the pull-up pMOS thereby improving the write ability.

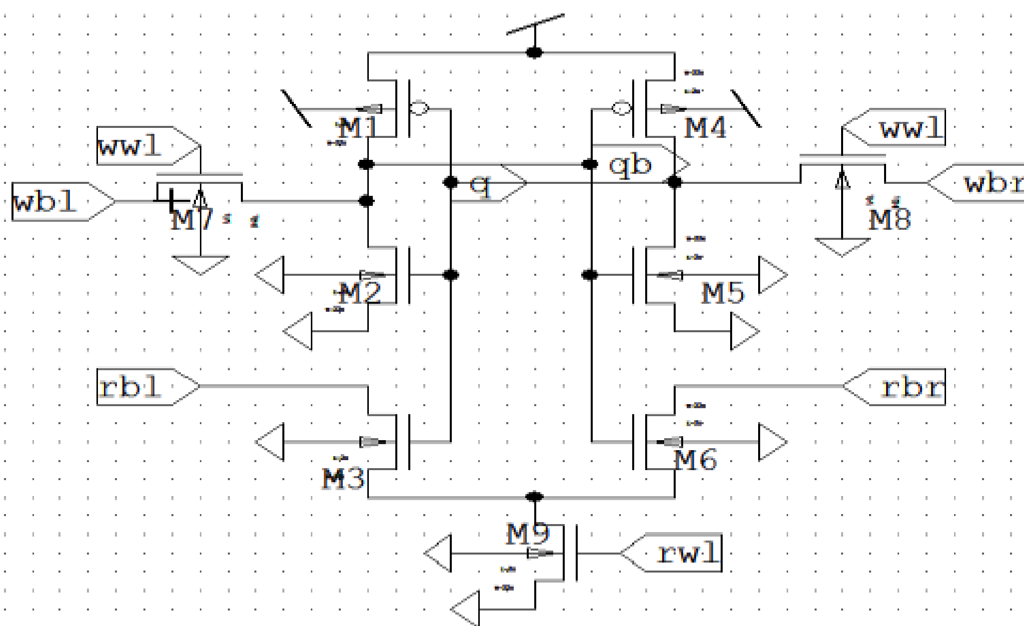


Figure 2 Differential Sensing Read Write 8T Cell

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## IV. Zigzag 8T SRAM cell

The Figure 3 shows the schematic view of Zigzag 8T SRAM cell. This cell is a combination of standard 6T SRAM cell and a 2T decoupled *read*-port. M7 and M8 are two decoupled *read*-port transistors used to transfer the data stored in Q and QB to the bit-lines. Because the storage nodes and the *read* bit-lines (RBL/RBLB) are separated by transistors M7 and M8, the storage nodes are entirely decoupled from RBL and RBLB thereby solving the issues in *read* line.

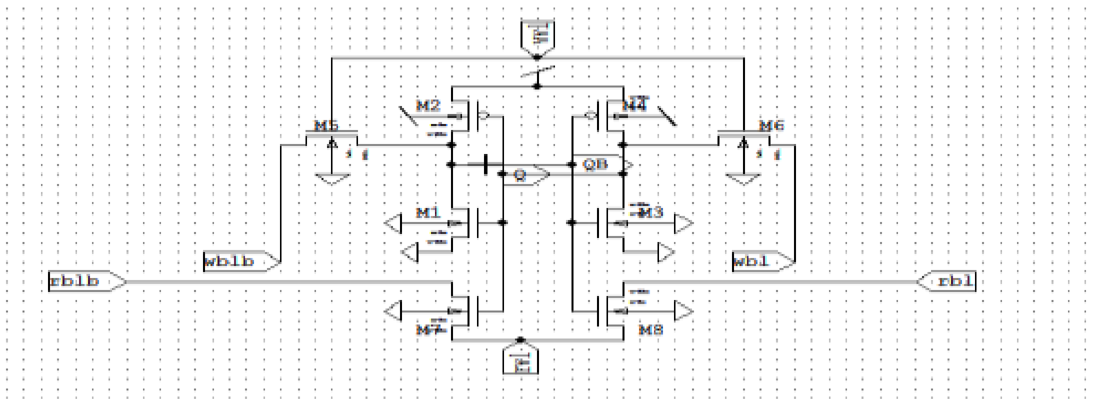



Figure 3.Zigzag 8T SRAM cell

**Read Operation:**

Before the read operation, the RWL remains at VDD and the read bit-lines ( RBL and RBLB) is initially pre-charged to VDD. During the read operation, the RWL is given a low voltage and pulled to VSS. If the storage node Q stores a low voltage, the transistor M7 will remain off and RBLB will remain at VDD during the read operation. The storage node QB stores a high voltage, the transistor M8 is turned on and RBL will be pulled low. A small voltage difference between the bit-lines will be developed and can be sensed by the differential sense amplifier. On the other hand if the storage nodes Q and QB store high and low voltage respectively the RBLB will remain at VDD and it will be pulled low.

**Write operation:**

For writing the data into the cell, the WWL is activated and turned ON to a high voltage, which in turn activates the pass gate transistors M5 and M6. The write data stored at the complementary write bit-line pair will be transferred to the storage nodes of the cross-coupled inverter, to overcome the original states stored in it. Here the writing of data is alike conventional 6T SRAM cell.

## V. AVERAGE 8T SRAM CELL

The basic architecture of the proposed write/read-decoupled SRAM block is illustrated in Figure 4. The number of transistors in each block depends on the number of bits stored in the block.

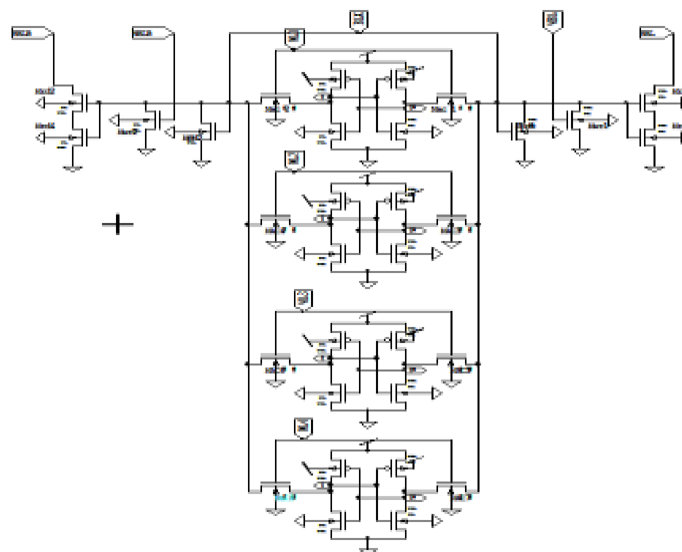


Figure 4.Schematic of Average 8T SRAM cell

The average-8T block holds four bits through four back-to-back connected inverters. The storage nodes are connected to the local bit-lines (LBL and LBLB*)* via access transistors .These local bit-lines are decoupled from the write bit-lines (WBL and WBLB*)* during a write operation and from the global read bit-lines (RBL and RBLB*)* during a read operation. This new write/read-decoupled (WRD) technique allows complete isolation of these four bits.

### ***Read*** **operation**

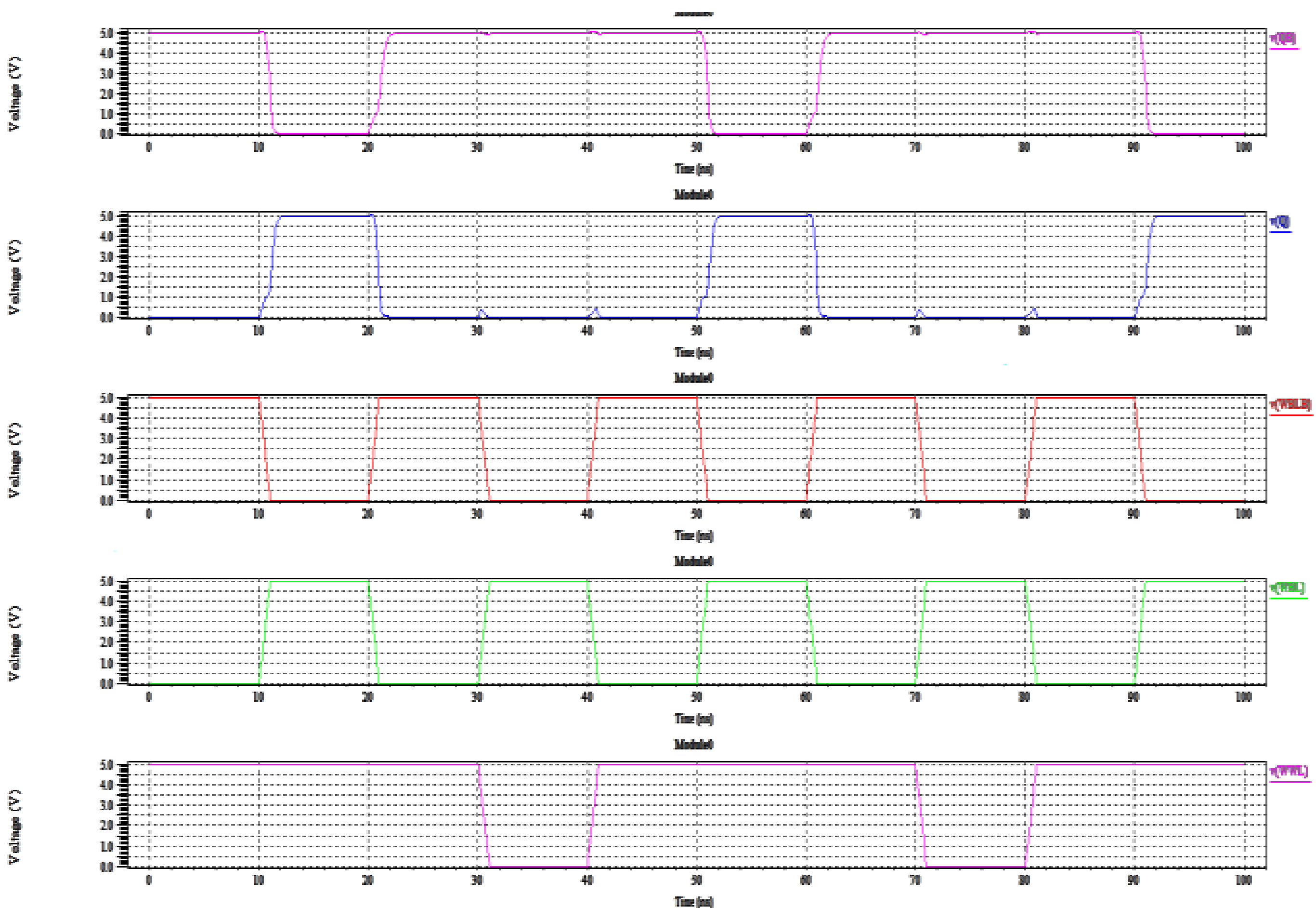
A new read decoupling technique that decouples more than one bit at both Q and QB sides is proposed to improve read robustness. During a read operation the intended block are turned off and the access transistors are turned on. The stored data turns one of the read-decoupling pair transistors) on and discharges one of the pre-charged read bit-lines (RBL or RBLB)

### ***Write operation***

A write operation, as shown in Figure is performed by selecting the intended block and bit in the same way as a read. Depending on the written data, one of the write decoupling transistor is turned on and pulls down the storage node in the intended bit. The proposed architecture allows bit interleaving. Half-selected bits during a write operation, experience the same situation as read, i.e., all pull-down transistors are off and access transistors are on.

## VI.SIMULATION RESULTS

Simulation results are performed using Tanner EDA tool in 125nm technology with supply voltage ranging from 5v and operating frequency of 50MHZ. To establish an impartial testing environment each circuit have been tested on the same input patterns. The below waveform shows



## VII. PERFORMANCE ANALYSIS

Comparison table depicts the transistors over a range of Power Supply. It is shown that the proposed technique has minimum Power and delay.

| PARAMETERS | SINGLE ENDED 8T SRAM | DIFFERENTIAL SENSING 8T SRAM | ZIGZAG 8T SRAM | AVERAGE 8T SRAM |
|---|---|---|---|---|
| AVERAGE POWER(W) | 0.0966 | 0.0709 | 0.0884 | 0.0498 |
| DELAY | 1.92 | 1.39 | 1.44 | 1.11 |

## VIII. CONCLUSION

The effect of the 8T SRAM Cell describing the leakage current through the load circuit was implemented. A new average-8T write/read decoupled SRAM architecture for low-power sub/near-threshold shows that low power dissipation and delay when compared to other techniques. The 8T SRAM cell and the load circuit were designed by using tanner technology. The advantages of different modes i.e its operating mode is high $V_{ds}$ to load circuits and for high speed operation in stand-by mode, high $V_t$ through load circuits for minimum stand-by leakage power, high noise immuntiy, stand-by power dissipation and delay.

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