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Power Optimization of Combinational Quaternary Logic Circuits

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***Abstract*—** Due to the need of interconnections design of binary circuits is limited. Interconnection increases area, delay and energy consumption in CMOS digital circuits. A possible solution could be here as, in the same chip area we use more sets of signals. Multiple value logic can decrease average power required for level transitions and reduces the number of necessary interconnections. In this paper we design various combinational modules using Quaternary logic. Various combinational circuits are Quaternary full adder using unique encoding, quaternary encoder & decoder and quaternary multiplexer. These designs are aimed to reduce the transistors used in the implementation of circuits and reducing the power dissipation. Power optimization is achieved using MTCMOS technique. Simulation has been done in Tanner 13 EDA tool on BSIM3 180nm CMOS technology.

Keywords- Multi value logic, power optimization, quaternary full adder, quaternary encoder & decoder, quaternary multiplexer and MTCMOS technique.

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I. INTRODUCTION

Multi-valued logic has been being considered as a suitable alternative for binary logic from many years. In the field of computing, multiple value logic can lead to significant improvement because of its higher information capacity and required fewer blocks of circuits per symbol as compared to binary systems [6].

Usually in binary digital circuits static power utilization is directly relate to leakage current. By applying lower supply voltage and reducing the number of transistors give evolution to CMOS process.

Hence it integrates more number of functions in same area. The threshold voltage of transistor is not proportional to power supply voltage thus increases leakage current, therefore increases CMOS circuit's static consumption of power.

Number of interconnections can be considerably reduced when data is represented in multi value logic system as it is effective than binary demonstration. These circuits greatly shows improvement in area reduction but power consumption is more and complication in implementation.

By grading the supply voltage power dissipation can be reduced. Grading of supply voltage started from half micron technology but it affects the speed of circuits. MTCMOS technology has developed as an effective alternate to usual CMOS to make the logic gates working at high speed with low power dissipation [3]. MTCMOS technique uses both low and high threshold voltage transistors which provide low power and high performance design.

There are four quaternary states 0, 1, 2 & 3 for which we can take binary equivalent as 00, 01, 10 & 11 [5]. They are called as absolute low, medium low, medium high and absolute high. If the bits of binary representation interchange their position and quaternary state remain unaffected then it is called as binary symmetry if not called as asymmetric.

Quaternary states (0, 1, 2, 3) can be imagined as 2-bit binary equals 00, 01, 10, 11. They are named as absolute low, medium low, medium high and absolute high respectively. If the bits of the binary equal exchange their positions and still the quaternary state remain unchanged, then it is said to have binary symmetry; otherwise it is asymmetric. Thus 0, 3 are symmetrical and 1, 2 are asymmetrical. When stated as a number, a single quaternary digit is called a qudit.

The total area of interconnections is determined by the number of interconnections and their length. The interconnection length is also determined by the complexity of the interconnections. Thus it is clear that the use of MVL is very useful for compact VLSI implementation.

This paper is organized as, section II introduces quaternary full adder using unique encoding, section III as quaternary encoder, IV discusses quaternary decoder, V as quaternary multiplexer. Introduction to MTCMOS and design of all the above circuits in this technique discuss in section VI. Comparison and result are discussed in section VII.

II. QUATERNARY FULL ADDER

Proposed quaternary full adder designed with unique encoding technique [6]. It consists of encoder block, code generator, sum and carry block. Encoder block consist of down literal circuits (DLC), binary EX-OR gate and inverters. DLC is a voltage mode circuit to recognize along the literal function with variable threshold and can inverse function.

X & Y are the two inputs to full adder circuit. Encoder converts this into binary form. Code generator again decodes the signals X & Y into two signals which are used to generate sum and carry of full adder. Sum and carry blocks are

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build with pass transistors and it can be replaced by transmission gates for proper logic level.

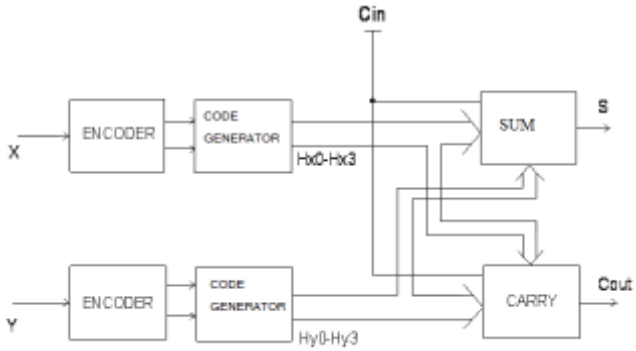


Figure1. Block diagram of full adder using unique encoding.

Table1. Truth Table when Carry In is 0.

Sum

A \ B	0	1	2	3
0	0	1	2	3
1	1	2	3	0
2	2	3	0	1
3	3	0	1	2

Carry

A \ B	0	1	2	3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	1
3	0	1	1	1

Table2. Truth Table when Carry In is 1.

Sum

A \ B	0	1	2	3
0	1	2	3	0
1	2	3	0	1
2	3	0	1	2
3	0	1	2	3

Carry

A \ B	0	1	2	3
0	0	0	0	1
1	0	0	1	1
2	0	1	1	1
3	1	1	1	1

Power dissipation of full adder using unique encoding in CMOS technique is 3.6261 x 10^{-6} watt.

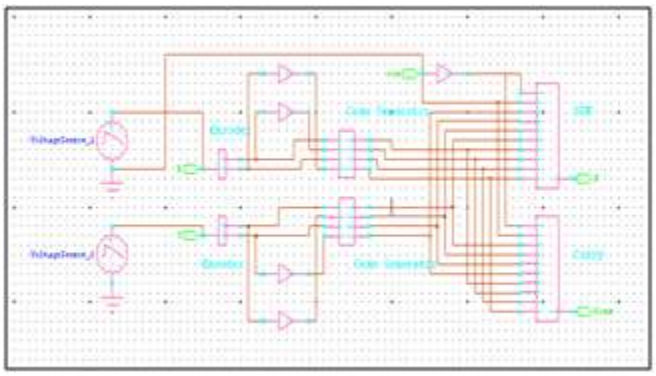
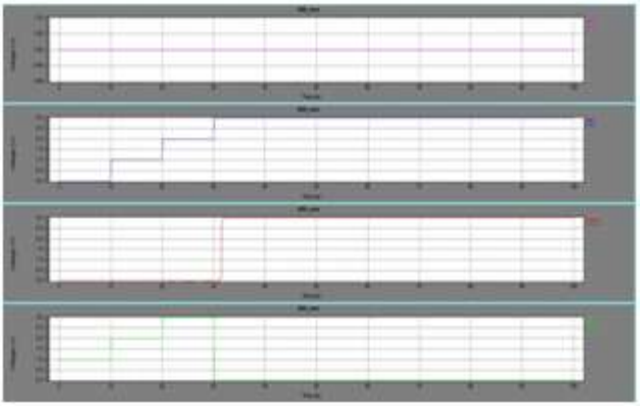


Figure2. Schematic of quaternary full adder circuit.

Figure3. Simulation result of quaternary full adder.



III. QUATERNARY ENCODER

Quaternary 4 to 1 encoder consist of 4 inputs 1 output and also consist of two OR gates two AND gates and a transmission buffer. Each 4 to 1encoder has two output stages. First gives logically applicable unbuffered output and second gives buffered key. This can be determined from four inputs. Buffer key is responsible for the appearance of Z at the final output.

Output shows 5 possible states including high impedance state if all the inputs are low. Z is an intermediate state with no logical meaning. Priority encoder can also be constructed using quaternary logic [9]. Ordinary encoder is not as practical as priority encoder as it handles the problem when more than one input is high simultaneously.

Figure 4 shows the block diagram of quaternary encoder circuit. Figure 5 shows schematic design of quaternary encoder designed in tanner tool. The simulation result of this circuit is shown in figure 6. Result is according to the truth table given in table 3.

Power dissipation of quaternary 4-to-1encoder using CMOS technique is 2.2356 x 10^{-7} watt.

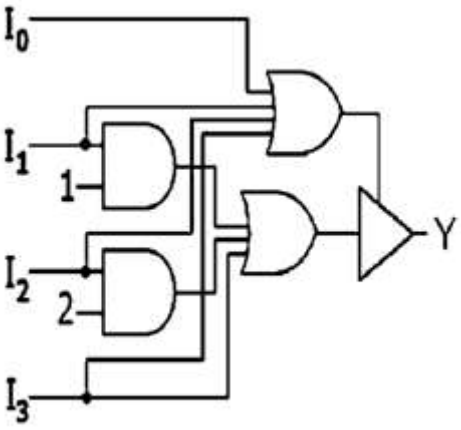


Figure4. Block Diagram of Quaternary 4-to-1 Encoder.

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Table3. Truth table of Quaternary 4-to-1 Encoder

I_0	I_1	I_2	I_3	Y
0	0	0	0	Z
3	0	0	0	0
X	3	0	0	1
X	X	3	0	2
X	X	X	3	3

According to the above truth table we have given a quaternary input to the encoder circuit. There are 4 stages of voltage as 0, 1, 2 and 3. When voltage 0 is given then input I_0 becomes high and appears at output.

Similarly when voltage levels 1, 2 and 3 appears then respectively I_1, I_2 and I_3 becomes high. When all the inputs are low then intermediate state Z appears. This is shown in figure 6 simulation results.

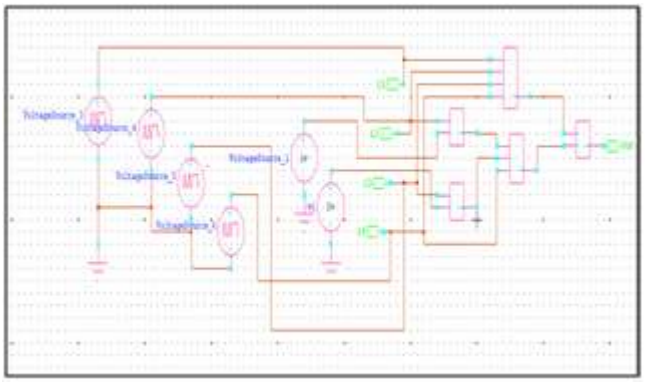

Figure5. Schematic of Quaternary 4-to-1Encoder

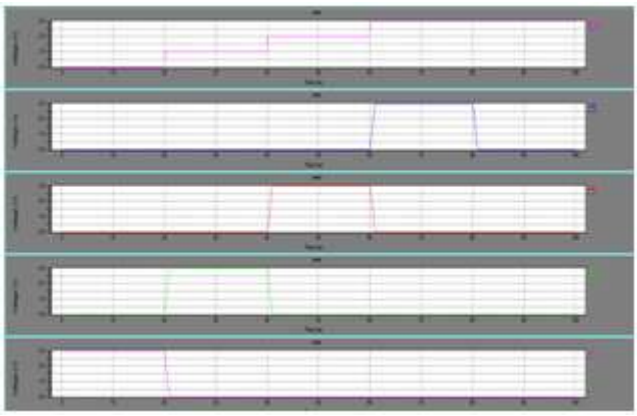

Figure6. Simulation result of Quaternary 4-to-1 encoder.

V. QUATERNARY MULTIPLEXER

Quaternary multiplexer is shown in figure 10. It consists of 3 down literal circuits, 3 inverters and 6 transmission gates. It has 4 inputs as A, B, C and D [7]. When quaternary logic is 0 input A will be transferred to output. Quaternary logic is 1 then input B transferred to output. Input C will be transferred when logic 2 occurs at input. When quaternary logic is 3 then at output input D will be transferred. All the inputs are transferred through transmission gate to the output.

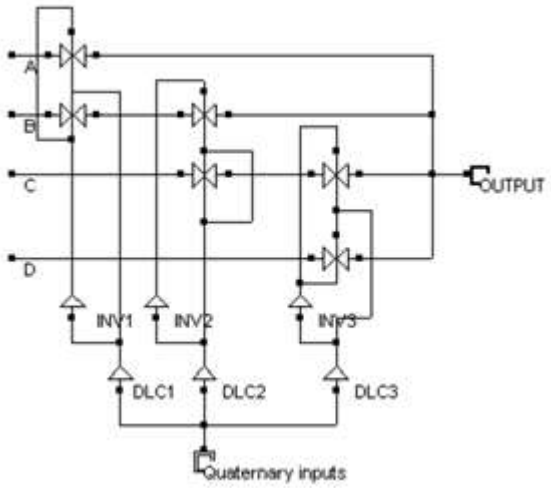

Figure7. Block diagram of Quaternary multiplexer

Table4. Truth table for quaternary multiplexer

Quaternary inputs	Output
0	A
1	B
2	C
3	D

Here the values of alphabets A, B, C and D are 1, 3, 2 and 0 respectively in this designed schematic of circuit shown in figure 11. Quaternary multiplexer can be used to design various other combinational modules such as adders, decoders, multipliers.

Power dissipation of quaternary multiplexer circuit using CMOS technique is 4.8252 x 10^{-6} watt.

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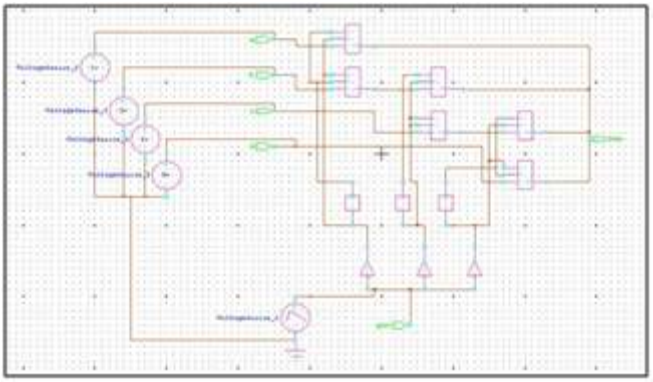

Figure8. Schematic of quaternary multiplexer

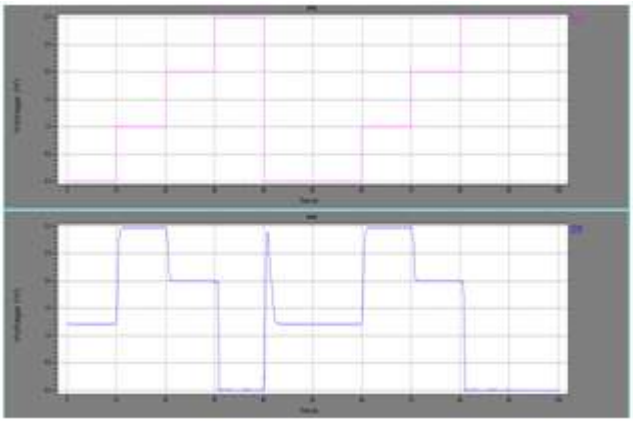

Figure9. Simulation result of quaternary multiplexer

VI. MTCMOS TECHNIQUE

MTCMOS technique utilizes low and high threshold voltage transistors and provides low power design and high performance. It is very helpful circuit level technique. This technique is used for maintaining circuit performance in standby mode and reduces sub threshold currents [3]. MTCMOS technique is a popular low leakage circuit technique. MTCMOS is multi threshold voltage CMOS.

It has two main operational modes as ‘active’ and ‘sleep’ for effective power management. In a single chip for N and P channel MOSFET two different threshold voltages are used.

In this technique a transistor with high threshold voltage is connected between supply voltage and ground. It disconnects the low threshold voltage from power supply and ground through this high threshold voltage. This transistor is called asleep transistor and also known as ‘power gating’. Low threshold voltage transistor is used to implement the logic and high threshold voltage transistor is used for isolation of low threshold transistor from supply and ground during sleep mode to prevent leakage dissipation.

In active mode sleep transistors are turned ON and low threshold transistor can operate at high speed and low power dissipation. In sleep mode high voltage transistors are turned OFF and isolate the low threshold transistor from ground and supply voltage hence reducing sub threshold leakage current.

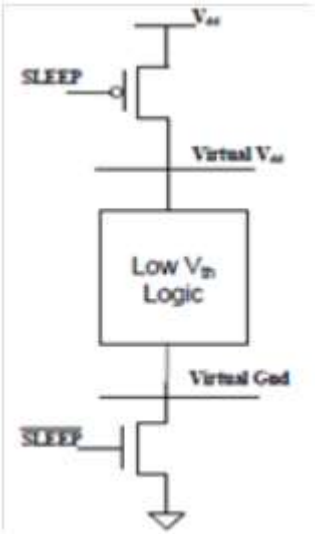

Figure10. Power gating technique using MTCMOS

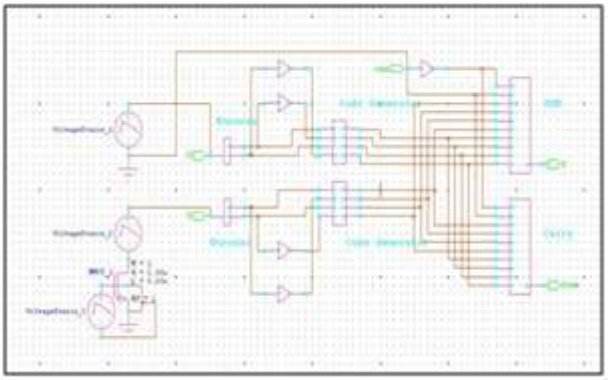

Figure11. Schematic design of quaternary full adder using MTCMOS technique

Above figure shows schematic design of quaternary full adder using MTCMOS technique. In this design a transistor with high threshold voltage is implemented between supply voltage and ground. It is used to isolate low threshold voltage transistors to prevent leakage dissipation. Similarly other combinational circuits with MTCMOS technique is shown below.

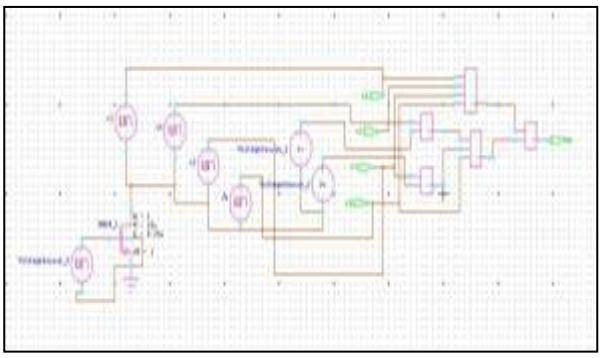

Figure12. Schematic of quaternary 4-to-1 encoder using MTCMOS technique

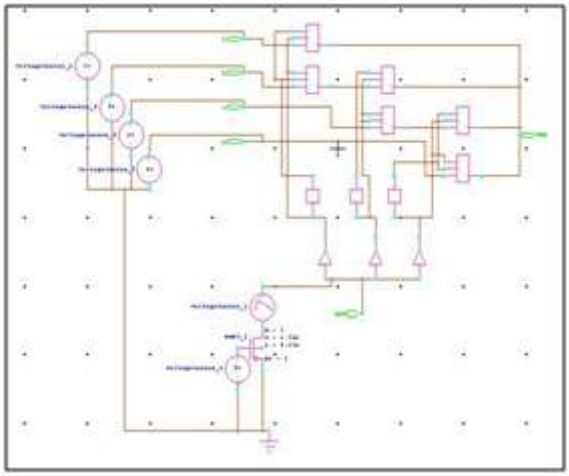

Figure13. Schematic of quaternary multiplexer using MTCMOS technique

By using MTCMOS technique power is reduced up to 10 – 30 % compared to the design of CMOS. The comparison and power values are given in table 5.

VII. COMPARISON AND RESULT

Table5. Simulation result for power dissipation of various quaternary circuits

Power Dissipation (10^{-6}) watt			
Combinational circuits	*CMOS*	*MTCMOS*	*Reduction*
Quatemary Full Adder using unique encoding	3.6261	3.2618	10.05%
Quatemary 4-to-1 Encoder	0.022356	0.014850	33.57%
Quatemary 1-to-4 Decoder	19.395	15.886	18.09%
Quatemary Multiplexer	4.8252	4.3360	10.14%

Implementation of various combinational circuits using CMOS and MTCMOS technique has been done in 180nm technology in Tanner EDA tool. Power dissipation comparison of various circuits is shown in above table with reduction percentage.

Here it clearly shows that quaternary full adder using MTCMOS technique reduces 10.05% power dissipation as compared to CMOS design. Similarly quaternary encoder using MTCMOS technique reduces 33.57% power compared to CMOS circuit. Quaternary decoder reduces power dissipation of about 18.09% compared to CMOS design. Quaternary multiplexer using MTCMOS reduces power 10.14% compared TO its CMOS design.

After comparison we can say that quaternary circuits using MTCMOS technique have less power dissipation as compared to CMOS design circuits.

VIII. CONCLUSION

Designs of different combinational circuits are analysed and proposed. These circuits are designed using different techniques on the basis of different parameters. Hence, we investigate and analyze the proposed circuits.

Different quaternary circuits are designed using CMOS and MTCMOS technique. The result analysis shows the flexibility of MTCMOS technique in different quaternary combinational circuits.

It shows reduction of about 10-30% in power as compared to CMOS designs with supply voltage of 3V. Design of circuits MTCMOS technique has marginal increase in area but overall it is better in terms of power dissipation as it achieve less power as compared to CMOS designs.

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