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A Novel Approach for Design of Pulse Triggered Flip-Flop to Enhance Speed and Power

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***Abstract*—** In VLSI Technology, flip-flops contribute a significant portion of chip area and power consumption to overall system design. Pulse triggered flip-flops (P-FF) have single latch and hence simpler in circuit complexity. Use of Explicit type design for P-FF gives the speed advantage. This paper presents various Pulse triggered Flip-flop (P-FF) designs and various techniques to achieve a better design in terms of power consumption and speed. Introduction of simple pass transistor in latch design can be used to speed up data transition. Dual edge triggering can be adopted as it consumes less power as compared to single edge triggering. Also conditional discharge technique can be used to reduce switching activity. The work is done in tanner tool software.

Keywords- *Flip-Flop, Pulse Triggered, Dual Edge*

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I. INTRODUCTION

In VLSI technology, there is continuous increase in the transistor densities and higher clock speeds are achieved which causes increase in power consumption of VLSI design. Flip-flops and latches are basic storage elements that are used in all kind of digital designs. These digital designs employ many flip-flop rich modules. Also the clock systems which are made up of clock distribution network and storage elements; causes almost 50% power consumption of total system power[11]. Hence Flip-flops contribute a significant portion of chip area and have a deep impact on total power consumed. Conventional master-slave flip-flops consist of two stages, first stage called as master and second stage called as slave. Another edge triggered flip-flop is sense amplifier based flip-flop (SAFF).These flip-flops called as hard edged and are characterized by positive setup time which causes large D-to-Q delays.

Pulse-triggered flip-flops are characterized by the soft edge property and reduce the two stages into single latch stage. In high-speed applications, pulse-triggered FF (P-FF) gives higher performance than the conventional transmission gate (TG) and master–slave based FFs because of its single-latch structure. Because reduced number of stages and reduced logic complexity, pulse-triggered flip-flops have small D-to-Q delays. Pulse-triggered flip-flop is only type of flip-flop which allows time borrowing capability with negative set up time.

In terms of pulse generation, P-FFs can be categorized as an implicit type or an explicit type. In implicit pulse triggered flip-flop, the pulse generation is part of latch design. In pulse triggered Flip-flop with Explicit design, the pulse is generated externally. Pulse generation logic separation in explicit pulse triggered flip-flop gives unique speed advantages.

P-FF with Dual edge triggering consumes less power as compared to single edge triggering and increases performance of system. A simple pass transistor can be included in design which can shorten the longer delay as the input signal is directly feed to an internal node present in the latch design (signal feed through).To reduce switching activity, conditional discharge technique can be adopted.

II. CONVENTIONAL P-FF DESIGNS

In terms of pulse generation, Pulse triggered flip-flops can be classified as an implicit or an explicit type.

A. Implicit Type Pulse Triggered Flip-Flop

In Implicit type P-FF, Pulse generator is a part of latch design

and pulse signals are not generated explicitly.

1. Implicit data close to output (ip-DCO)

Implicit data close to output (ip-DCO) [1] contains a pulse generator which is based on AND logic with a latch design consisting of semi dynamic structure. It is an implicit type flip-flop having small delay, simple topology, occupies small area and uses single phase clocking. The inverter I5 and I6 are used for latching data and for holding the internal node inverter I7 and I8 are used. Two problems exist in this design. First is during the rising edge (0 to 1), NMOS transistors N2 and N3 are turned on and if data input D remains at logic ‘1’(high), then on every rising edge of the clock, node X will be discharged resulting in large switching power dissipation.

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Second problem is two larger MOS transistors (P2 and N5) are controlled by node *X*. The large capacitive load to node *X* causes speed and power performance degradation. As implicit type P-FF does not generate pulse signals explicitly they suffer from a longer discharging path problem, which leads to inferior timing characteristics.

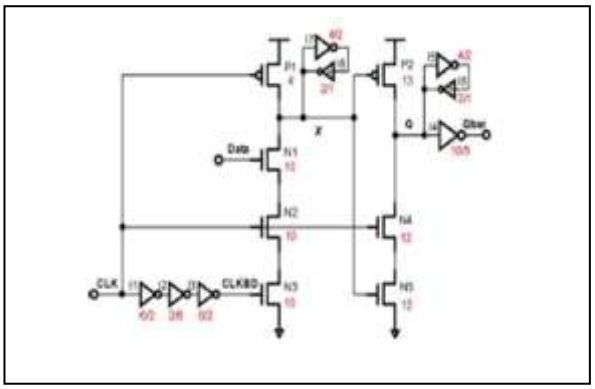

Fig.1 Implicit data close to output (ip-DCO)

B. Explicit Type Pulse Triggering Flip-Flop:

In an explicit type P-FF, the latch design and the pulse generator are separate part. Explicit P-FF causes more power consumption. But circuit complexity and power consumption can be effectively reduced by sharing single pulse signal by a group of FFs. CDFF, ep-DCO, Static-CDFF, MHLFF are the existing designs which uses explicit pulse generation scheme.

1.Explicit data-close to-output (ep-DCO).

This is an explicit P-FF design [1], named data-close to-output (ep-DCO) shown in "Fig.2" which consist of a semi dynamic true-single-phase-clock (TSPC) structured latch design and a NAND-logic-based pulse generator. Here two Inverters are used to latch data, and another two inverters are used for holding the internal node *X*. In this design, on every rising edge of the clock, the internal node *X* is discharged even in the presence of a static input "1". Because of this reason there is large switching power dissipation. For reducing the switching power dissipation various techniques can be employed.

2. Conditional Discharge (CDFF) P-FF

Fig3. Shows CDFF[3].An extra transistor NMOS_5 controlled by the output signal is employed. Thus if the input data remains high, no discharge occurs. Also for the internal node X , the keeper logic consists of an inverter along with pull-up PMOS_3 transistor provides a simplified design.

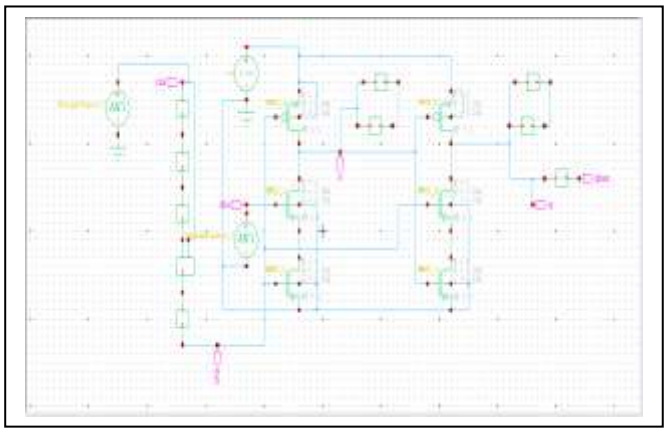

Fig.2 EP-DCO

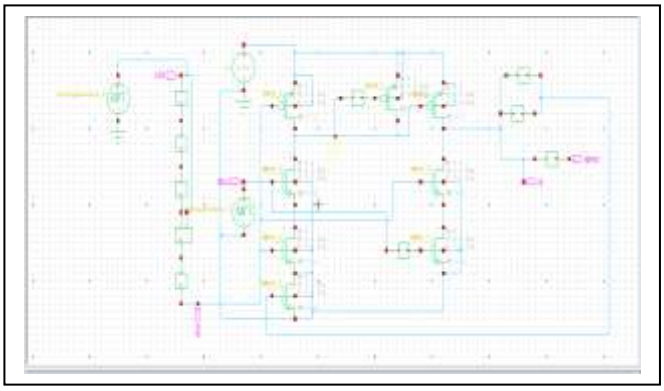

Fig.3 CDFF

3. Static Conditional discharge (SCDFF) P-FF

Fig 4 shows a P-FF design (SCDFF) [4] using a static conditional discharge technique. This design uses a static latch structure. Thus Node X is exempted from periodical precharges. It exhibits a more data-to-Q (D-to-Q) delay as compared to the CDFF design. Both CDFF as well as SCDFF designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e. NMOS_1-NMOS_2 - NMOS_5.

4. Modified hybrid latch(MHLFF) P-FF

Fig5 shows the modified hybrid latch flipflop (MHLFF) [10] which also uses a static latch. The keeper logic at node X is removed and a weak pull-up transistor PMOS_1 controlled by the output signal q. Thus level of node x is maintained when q equals 0. MHLFF design have circuit simplicity but it has two drawbacks. First, a prolonged 0 to 1 delay is expected since node X is not predischarged. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor NMOS_3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.

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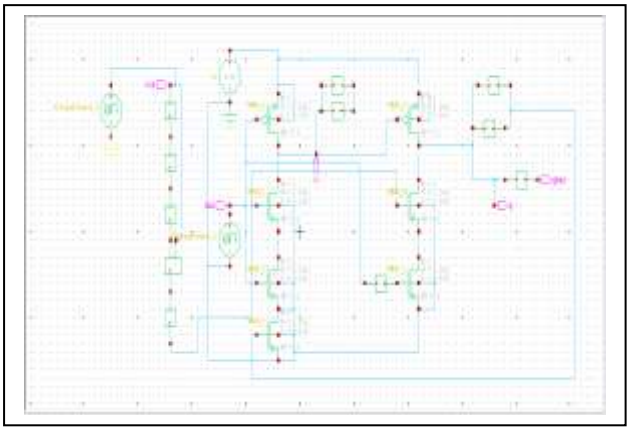

Fig.4 SCDFF

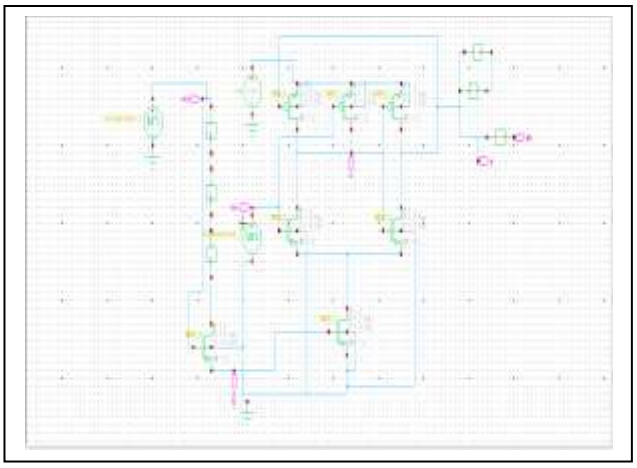

Fig.5 MHLFF

III. TECHNIQUE FOR ENHANCING SPEED AND TO LOWER POWER CONSUMPTION

A. Signal feed-through scheme.

Existing explicit Pulse triggered Flip-flop circuits such as ep-DCO, CDFF, Static-CDFF, MHLFF encounters a problem of delay discrepancy in latching data "1" and "0". The input signal is directly feed to an internal node of latch design to shorten the longer delay which is called as signal feed through scheme. This mechanism can be implemented by introducing a simple pass transistor in latch design which will be controlled by a pulse clock. Hence the combination of pass transistor with the pulse generation circuitry leads to a new P-FF design which can achieve enhanced speed by improving data transitions along with improved power-delay-product performances.

B. Dual Edge Triggering

Power consumption is assessed by several factors including frequency *f*, supply voltage V, data activity α, capacitance C, leakage, and short circuit current [5]. Power dissipation in CMOS circuits can be given as

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage,} \quad (1)$$

The equation represents three major sources of power dissipation i.e. dynamic or switching power dissipation given by equation(2), direct path short circuit power dissipation given by equation (3) and leakage power given by equation (4).

$$P_{dynamic} = \alpha f C V^2 \quad (2)$$

$$P_{short\ circuit} = I_{short\ circuit} * V_{dd.} \quad (3)$$

$$P_{leakage} = I_{leakage} * V_{dd.} \quad (4)$$

From the equations it is clear that decreasing the supply voltage has a quadratic effect on decreasing the power dissipation P. But if we decrease the supply voltage beyond the certain limit, it will lead to exponential increase in the leakage current. Thus, another alternative way to reduce power consumption is reduction in the clock frequency. A single edge triggered Flip-Flop takes the data on the one edge of the clock pulse either on rising edge or falling edge of the clock. But the dual edge triggered flip-flop (DETFF) can sample the

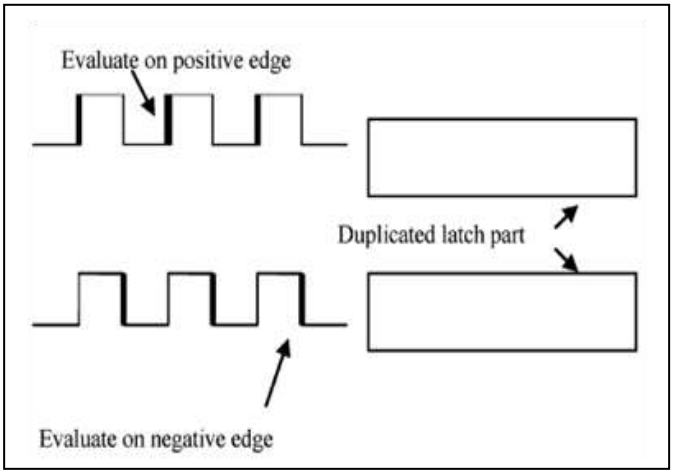

Fig.6 Scheme for conventional DEFF

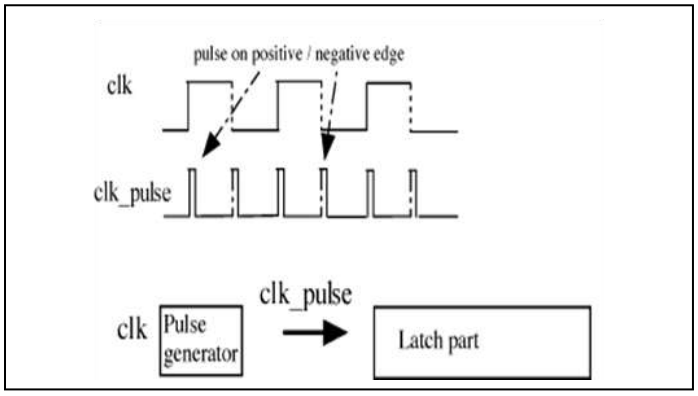

Fig.7 Scheme for proposed explicit pulsed DEFF

input data on rising as well as falling edge. Thus dual edge triggered flip-flop operates on lower clock frequency than single edge triggered flip-flop. Hence consumes less power and increases performance of the system. General Scheme For

conventional dual edge flip-flop is given in "Fig.6"and "Fig.7" represents the general Scheme for proposed P-FF design.

IV. Review Of Techniques For Reducing Switching Activity For Proposed Design

Reducing the switching activity causes reduction in power consumption [3] . In literature many techniques are presented for this purpose. In this paper three techniques are discussed as follows.

C. Conditional Precharge Technique

In this technique, the precharging of internal nodes is avoided when D-input is in high state for long duration. In the precharging path, one PMOS transistor is placed to prevent the redundant switching activity of internal node X when the D-input is in high state. Flip-flops which use conditional precharge technique are CPFF, DE-CPFF and CP-SAFF.

D. Conditional Capture Technique

This technique uses clock gating based method and is mainly used for implicit pulse triggered flip-flops. Q-controlled gate is placed on the path of the delayed clock to the stage one. This technique prevents the redundant switching activity. But use of clock gating causes more power consumption by the gate controlling the delivery of the delayed clock to flip-flop.

E. Conditional Discharge Technique

Conditional precharge technique is better than conditional capture technique but it is difficult to use for dual edge triggering as it requires more transistors. In conditional discharge technique, for the stable high input, the extra switching activity can be eliminated by controlling the discharge path. This technique is suitable for dual edge as well as single edge triggering. Hence in proposed design this technique can be used.

V. Conclusion

In this paper various techniques and designs are presented for achieving high speed and low power consumption. Explicit type P-FF gives speed advantage because of logic separation from latch design and adoption of signal feed-through scheme can shorten the longer delay and enhances both speed and performance. The use of dual edge triggering leads to lower power consumption than single edge triggering. After surveying the different techniques for reducing the switching activity, Conditional discharge technique is better than conditional precharge technique and conditional capture technique for dual edge triggering.

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