

A Literature Review on Leakage and Power Reduction Techniques in CMOS VLSI Design

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Abstract :A rapid growth in semiconductor technology and increasing demand for portable devices powered up by battery has led the manufacturers to scale down the feature size, resulting reduced threshold voltage and thereby enabling integration of extremely complex functionality on a single chip. In CMOS circuits, increased sub-threshold leakage current refers static power dissipation is the result of low threshold voltage. For the most recent CMOS technologies static power dissipation i.e. leakage power dissipation has become a challenging area for VLSI chip designers. According to ITRS (International technology road-map for semiconductors), leakage power is becoming a dominant part of total power consumption. To prolong the battery life of portable devices, leakage power reduction is the primary goal. The main objective of this paper is to present the analysis of leakage components, comprehensive study & analysis of leakage components and to present different proposed leakage power reduction techniques.

Keywords: CMOS, Leakage Power, Sub-threshold Leakage, Threshold voltage.

I. INTRODUCTION

With the advancements in technology, power consumption has become one of the critical design issues. According to Moore's law, with doubling of transistors on a chip device, optimizing the power consumption in a device has become a vital area for research. With scaling, the channel length and the oxide thickness both decreases thereby reduces threshold voltage. This low threshold voltage with scaled supply voltage for high density and improved performance leads to exponential increase in sub-threshold leakage current because transistor cannot be turned off. Researchers have presented several ideas to solve the problem of power dissipation in CMOS circuits. In a CMOS circuit, the total power dissipation is categorised as static power dissipation and dynamic power dissipation. In a stand-by mode, power dissipation is due to stand-by leakage current through each transistor. Dynamic power dissipation is either due to charging and discharging of load capacitance and due to non-zero rise and fall time of input waveforms. There are several current components which are responsible for the leakage power dissipation in VLSI circuits. The modernised cooling and packaging strategies are of little help to the rapid increase of the power consumption in today's chips. The diagram of leakage current mechanism of deep-sub micrometer transistors is depicted below:

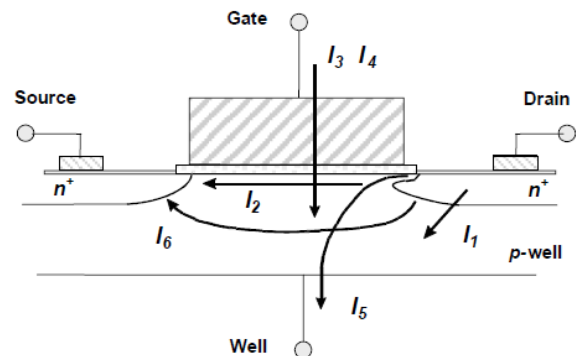


Figure1. Leakage Current Mechanism of deep-submicron transistor

I1 = Reverse-bias p-n junction diode leakage current

I2 = Subthreshold leakage current

I3 = Gate Oxide tunnelling current

I4 = Hot-carrier injection current

I5 = Gate induced drain-leakage current (GIDL)

I6 = Channel punch-through

Apparently, main sources of leakage current are reverse-bias p-n junction leakage, subthreshold leakage and gate oxide tunnelling leakage. The reverse bias p-n junction leakage is either due to minority carrier diffusion/drift near depletion region edge or due to electron-hole pair generation in depletion region. Subthreshold voltage is due to the low threshold voltage due to the reduced potential barrier because of the close vicinity of source and drain regions in short channel devices. Gate oxide leakage occurs due to presence of high electric field across the scaled down oxide

thickness which causes electrons to tunnel either from substrate to gate or gate to substrate. Gate induced drain leakage results due to the movement of minority carriers between channel and substrate regions due to the application of large negative gate bias. Punch through leakage is due to the current flowing between source and drain regions when channel disappears. Hot carrier injection results due to the lowering of threshold voltage by electrons/holes.

II. Leakage reduction technique

In today's VLSI circuits, low power is an important consideration factor along with high performance and high density. There are several techniques to reduce the leakage power but disadvantage of each technique limits its implementation. In this paper, our main focus is to analyse leakage reduction techniques with their usage area.

A. Dual V_T and MTCMOS

This is a basic approach to reduce the leakage power. MTCMOS reduces the leakage by introducing the high threshold NMOS gating between pull down network and ground terminal, in series to low threshold voltage circuitry. As stated in [6] Dual V_T technique is a variation in MTCMOS, in which high threshold voltage can be assigned to transistors of non-critical path to reduce leakage current and low threshold voltage transistors are used in critical paths. An additional mask layer is required due to V_T (Threshold voltage) variation, thereby making fabrication process complicated. This technique suffers from latency period i.e. it need some time to get into normal operating mode after reactivation. The structure for dual V_T and MTCMOS technique is shown as:

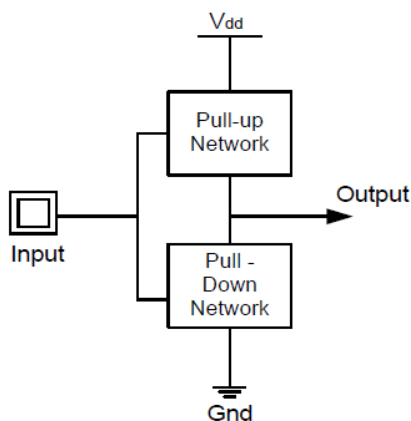


Figure 2: Dual V_T and MTCMOS Structure

B. Sleep Transistor Technique

Addition to the MTCMOS technique, high V_T sleep transistor is introduced between V_{DD} (supply voltage) and pull up network, and between pull down network and ground for high switching speed, where low V_T transistors are used in circuit [10]. Efficient power management is done by sleep control mechanism. This modified MTCMOS

technique can only reduce the standby leakage power and the introduced MOSFETs results increase in area and delay. During stand-by mode both sleep transistors gets turned off, introducing large resistance in conduction path and thus, leakage current is low. Isolation between V_{DD} and ground path is necessary for leakage reduction. This technique faces a problem for data retention purpose during sleep mode. The Wakeup time and energy of the sleep technique have a significant impact on the efficiency of the circuit

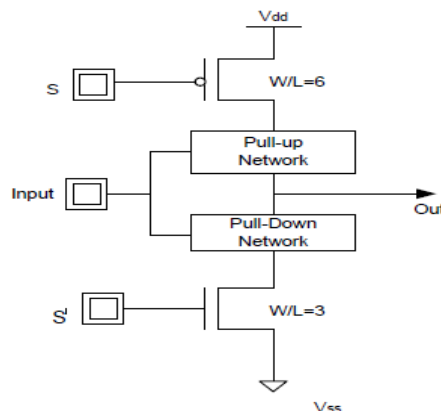


Figure 3: Sleep Transistor Approach

C. Forced Stack Technique

The authors in their work [1] have proposed new technique named as forced stack technique because of the limitations of previously introduced techniques. This technique includes duplication of an already present transistor into two half sized transistors. There exists a reverse bias due to duplicated transistors when both the transistors are turned off, which results in sub threshold leakage current reduction. It is a state retention technique with disadvantage of increased delay and area.

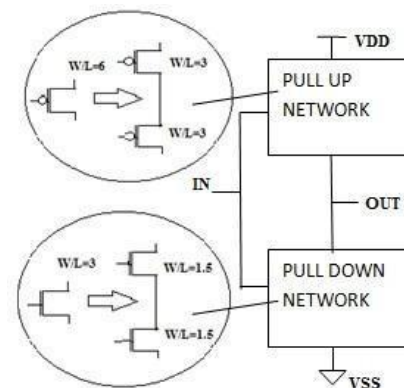


Figure 4: Forced Stack Approach

D. Zigzag Technique

To reduce the power consumption to a maximum possible extent, this technique uses one sleep transistor in each logic state either in pull-up or pull-down network according to a particular input vector. Then, we either assign a sleep

transistor to the pull-down network if the output is '1' or else assign a sleep transistor to the pull-up network if the output is '0'. The zigzag technique is introduced to reduce the wake-up cost by choosing a specific state but it has a limitation of state destruction. As mentioned in [2] it may require extra circuitry to regenerate a specific input vector through some means on wake up mode.

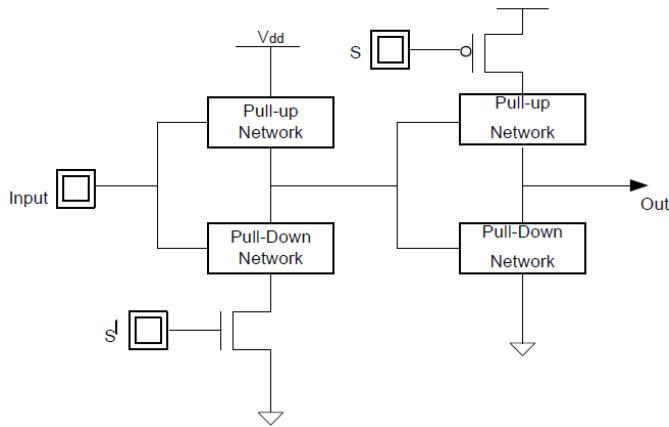


Figure 5: Zigzag Approach

E. Sleepy Stack Technique

This technique combines the features of sleepy transistor technique and forced stack technique. In this technique, the sleep transistor is added parallel to the two half sized transistors configuration is used to replace the original transistor in the circuit. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Variation in the width of sleep transistor results tradeoffs in power, area and delay. Additional control and monitoring circuit is required for the sleep transistor.

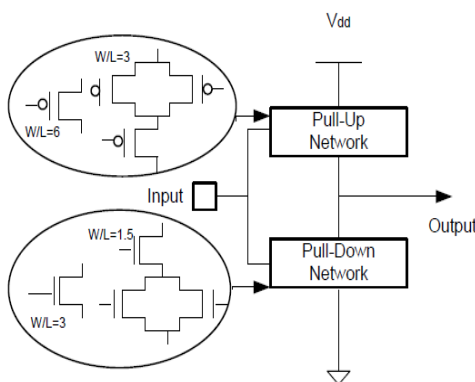


Figure 6: Sleepy Stack Approach

F. Leakage Feedback Technique

To maintain logic during sleep mode, the leakage feedback technique uses two additional transistors and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage

feedback [3]. Performance degradation and increase in area are the limitations along with the limitation of sleep technique.

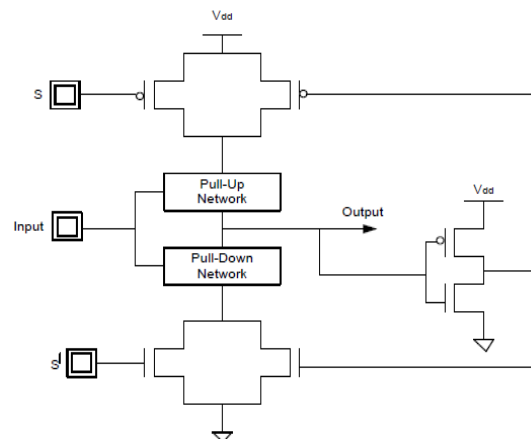


Figure 7: Leakage Feedback Approach

G. Sleepy Keeper Technique

In this technique [7] parallel connected combination of PMOS and NMOS transistor is inserted between pull up network and V_{DD} and pull down network and GND (Ground). When in sleep mode, this additional NMOS transistor is the only source of V_{DD} to the pull-up network and additional PMOS transistor is the only source of GND to the pull down network since the sleep transistor is off. To maintain output value '1' in sleep mode, this approach uses pre-estimated output logic '1' and NMOS transistor connected to V_{DD} . Similarly to retain output logic '0' the PMOS transistor connected to GND is used in sleep mode. This technique uses extra retention transistors to maintain logic state during sleep mode.

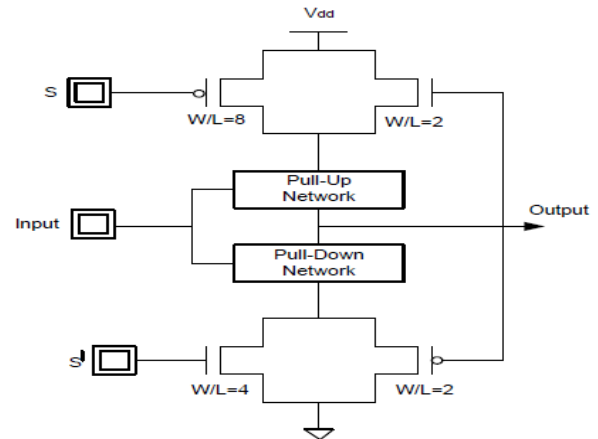


Figure 8: Sleepy Keeper Approach

H. Lector Technique

In LECTOR [8], the concept of effective stacking transistors has been introduced between the V_{DD} and GND for the leakage power reduction. In this technique two leakage control transistors i.e. P-type and N-type are inserted

between the pull up and pull down network of a circuit, in which each LCT gate is controlled by the source of other, hence termed as self-controlled stacked transistors. Since it is a self-controlled technique so no external circuit is required for controlling purpose. These LCT produces high resistance path between the V_{DD} and GND by turning more than one transistor OFF, thereby reducing the leakage current. This technique has a very low leakage but there is no provision of sleep mode of operation for state retention.

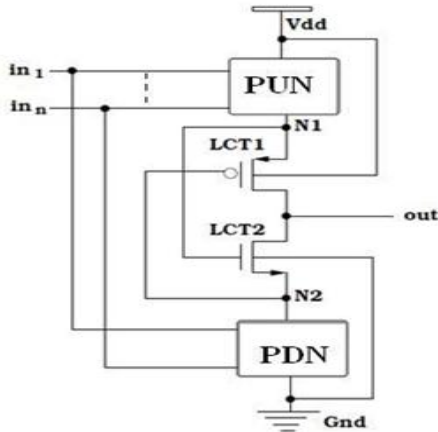


Figure 9: LECTOR Approach

I. GALEOR Technique

Introduction of stacking effect in the circuit results reduction in leakage current flowing across circuit, in GALEOR technique. In this approach, one gate leakage high V_T NMOS transistor is introduced between the output and the pull up network and another gated leakage high V_T PMOS transistor in inserted between output and the pull down network. Due to the threshold voltage loss caused by high V_T MOS transistors, this technique suffers from significant low voltage swing where low logic level appears much above than 0 and high logic level occurs much below than V_{DD} . Increase of propagation delay is result of low output voltage swing.

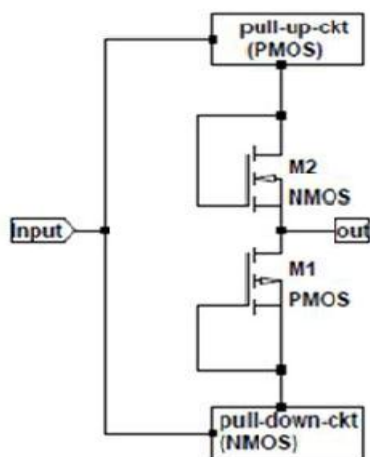


Figure 10: GALEOR Approach

J. LECTOR Stack State Retention (LSSR)

This technique combines the feature of both, LECTOR approach and the Forced Stack Technique with the additional feature of state retention in circuit. The circuit configuration includes [1], two leakage control transistors are added between the pull up and pull down network, and the stack effect is introduced to pull up and pull down network by replacing each existing transistor with two half sized transistors. It provides the limitation of area because of usage of extra transistors to preserve the circuit state during sleep mode. But this technique provides good leakage current reduction without any delay penalty.

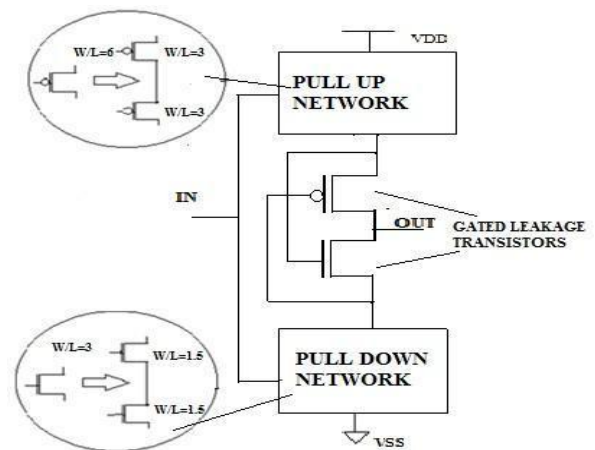


Figure 11: LECTOR Stack State Retention (LSSR) Approach

K. Zigzag Keepers Technique

This approach is proposed to reduce the leakage power consumption to a large extent along with the property of state preservation during sleep mode. Zigzag Keepers approach [9] has added the qualities of both the approaches, Zigzag approach and sleepy Keepers Technique. Here, along with the sleep transistors, two additional transistors which are driven by pre-estimated output logic are introduced in a parallel with sleep transistors which are for saving the logic state.

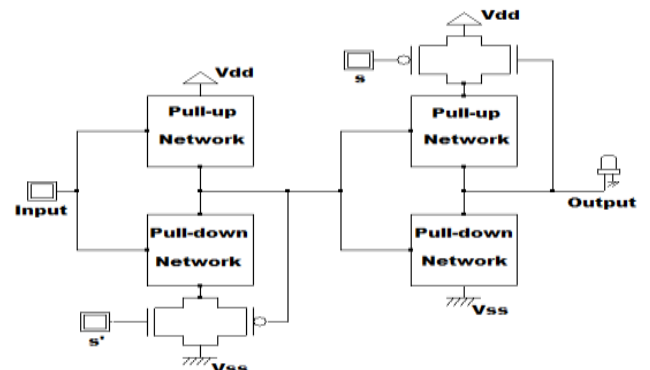


Figure 12: Zigzag Keepers Approach

III. CONCLUSION

With nanometre scale CMOS technology, leakage power consumption is a critical design constraint for the low power portable devices. Recent technological advances in Wireless Communications have shown the convergence of terminals and networks that support multimedia and real-time applications. This obviously puts an immense pressure on the battery of any mobile device. To solve the problem, several approaches have been implanted and still work is in progress on many more. The designers, therefore, have to select particular technique depending on application and product requirements. In this paper, we have presented the several leakage power reduction techniques along with their respective advantages and disadvantages. We conclude that LECTOR and the new approach LSSR circuit may lead to much large reduction of leakage power than the previously introduced techniques.

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