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Analysis of Digitally Controlled Delay Loop-NAND Gate for Glitch Free Design

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Abstract **-** This paper presents a glitch free NAND based digitally controlled delay-lines for the avoidance of glitches. DCDL circuit uses control bits which can be generated using circuits called driving circuits. Different techniques of driving circuits are proposed to reduce the power consumption and the critical path delay. The proposed NAND based DCDLs have been designed in 90nm CMOS technology and it is adopted in the PLL application in order to reduce the power and delay time too. The analysis of present and proposed NAND based DCDL has been represented. Simulation result shows that the circuits designed with modified DCDL reduce both the power consumption and critical path delay.

Keywords **–** *Digitally controlled delay line, NAND based DCDL, glitches, Driving circuits.*

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I. INTRODUCTION

NAND based DCDL is a digital circuit whose delay is controlled by the digital control word. DCDL plays an important role in many applications such as All-Digital Phase Locked Loop (ADPLL) [3], All Digital Delay Locked Loop (ADDLL) [4], [5], All Digital Spread-Spectrum Clock Generator (SSCG) [2], Clock Generators, microprocessors etc.

Glitching is the most common design problem in digital circuits which may affect the results such as loss of data, increased throughput and power consumption. An electronic glitch is an unwanted pulse which occurs in a digital circuit.

In other perception, glitch is an undesired transition or unpredicted output of a digital circuit which occurs before the signal settles to its specified value and hence it results in false output. Glitches occur due to the propagation delay in the digital circuit. The proposed NAND based DCDL avoids the glitches problem and also achieves the low power and delay time.

II. EXISTING METHODOLOGY

A. Glitches problem of NAND based DCDL

NAND based DCDL is constructed by a series of delay elements (DEs) [1]. Each delay element is composed by four NAND gates. In Fig.1, gates marked with 'A' are the fast input of each NAND gate and 'D' are the dummy cells used for load balancing. The delay of the DCDL circuit is controlled through the control bits (S_i), i.e., S_0, S_1, S_2, S_3 and S'i are complementary of those control bits.

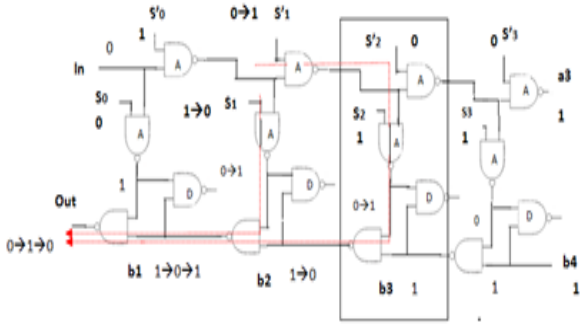

Fig.1.Single glitch when the control code increased by one

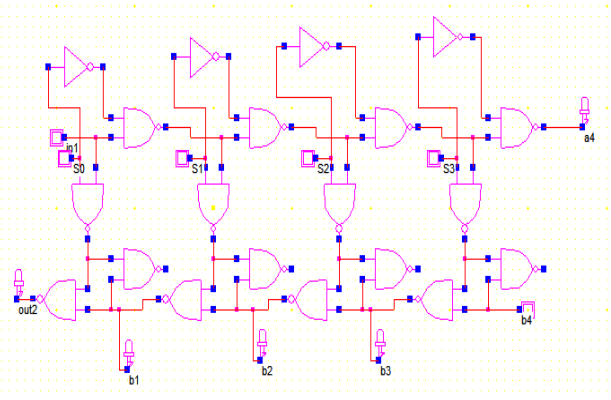

Fig.2. Schematic of NAND based DCDL with glitches

Consider the situation if the control code 'c' is switched from 1(s=0,1,1,1) to 2(s=0,0,1,1), glitches are generated in two different paths as shown in red lines. If it is one bit variation,a single glitch occurs. The corresponding schematic diagram of NAND based DCDL with glitches is shown in Fig.2.The control bits Si encode the delay control code c.

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If i<c, then Si=0 (pass state); if i≥c, then Si=1 (turn state);where i is the number of stages, c is the control code and Si is the control-bits.

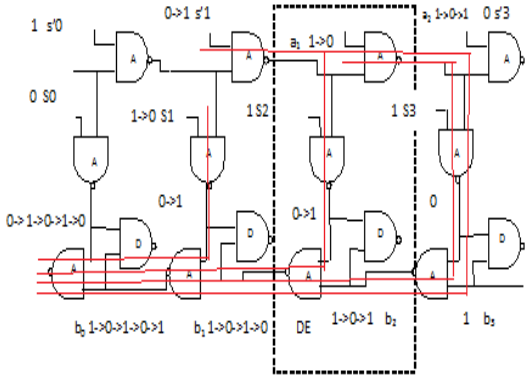

Fig.3. Multiple glitches when the control code increased by more than one

Fig.3 shows, if the control code 'c' is switched from 1(s=0,1,1,1) to 3(s=0,0,0,1), glitches are generated in four different paths as shown in red lines. If there were more than one bit variation, then there would be the occurrence of multiple glitches.

B. Glitch-free NAND based DCDL:

Glitches can be avoided by adding the delay cells 'D' in each stage of DCDL as shown in Fig.4, so that, each delay element in DCDL requires two sets of control bits Si and Ti which controls the DCDL with the conditions:

Consider the state if i<c, then Si=0 and if i ≥c, then Si=1; and also the control code Ti=1 and Tc+1=0 for i≠c+1.

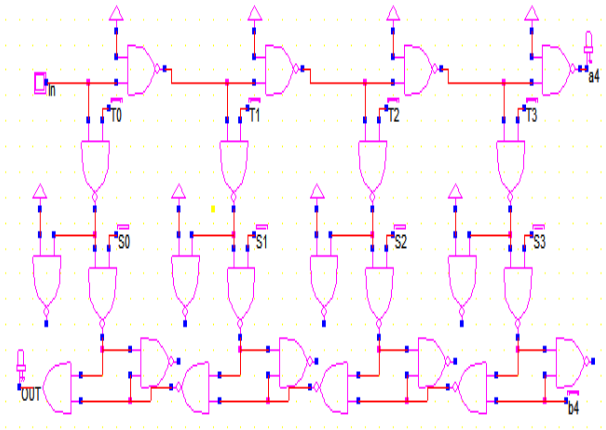

Fig.4.Schematic of glitch-free NAND based DCDL

The three possible delay element states of glitch free DCDL and the corresponding values of Si and Ti are shown in the table I.

TABLE I

POSSIBLE STATES OF DE IN GLITCH-FREE DCDL

S_i	T_i	DE STATE
0	1	*Pass*
1	1	*Turn*
1	0	*Post-Turn*

III. DRIVING CIRCUIT

A. Double clocked sense amplifier based flip-flop

The existing DCDL uses the double clocked flip-flop as a driving circuit [1], [6]. This is one of the special flip-flops which employs two different clock signals, so that it can provide different delays for LH and HL transitions. One of these clock signals is CLH. i.e., clock signal rises when low to high transitions.

Another one is CHL. i.e., Clock signal falls when high to low transitions. But this too have some of the drawbacks such as consumption of more power and consumes more delay time.

This sense amplifier based flip-flop consists of SA (sense amplifier) in the first stage and set-reset (SR) latch in the second stage. This technique is shown in the Fig.5.

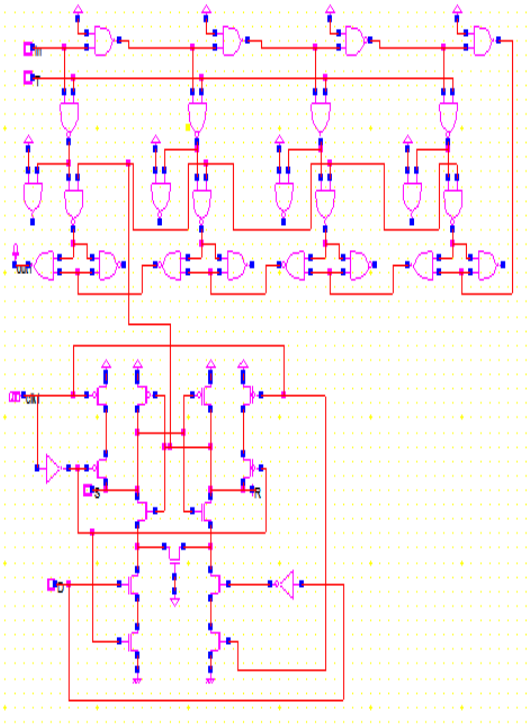

Fig.5. Schematic of Existing DCDL with double clocked sense amplifier based flip-flop

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IV. PROPOSED DCDL SYSTEM

Proposed DCDL uses various flip-flop techniques as a driving circuit. This thereby reduces power consumption and path delay.

A. Dual edge triggered sense amplifier based flip-flop

This flip-flop provides the pulse at both rising and falling edges. It can be constructed using three stages. They are pulse generating stage, sensing stage and latching stage. The first stage is used to generate the pulses; second stage is used to sense the pulse and third stage used to produce the output at rising and falling edges. The main advantage of this flip-flop is consuming less power rather than the other proposed flip-flop techniques. This technique is represented in Fig.6.

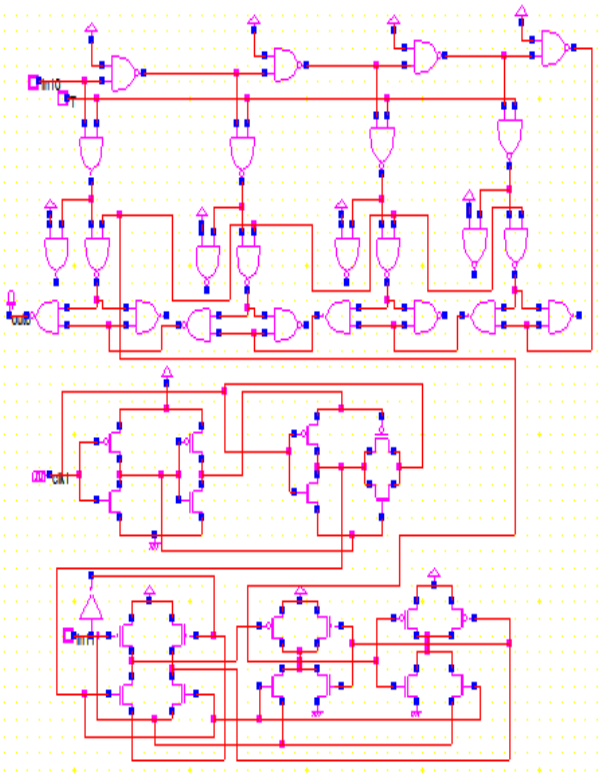

Fig.6. Schematic of Proposed DCDL with dual edge triggered sense amplifier based flip-flop

B. NIKOLIC- sense amplifier based flip-flop

A clocked CMOS based design is shown in the Fig.7. It can be constructed using inverter, cross coupled inverter, PMOS transistors at both Q and QB and four extra transistors are used to drive the flip-flop. A role of this flip-flop is to reduce the use of clock signal so that NIKOLIC latch had a better power consumption.

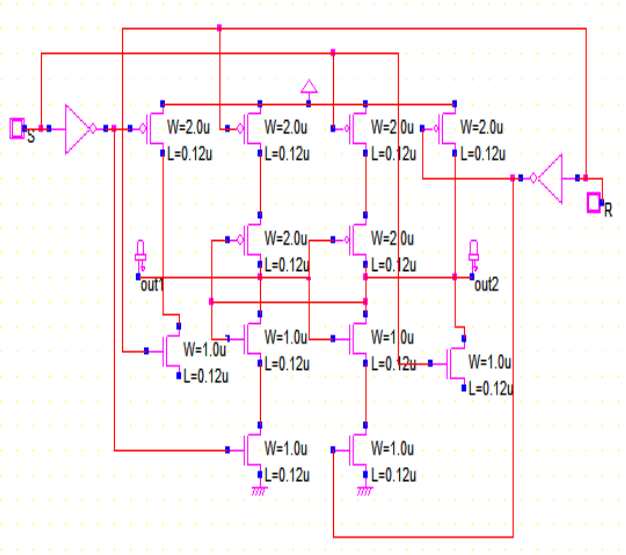

Fig.7. NIKOLIC- sense amplifier based flip-flop

V. SIMULATION ANALYSIS

A. Simulation result of glitches in NAND based DCDL

The schematic of NAND based DCDL circuit is designed in DSCH tool and simulated with the help of MICROWIND tool. The parameter description of the below simulation result with initial input In, output OUT and control bits S0, S1, S2, S3.

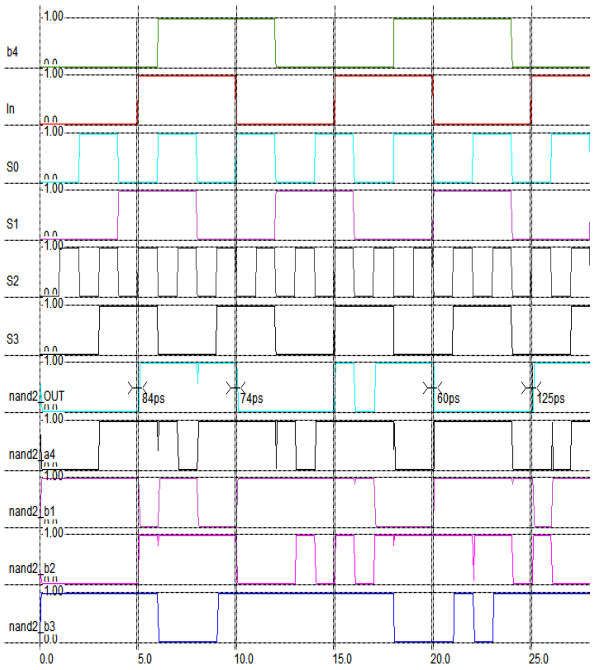

Fig.8.Simulation result of glitches in NAND based DCDL

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B. Simulation result of glitch free NAND based DCDL

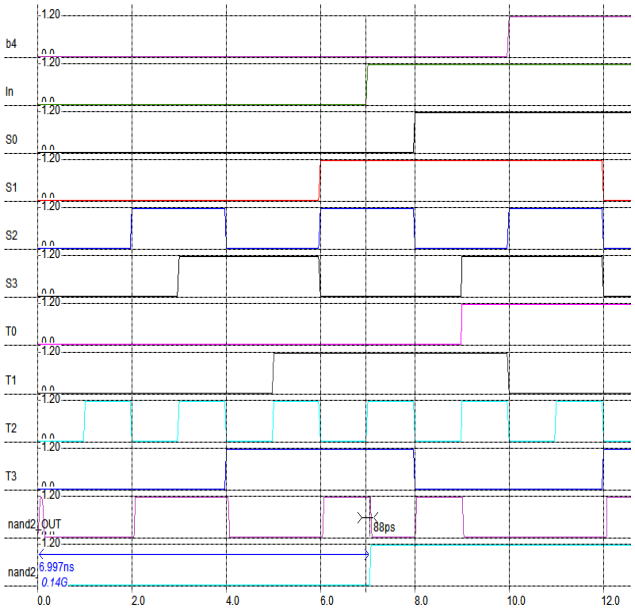

Fig.9. Simulation result of glitch free NAND based DCDL

During the switching activity, the output of the DCDL produces without glitches.

C. Simulation result of DCDL with double clocked flipflop

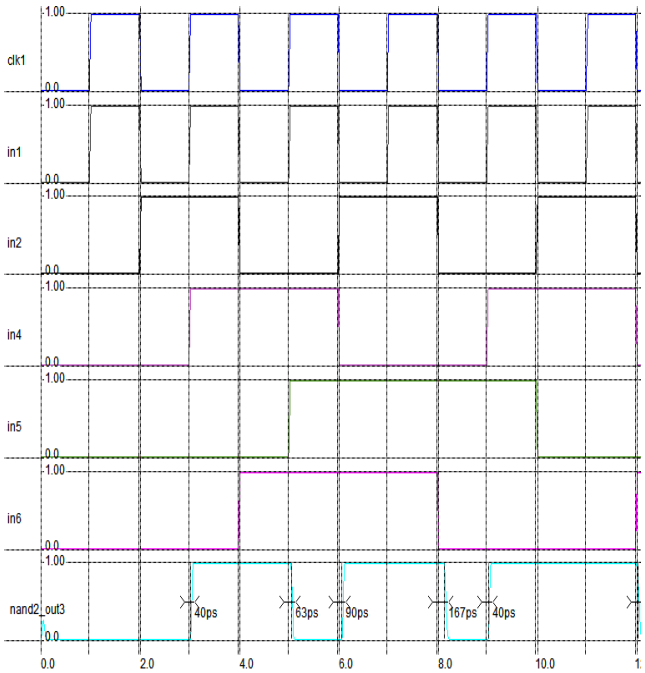

Fig.10. DCDL with double clocked flip-flop

Simulation result of Existing DCDL with double clock flip-flop as shown in the fig.10.

D. Simulation result of proposed DCDL with dual edge triggered flip-flop

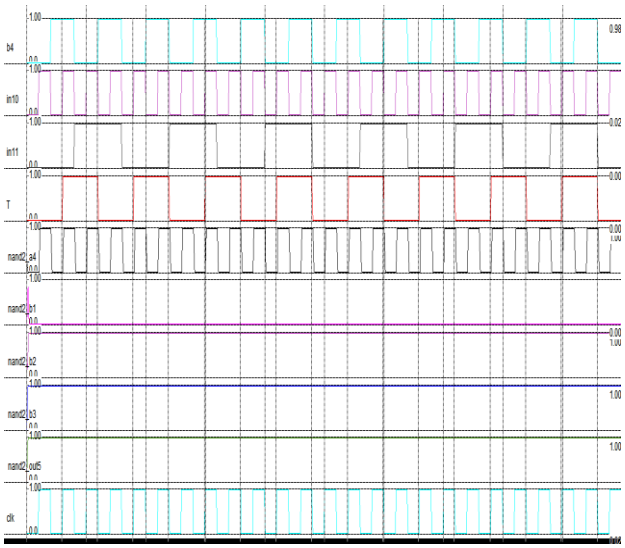

Fig.10. Simulation result of proposed DCDL with dual edge triggered flip-flop

This is the simulation result of proposed DCDL with dual edge triggered flip-flop. It consumes less power than existing DCDL.

VI. RESULT ANALYSIS

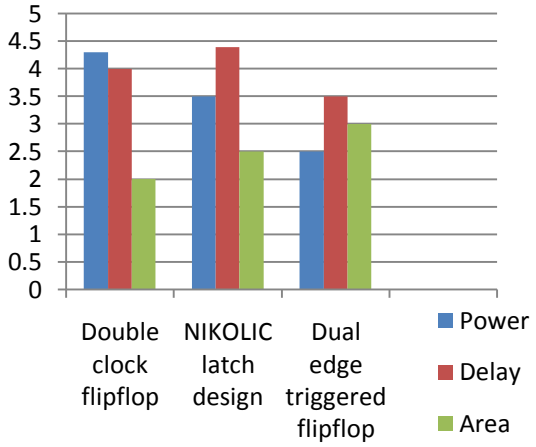

Fig.11. Comparison chart for power, area and delay

The result analysis shows that the dual edge triggered sense amplifier based flip-flop had better performances in power and delay than conventional sense amplifier flip-flop.

VI. CONCLUSION

In this paper, a glitch-free NAND based DCDL has been presented which avoids the glitch problem. Two different techniques of driving circuit have been considered to generate the control bits for DCDL. By using these techniques, low power consumption and critical path delay are achieved. All the simulation results are carried out using MICROWIND technology, designed at 90nm CMOS technology.

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FUTURE WORK

The future work may be preceded with this proposed DCDL by implementing it in applications such as Phase Locked Loop, which reduces power consumption and delay time.

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