International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 2 Issue: 8 2415 – 2418

Impact of LFSR Seeding on the Test Pattern Generator in BIST

Mohammed Sabir Hussain
Assistant Professor, ECE Dept,
Muffakham Jah College of Engg & Tech,
Hyderabad, India.
Email: sabir.mj@gmail.com

Syed Mohd Ali Faraz
Student, M.E. (Digital Systems),
Muffakham Jah College of Engg & Tech,
Hyderabad, India.
Email: syed.ma.faraz@gmail.com

Abstract: This paper considers the problem of minimizing the power required to test a BIST based combinational circuit without modifying the test pattern generator and with no extra area or delay overhead. The objective of this paper is to analyze the impact of the polynomial and seed selection of the LFSR on the power consumed by the circuit. It is shown that proper selection of the seed of the LFSR can lead to significant decrease in the power consumption of the BIST sessions. For this purpose, a Bit Flipping LFSR is used as a test pattern generator in the BIST design. Experimental results using the ISCAS benchmark circuits are reported, showing variations of the seed selected for the LFSR, the power consumed is ranging from 5.5% to 13.5%.

Keywords*: Linear Feedback Shift Register (LFSR), Logic BIST, Low Power Test Pattern Generator, Array Multiplier.*

*****

I. INTRODUCTION

The main challenging problem today, in the system on chip (SoC) design and testing is power dissipation. The power dissipation of a system in test mode is more than that of the power dissipation in the normal mode[1]. The reason for this is the significant correlation between the consecutive test inputs given to the circuit during its normal operation, while this may not be necessarily true for applied test vectors in the testing mode. Less correlation between the test vectors leads to increased switching activity which eventually leads to power dissipation in the circuit. There are two main sources of power dissipation in digital circuits viz. static power dissipation and dynamic power dissipation. Static power dissipation in a circuit is mainly due to the leakage current and its contribution to the overall power dissipation is negligible. Dynamic power dissipation is due to switching i.e. the power consumed due to short circuit current flow and charging of load capacitances given by the equation:

$$P=0.5V_{DD}^2E(sw)C_LF_{clk} \text{ ---------- } (1)$$

Where V_{DD} is supply voltage, E(sw) is the average number of output transitions per$1/f_{clk}$, f_{clk} is the clock frequency and C_L is the physical capacitance at the output of the gate. From the above equation it is clear that the dynamic power dissipation depends on three parameters: supply voltage, Clock frequency, switching activity. To reduce the dynamic power dissipation by considering the first two factors degrades the performance of the circuit. When power reduction is done considering the switching activity, the performance of the circuit is not compromised [1].

In VLSI circuit design, BIST architecture is mainly used for testing. The primary goal of BIST is to reduce the power dissipation without degrading the overall system performance and fault coverage [2]. BIST has now become an alternative solution to the increasing costs of external circuit testing. The BIST approach promises to find greater use in a wide variety of circumstances as more and better BIST techniques are developed [2].

The rest of the paper is organized as follows. In section II, previous works related to power optimization in BIST have been proposed. Section III presents an overview of the BIST architecture. In section IV, an Algorithm for the low power test pattern generation is presented along with the Circuit under test (CUT) i.e. an Array Multiplier and its architecture being discussed briefly. In section V comparisons of the results are done between the existing method and the proposed method and finally this section summarizes the conclusion and future scope of work.

II. PRIOR WORK

Various authors report on techniques to cope with power problems during testing, few techniques of the earliest works that have been proposed for optimizing the power during testing are discussed in this section of the paper. Balwinder, Arun and Sukhleen present power optimization of linear feedback shift register for low power BIST using novel bipartite technique [1]. A modified clock scheme in which only half of the D flip-flops work, thus only half of the test pattern can be switched proposed in [4]. In [6] and [7] S.K.Guptha proposed a BIST TPG for low switching activity in which there is d-times clock frequency between slow LFSR and normal LFSR and thus the test pattern generated by original LFSR is rearranged to reduce the switch frequency. LT-TPG is proposed in [6] to reduce the average and peak power of a circuit during test. The above said techniques can reduce the average power compared to traditional linear feedback shift register (LFSR).A better low power can be achieved by using single input change pattern generators. It is proposed by Kavitha and Seetharaman in [2] that the combination of LFSR and scan shift register is used to generate random single input charge sequences. M.Suriya and Mohandas in [3] proposed that (2^m-1) single input change test vectors can be inserted between two adjustment

ISSN: 2321-8169
2415 – 2418

vectors generated by LFSR, where m is the length of the LFSR.

III. TPG ARCHITECTURE

BIST is a DFT methodology that aims at detecting faulty components in a system by incorporating the test logic on chip. Built-In-Self-Test (BIST) has emerged as a promising solution to the VLSI testing problems. BIST is well known for its numerous advantages such as improved testability, at-speed testing, and reduced need for automatic test equipment (ATE). In BIST, a linear feedback shift register (LFSR) generates test patterns and a multiple input shift register (MISR) compacts test responses. Test vectors that are applied to a circuit under test at nominal operating frequency may have more average and/or peak power dissipation than those in normal mode. The reason is that the random nature of patterns reduces the correlation between the pseudorandom patterns generated by LFSR compared to normal functional vectors. It results in more switching and power dissipation in test mode [4].

A typical BIST architecture consists of a test pattern generator (TPG), usually implemented as a Linear Feedback Shift Register (LFSR), a test response analyzer (TRA), implemented as a Multiple input signature register (MISR), and a BIST control unit (BCU), all implemented on the chip. This approach allows applying at-speed test patterns and eliminates the need for an external tester. The TPG architecture components are explained below.

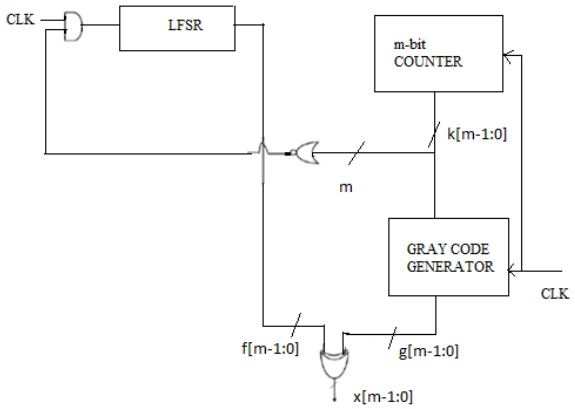

Fig 1 : The TPG Structure

An LFSR is used to generate test patterns for BIST. In this paper, we designed three different architectures of LFSR which generates the test patterns with reduced switching activities. TPG structure consists of linear feedback shift register , m-bit counter, gray counter, NOR-gate structure and XOR-array. The m-bit counter is initialized with Zeros and which generates 2m test patterns in sequence. The m-bit counter and gray code generator are controlled by common clock signal [CLK]. The output of m-bit counter is applied as input to gray code generator and NOR-gate structure. When all the bits of counter output are Zero, the NOR-gate output is one. Only when the NOR-gate output is one, the clock signal is applied to activate the LFSR which generates the next seed. The seed generated from LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns.

IV. LOW POWER ALGORITHM

A. Standard Exor LFSR

Figure 2 shows an external Exor LFSR also called standard LFSR; it is basically a shift register having D flip-flops where the output of the last flip-flop provides feedback to the input of the first flip-flop. If there are *n* flip-flops, then the LFSR is called *n* -stage LFSR. The feedback is basically a linear XOR function of the outputs of the flip-flops. Output of any flip-flop may or may not participate in the XOR function; if output of any flip-flop X_i say, provides input to the XOR function then corresponding tap point h_i is 1. Similarly, if output of flip-flop X_i does not provide input to the XOR function then corresponding tap point h_i is 0. In the circuit if h_i =0, then there is no XOR gate in the feedback network corresponding to the output of the flip-flop X_i; otherwise, the XOR gate is included. A properly-designed LFSR can generate as a near-exhaustive set of patters, as it can cycle through distinct 2^n-1 states except all 0s, If the seed is all 0 state, then the LFSR will be stuck at all 0 state. Because of simplicity of the circuit and less area occupation, linear feedback shift register [LFSR] is used at the maximum for generating test patterns [6]. In this paper, we proposed a novel architecture by replacing XOR function which generates the test patterns with reduced switching activities using multiplexer based LFSR and compared with Exor-LFSR.

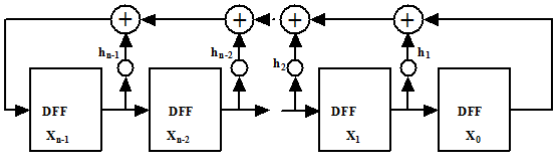

Figure 2: Standard Exor LFSR

In Multiplexer based LFSR all the XOR functions of conventional LFSR are replaced with 2x1 MUX and inverter hence this modified LFSR reduces switching activities compared to conventional method as shown in figure 3.

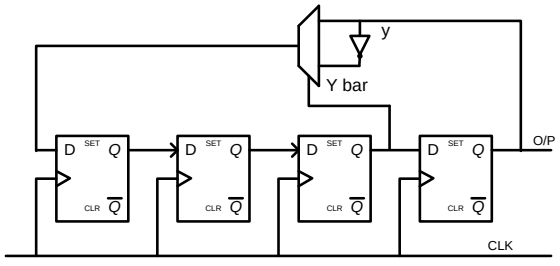

Figure 3. MUX based LFSR

B. Bit Flipping LFSR

The algorithm for BF-LFSR is given below:

- Consider a n-bit standard linear feedback shift register [n>2].The proposed designed consist of

 ISSN: 2321-8169
2415 – 2418

n=16, which consists of 16-flip flops in series. A common clock signal is applied as control signal for all flip flops.

- The XOR of conventional LFSR design in terms of 2x1 Multiplexer by adding extra inverter gate to achieve required patterns.
- The seed generated from modified LFSR is Exclusive–ORed with the data generated from gray code generator. The patterns generated from the Exclusive–OR array are the final output patterns

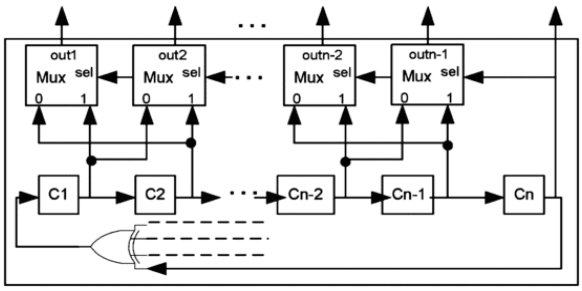

Figure 4. Bit Flipping LFSR

- Gray converter modifies the counter output such that two successive values of its output are differing in only one bit. Gray converters can be implemented as shown below.

g[n-1]= k [n-1]
g[n-2]= k [n-1] XOR k[n-2]
.
.
g[2]= k [2] XOR k[3]
g[1]= k[1] XOR k[2]
g[0]= k[0] XOR k[1]

In [2] it is stated that that the conventional LFSR's outputs cannot be taken as the seed directly, because some seeds may share the same vectors. Thus the proposed LFSR should ensure that any two of the signal input changing sequences do not share the same vectors or share as few vectors as possible. Test patterns generated from the proposed structure are implemented as following equations.

x[0] = f[0] XOR g[0]
x[1] = f[1] XOR g[1]
x[2] = f[2] XOR g[2]
x[3] = f[3] XOR g[3]
x[4] = f[4] XOR g[4]
x[5] = f[5] XOR g[5]
.
.
.
X [n-1] = f[n-1] XOR g[n-1]

Thus the XOR result of the sequences is single input changing sequence. In turn reduces the switching activity and so power dissipation is very less compared with conventional LFSR. Below is an example of counter and its respective gray value. It is shown that all values of g[2:0] are single input changing patterns.

Patterns**:**

K [2:0]	g [2:0]
K0= 000	g0= 000
K1= 001	g1= 001
K2= 010	g2= 011
K3= 011	g3= 010
K4= 100	g4= 110
K5= 101	g5= 111
K6= 110	g6= 101
K7= 111	g7= 100

The above figures 2 & 3 show a pictorial comparison between the conventional Exor LFSR and the modified MUX based LFSR. Finally modified Bit Flipping (BF-LFSR) is used generate effective test patterns using different seed values, then the lowest transition seeded value consumes less power when compared to the other seeds generated by LFSR circuit to test ISCAS 85 benchmark circuits.

C. Array Multiplier (CUT)

Multipliers are widely used in DSP operations such as convolution for filtering, correlation and filter banks for multirate signal processing. Without multipliers, no computations can be done in DSP applications. For that reason, multipliers are chosen for testing in our proposed design.
Braun array multiplier is selected among various multipliers as it follows simple conventional method.

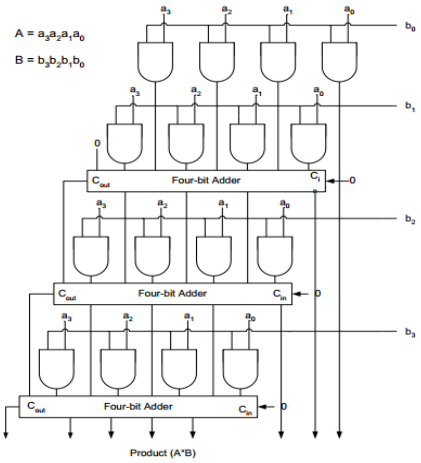

Figure 5: Braun Array Multiplier

Also, pipelined Braun array multiplier is selected as it is faster in speed than non-pipelined multiplier. To avoid carry propagation delay at every stage, the carry bits are propagated to the next stage. Finally at the last stage, ripple carry adder is used to get the product term. By instantiating four such 4x4 Array Multipliers, we obtained a 16x16 Array Multiplier and the same has been used as circuit under test.

V. RESULTS AND CONCLUSION

The results obtained from the Xilinx 14.5 implementation with the device xc3s200-4pq208 in which we have

generated VCD file after the post simulation. Xpower Analyzer is used to calculate the power.

Table 1: Comparison of power on various seed values

SEED VALUE	11111111 00000000	11110000 11110000	11001100 11001100	10101010 10101010
NO. OF BIT TRANSITIONS	1	3	7	15
XOR LFSR (mw)	102	104	107	116
% POWER SAVING XOR LFSR	12	10.3	7.7	--
MUX LFSR (mw)	99	102	105	112
% POWER SAVING MUX LFSR	11	8.9	6.25	--
BFLFSR (mw)	96	99	103	109
%POWER SAVING BF LFSR	13.5	9.1	5.5	--

Results are obtained for each case and compared in terms of number of bit transitions and power dissipation is made on the basis of experimental reports is given table 1. It is observed that as the bit transitions decrease total power consumed ranges between 5.5% and 13.5%. Hence it is concluded that an efficient low power LFSR can be designed by the effective seeded value of LFSR. It is useful for BIST implementation in which the CUT may be combinational, sequential or a memory circuit.

REFERENCES

[1] Balwinder Singh, Arun khosla and Sukhleen Bindra "Power Optimization of linear feedback shift register(LFSR) for low power BIST", IEEE international advance computing conference, Patiala, India 6-7 March 2009.

[2] A.Kavitha,G.Seetharaman,T.N.Prabhakar and Shrinithi "Design of Low Power TPG using LP/LFSR", 3rd IEEE Conference on international conference on intelligent systems modeling and simulation 2012.

[3] Mohammad Tehranipoor, Mehrdad Nourani, Nisar Ahmed, "Low Transition LFSR for BIST Based Applications",

[4] S.C. Lei, X.Y.Hou ,Z.B.Shao and F.Liang," A class of SIC circuits: theory and application in BIST design," IEEE trans. circuits syst. II, vol.55,no.2,pp.161-165,Feb.2008.

[5] DS-LFSR : A BIST TPG for Low Switching Activity. Seongmoon Wang, Sandeep K. Gupta. IEEE transactions on Computer-Aided Design of Integrated Circuits and Systems. Vol.21,No 7 July 2002.

[6] N. Ahmed, M. Tehranipoor, and M. Nourani, "Low Power Pattern Generation for BIST Architecture," Proc. Int'l Symp. Circuits and Systems, vol. 2, pp. 689-692, 2004.

[7] M. Tehranipoor, M. Nourani, and N. Ahmed, "Low Transition LFSR for BIST-Based Applications," Proc. IEEE 14th Asian Test Symp, 2005.

[8] M.Suriya, R.Mohandas, Design and Implementation of Low Transition LFSR for Efficient BIST Architectures, International Journal of Engineering Research & Technology (IJERT) ISSN: 2278-0

[9] Low Power Testing of VLSI circuits:Problems and Solutions. Patrick Gigard.

[10] F.Corno, M.Rebaudengo, M.Sonza Reorda, "A Test Pattern Generation Methodology for Low Power Consumption", pp.1-5, 2008.

[11] Tiwari, Honey Durga, et al., "Multiplier design based on ancient Indian Vedic Mathematics," Int. SoC Design Conf., 2008, vol. 2. IEEE Proc., pp. II-65 - II-68.

[12] N. Basturkmen, S. Reddy, and I. Pomeranz, "A Low Power Pseudo-Random BIST Technique," Proc. 1st International Conference on Computer Design, pp. 468-473, 2002.