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# "Review On High Performance Quaternary Arithmetic and Logical Unit in Standard CMOS"

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***Abstract*—**Arithmetic circuits play an important role in computational circuits. Multiple Valued Logic (MVL) provides higher density per integrated circuit area compared to traditional two valued binary logic. Quaternary (Four-valued) logic also provides easy interfacing to binary logic because radix 4($2^2$) allows for the use of simple encoding/decoding circuits. The functional completeness is proved by a set of fundamental quaternary cells and the collection of cells based on the Supplementary Symmetrical Logic Circuit Structure (SUSLOC). Cells are designed, simulated, and used to build several quaternary fixed-point arithmetic circuits such as adders, multipliers etc. These SUSLOC circuit cells are validated using SPICE models and the arithmetic architectures are validated using System Verilog models for functional correctness. Quaternary (radix-4) dual operand encoding principles are applied to optimize power and performance of adder circuits using standard CMOS gates technologies.

***Index Terms*—** *Quaternary logic, standard CMOS technology, Multi valued logic (MVL), Symmetrical Logic Circuit Structure (SUSLOC).*

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## I. INTRODUCTION

The remarkable increase in the density of Very Large Scale Integrated (VLSI) circuits is the result of advanced Integrated Circuits (IC) fabrication processes and the progress of automated design tools. When the number of devices accommodated on VLSI chips increases, many problems arise. The interconnection between devices inside and outside a chip becomes significantly complicated and the area occupied by interconnections rise in haste. Aggressive interconnect scaling following Moore's law introduces many challenges in integration, performance and reliability. Inappropriate routing results in a larger chip size and cause timing and cross-talk problems. In deep submicron designs these problems are of outstanding importance.

The partial solutions to this problem in today's VLSI circuits are to use several metal layers, flip-chips and other methods. Improvement in metal stack material have enabled industry to reduce interconnect resistance in narrow lines and at the same time changes in interlayer dielectric (ILD) material have lowered the line to line capacitance resulting in Resistor-Capacitor (RC) delay improvement and thus interconnect power consumption, and deep submicron technology introduces formidable integration and reliability challenges such as higher narrow Cu line resistivity, higher current density and inferior thermo-mechanical properties which must be overcome. It is well known that the binary number system is the leading choice for conventional voltage-mode design of digital systems. However, in a typical binary number system based VLSI circuit about 70 percent of chip area is occupied by interconnections which occupy a large portion of physical area even when it is not in use. Therefore the interconnections will be more efficient if several levels of logic are injected into a single wire, as in multiple valued logics (MVL). Not similar to binary logic, multiple valued logics require more than two discrete levels of logic signals and allow more than two logical concepts to present in a logic system. So, the direct benefit of such logics is the improved overall information efficiency. It is because each r-valued signal can carry times more information than a binary signal does. As a result the routing area is reduced on a logarithmic scale as r increases. This reduction in number of interconnections and area of a chip. As can be seen, the routing area of a 4-valued logic design is two times smaller than the corresponding binary logic system. 2 log r logr 2 the choice of the most favorable logic radix in term of implementation cost has been also studied by some researchers. The circuit implementation cost is decreasing with increasing logic radix and according to C.M. Allen and D. Given, the optimal radix is greater than Euler constant. Since in practice the radix r is an integer, it comprehends that the more advantageous radix must be at least 3. Secondly, conversion with binary is most efficient if special radices are chosen in such a way that no information is lost or left unused.

## II. SUSLOC TECHNOLOGY

Several implementation methods have been proposed in the recent past to realize the MVL circuits. The MVL circuits can be categorized as: Current-mode, Voltage-mode and Mixed-mode circuits. Current-mode circuits have been popular and offer many benefits. Its power consumption is high if they

compared to Voltage-mode circuits due to their inherent nature of constant current flow during the functional
operation. Alternatively, Voltage-mode circuits consume a large majority of power only during the logic level switching plus any additional leakage currents that may be present. So, Voltage-mode circuits do offer minimum power consumption which has been the key benefit of traditional CMOS binary logic circuits from the perspective of dynamic switching activity. Lower power is shown in traditional CMOS binary logic circuits for several technology nodes. Because of increased proliferation of portable battery powered personal computation devices, reduced power dissipation is an important design constraint and motivates us to explore Voltage-mode multiple-valued circuits MVL technology primarily refers to circuit technologies where more than two logic levels are used to represent signal levels design larger circuits. Now,a self-sustaining and consistent circuit architecture called the Supplementary Symmetrical Logic Circuit (referred as SUSLOC) structure is proposed and patented. This proposed circuit architecture also allows the use of readily available circuit elements to construct logic circuits based on any radix number system.

We required 3 things to design quaternary MVL circuits using SUSLOC:

1) There are three different sources of power available, with each source of power representing one of three different logic levels with the ground plane representing the fourth level

2) There is one controllable path, or branch, from a source of power to an output terminal of the circuit per output logic level and

3) That one controllable path, or branch, conducts from a source of power to an output terminal per input logic level, contiguous group of input logic levels, or a unique combination of input logic levels.

## III. RADIX SELECTION

Several factors have influence in deciding the best radix usable. Obviously, in theory, higher radix would be best to represent as many numbers as possible. But, in practice, the limits of usability and availability of suitable devices limits the usability of higher radix based MVL circuits.

i. **Area**: Increased data density of multiple valued logic circuits does help, in principle, to reduce the area when compared to equivalent binary circuits. Each of the circuits stores more information per bit. Then net result is that the large amount of data sets can be combined and implemented in minimum area. At smaller circuits, the additional overhead of "supplementary" logic in the proposed SUSLOC circuit structures does increase the area when compared to their equivalent binary gates. The area advantages can only be seen in larger circuits. Maximum radices would allow the increased number of functions that can be implemented, making it easier for larger and more complex functions implementation

The interface from binary logic to the MVL logic does need to have the level conversion to allow successful integration as shown in fig.1. Circuits called "radix converters" help to address the cross-region interface requirement. The radix conversion is simple for radices which are power of two ($2^x$). (Example, radix-2, radix-4 and radix-8, radix-16 etc.) The radix conversion process gets complex and more careful handling for other radices like radix-3, radix-5, radix-6, radix-7, radix-9 etc.

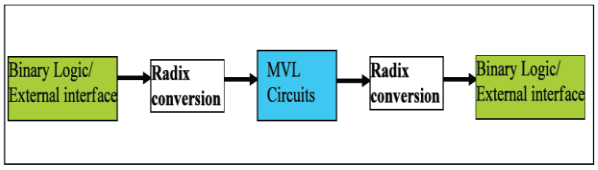


**Figure 1: Area Impact due to Radix Conversion**

So, the area advantages can only be seen in larger circuits. The logic duplication due to binary logic spread is avoided in MVL circuits. And maximum radices would allow the increased number of functions that can be implemented, making it easier for large and more complex functions implementation. Another important advantage is the reduction of signal connections/wires. The reduced wires would reduce the size of the chip and also improve the rout ability of the design. One of the critical challenges in the Deep Sub-Micron technologies is the routing congestion and also the printability (fabrication) of close proximity of the wires. The limitations of the existing fabrication equipment would create several manufacturing defects like close of the wires, open of the wires etc. make lot of part defects and yield loss. So, reducing the number of wires would significantly improve the device manufacturability and area improvement.

ii. **Performance:** Performance of multiple valued circuits gets better with the increased radix. For maximum radix, the more difficult the timing analysis would get because we need to account for several design margins for various physical and electrical effects. But, primarily, the increase in radix would achieve better performance with some caveats of increased complexities in the actual timing closure.

iii. **Power consumption:** Power primarily consists of three parts: Dynamic power, Active leakage power and Standby leakage power. The Dynamic power is also referred to as the Switching power. Typically, this power is dominant of total power consisting of 70-75% of the total power. The Active leakage being the next higher component, generally

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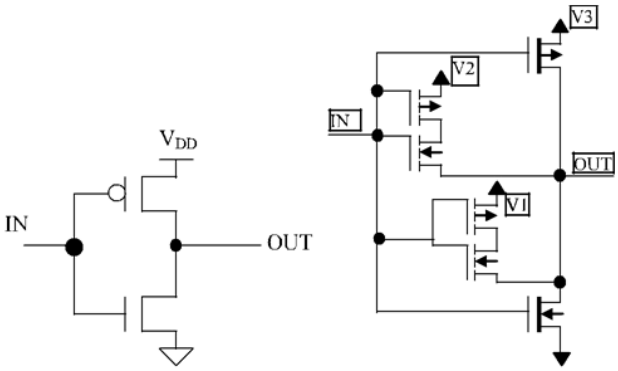
consisting of 15-20% range. The remaining 5-10% power is the leakage power.




a) CMOS inverter b) Quaternary Radix-4 inverter

**Figure 2: Inverter Comparison: Radix-2 vs Radix-4**

The comparison of power can be done using the Quaternary inverter case. As can be seen from the Figure 2, Radix-4 circuit (SUSLOC) requires additional two transistors for each logic level. Every additional transistor introduces the additional input capacitance. For correct comparison, each SUSLOC inverter is equivalent of two CMOS binary inverters

## IV. Validation of Quaternary Circuits

The methodology used is to design the quaternary cells at the transistor level and using SPICE simulations to characterize their behavior. The quaternary cells are then used to manually construct the addition and multiplier circuit architectures. The architectures are functionally simulated using the System Verilog language that allows for efficient modeling capabilities for the description and simulation of large MVL circuits. Analysis of resulting circuits is performed using commercially available Synopsys tools. The equivalent two-valued (binary) logic circuits are coded in
Verilog HDL and synthesized using Synopsys design compiler for benchmarking. Area (number of transistors), Switching power and logic depth (number of stages in timing
critical path) are used as metrics for comparison to quaternary circuits with their binary circuits.

## V. LITERATURE REVIEW

According to review paper [1] present a full adder prototype based on the designed LUT (look up table), fabricated in a CMOS technology, will work at 100 MHz while consuming 122 μW(power). Results demonstrate the correct quaternary and confirm the power efficiency of the proposed design. By using CMOS technology we can design Arithmetic and logical unit which is not presented in this paper. We can use DLC circuit for designing ALU.

According to review paper [2] here they propose an arithmetic unit based on QSD number system based on quaternary system. The given design is developed using VHDL and implemented on FPGA device and results are compared with conventional arithmetic unit. Here we can use standard CMOS technology for designing Arithmetic and logical unit. The circuit performed with standard CMOS technology, with a voltage supply and use only simple voltage mode structures. Here, a clock boosting technique is used. It optimizes the switches resistance and power consumption. The proposed implementation reduces limitations seen in previous quaternary implementations published, such as the requirement of special advantages in the CMOS process or power-hungry current-mode cells.

According to review paper [3] circuits The proposed approach yields very good results for the circuits studied in this paper, with almost optimal results for binary full adders up to 32 bits. For 64 bit,128 bit and more, This technique is not cost efficient and more complexity.

## VI. DOWN LITERAL CIRCUIT (DLC)

Down literal circuit (DLC) is one of the most useful circuit element in multi-valued logic (MLV). The down literal circuit (DLC) shown in fig 3 can divide the multi-valued signal into a binary state at an arbitrary threshold. It consisting of variable threshold voltage by way of controlling only two bias voltages.

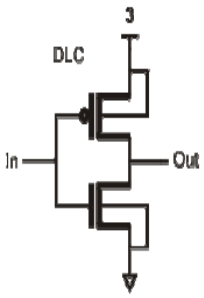



**Figure 3: Circuit diagram for DLC**

## VII. DESIGN OF QUATERNARY CONVERTER CIRCUITS

Objective of optimization is to minimize number of gates needed and also to minimize depth ofnet. Depth of net is the largest number of gates in any path from input to output. The reason for choosing these two objectives is that they will give very good properties when implemented in VLSI. Minimizing

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number of gates will reduce the chip area, and minimizing depth will give highest clock frequency.

### i. Quaternary to binary converter:

A basic Quaternary to binary converter uses three down literal circuits DLC1, DLC2, DLC3. Each DLC having different threshold voltage and also have 2:1 multiplexer. Q is the quaternary input varying as 0, 1, 2 and 3 given to three DLC circuits. The binary outputs thus obtained will be in complemented form and are required to pass through inverters to get actual binary numbers. Down literal circuits are realized from basic CMOS inverter by changing the threshold voltages of pmos and nmos transistors

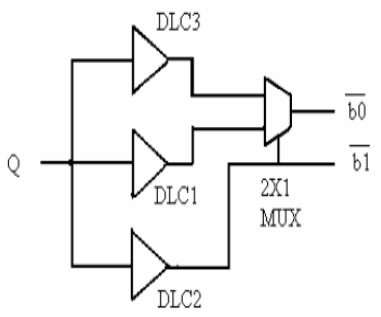


**Figure 4: Quaternary to binary converter circuit:**

### ii. Binary to Quaternary converter :

Binary to quaternary converter circuit is shown in the circuit. LSB and MSB of a two bit binary number are given to DLC 1.

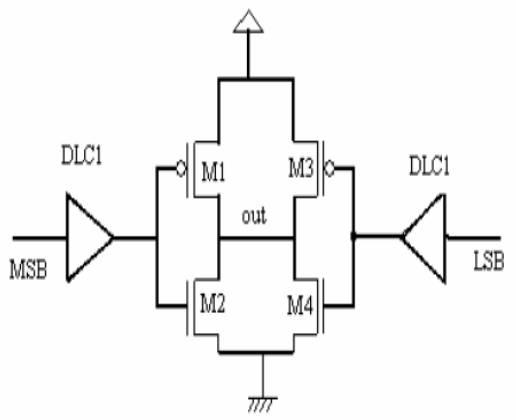


**Figure 5: Binary to Quaternary converter circuit**

## VIII. CONCLUSION

In this paper we review on, SUSLOC circuit structure is used to implement quaternary circuits. The conversion of binary to quaternary circuit is feasible and efficient in terms of power consumption and speed while being implemented in a standard CMOS technology.

As technologies are becoming more complex, multi valued logic (MVL) will be the future of circuit design. Since the research is still in initial stage on MVL the work is fundamental. When hardware implementation using MVL circuits is famous and more exposed to companies then one day MVL will surely turn over the binary logic. The advantages of lower power, higher performance, and reduced interconnect congestion motivate the use of quaternary circuits in a wide variety of applications.

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