International Journal on Recent and Innovation Trends in Computing and Communication ISSN: 2321-8169
Volume: 2 Issue: 12 3994 - 3998

Low Power Design Of Asynchronous Fine-Grain Power-Gated Logic

P. BalaPadma ,(M.Tech)
Department Of Electronics and Communication Engineering
Vardhaman College of Engineering, Hyderabad, India.
balapadma.7@gmail.com

BabuIlluri, Assistant professor
Department of electronics and communication
Vardhamancollege of engineering, telangana, india
i.babu@vardhaman.org

***Abstract*—**In technology improvement power dissipation has one of the major factor well known short circuit dissipations, leakage dissipations and dynamic switching dissipations are major power dissipation sources of CMOS Chips. For reducing power dissipation in CMOS logic blocks various techniques were there among these techniques most effective new technique implemented with low power dissipation. That is "low power design of Asynchronous fine-grain power gated logic"(LPAFPL). Low power AFPL is a new logic family. It consist of ECRL (efficient charge recovery logic gate), Pipeline system, C-element and Partial Charge Reuse mechanism (PCR). Each pipeline stage is comprised efficient charge recovery logic gate gains power and it is became active when useful computations are there and does not requires power at idle stage. Thus gives negligible leakage power dissipation. PCR is the output node of the ECRL logic, To evaluate the CMOS logic circuit level. Then it automatically reduced the power dissipation in complete evaluation of CMOS circuits.

Keywords- *Asynchronous circuits, ECRL logic gate, C-element, Power gating and Low power electronics.*

*****

I. INTRODUCTION

In nowadays technology power consumption techniques are increased rapidly but most important factor is power consumption. In CMOS power dissipations are static power dissipation and dynamic dissipation. Static power dissipation caused by leakage currents, main source leakage of sub circuit leakage, reverse bias junction leakage, gate leakage, gate leakage, sub threshold leakage. Dynamic power dissipation consumed when the device is powered up like switching power to charging as well as discharging of capacitance. Short-circuit current caused by internal power. To overcome this power dissipation, For this in electronic circuits, if area is high then power consumption is less but in nowadays technology both area and power consumption important factors. So, To reduce power consumption various technologies are there, in that efficient technique is low power AFPL. Low power AFPL combined with ECRL logic gate, HC(handshake controller) and partial charge reuse mechanism(PCR) AFPL. The ECRL(Efficient Charge Recovery Logic) Gate can reduces the power when compare with the static circuits, it is a combination of logic gates i.e AND/NAND logic gate. Then handshake controller is controls the data transmission between neighboring nodes when the useful performance is there. Partial charge reuse mechanism is used between the stages of low power AFPL. Including all these the power consumption is reducing efficiently in mitigate design of low power AFPL in digital design of VSLI.

II. LOW POWER DESIGN OF ASYNCHRONOUS FINE-GRAIN POWER-GATED LOGIC (AFPL)

The Asynchronous circuits design completely different from the synchronous design technique. The synchronous total logic design depends upon the central clock signal but in Asynchronous design does not have central clock signal. In place of central clock signal the handshaking is working, handshaking technique main advantage is it transfers the data when useful performance is there between neighboring logic blocks. No waste work is not there power is saving by using handshaking process[2].

The Asynchronous circuits can be using power-gating technique, power gating shutting off the current to blocks which are not useful in low power of logic block. It is using a high voltage sleep transistor with series of pullup and pulldown of a low voltage logic block design. If low voltage logic block is out of action then the sleep transistor is turned off the logic block. So it is reducing leakage current.

The ECRL (Efficient Charge Recovery Logic Gate) has the simplest structure for best efficiency. It is a function block of AFPL in implementation of low power design. ECRL is dual-rail data encoding for input of ECRL logic gate[6] requires to represent computations of a logic block and its complement. Because it is combination of AND gate and NAND logic gate.

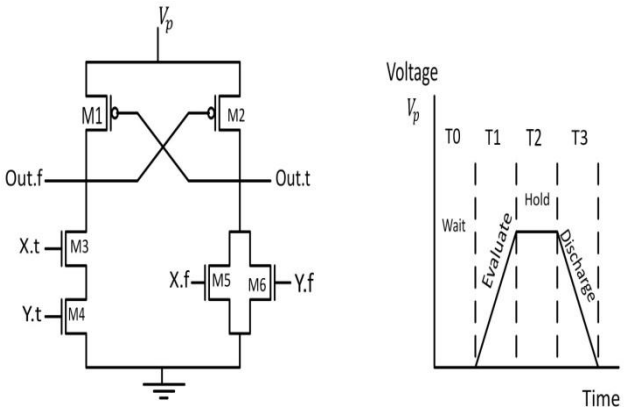

Figure: 1. ECRL AND/NAND logic gate and operation phases of ECRL.

The ECRL AND/NAND logic gate operation cycle consist wait, evaluate, hold and discharge phases. In wait phase Vp is kept 0V, ECRL gate do not draw current from Vp then outputs of Oi.t and Oi.f are LOW. In evaluate phase, if M3 and M4 are HIGH those turns ON and draw Vp voltage, it ramps from 0V to Vp then it starts evaluation of outputs. In hold stage M2 is turns ON then current begin to charge Out.t from Vpand it stays at VDD. In discharge phase voltage Vp from VDD to OV means it rams down and the power charge in outputs nodes Out.t and Out.f transfers back power node Vp[1].

 ISSN: 2321-8169
3994 - 3998

The C-element is a fundamental building block of many asynchronous circuits, can be thought as a AND gate for events. If inputs match in a state then copy it for output else hold previous state. C element also referred as state holding device and when the AFPL circuits starts up, the reset signal is used to initialize outputs of C element for AFPL to LOW, All power nodes will set to 0V. means each stage of low power AFPL operation begin with wait phase. The C element used as a Traditional C element in low power design of AFPL w/o PCR pipeline. and Enhanced Celement(C*) in low power design of AFPL-PCR pipeline.

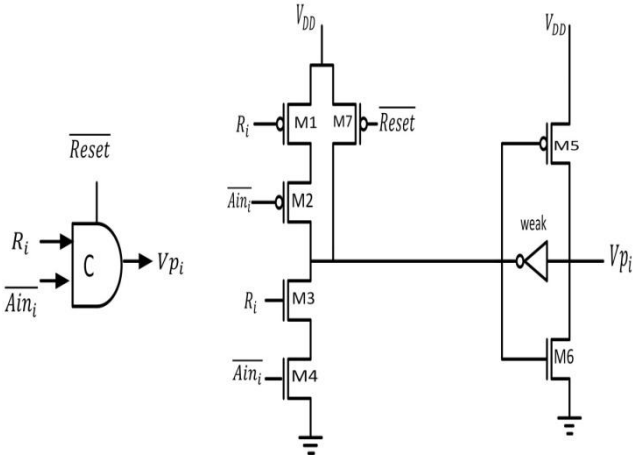

Figure: 2. Traditional C-element used in AFPL w/o PCR pipeline.

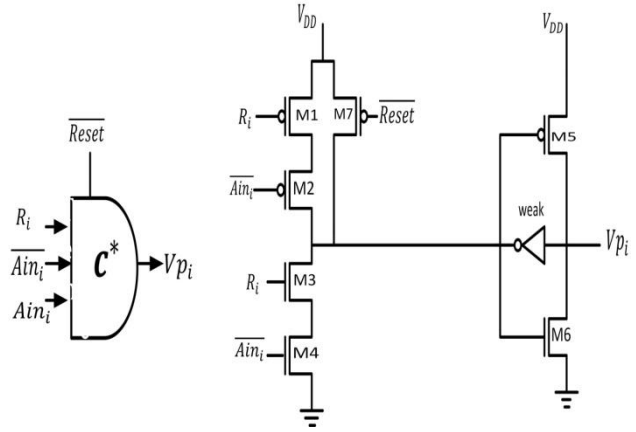

Figure: 3. Enhanced C-element (C*) used in AFPL-PCR pipeline.

The structure of low power AFPL with PCR mechanism is shown below figure.

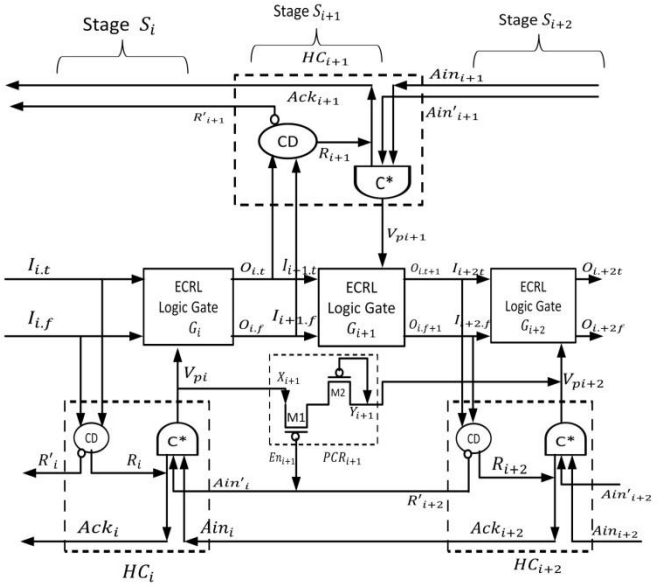

Figure: 4. structure of AFPL-PCR pipeline

The structure of low power AFPL without PCR mechanism is shown below figure.

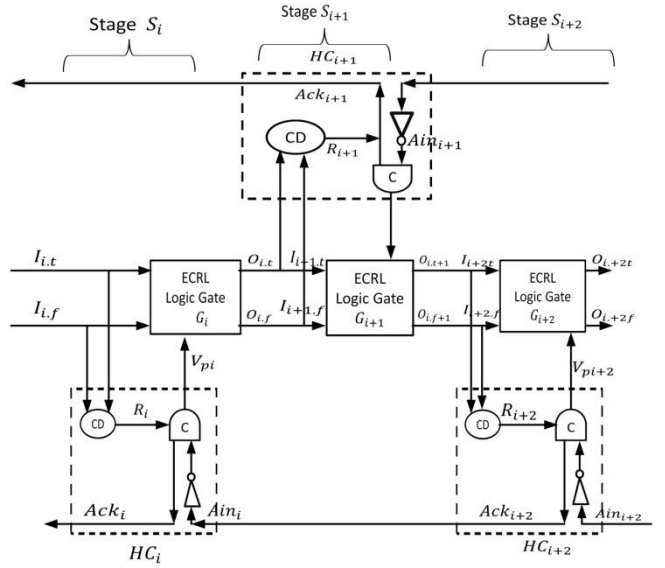

Figure: 6. structure of AFPL w/o PCR pipeline

From the AFPL-PCR pipelines advantage is to get low power with number of stages, the stages will be high structure but it getting low power results at VLSI designs.

III. IMPLEMENTATION OF C ELEMENT

The C element is state holding element and it is a fundamental building block in Asynchronous circuit design, it can be work as AND logic gate. If all inputs are high the output will be high otherwise output will be holds previous state result.
For the best result in C-element here added the one pMOS in series of VDD and nMOS added in pulldown both Traditional and Enhanced C elements(C*). From these modification we can get best state holding state in AFPL-PCR pipeline and reducing the power consumption in asynchronous circuits design.

 ISSN: 2321-8169
3994 - 3998

The output of C element is connected in HC to Vp, it is shown in low power AFPL pipeline. The C element provides output when all inputs are HIGH else it produce previous result. When AFPL circuits starts up, reset signal is used to initialize all C element outputs set to AFPL to LOW so all nodes power will be set to 0V, that means every AFPL pipeline stage operation will begin in wait phase.

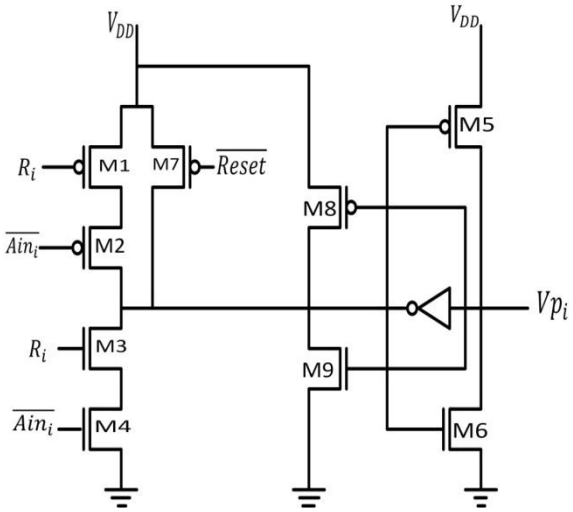

Figure: 7. Modified Traditional C-element structure

The enhanced C element(C∗) provide advantage that is ECRL logic gate consist early discharging of output no need longer time for discharging and without waiting for next empty token it is arrive in this stage.

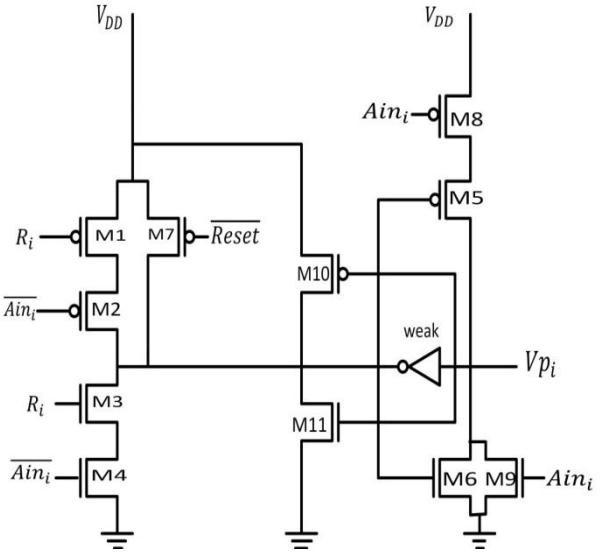

Figure: 8. Modified Enhanced C-element structure

The AFPL- PCR pipeline and PCRi+1 unit. If M2 worked as a diode allows current enhanced C element it flows direction of VP+2 and M1 sued as a swith, it is ON when charge reuse is activated.

In C*-element, HCi has three inputs, Ri, Ainibar and Aini both are complementaries. Ri is request signal of CD in HCi and Aini, Ainibar are the acknowledgement signals from HCi+2. After completion of reset the Ri and Ainioccure four events.

1. Event Req↑: If valid token arrives in stage Si, Ritransits LOW to HIGH
2. Event Ack↑: If valid output at stage Si has been received by stage Si+2 then Aini draws from LOW to HIGH and also draws HIGH to LOW.
3. Event Req↓: At the stage Si arrives a empty token then Ri transits from HIGH to LOW.
4. Event Ack↓: If empty output at stage Si has been received by stage Si+2 then Aini draws from HIGH to LOW and aslo draws LOW to HIGH.

Event Ack↑ may occur before or after event Req↓ does. If we use a traditional C-element controls the power at nodes of ECRL logic gate, The C-element can transit from HIGH to LOW until events Ack↑ and Req↓ both have occurred. Instead, if we use the C∗-element to control the power node of ECRL gates, the C∗-element can transit from HIGH to LOW if event Ack↑ has occurred no matter whether event Req↓ has occurred or not. Thus, the ECRL logic gates in Si can enter the discharge phase to achieve early discharging as soon as the valid output of stage Si has been received by stage Si+2 (i.e., event Ack↑), without waiting for the next empty token to arrive at Si (i.e., event Req↓).

From the operation of AFPL-PCR pipeline early discharging to further reduce energy dissipation.

IV. SIMULATION RESULTS

A) Simulation environment

All the circuits have been simulated using HSPICE tool using 180nm technology. AFPL w/o PCR pipeline and AFPL-PCR pipelines are simulated on same input patterns.

B) Simulation comparison

In this section proposed design of low power AFPL-PCR pipeline is compared with the existing AFPL-PCR pipeline technology.

In the AFPL pipeline, the handshake controller HCi in stage Si performs the following tasks:

1. detecting the validity of the inputs to the ECRL logic gates in stage Si;
2. offering power to the ECRL logic gates in stage Si;
3. detecting whether the outputs of stage Si have been received by the downstream stage Si+2; and
4. informing the upstream stage Si−2 when Si−2 can remove its outputs.

ISSN: 2321-8169
3994 - 3998

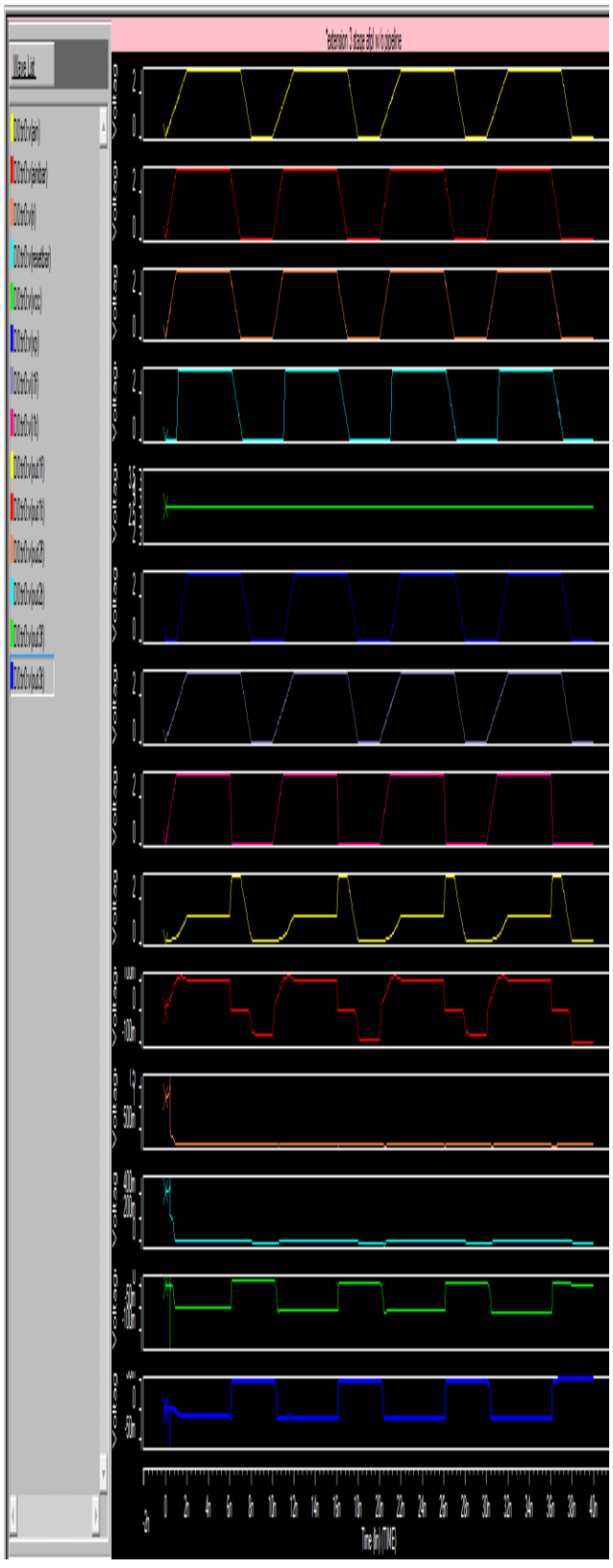

Figure:9. Extension of AFPL w/o PCR pipeline simulation

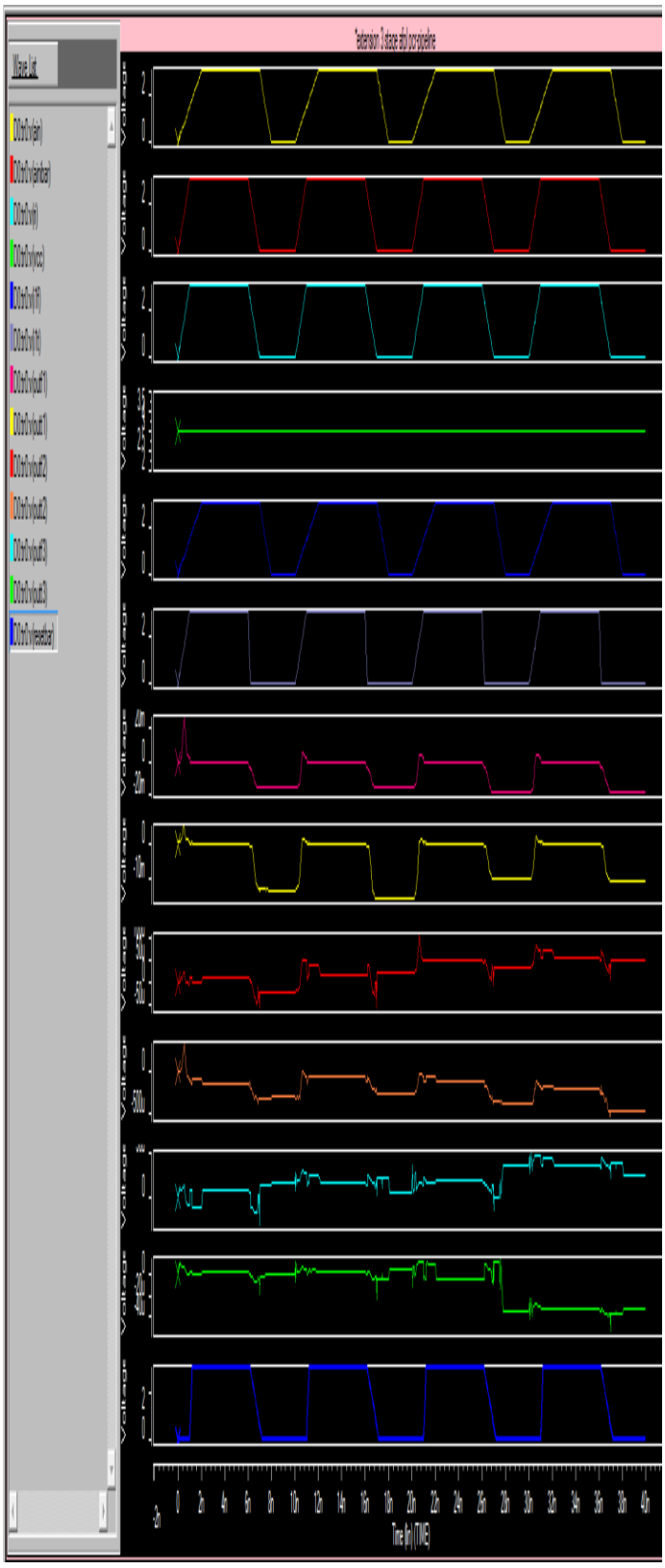

Figure: 10. Extension 3 stage AFPL-PCR pipeline simulation results

Table: 1. Power comparison with previous technique

Stages	Existing AFPL w/o PCR pipeline POWER(nW)	Existing AFPL- PCR pipeline POWER(nW)	Extended Low power AFPL w/o PCR pipeline POWER(nW)	Extended Low power AFPL-PCR pipeline POWER(nW)
First stage	0.021	0.029	0.010	0.015
Third stage	0.0295	0.0142	0.0236	0.0100

From proposed low power design of AFPL simulation doneby using HSPICE Tool. By using this simulation will be easy process for critical designs. Here low power design of AFPL consumes the less power comparing to existing design of AFPL. The AFPL w/o PCR reduces power negligible that is 20% of existing because this design does not have Partial Charge Reuse mechanism (PCR) and the AFPL-PCR Pipeline system reduces power effectively that is 30.55%.

V. CONCLUSION

Low power design of AFPL highly reduces leakage power as well as reduces power consumption when compare to coarce grain power gating technique.
The AFPL w/o PCR reduces power negligible that is 20% of existing because this design does not have Partial Charge Reuse mechanism (PCR) and the AFPL-PCR Pipeline system reduces power effectively that is 30.55%. Thus gives negligible leakage power dissipation. PCR is the output node of the ECRL logic, To evaluate the CMOS logic circuit level. Then it automatically reduced the power dissipation in complete evaluation of CMOS circuits.

REFERENCES

[1] Meng-Chou Chang, Member, IEEE, and Wei-Hsiang Chang,"Asynchronous Fine-grain Power-gated Logic" *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, VOL. 21, NO. 6, JUNE 2013.

[2] M.-C. Chang and C.-C.Tsai, "Handshaking quasi-adiabatic logic," in *Proc. Int. Midwest Symp. Circuits Syst*., 2009, pp. 531–534.

[3] M.Arsalan and M. Shams,"Asynchronousadiabetic logic", inn Proc. *IEEE Int. Symp. Circuits Syst*., May 2007, pp. 3720-3723.

[4] C. Ortega, J. Tse, and R. Manohar, "Static power reduction techniques for asynchronous circuits," in Proc. *IEEE Symp. Asynchronous Circuits Syst*., May 2010, pp. 52–61.

[5] Y. Moon and D. K. Jeong, "An efficient charge recovery logic circuit," *IEEE J. Solid-State Circuits*, vol. 31, no. 4, pp. 514–522, Apr. 1996.

[6] J. Hu, W. Zhang, X. Ye, and Y. Xia, "Low power adiabatic logic circuits with feedback structure using three-phase power supply," in Proc. *Int. Conf. Commun. Circuits Syst*., May 2005, pp. 1375–1379.

[7] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design*: *A Circuits and Systems Perspective*, 4th ed. Upper Saddle River, NJ: Pearson Education, 2010.

[8] J. Sparsø and S. Furber, *Principles of Asynchronous Circuit Design: A Systems Perspective*. Norwell, MA: Kluwer, 2001.