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An Area Efficient Pulse Triggered Flipflop Design under 90nm CMOS Technology

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***Abstract*—** The choice of flip-flop technologies is an essential importance in design of VLSI integrated circuits for high speed and high performance CMOS circuits. The main objective of this project is to design an area efficient Low-Power Pulse- Triggered flip-flop. It is important to reduce the power dissipation in both clock distribution networks and flip-flops. The comparison of low power pulse triggered flip-flops such as Ep-DCO, MHLFF, ACFF, Ip-DCO, conditional enhancement scheme and signal feed through scheme. Logics are carried out and the best power-performance is obtained. Here simulations are done under 90nm technology and the results are tabulated below. In that signal feed through scheme is showing better output than the other flip-flops compared here.

Keywords- *Flip flop, P-FF (pulse- triggered),DCO (data close to out),Ep-DCO (Explicit pulse triggered DCO), MHLFF (Modified hybrid latch flip flop), ACFF (Adaptive coupling configured flipflop), Ip-DCO(Implicit-Type P-FF),*

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I. INTRODUCTION

Flip-Flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements.

In recent VLSI's, a clocking system, including clock interconnections and flip flops. This is partially because the activation ratio of a clock system is unity. In this clocking system power, 90% is consumed by the last branches of the clock distribution network.

P-FF has been considered a popular alternative to the conventional master-slave based FF in the application of high speed operations. High performance flip flops are key elements in the design of contemporary high-speed integrated circuits.

In these circuits, high clock frequencies are generally gained by using a fine grain pipeline in which only few logic levels are inserted between pipeline stages. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced..

II. PULSE TRIGGERED DESIGNS

A. *Implicit-Type P-FF- DCO*

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a).

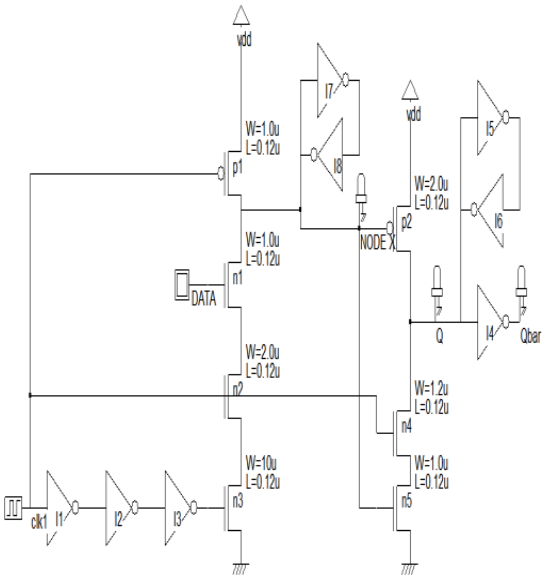

Fig. 1(a) Ip-DCO

It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, MOS Transistors N2 and N3 are turned on. If data remains high, node will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node controls two larger MOS transistors (P2 and N5).The large capacitive load to node causes speed and power performance degradation.

B. *MHLFF*

An improved P-FF design, named MHLLF Fig.1 (b), by employing a static latch structure presented. Node is

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no longer pre charged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node level at high when Q is zero. The Modified Version of Hybrid Latch Flip-Flop is also falls under the hybrid category of flip flop that has impressive delay property and can have negative setup time with brief transparency period

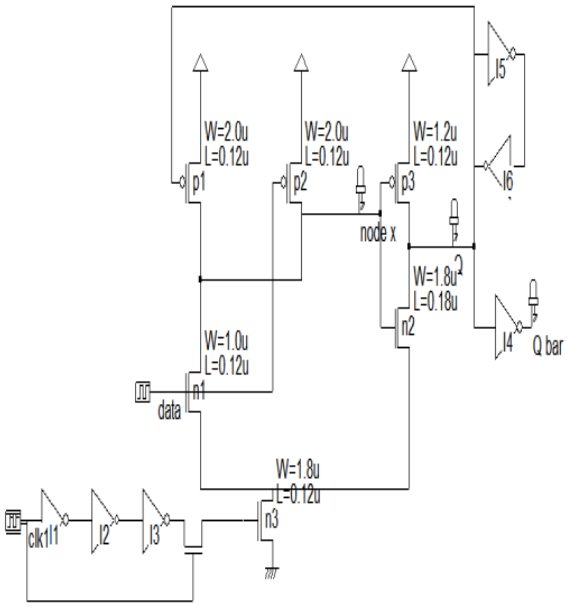

Fig. 1(b) MHLLF

This design eliminates the unnecessary discharging problem at node. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".

C. Ep-DCO

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 1(c) shows a classic explicit P-FF design, named data-close- to- output (ep-DCO). It contains a NAND-logic- based pulse generator and a semi dynamic true- single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X . The pulse width is determined by the delay of three inverters.

This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation.

To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

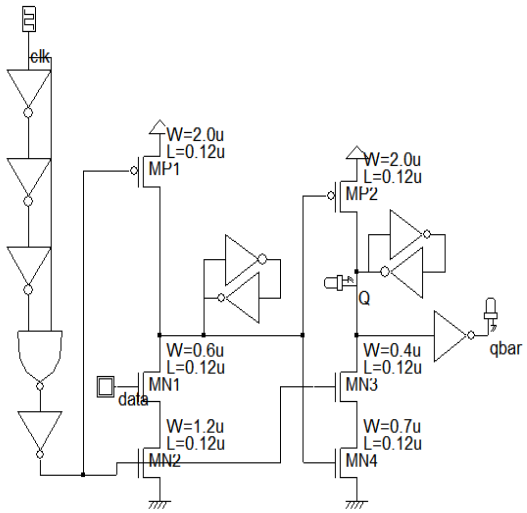

Fig. 1(c) Ep-DCO

D. ACFF

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. The ACFF design leads in power efficiency because it uses a simplified pMOS latch design and exhibits a lighter loading to the clock network (only four MOS transistors are connected to the clock source directly).Its power efficiency is even more significant in the cases of zero or low input data switching activity.

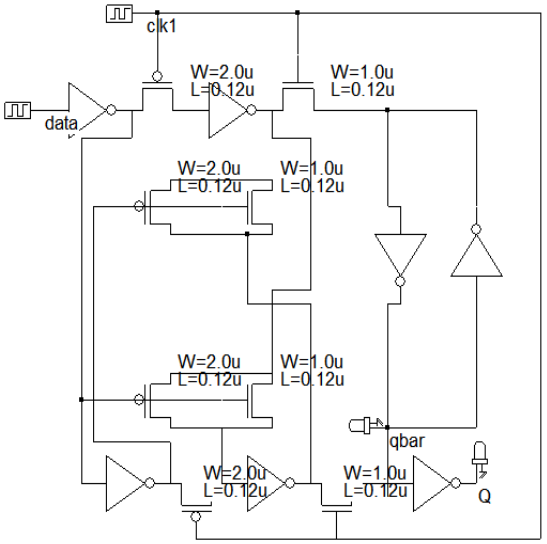

Fig. 1(d) ACFF

E. Conditional pulse enhancement scheme(CPE)

The design, as shown in Fig. 1(e), adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path.

The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." As opposed to the transistor stacking design in Fig. 1(a) and (c), transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3,forms a two-input pass transistor

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logic(PTL)-based AND gate, to control the discharge of transistor N1.

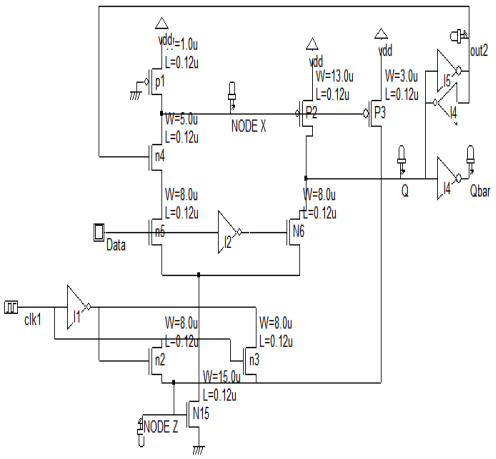

Fig. 1(e) Conditional pulse enhancement scheme

Since the two inputs to the AND logic are mostly complementary, the output node is kept at zero most of the time. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node can be reduced due to a diminished voltage swing.

F. Signal Feed Through Scheme(SFT):

This design adopts a signal feed-through technique to improve this delay. Similar to the SCDFF design, the proposed design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at an internal node. However, there are three major differences that lead to a unique TSPC latch structure and make the proposed design distinct from the previous one. First, a weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved.

In addition to the circuit simplicity, this approach also reduces the load capacitance of node X. Second, a pass transistor controlled by the pulse clock is included so that input data can drive node Q of the latch directly. Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor provides a discharging path.

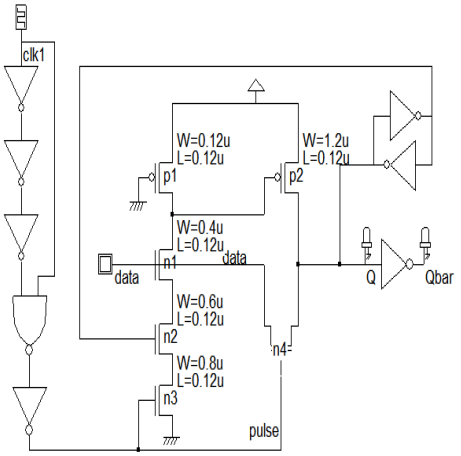

Fig. 1(f) Signal Feed Through Scheme

III. RESULTS

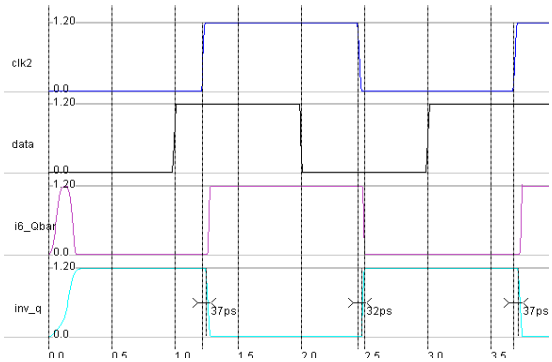

Fig.2(a). Simulation waveforms of ip-DCO

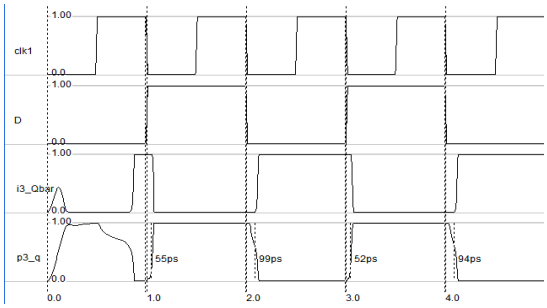

Fig.2(b). Simulation waveforms of MHLFF

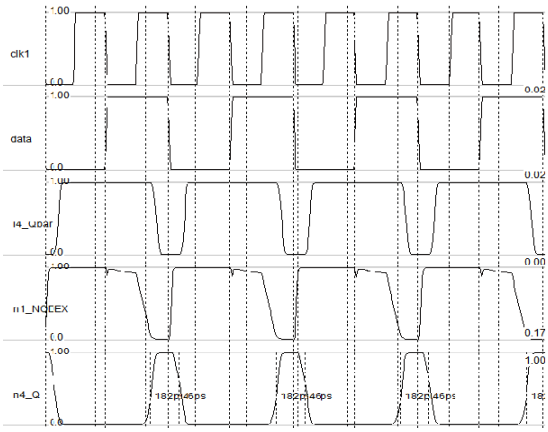

Fig.2(c). Simulation waveforms of Ep-DCO

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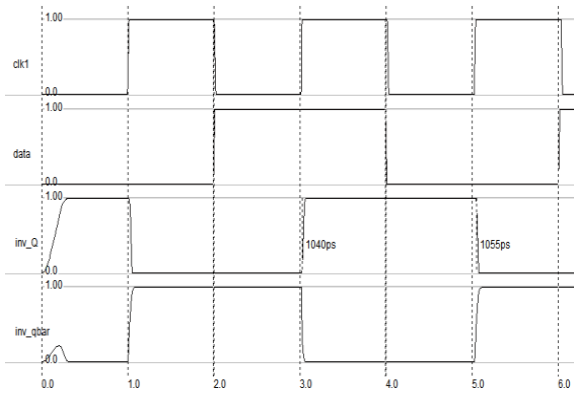

Fig.2(d). Simulation waveforms of ACFF

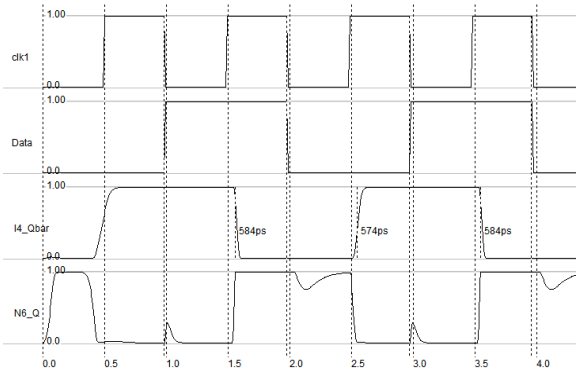

Fig.2(e). Conditional pulse enhancement scheme

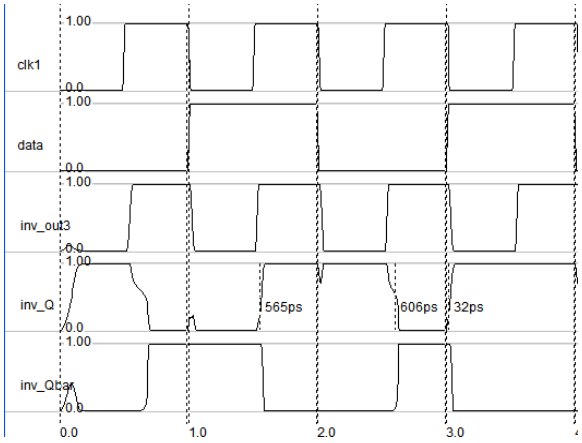

Fig.2(f). Signal Feed Through Scheme

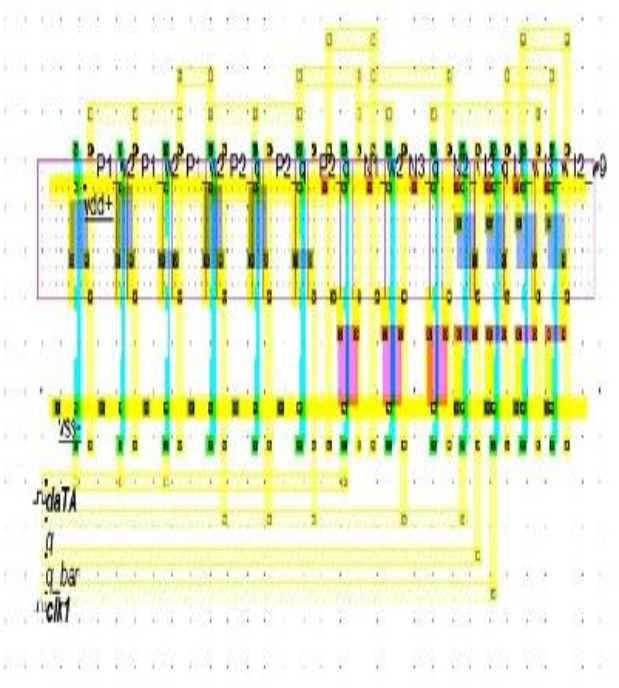

Fig.4. Layout For Signal Feed Through Scheme

IV. DESCRIPTION

To demonstrate the superiority of the design, layout simulations on various P-FF designs were conducted to obtain their performance using MICROWIND /DSCH2 tool. The target technology is 90-nm CMOS process. The operating condition used in simulations is
1.0V.

Comparison table is added to verify the various factors such as rise delay, fall delay, data to Q delay, layout area, power and the transistor count. Table 5 summarizes the circuit features and the simulation results. For circuit features, although the design does not use the least number of transistors, it has the smallest layout area. This is mainly attributed to the signal feed-through scheme, which largely reduces the transistor sizes on the discharging path. In terms of power behavior, the Signal Feed through Scheme design is the most efficient in five out of the six designs. The Ep-DCO design consumes the largest power because of the superfluous internal node discharging problem.

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V. COMPARISON TABLE

Types	No. of. Transistors	Power	D to Q delay (ps)	Layout area (μm)^2	Rise delay (ps)	Fall delay (ps)
Ep-DCO	28	0.287mw	186	437.5	60	46
ACFF	22	210 µw	1041	210	26	31
Ip-DCO	23	0.043mw	82	237.9	32	37
MHLFF	19	40.7µw	55	148.5	52	94
CPE SCHEME	19	0.159mw	564	777.7	64	34
SFT SCHEME	24	41.7µw	565	112	58	94

Table 1.Comparisions of different flip flops designs

VI. CONCLUSION

In this paper, the various Flip-flop design like, Ep-DCO, ACFF, Ip-DCO,MHLLF, Conditional pulse enhancement scheme and Signal Feed Through Scheme are designed and those resulted waveforms are also presented. The simulations are done using Micro wind & DSCH analysis software tools and the result between all those types are listed. The comparison table also added to verify the designed methods. With these results Signal Feed through Scheme is an area efficient.

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