Embedded Reconfigurable Techniques in Wireless Sensor Network Applications

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***Abstract*—** Reconfigurable techniques are used in many engineering and industrial applications for the efficient data transmissions through the wireless sensor networks. Nowadays, most of the industrial applications are working to try to minimize the size and cost. During runtime the reconfigurable technique avoids the unwanted hang and delay in the system performance. In recent world Field Programmable Gate Array (FPGA) as one of the most efficient reconfigurable devices and widely used for most of the hardware and software reconfiguration applications. In this paper, the work deals with whatever going to make changes in the hardware and software during runtime, it's should not affect the current running process that's the main objective of the paper our changes are done in a parallel manner at the same time concentrating the cost and power transmission problems during data transreceving. Analog sensor (Temperature) as an input for the controller (PIC) through that control the FPGA digital sensors in a generalized manner.

Keywords- *Field Programmable Gate Array (FPGAs), Peripheral Interrupt Controller (PIC), Runtime Reconfigurable Techniques. Wireless Sensor Networks (WSNs).*

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I. INTRODUCTION

Embedded and VLSI techniques are joined and to a major role in the recent technologies at the same time research basis for wireless network also difficult one due to the nodes in the networks are want to work be in automatically, low-range of power demanding, and compact [1], [2]. In the modern world application may have millions and trillions of sensor nodes revolve in an environment, these all make a complex task for the network researches. The major part of the industrial wireless sensor is an ultra-low power wireless sensor nodes want to collect the processing signals from wherever the industrial sensor be present in the particular location then transmit the information through wirelessly toa base station for controlling and monitoring.

If we want to interfaces and data processing between the sensors the communications are very difficult not only from one sensor to another, it's also vary from one application to another application so the designers are trying to overcome these all problems in their day to day environment for these things the devices are wanting to programmed and reprogrammed with application-specific hardware designs. In olden days FPGAs were limited to performing tasks that required only fixed-point arithmetic, but in the recent advances in FPGAs

Hardware have made floating-point arithmetic on FPGAs possible lot of exciting challenge is to use FPGAs to accelerate computationally intensive scientific computing applications that require floating-point arithmetic operations be done in an efficient manner[3].

For all this major things the main reasons are nodes and their power utilization based on this two major scenario the cost and memory utilization of the device be increased so the recent upcoming inventions are mainly based on these two things the recent inventions are mostly based on VLSI orientated the major advantage of this technology are power utilization is very low compare to previous invention technologies.[4] Runtime reconfigurablity is a one of the up growing topic, within the reconfigurable computing area, where changes be done in the FPGAs configuration are at runtime, even the input/output device is inactive and any other logic is kept active. This powerful aspects are developed in Atmel FPGAs and Xilinx permits not only to perform hardware updates at runtime and at any time, but also compared with to save memory space and programming time to full FPGA reconfiguration.

This paper mainly deals with a reconfiguration system in wireless sensor networks in FPGAs very difficult to give the analog input as directly for that purpose the controller be used here the major part of the controller is convert the getting analog input into digital output through that the FPGAs be done the reconfigurable process [5], [6]. In this PIC act a part of microcontroller compare to the previous microcontroller devices, it's very efficient one, it works under the Reduced Instruction Set (RISC) in the manner of instruction wise user friendly device, 40pin configuration, 6 ports, and inbuilt analog to digital conversion unit these are the special things of the PIC microcontroller.

II. SENSOR NODE,PART

In this section, a general part of the processing layer unit and the WSNs nodes part is presented. Both the industrial based and academic related approaches are presented here. PIC and FPGAs be act as a processing layer unit in this paper.

A. PIC 16F877A

In the previous papers the research be based on 8051 microcontroller in that for the analog operation the designer wants to make the Analog to Digital convertor (ADC) part separately so it attain some amount of power consumption and also make delay in the design process, then want to make separate interface so now most of the embedded designs are coming under the Peripheral interrupt Controller (PIC) unit.

ADC part be act as a major role in this paper, it should be the input part of the controller unit. In the PIC the ADC is one of the special units compare to the previous microcontroller families avoid the unwanted power consumption the designers are mostly like this controller family. In the PIC the designers made

Successive Approximation Type *a*s inbuilt ADC. In the PIC the ADC designs up to 10-bit conversion, giving a result of 1024 ways: ADC internal reference voltage 5.00 V and the bit resolution are being as 5.00/1024 4.88 MV per bit. Temperature measurement be as 10 mV per ºC and finally temperature resolution calculated per bits as 4.88/10 0.488ºC per bit.

In PIC there are eight pins allocated for ADC pin configurations this eight pins come under the PORT A and PORT E so the PIC provide eight different analog applications at a same time, in this paper temperature sensor (LM235) only one be act as a input for the microcontroller it collects the analog value from the environment continuously here previously set some threshold value for the controller whenever the controller attain that voltage are get excess that time it give trigger to the one of the processing layer of FPGA that time FPGA check the digital sensors current stage and replied to the microcontroller through the serial cable communication.

B. Power Supply Layer Unit

This unit generates all, the entire voltages for the node, there are two ways of power generation version have been developed here. The one is Universal Serial Bus (USB) connected, it's been a Tran's receiver between the node and

PC and also receive power supply from that, the PIC also utilize the same power generated from the power supply layer through the normal wired connection or from the minute soldering.

C. Communication Layer Unit

This paper deals with a Zigbee module for the data transmitting and receiving part this module was controlled by PIC through the serial communication of Universal Asynchronous Receiver Transmitter (UART) in future try with Wi-Fi or Bluetooth if the node distance be suppose increased.

D. Sensor Layer Unit

The sensor layer has one of the additional feature is interfaced with both analog and digital sensors for the process the analog sensor (Temperature) be connected with PIC microcontroller and the digital sensors be connected with FPGAs here the digital sensors only considered as in generalized manner (shown in the "Fig. 1") depending on the output from the microcontroller the FPGAs control the digital sensors the information be passed through the serial cable if any changes happen in the environment the controller automatically passes the trigger to the FPGAs depend on the triggering the it check the current status of the digital sensors and again it reply back the strategy to the microcontroller this event is being as Runtime Reconfiguration.

During this process whatever the changes may arise in the both hardware and software it's not affect the all process it only make changes in the our particular partial reconfiguration this things depend on the coding and real time environment changes the remaining process be run in a parallel manner this the specialty of the FPGAs due to the interconnection between the blocks and wires so it save most of the power loss at the same time reduce the designer work time in a single coding monitoring the all the process .In recent days,[7] there are lot of myriad sensors are available in the market with many different interfaces. Most of them are digital sensors, with various [8] such as I2C, SPI, 1-Wire, etc. When the problems related to timing and processor overhead can appear that time this kind of signals have to be processed using a microcontroller. Some manufacturers provide Hardware Description Language (HDL) code to implement the sensor interfaces in a coprocessor. A digital sensor is an electrochemical sensor, where data transmission and data conversion are done in a digital manner. Sensors are commonly used for analytical measurements, i.e. the measurement of physical and chemical properties of liquids. Some of the measured parameters are pH value, oxygen, conductivity, redox potentials and others.

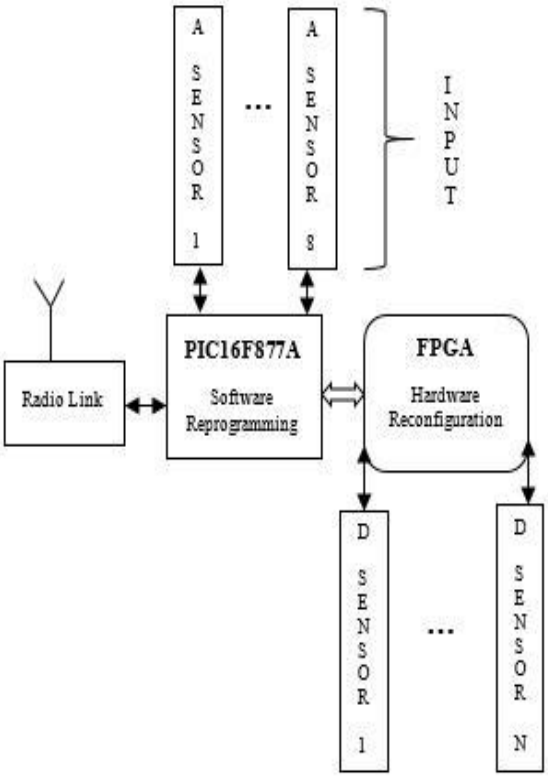

Fig. 1. The architecture of a sensor node system (A sensor means the analog sensor and D sensor means digital sensor).

III. RECONFIGURATION SCENARIOS OF NODE AND CONTROL FLOW

Network level based reconfiguration is the first reconfiguration scenario, this is one of the most required process during deployment, due to the response of final function of each node is defined here, this layer includes the used sensors and data processing otherwise the network may get any defect or the function is changed like in an emergency situation. Substantially this scenario may put-on both, the hardware reconfiguration technique and software reprogramming. In the context of node platform, hardware reconfiguration is compulsory when modifications affect digital sensors (mentioned with "D" in the Fig. 1), as they are directly fastened with the FPGA. Opposite, software reprogramming is required for analog sensors (mentioned with "A" in the Fig. 1) are involved, due to they are directly fastened to the PIC ADCs. The important thing in this scenario is node runtime reconfiguration is possible only when dealing with hardware reconfiguration, for the reason that software reprogramming need rebooting the system.

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Reconfiguration at Node Level is the second scenario, it mainly involves in the hardware configuration. In this scenario, a reconfigurable array blocks act as a reconfigurable coprocessor where the repetitive tasks lighten by the node platform hardware device (FPGA) in parallel manner this parallel task be done with the help of reconfigurable array blocks[9],[10]. Here the FPGA has two main functionalities one is when its deal with the analog sensor it fully act as coprocessor functionality is when its deal with the digital sensors it be acting as both coprocessor and digital sensor control. According to this both scenario a partial runtime reconfiguration technique has been built on the top of the node this partial reconfiguration and FPGA be act as a reconfiguration technique.

The runtime reconfiguration resulting allows to modify the data processing, digital sensor interface or the interface between PIC and FPGA even the system in running time. The PIC is the core element for controlling all the reconfigurable process it acts a position of receiving the software reprogramming and hardware configuration changes and manage with the FPGA reconfiguration. Therefore, all the reconfigurable process be controlled by the simple software coding parts done by the designer. The top of the node (shown in the "fig. 2") have abstraction layer part it has various platforms the platform have both hardware file and software library files. The one unit of the abstraction layer is traditional hardware abstraction layer and the remaining one is reconfigurable hardware abstraction layer. The FPGA have the inbuilt of hardware configuration files the files will be utilized be utilized by the designers depend upon on their application.

The various applications have different kinds of coding and their functionality also varied that time this inbuilt library act a major role with the designers its saves lots of work time. And the software programmer making the FPGA blocks depends on the functionality. After the abstraction layer the above layer is node definer and state variable unit part this indicates the future work of the node and also it have some compressed messages like radio communication, sensor working unit, sensors working part and the variable defines the current using state of the resource node. Another layer is controlling unit part, it's directly maintain the node decision part.

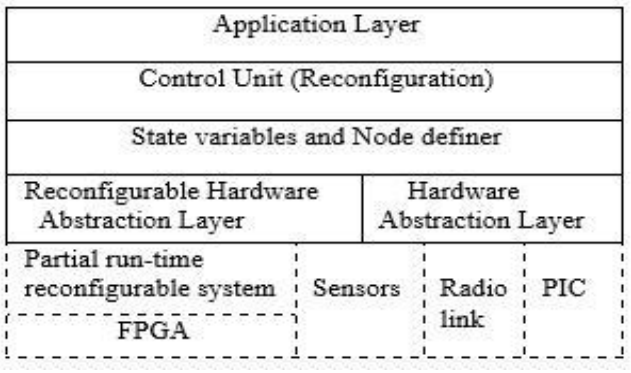

Fig. 2. Software stacks of Reconfigurable Node

IV. Role Of Partial Runtime In WSN

In that the node should take their decision in an independent manner during the time of when the reconfiguration is needed for the node another one is if the reconfiguration is not available at the time what the node going to decide these are the two main works taken care by this unit. The final top most layers are application layer this layer decides the transmitting, receiving, sensing, data processing, etc.

The partial runtime system is the most efficient technique for runtime reconfiguration in recent days most of the parallel processing industrial applications are based on these techniques. The file based on partial configuration are in a compact manner during the runtime or in normal working condition it attains only less amount of energy and bandwidth. The designer needs to make the partial reconfiguration want to allocate the configurable logic blocks (CLB) for the specific operations in a correct manner. In this paper the FPGA reconfigurable blocks are arranged based on Virtual Architectures (Vas) [11].

The following paragraphs detailed about the vase partial configurations and its partial blocks regarding to the node. In this the virtual architecture has been divided into three major functionality's the first one is between microcontroller (PIC) and FPGA this part is fixed one it only do the interfacing operations (left side), the second one is a digital sensor accessing part in this paper only deal the sensors in a generalized manner (right side) and the final one is in between this two major functionality that part is paper reconfigurable (FPGA) part full of configurable logic block columns. The each CLB is a combination of four Lookup Tables. The lookup table is a combination of basic gates the designer functionality and logical things all coded in this lookup table. The Spartan 3 FPGA has 16 CLB columns and 24 CLB rows each have some special slot functions [12].

In this paper the reconfigurable FPGA has three major functions the first one is sensor interfacing part, the second one is reconfigurable part (Co processing unit) and the final one is FPGA and PIC interfacing part (shown in the "Fig. 3"). Thus, all functions to be split as three slots, the first slot 0 for PIC communication with the FPGA, then slot 1 for reconfigurable functions and slot 2 for sensor interfacing. This all interfacing work done with the help of Buses.

In this both unidirectional and bidirectional buses be used for data transferring between the slots, by the use of bidirectional bus the data's be moved from left to right (4 bits) at the same time the data transfer from right to left (4 bits) in this also pipelining technique be used in the architecture concept [13], it reduces most of the delay in the data transmission apart from this (environmental condition, cable's, working mode) also decide the data transmission speed the following paragraphs explain detailing about the above delay things (Section 5).

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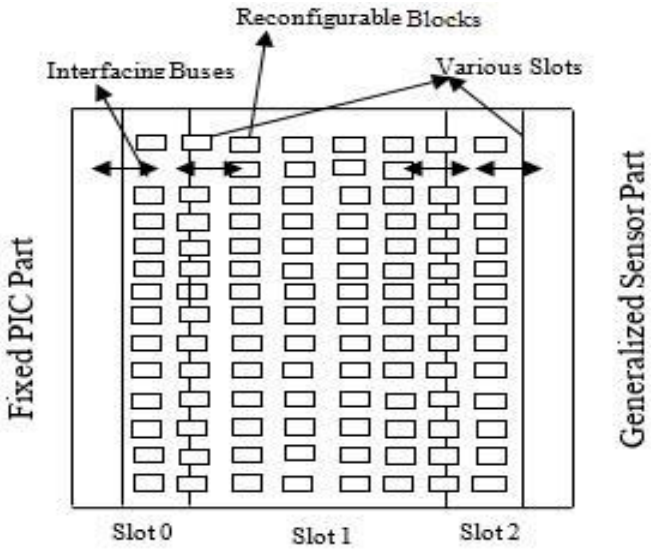


Fig. 3. FPGA virtual architecture view and slot allotments for node and hardcore.

V. Result And Parameter Analysis

In the result and parameter analysis part mainly concentrate on memory and energy these two things related to the term of cost. These two parameters, analyze in the I) the reconfigurable systems, use of wireless sensor network and II) the changes of new hardware configurations and software programs along with wireless sensor network [14].

A. Hardware Part

In this paper the hardware part design with the help of GPBs board (shown in the "fig. 4") in this one of the processing

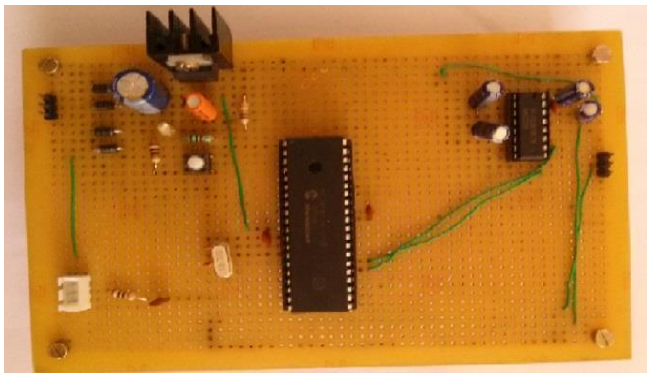


Fig. 4. General Purpose Board (GPB) processing layer unit.

layer may built with the help of active and passive components, the PIC be act as a heart of the nodes all the controlling functions and reconfigurable function be carried by the microcontroller the sending unit is at one end (analog sensor) it always analyze the environment condition depend on that reconfigurable function be carried on in wireless sensor networks the node be increased depending on the application.

B. Simulation Results

The below simulation results (shown in the "fig. 5" and "fig. 6") clearly shows the exact reconfigurable process of the FPGAs depend upon the receiving inputs from the PIC to FPGAs. The FPGAs did the transmitting part from FPGA to PIC depend on the environmental condition the reconfiguration will occur.

This result shows the simulation output of a reconfigurable process between the controller and FPGA kit through the medicine tool. Fatherly wants to analyze the exact automation process want make the practical setup for viewing the exact range of output by through that see the data transmission range be increased through the Zigbee.

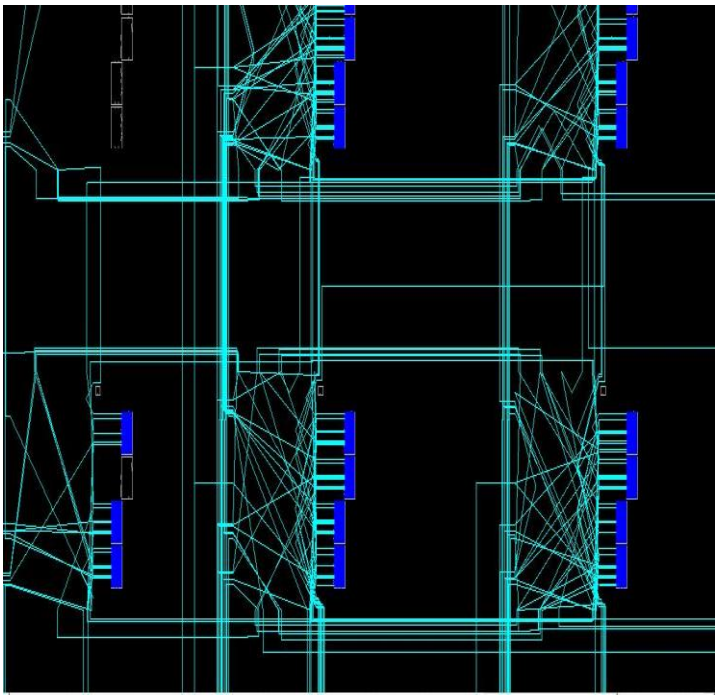
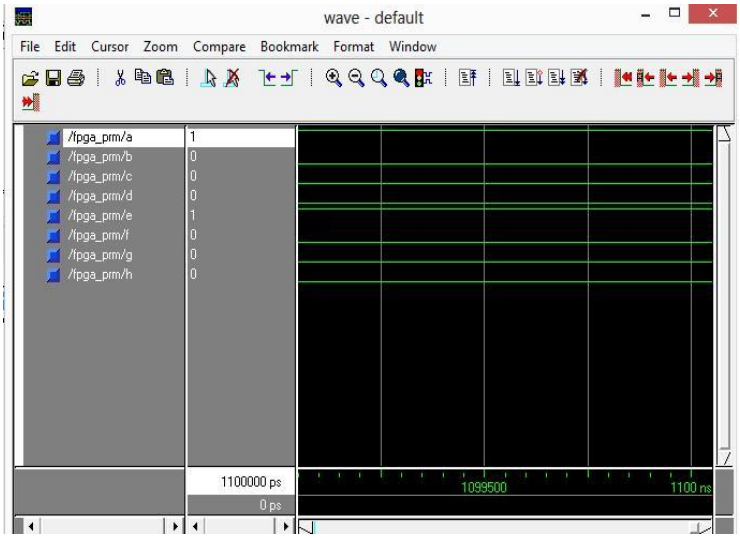


Fig. 5. Slot allotments for the digital sensors in various CLB



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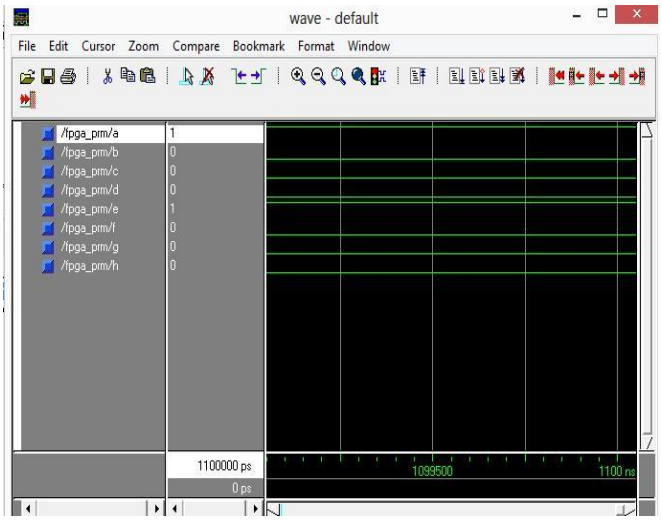

Fig. 6. Reconfigurable simulation results of FPGA to The Microcontroller From D. Sensor 1 and D. Sensor 2

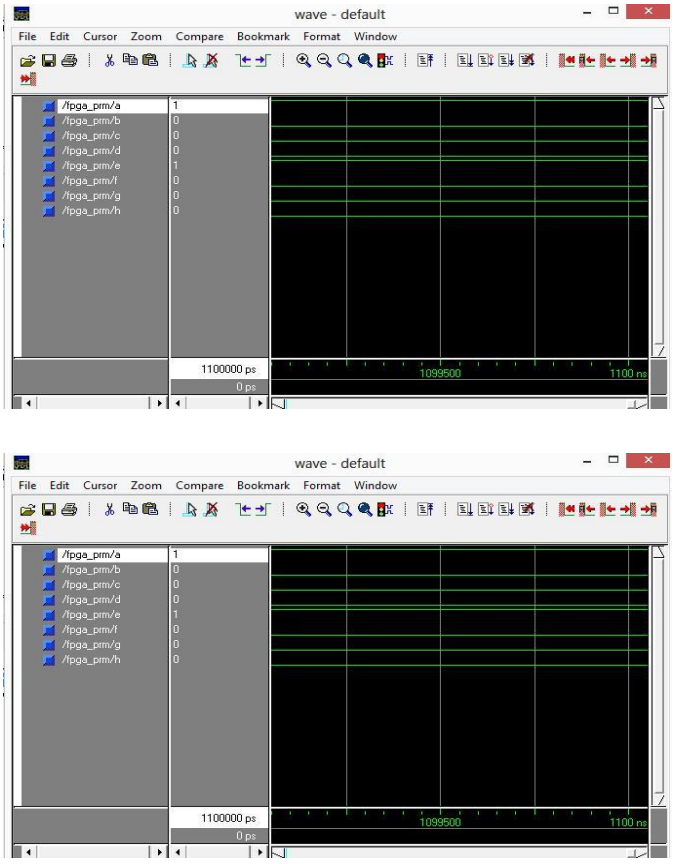

Fig. 7. Reconfigurable simulation results of FPGA to The Microcontroller From D. Sensor 3 and D. Sensor 4

The first thing in the equation, related to energy, the amount of energy utilized by the nodes (processing layer unit) for finishing the certain tasks and the related formulas be analyzed below. The cost

and efficiency, analyzed with the data rates.

Transmission Energy: The energy utilized by the hardware and software configuration during the data transmission.

Etrans = Ttrans * Ptrmode (1)

Ttrans is the time needed to transmit a configuration Ptrmode is the power consumption in this working

Reception Energy:

Erec = Trec * P recmode (2)

Reconfiguration Energy is the energy needed for a single reconfiguration

Erecnf = Treconf * Preconfmode (3)

Transmission Cost

Ctrans = Etrans / Enode (4)

Reception Cost

Crec = Erec/Enode (5)

Retransmission Cost

Cret = Eret/Enode (6)

Reconfiguration Cost

Creconf = Ereconf/Enode (7)

C. *Baud rate Analysis*

In normal form of the signal has 8 data bits and also has start and stop bit. The time period of bit is set by the baud rate. The typical value is 9600 baud means, which is about 10 k bits per second. In this paper 16 MHz crystal oscillator as used as clock for this kind of mid-range PIC this clock rate gives better resolution and the attain baud rate is 9600 compared to previous reconfigurable analysis work this reduce more delay in the data transmission path. For a device with FOSC of 16 MHz, desired baud rate of 9600.The following equations referred from [15]. Asynchronous mode 8bit BRG. The term BRG means Baud Rate Generator.

Desired Baud rate = FOSC/64 ([SPBRGH: SPBRG] +1)

Solving for SPBRGH: SPBRG

X = ((FOSC/Desired Baud rate) /64) /1

= ((16000000/9600)/64) /1, = 25.042 =25

Calculate baud rate = 16000000/ (64 (25+1)) =9615

Error = ((Calculate baud rate - Desired baud rate) / desired baud rate) *100.

= ((9615 - 9600)/9600) * 100=0.16%

Another formula for calculating the baud rate depend on the bit rate:

X = ((FOSC/baud rate) -16) / 16

Formula for producing 8bit or16 bit SPBRG solutions; SPBRG = INT (Fosc / Baud Rate / Divisor-1. The whole analysis part detail about the different baud rate medium in PIC how much the data transmission be varied in different baud rate condition. (Shown in Table. I).

TABLE I
DATA TRANSMISSION RATE

S. No	Desired Baud Rate	Calculated Baud Rate	X	Error Rate
1	9600	9615	25	0.16
2	2400	2377	104	0.96
3	4800	4717	52	1.73
4	19200	17857	13	6.99

VI. Summary And Discussion

This paper starts with how the embedded and VLSI field act a major role in the recent day real time applications after that, explain about the various layers in the design node in that how the PIC act an efficient one compare to the previous controllers whatever the advantage it's have like inbuilt ADC. Then how the interfacing work be done with the FPGA (Spartan 3) and how the Zigbee efficiently transmit the data's in quick time, the data transmission compare with the various baud rate set condition in that how 9600 baud rate efficiency. The main thing of usage of FPGAs is it to assume less amount of power and the same time all the interconnections in a reconfigurable manner so the hardware and software reconfiguration done in quick and efficient manner these things avoid the unwanted delays during the node reconfiguration. So now most of the designers refer the FPGA for industrial real time applications.

VII. Conclusion

The work deal in this paper is trying to improve the efficiency of data transmission in runtime reconfigurable techniques in wireless sensor network. From the help advanced microcontroller (PIC) lot of work time be reduced for the designer at the same time the resolution and the data transmitting efficiency also be improved. In future work the processors like ARM series may improve the data transmission rate by using various transmitting protocols. The most efficient thing is whatever the task may allocate in dynamic manner the changes be done in the both hardware and software configuration in a runtime condition. This kind of real time application will act a major role in the industrial automation and maintenance function.

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