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A Review of Ground-Bouncing-Noise Minimization Techniques in MTCMOS Circuits

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Abstract: Sub-threshold leakage current is exponentially increased with the scaling down the technology in CMOS circuits. MTCMOS is the method to reduce the leakage current but it arise a problem Ground bouncing noise which degrades the circuit reliability. Ground bouncing noise is important issue in MTCMOS circuits. It produced when circuit is transition from SLEEP to ACTIVE mode. This paper describes the various noise minimization MTCMOS techniques. The comparison of different techniques according to magnitude of Ground bouncing noise is tabulated. Dependency of Ground bouncing noise and power consumption on the various parameters like sleep transistor size, controlling transistor size, Temperature, supply voltage and threshold voltage is also characterized in this paper.

Keywords- *Battery lifetime, Leakage current, SLEEP modes and SLEEP to ACTIVE mode Transitions*

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1. INTRODUCTION

As the Technology advanced the dimension of MOSFET is continuously shrink, the supply voltage is also scaling down which maintain reliability of devices and decrease the power consumption [1]. To maintain a speed performance of the circuit the threshold voltage (*Vth*) of MOSFET is also scaling down. But for Low threshold voltage there is exponential increase in sub-threshold leakage current [2]. This sub-threshold leakage current contributes as a major part of the total power consumption of CMOS integrated circuits [3]. To extend the battery lifetime of portable devices such as laptops, notebook and mobile phones, sub-threshold leakage suppression is highly important [4],[5]. MTCMOS is the popular leakage power minimization strategies and it is also called power gating [6]. MTCMOS circuit, use high threshold voltage (*high-|Vth|*) sleep transistors (header and footer) which cut off the power supply or the ground connection to the low threshold (*low-Vth)* circuit blocks [7]. During the transition of MTCMOS circuit from the SLEEP to the ACTIVE mode, an instantaneous currents flow through the sleep transistors and the large amount of voltage fluctuations occur on both the real ground (ground bouncing noise) and the real power line (power bouncing noise) as illustrated in "Fig.1". Through the shared ground and power distributed network during wake up event the bouncing noise generated in one domain is transferred to the active blocks which will filliped the logic states of internal nodes distributed sleep transistors which shows the higher savings in leakage power consumption. This voltage fluctuation is known as ground-bounce noise or simultaneous switching noise [8]. Power and ground bouncing noise are activation noise are important reliability issues in future deeply scaled MTCMOS integrated [9].

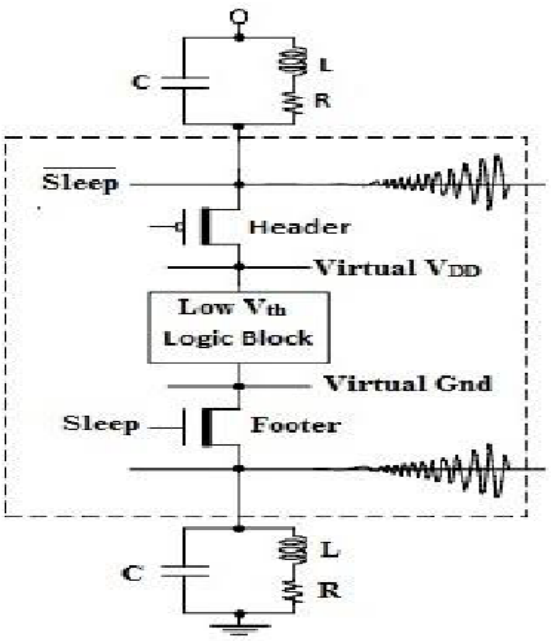

Fig. 1.Ground and power bouncing noise in conventional MTCMOS circuit

This paper is organized as: Sources and Factor affecting the ground bouncing noise is describe in section 2.Noise minimization techniques are introduced in section 3.Analysis on the basis of comparison of different techniques are described in section 4.This paper is concluded in section 5.

2. Ground Bouncing noise in VLSI circuits

Ground Bouncing noise is the primary causes of false switching in high speed circuits and a major cause of poor signal quality. While ground bounce is easily and

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accurately measure on CMOS components, Ground Bounce is a voltage fluctuation between the ground pin on a package of the component and the ground reference level on the die of the component. it is caused by current surge passing through the lead inductance of the package [10][11]. The effect of ground bounce more pronounce when all outputs simultaneously switched, Package pins, bonding wires, and on-chip IC interconnects all have parasitic inductances due to which the ground bouncing noise generated [12]. The ground bounce effect could result in not only the voltage fluctuations on the ground line but also electro-migration, which cause problems in the power gating circuit

2.1 Sources of Ground Bouncing Noise

The ground bouncing noise is produced by resistive and inductive of pins of package, on-chip bonding wires and power distribution network. The package parasitic impedances play major role in ground bouncing noise generation. MTCMOS circuit with package parasitic is shown in "Fig. 2.1". R, L, and C are the package parasitic respectively.C1and C2, are the parasitic capacitor of header and footer, parasitic wire capacitor of the virtual power and ground line.C3 and C4 are the parasitic capacitors of the low-Vth circuits connected to the virtual power line and the virtual ground line, respectively. In SLEEP mode, the circuit nodes between the virtual power and virtual ground lines have some intermediate steady-state voltages between VDD and GND. The four parasitic capacitors (C1, C2, C3 and C4) are charged or discharged to these steady-state voltages. During mode transition from SLEEP to ACTIVE a large transition current are produced ,due to which the internal node voltage of the low-Vth logic circuit transit toward either ~VDD or ~GND depending on the inputs values by each logic gate. The internal node, such as A of low- Vth logic block as shown in "Fig.2" is maintained at intermediate voltage in SLEEP mode. After the transition from SLEEP mode to ACTIVE mode header and footer is turn on, Due to degradation of voltage level of internal node such as A, P1 and N1 are activated simultaneously which produced short circuit current [13]. The transition current produced by the parasitic capacitors and short circuit current arise by the logic circuit is flow through the package parasitic impedances therefore cause voltage and current fluctuation on the real ground line.

2.2 Factor Affecting the Ground Bouncing noise

There are several factors which affect ground bouncing noise, such as Power Supply Voltage, Magnitude of Current Surge, Voltage Swing of virtual ground during Wake-up, Output and Ground Inductance Value, Output Pin Location, Number of Output Switching ,Sleep and controlling transistor size, Temperature, Threshold voltage and The Device Technology.

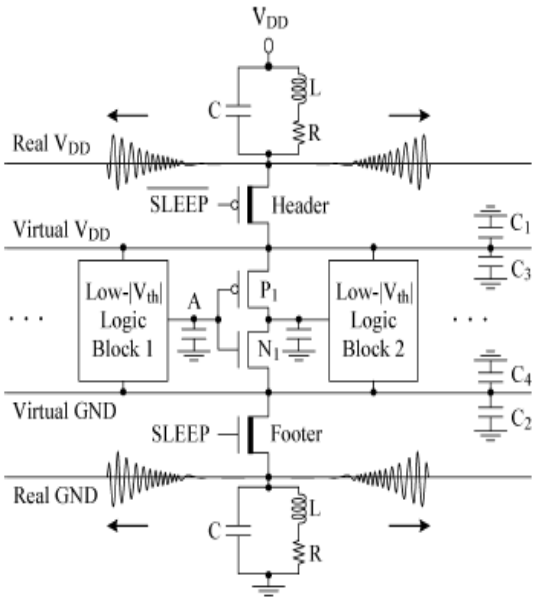

Fig.2.1 MTCMOS circuit with parasitic impedances of internal nodes and packages

2.2.1Power Supply Voltage Effects

The supply voltage magnitude VDD affects the amplitude of the ground bouncing noise. By reducing the VDD the output voltage swing, and the amount of current that the output can deliver is reduced. This will reduce the amplitude of ground bouncing noise. While reducing VDD by 40% the ground bouncing noise reduces approximately 60% [14].

2.2.2 Magnitude of Current Surge

Ground bouncing noise tends to limit the available current in CMOS outputs by reducing the voltage across the output impedance, therefore, reduces the current that flow. As the current surge increase the magnitude of ground bouncing noise.

2.2.3 Voltage Swing of virtual ground during Wake-up

As the voltage swing level at virtual ground line increases, it increase the peak of current surge during wakeup so the peak of ground bouncing noise is also increases.

2.2.4 Ground and Output Inductance Value

The inductance in the package is the inductance in ground lead and the inductance associated with all of the output pins. So the inductances in the outputs contribute the ground bouncing noise. While reducing the ground or VDD will not significantly reduce ground bounce, reducing the inductance in both the power leads and the outputs does reduce ground bouncing noise.

$$V = L\,dI/\,dt \qquad (2.1)$$

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By reducing the ground lead inductance a small reduction in ground bouncing noise can be realized, but it arises additional problems, like increase in crosstalk, may occur. Smaller packages, such as SOIC and LCC/PLCC packages, do reduce ground bouncing over both standard and center-VDD/ground-pinned DIP packages.

2.2.5 Output Pin Location

The amplitude of ground bounce is also affected by the position of the output pin with respect to the device ground. The effects of pin location are, when the output pins farthest away from ground produce large amount of ground bounce and when the output pin closest to ground shows the ground bounce on the best case pin. Choosing outputs close to ground, the magnitude of ground bounce may be reduced by nearly half [14].

2.2.6 Number of Outputs Switching

The simultaneous switching of number of outputs affects the amplitude of ground bouncing noise. In a simple model assume the output impedances of each active output as resistors and inductors in parallel. For resistors of same value in parallel, the net resistance is R/n, where R is the output impedance of each transistor, and n is the number of resistors. As more outputs switch at the same time, the output resistance is decrease and more ground bounce Since, As the number goes up, the amplitude of the bounce will be generated ground bounce pulse also increases. Therefore, devices that have less number of outputs will have less ground bounce [14].

2.2.7 Sleep and controlling transistor size

The amplitude of ground bouncing noise is also affected by the size of Sleep transistor. For high speed operation of the circuit the size of sleep transistor should be large but this will increase the current surges during mode transition from SLEEP to ACTIVE mode. It will increase the amplitude of ground bouncing noise. To reduce the amplitude of ground bouncing noise the size of Controlling transistor should be large. Large widths of controlling transistor decrease the steady state voltage, which reduce current surges, since reduce ground bounce.

2.2.8 Temperature

Ground bounce is increase with increase of temperature and the leakage power consumption is more at higher temperature.

2.2.9 Device Technology

With advance of technology the amplitude of bouncing noise is increase. As the technology shrink the ground bounce is most effective. it is desirable to reduce the bounce at deeply scaled technology.

3. Different Noise Minimization MTCMOS Techniques

3.1 Trimode or Novel MTCMOS Technique

In Trimode MTCMOS structure an intermediate PARK mode is introduce between the SLEEP and the ACTIVE modes to reduce the amplitude of ground bouncing noise. A high-Vth PMOS transistor called Parker is connected in parallel to the footer sleep transistor of MTCMOS circuits [14] as shown in "Fig.3.1(a)". Sleep transistor (N1) and the Park transistor are turned off in SLEEP mode to reduce the sub-threshold leakage current of an idle circuit. The virtual ground line is maintain at Voltage ~VDD in SLEEP mode. Before transition of circuit at Active mode, the Park transistor is turn on and (N1) maintain in cut-off mode.The circuit at intermediate PARK mode. Since virtual ground line is discharge to the threshold voltage of Park transistor lower the voltage swing range, which reduces the amplitude of ground bouncing noise. The footer sleep transistor is turned on and the Park transistor is turned off. The virtual ground line is discharge to ~Vgnd to complete the reactivation process, and to fully activate the circuit.

The peak amplitude of ground bouncing noise when the circuit is directly transition from SLEEP to ACTIVE mode without any intermediate mode. Noise amplitude also analyzed while varying the supply voltage from 0.9V to 1.5 V as shown in "Fig.3.1(b)". The peak amplitude of ground bouncing noise when the circuit is transition from SLEEP to ACTIVE mode through intermediate PARK mode Intermediate mode reduced Noise amplitude is analyzed while varying the supply voltage from 0.9V to 1.5 V as shown in "Fig.3.1(c)" While comparing the "Fig.3.1(c)" results with the"Fig.3.1(b) shows the ground bouncing noise reduces 50% through intermediate mode.

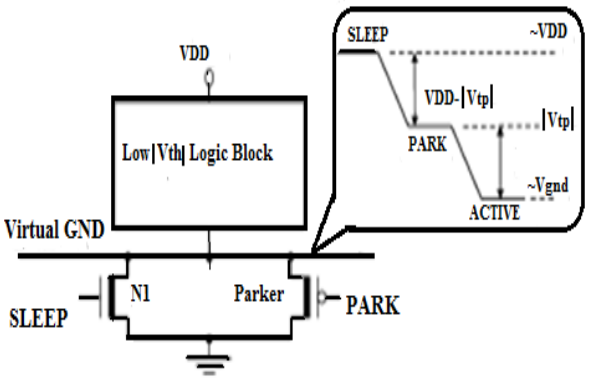

Fig.3.1 (a) Trimode power gating structure with high Vth SLEEP and PARK Transistor

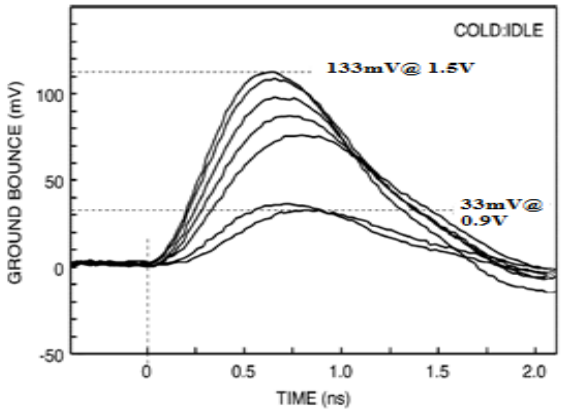

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Fig.3.1 (b) Ground bounce amplitude when power mode switched directly from SLEEP (COLD) to ACTIVE (IDLE) mode

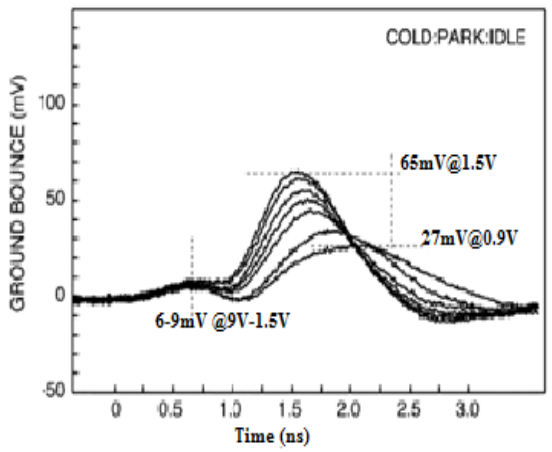

Fig.3.1 (c) Ground bounce amplitude when power mode switched from SLEEP (COLD) to ACTIVE (IDLE) mode through PARK mode

3.2 Dual-Switch MTCMOS Technique

In dual switch technique [15], an intermediate HOLD mode is introduced to suppress the ground bouncing noise, similar to Trimode [14]. It is an alternative method to suppress the ground bounce in gated- &ground structure As shown in "Fig. 3.2" A high-Vth NMOS transistor is connected in parallel to the header sleep transistor connected in between real power line and virtual power line similarly high-Vth PMOS Transistor is connected in parallel to the footer sleep transistor which is connected in between the real ground and the virtual ground line. In an intermediate HOLD P2 and N2 high Vth transistor turned on and the header (P1) and the footer (N1) are maintained at cut-off mode. In the SLEEP mode, all the transistors i.e Sleep transistors (P1, N1) and Dozer transistor (P2, N2) are turned off which reduced the sub-threshold
leakage currents. The voltages maintained at virtual power and ground lines are approximately equal to (Vmid). Before the activation of the circuit, The circuit transitions to the intermediate HOLD mode i.e from the SLEEP mode to the HOLD mode. VDD- Vtn-Vtp voltage is produced between the virtual lines. And from the HOLD mode to the ACTIVE mode transition P1 and N1 are activated. The virtual power line and ground line is charged and discharged to ~VDD and ~Vgnd. HOLD mode reduces the voltage swing range which reduces the amplitude of Ground bouncing noise.

3.3 Dual Diode Vth MTCMOS Technique

In Dual diode Vth power gating technique diode is connected in parallel path of sleep transistor (header and footer), this will reduce the voltage swing range. Which reduced the ground bouncing noise This will also provided the significant higher reduction in leakage.[16] As shown in "Fig. 3.3" Dual Diode Vth technique is one of the alternative of dual switch MTCMOS technique which further reduce the ground bouncing noise compare to dual switch technique. In conventional power gating technique the voltage swing is VDD-0V during RUN to CUT-OFF mode produce the large amount of Ground bounce. In case of "Fig.3.3 (a)" swing range is (Vthp+Vthn)-0V.which reduces the ground bouncing noise.

In case of "Fig.3.3 (b) the voltage swing is VthD -0V, VthD is the diode threshold voltage. Swing range is less and there is no bounce produced during RUN to HOLD mode in this case, so have less ground bouncing noise in this case, and HOLD intermediate mode reduces the voltage fluctuation and hence Ground bounce..Dual diode Vth give the better performance than other techniques [17].

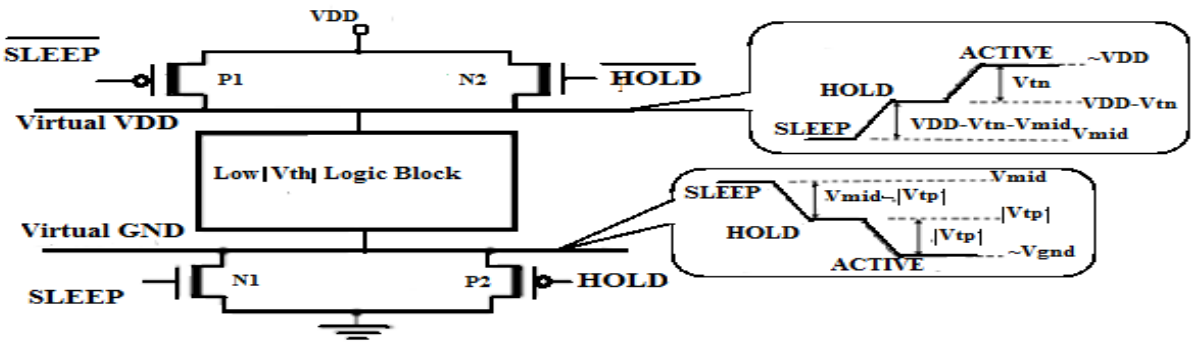

Fig. 3.2. Dual-switch power-gating structure High-Vth sleep transistors are represented with a thick line in the channel region with HOLD mode. 0V < Vmid < VDD

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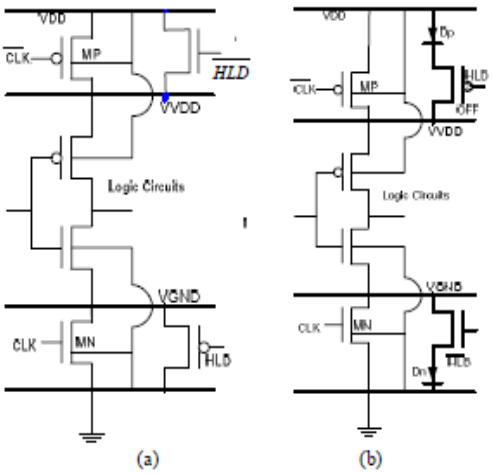

Fig. 3.3(a) Dual Switch power gating structure Fig. 3.3(b) Dual diode Vth power gating structure

3.4 Tri-Transistor- controlled MTCMOS Technique

In tri-Transistor-controlled MTCMOS technique to implement the intermediate DOZE mode for ground bouncing noise suppression from SLEEP to Active mode .A .high-Vth PMOS sleep transistor (called Dozer) is connected in parallel with the footer [18] .as shown in" Fig.3.4(a)". In the SLEEP mode, all the transistors i.e Sleep transistors and Dozer transistor are turned off which reduced the sub threshold leakage currents.

In the DOZE mode, the Dozer and header are turned on. The footer is at cut-off mode. In ACTIVE mode, the header and footer are turned on. The MTCMOS circuit operates with high speed .The SLEEP mode is the preferable mode of operation for minimization the leakage power consumption. DOZE mode is an intermediate mode during SLEEP to ACTIVE mode to suppress the ground bouncing noise .The virtual power line is charged from intermediate voltage level Vmid (0V < Vmid < VDD) towards ~VDD and The virtual ground line is discharged from Vmid toward the threshold voltage of the Dozer. At the end of the intermediate transition period to complete the circuit activation process footer transistor is turned on.

During the transition from DOZE mode to the ACTIVE mode, the virtual ground line is discharged from Vtp to ~Vgnd. Two-step wake-up process reduce the range of voltage swing on the virtual ground line which will reduced ground bouncing noise To reduce the transition delay from the SLEEP to the DOZE mode, a low-Vth Dozer can be used, as shown in "Fig.3.4(b)".Tri-transistor-controlled MTCMOS with high- Vth dozer transistor (TTH) and the tri-transistor-controlled MTCMOS with low-Vth dozer transistor (TTL) of the tri-transistor-controlled technique is use for ground bouncing noise reduction.

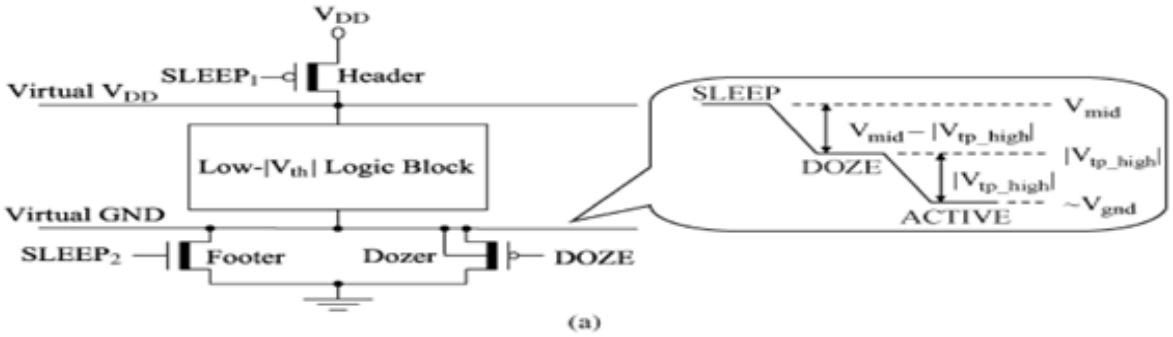

Fig. 3.4 (a) Tri-transistor-controlled MTCMOS circuit technique presented in [18]. High Vth sleep transistors are represented with a thick line in the channel region

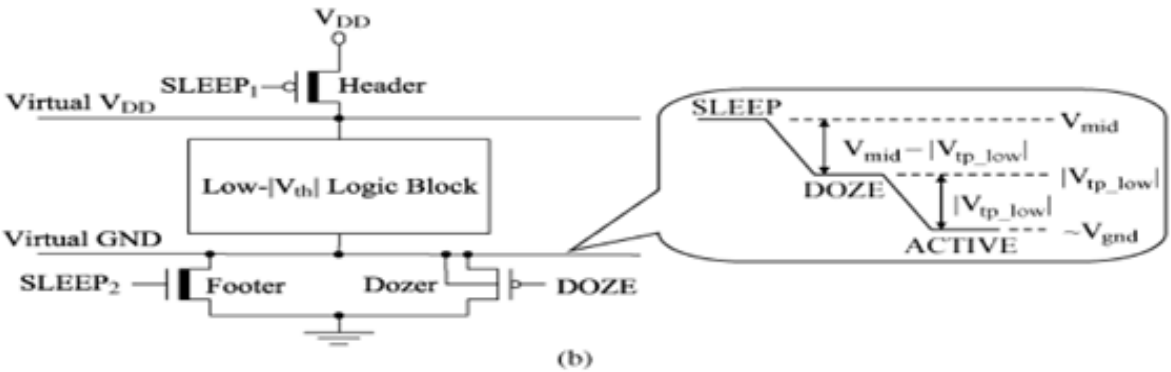

Fig. 3.4 (b) Tri-transistor-controlled MTCMOS circuit technique presented in [18]. High Vth sleep transistors are represented with a thick line in the channel region. (b) TTL. 0V < Vmid < VDD

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3.5 Trimode Technique with low Vth parker (TML)

In the standard tri-mode circuit as shown in "Fig. 3.5(a)" high-Vth Parker replaced by a low Vth- Parker as shown in "Fig. 3.5(b)".TML technique is implemented.TML i.e Trimode with low Vth parker the discharging speed of virtual ground line is increase during mode transition from SLEEP mode to ACTIVE mode compare to standard Trimode technique. Steady-state voltage at PARK-mode on the virtual ground line is decrease because of the lower resistance of the low Vth Parker, which reduces the voltage swing of the virtual ground line during the mode transition from PARK to ACTIVE mode. The peak amplitude of the second wave of activation noise is decreased with the TML technique as compared to standard Trimode circuit. The maximum activation noise produced by an MTCMOS circuit is reduced through Parker resizing [19]. The small size Parker transistor is required to minimize noise in a TML circuit as compared to the standard tri-mode MTCMOS circuit.

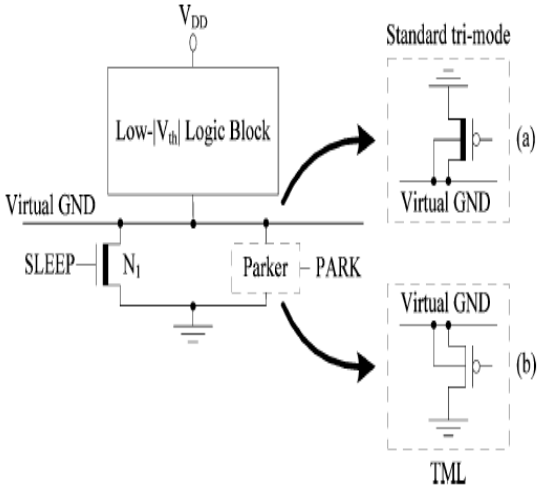

Fig.3.5. Trimode MTCMOS circuits. (a) Standard tri-mode with zero body biased high-Vth parker. (b) Tri-mode with zero body biased low-Vth parker.

3.6 Trimode Technique with Forward Body biased Parker

A new design technique of Trimode is based on forward body bias. Two forward-body-biased noise-aware tri-mode MTCMOS circuit techniques are proposed as shown in "Fig.3.6 (a)" and (b). The forward body bias power gating technique further suppresses the activation noise and delay as compared to the standard zero-body-biased tri-mode and TML techniques. "Fig.3.6 (a)" shows The forward body-biased high-Vth Parker transistor. "Fig. 3.6 (b)" shows The forward body-biased low-Vth Parker transistor. The threshold voltage of Park transistor is decreased by applying the forward body bias, During the transition from SLEEP to PARK mode the first wave of activation noise is increased but low Vth parker suppress the second wave of activation noise during transition from PARK to ACTIVE mode [20].

The minimum achievable peak amplitude of activation noise is further decreased with a smaller sleep transistor.

The Voltage of virtual ground line varies with the mode of operation of an MTCMOS circuit, the size of the Parker, and the size of the Low-vth circuit block. To dynamically adjust the body voltage of the Park transistor a low- Vth NMOS transistor (Biaser) and a negative dc voltage source (Vbias) are attached to the tri-mode circuit. The Biaser is maintained cutoff mode by shorting the gate and source terminals. The body bias voltage of the Parker is controlled by the drain current of the Biaser. The Park transistor experiences forward body bias in all three modes of operation (SLEEP, PARK, and ACTIVE) with this body bias generator. The tuning of forward body bias voltage of the Parker is done by adjusting Vbias.

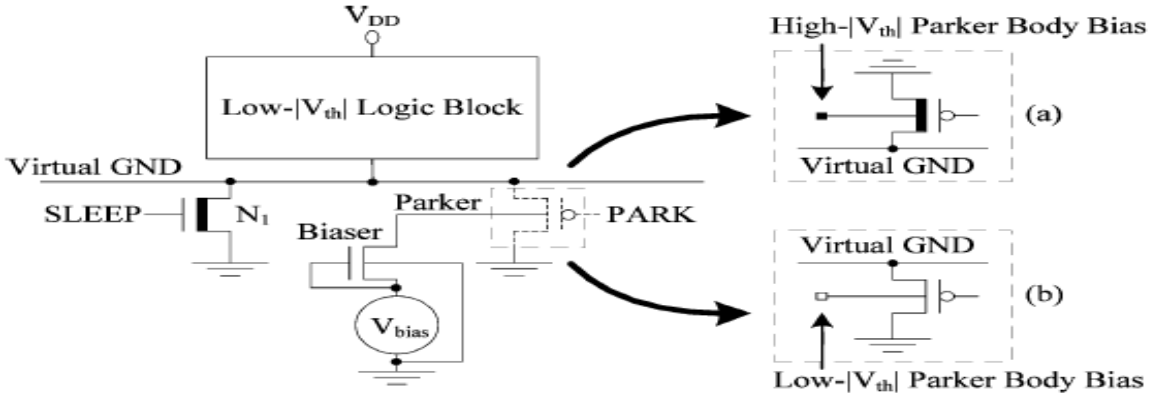

Fig.3.6. MTCMOS circuits with forward-body biased Parker (FBB) (a) Tri-mode MTCMOS circuit with forward body biased high-Vth parker (FBBH) (b) Tri-mode MTCMOS circuit with forward body biased high-Vth parker (FBBL).

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TABLE-1 Comparison of Peak amplitude of Ground bouncing Noise (mV) in different Techniques based on different parameters at 110 ^{o} C and 0.12um Parker size.

Researchers		S.kim et.al[]		M.H.Chowdhury et.al[]	H.jiao et.al[]	H.jiao et.al[]	H.jiao et.al[]
Techniques/Year		2007		2008	2010	2010	2012
Circuit used		32 bit carry look ahead adder		2 input NAND Gate	32 bit brunt kung adder		32 bit brunt kung adder
Technology		130nm		65nm	90nm	90nm	80nm
Supply Voltage VDD		1.5V	0.9	-----	1V	1V	1V
Trimode		65mV	27mV	-----	25.63mV	15.44mV	22.91mV
Dual switch		----		3.4mV	53.11 mV	41.78mV	-----
Dual diode Vth		----		3.1mV	----	---	-----
TTH		----		-----	27.97 mV	22.94mV	----
TTL		----		----	36.34mV	21.68mV	------
TML		----			-----	----	19.72mV
FBBL	**Vbias=0V**	----			-----	----	18.88mV
	Vbias=optimum						16.58mV
FBBH	**Vbias=0V**	----			----	----	21.55 mV
	Vbias=optimum						19.43Mv

4. ANALYSIS

In "Table-1" Comparison of peak amplitude of ground bouncing noise in different MTCMOS techniques based on different parameters has been presented."Table-2", Power consumption, Area overhead and Delay in different Techniques have been tabulated. In this paper, comparative study of different MTCMOS techniques has been made at 110^{o}C temperature with 0.12um Parker size.

5. CONCLUSION

After analysis, it is found that FBBL power gating technique with optimum bias show the minimum ground bouncing noise and Delay as comparison of other techniques. Leakage power reduction in this case is 95.05 %.and also having less Area overheads.

TABLE-2 Comparisons of Leakage Power, Area and Delay in different Techniques based on different parameters at 110^{o} C Temperature and 0.12um Parker size.

Techniques		32 bit Shift Register			32 bit brunt kung adder			
		Leakage Power consumption (nW)	Area Overheads reduction	Leakage Power Reduction	Leakage Power Reduction	Leakage Power consumption (nW)	Area (micro-meter square)	Delay (ns)
Trimode		3585.18	88.87%	46.92%	99.90%	88.1	1506	88.56
Dual switch		1983.16	85.16%	94.11%	99.80%	100.8	1691	133.82
TTH		3786.02	85.16%	49.81%	99.80%	102.4	1778	87.41
TTL		4094.27	85.16%	55%	99.80%	102.4	1778	79.66
TML		----	---	---	98.40%	----	----	78.6
FBBL	Vbias=0V	----	---	----	96.86%	----	----	79.9
	Vbias=optimum	----	---	---	95.05%	----	----	75.95
FBBH	Vbias=0V	----	---	---	98.98%	----	----	103.8
	Vbias=optimum	----	---	---	96.76%	----	----	101.12

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