Design and Analysis of A Dual Chamber Cardiac Pacemaker Using VHDL in Biomedical Application

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***Abstract*—** This research paper aims at a dual-chamber pacemaker design which is being simulated using VLSI architecture in Xilinx and is being modified by changing clock cycle to provide better results as compared to other pacemaker. It follows a state machine approach to achieve the desired purpose. The heart of the system is the pacing pulse generator, which forms the major part of the project. It is being designed using VHDL and implemented in hardware using FPGA. The code has been modified and optimized for different modes of stimulation. Reasonable components in the construction of the detection circuit and other peripherals had been used for simulation. It had been assured that memory and data compression techniques monitoring devices remotely had been used for improvements in the overall performance.

Keywords- *Dual chamber pacemaker, State machine, Data compression techniques*

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I. INTRODUCTION *(HEADING 1)*

The first pacemaker was introduced in the 1950s. It had very few transistors because of advancing of technology. A pacemaker system that is implanted in a patient has millions of transistor. Heart diseases cause a lot of deaths. The deaths caused due to a combination of accident; cancer and diabetes is equal to the ratio of deaths due to heart diseases. Bradycardia is one of the common heart diseases and by using the pacemaker devices it can be treated. The pacemaker monitors the rate of the heart and the rhythm. The pacemaker provides the electrical stimulation through the electrodes if the heart beats too slowly or does not beat at all. Therefore, improvement of these devices for their enhanced performance and for increasing their operational ranges is needed.

Depending on the number of the heart chambers that are stimulated and monitored, the pacemakers can be classified as single chamber and dual-chamber. Dual-chamber pacemaker offers more advantages than the single one in term of patient life quality, such as reduction in atria fibrillation, pacemaker syndrome and heart failure. [1]

It contains three components: a pulse generator, Stimulation and detection circuit [2]. The pulse generator includes an energy source of the pacemaker and other digital circuits. A lithium vanadium oxide / silver which have a shelf life up to 10 years are the main energy source. The digital circuit is different in a microcontroller which manages the control and does manipulation of high as well as a low sequencer for handling routine function of stimulation. In this paper, both components are written in the VHDL code contained and are based on the FPGA card that controls the execution of the stimulation into account by taking input from the other components of the pacemaker [2].

The pulse generator receives inputs by a detection circuit from the heart through the electrode or electrodes. The pulse generator detects electrical activity of the heart and responds according to the way it was programmed. Electric stimulus pulse generator move by simulation leads to the tip of the electrode. The pacing wires are used to stimulate the atrium or the right ventricle of the heart. As such, it performs twofold function of the transmission of signals from one side to the other pulse generator [3].

The detection circuit performs the necessary signal processing of the signals from the heart and provide input to the pulse generator. It acts as an interface between the generator and cable [4].

II. MATERIALS AND METHODS

A. Dual Chamber Pacemaker:

A dual-chamber pacemaker typically necessitates two pacing leads: one lead is placed in the right auricle and the other inside the right ventricle. A dual-chamber pacer monitors (i.e. senses) electrical body process in the atrium and the ventricle to see the need of tempo. If need be, then, the pacing pulses of the atrium and ventricle usually are timed so that they mimic the natural way of pumping. The trial-stimulating impulse is generated, and, after a pre-determined time interval (two hundred milliseconds), the ventricular-stimulating impulse is generated.

The same logic can apply to the left side of the heart in case it is not functioning properly. From the time to time, the dual chamber pacemaker can be programmed to behave as a single slot provided pacemaker depending on the excitation inputs and corresponding outputs.

B. State Machine

This is an extension of the single chamber to dual chamber pacemaker. The actual basic working principle is the same. In

the dual chamber pacemaker, after the pacing of atrium, the state of the pacemaker changes to the 'Reset Timer' condition of the ventricle. In the case of single-chamber pacemaker, it changes the 'Reset Timer' state of the atrium. Accomplishment of this task continues in a cyclic manner time and again [6].
The following is the state diagram.

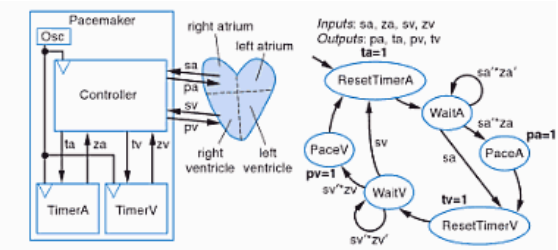

Figure1: State Diagram of Dual chamber pacemaker. [6]

C. *Pacemaker modes*

Pacemakers pulse generators can be of assorted types depending on the modes involving pacing. The human body has unlike requirements, and those vary from one to another. Accordingly the pacemaker for one person cannot be generalized for many. Depending on the requirements, the pacing pulse can be sensed by the 3rd wave of the ECG. Also, you can find competitive or non-competitive modes connected with pacing depending on if the implicit pacing of the heart is perceived by the pacemaker or not. Pacemaker's modes can be:

- Demand: if the particular pacemaker senses the presence of a real R wave and paces only if your R wave is not present.
- Not Demand: if the pacemaker paces from center with time interval irrespective of the presence of a real intrinsic R wave.
- Triggered: if the actual pacemaker paces the heart every clip an R wave is detected i.e. the pacing function is activated by the R wave.
- Inhibited: if your pacemaker paces the heart every clock time an R wave is skipped, and the pacing function inhibited because of the R wave. [1]

D. *Automatic capture recognition of Pacemaker pulses*

Electrodes - A fundamental requirement is a very low after potential of the electrode which can be used to measure the actual signal values at that point. This is because the practical usage requires that the signal strength must be measured by the stimulating electrode itself so that we can avoid the implantation of additional sensors and that no discharging pulses are required to reduce their additional energy consumption. Subsequently these electrodes needed to be used so that after potentials are under one mV (pulse: 4.8 V, 0.5 ms, auto short 10 ms). Also it should be negligible as compared to their surface structure so that it is possible to increase the surface area by magnitude of more than three orders. [8]

Basic functioning – The basic functioning and simulation of the pacemaker is based on the recognition. It depends on the examination of the performance. As it can be sensed by the waveform of an intrinsic activity, so it can be used to add other parameters for comparison. A reliable differentiation has to be done by the measurement of the potential in an interval having a duration near about 60 ms which start when the pulse has been released after 150ms. If the reference value exceeds by all measurements taken in this window then, the pulse can be put in the capture mode. This procedure avoids the disturbances of the initial peaks of the intrinsic activity which have high amplitudes.

In addition, the digital circuit also has to handle the effect that the instrument has on the heartbeat of the human body. An artificial stimulation and an intrinsic activity coincide, which results in an undefined waveform of the signal. Therefore, these signals cannot have interference and must be avoided. This can be accomplished by altering the pacemaker timing and clock pulse circuit [8].

III. RESULTS AND DISCUSSION

The Dual chamber pacemaker had been designed by using different VHDL module written for each component as per the functional block diagram. The overall functionality of the pacemaker is as shown by the behaviour simulation of the model.

The behaviour simulation screen shows that there are no error in the components when checked at the individual level. After that all these components are connected together to create a complete system which taken proper input, processes the signals and activates various circuits if an irregular activity is sensed. After this simulation, we get the synthesis and RTL schematic report of the components which are part of a complete circuit.

All the variables and blocks can store 32-bit data at a time so the data transfer between the components can also be less than or equal to 32 bits. The blocks are used to store the data rate of the pacemaker and to sense the heart rate by using the circuit elements.

In figure 2, the overall schematic diagram after simulation is shown. The sensing circuit collects the signals from the patient's heart and then performs ample signal conditioning so as to get a pulse at every sensed or non-sensed contraction of the heart depending on whether it is in the triggered mode or inhibited mode. This circuit first taps out the ECG signal from the heart and then detects the R wave of that signal and then generating a pulse which will act as an input to the pulse generator according to the R wave so that the routing pacing operation may continue after that. The leads of the pacemaker are of direct contact type. They work as transducers which converts the ionic flow of the body to electron current and then convert the electron current to an electric potential. Ag/AgCl electrodes and electrolyte pair are used. A half-cell potential is created at the interface with a Nernst potential at the electrolyte-skin interface. Two electrodes should be used to measure the potential differences between two-skin surfaces.

The basic output is dependent upon the sensing circuit and its design concept. Therefore, lesser importance has been given to that parts which are associated with the normal activities of the pacemaker.

The simulation in figure 1 shows the following behavior of the timer. It starts to count from 0 to the timeout value. If the start is held high, it just repeats but if the start is not held high; it resets and stops at zero.

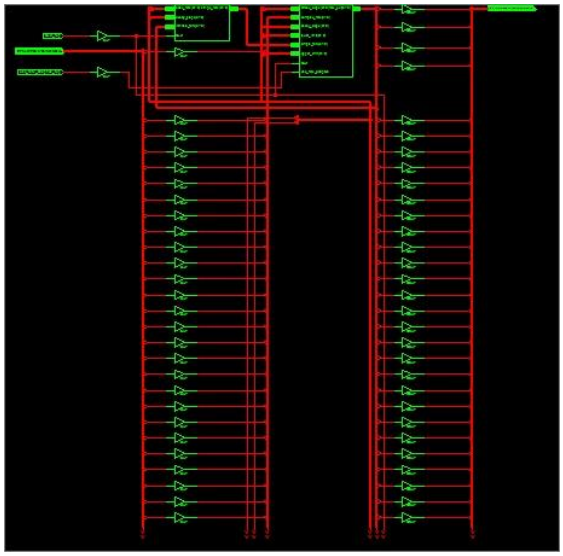

Figure 2: Complete schematic diagram of the circuit

The timeout value of the circuit is changed from 255 to the value which is less than the current count then the timer times out immediately.

The following simulation result shows that the tests conducted for the pacemaker controller component are in the normal condition at present. In the case of systems which are driven by the timers, testing the controller independently is an excellent way to increase the speed of the system.

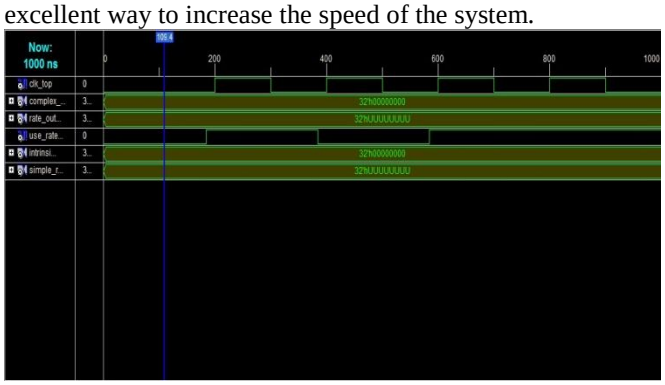

Figure 3: Timing diagram of the different pacemaker components after 1000 ns

The test shows that the system is responding to the sense, timeout and reset inputs while delivering the suitable reset timer and pace request outputs.

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