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Comparative Study of Leakage Reduction Techniques for Domino Logic Circuit

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***Abstract*:** With the advancement of technology, size of transistor, supply voltage, gate oxide thickness has been decreased but the leakage in device has increased. Projecting these trends, it can be seen that the leakage power dissipation will equal to the active power dissipation within a few generations. Hence, efficient leakage power reduction methods are very critical for the deep-submicron and nanometer circuits. In this paper Lector based Footed Diode Domino Logic circuit technique is introduced for leakage reduction, which provides efficient reduction in leakage in ideal and non ideal mode of operation. In this technique a p-type and an n-type leakage control transistor (LCT) are introduced between the pull-up and pull-down network, and the gate of one is controlled by the source of the other. For any combination of inputs, one of the LCTs will operate near its cut-off region and will increase the resistance between supply voltage and ground, resulting in reduced leakage current.

Keywords: Delay, Deep submicron, Domino Logic, Power optimization, Sub-threshold Leakage, Transistor Stacking.

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1. INTRODUCTION:

Power dissipation is an important factor of consideration in the design of CMOS VLSI circuits. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. There are mainly three sources of power dissipation: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub-threshold currents. The former is due to the stored charge between the drain and bulk of active transistors while the latter is due to the carrier diffusion between the source and drain of the OFF transistors. Latest portable electronic device contains complex design as compared to single VLSI design. Much of the power dissipation in a portable electronic device comes from non-digital components. IC power dissipation consists of different components depending on the circuit operating mode. First, the switching or dynamic power component dominates during the active mode of operation. Second, there are two primary leakage sources, the *active* component and the *standby* leakage component. The standby leakage may be made significantly smaller than the active leakage by changing the body bias conditions or by power-gating.

2. SOURCES OF POWER DISSIPATION:

There are four main sources of leakage current in a CMOS transistor as shown in Fig. 2:

1. Reverse-biased junction leakage current (IREV)

2. Gate induced drain leakage (IGIDL)

3. Gate direct-tunneling leakage (IG)

4. Sub-threshold (weak inversion) leakage (ISUB)

2.1 Reverse-biased junction leakage current (IREV)

The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is OFF.

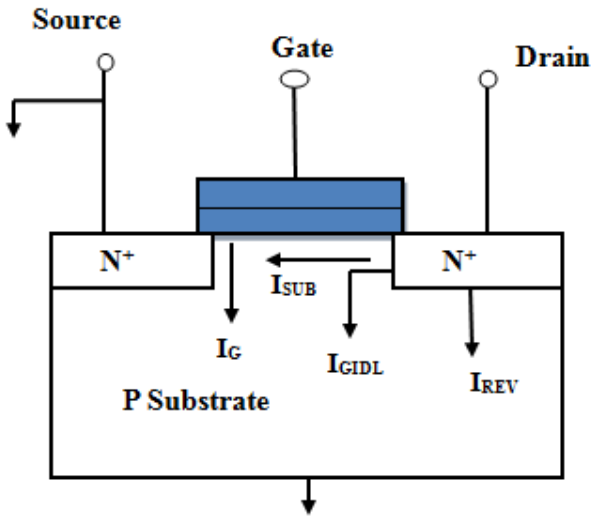

Fig. 2: Sources of Leakage

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2.2 Gate-induced drain leakage (GIDL)

The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors.

2.3 Gate Direct Tunneling Leakage (IG)

The gate leakage flows from the gate through the "leaky" oxide insulation to the substrate. In oxide layers thicker than 3–4 nm, this kind of current results from the Fowler-Nordheim tunneling of electrons into the conduction band of the oxide layer under a high applied electric field across the oxide layer.

2.4 Sub-threshold Leakage (ISUB)

The sub threshold leakage is the drain-source current of a transistor operating in the weak inversion region.

3. LEAKAGE REDUCTION TECHNIQUES:

3.1 High-Speed Domino Logic**:**

HS-Domino resolves the trade-off between performance and noise margins in conventional CD-Domino logic while dissipating low dynamic power with minimal area overhead.

HS-Domino has a speed advantage of 30% at low threshold values. This circuit also dissipates up to 24% less dynamic power. [1]

As Domino Logic works in two phases ie. Precharge phase and evolution phase. During precharge phase when the clock signal is low, keeper transistor Q_2 becomes off. (fig.2)So at the beginning of evolution phase keeper transistor will be off. Contention is thus eliminated between the keeper and the pull- down devices during evaluation. Therefore the Domino Logic works faster in comparison to the previous circuit.

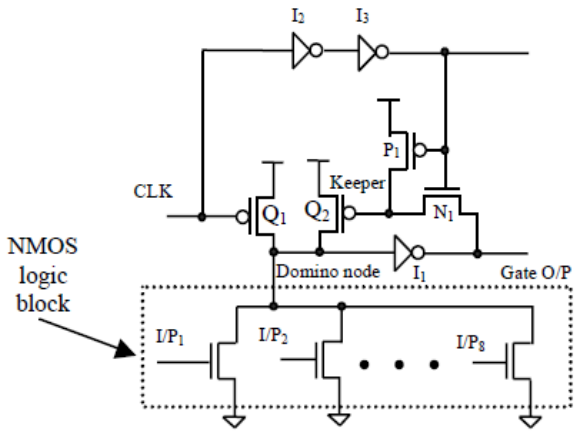

Fig. 2: An 8-input HS-Domino OR gate

3.2 Leakage Control with Efficient use of Transistor Stacks:

An approach which does not require multiple threshold voltages or substrate biasing, but takes advantage of leakage behavior in stacks of MOS transistors to reduce sleep mode leakage while avoiding active mode performance loss. A low leakage state occurs when as many MOS transistors as possible are turned off in each leakage path. We then insert leakage control transistors away from the critical path in leakage paths where only one transistor is off. It offers a leakage reduction on the order of 35% to as much as 90% relative to an unmodified circuit with a minimum-leakage vector applied. Stacking transistor insertion exploits the circuit state once a minimum-leakage-input vector has been applied. For each gate in a high-leakage state, we insert a leakage-control transistor between the power supply and the pull-up network or between

ground and the pull-down network no leakage path

passes through more than one transistor which is turned off. [2]

3.3 Sleep Switch Dual Threshold Voltage Domino Logic with Reduced Standby Leakage Current **:**

The sleep switch circuit technique significantly reduces the subthreshold leakage energy as compared to both standard low-threshold voltage and dual threshold voltage domino logic circuits. This technique enhances the effectiveness of actual V_{th} CMOS technique to reduce I_{sub} by strongly turning off all of high V_{th} transistor.

High threshold NMOS transistor is added to the dynamic node of domino logic circuit. Operation of this transistor is controlled by separate sleep signal.

During Active Mode- Sleep signal is low and sleep switch is off and the proposed dual V_{th} circuit operates as standard dual-V_{th} domino circuit (as shown in fig.4).

During standby mode- The clock signal is maintained high, turning off the high- $_{Vth}$ pull-up transistor of each domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, thereby turning off the high-V_{th} nMOS transistor within the output inverter.[3]

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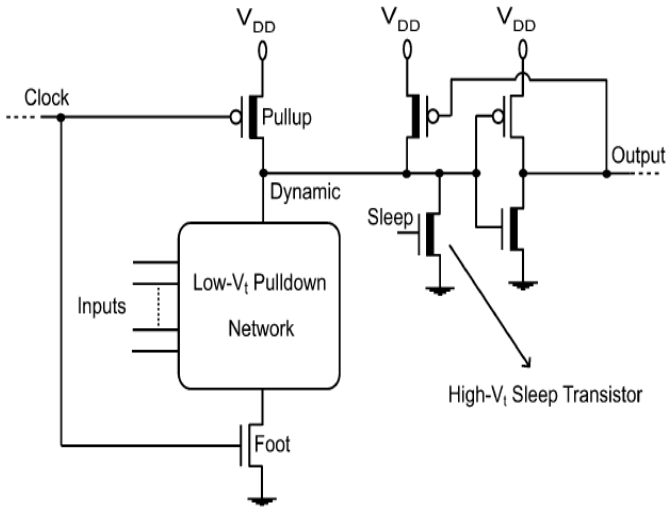

Fig.3.3. Sleep Switch Dual Threshold Voltage Domino Logic

3.4 PMOS-Only Sleep Switch Dual-Threshold Voltage Domino Logic**:**

A circuit technique for simultaneously reducing the sub-threshold and gate oxide leakage power consumption in domino logic circuits has been proposed. Only p-channel sleep transistor and dual threshold CMOS technology are utilized to reduce leakage. One sleep transistor is added at the dynamic node of the circuit to reduce Isub by turning off all the high Vt transistor.

Similarly a sleep switch is added at the output node of the circuit to suppress the voltage across the gate and minimizing the Igate. As shown in fig. 3.4.

The energy overhead of the circuit technique is low,

justifying the activation of the proposed sleep scheme by providing a net savings in total energy consumption during short idle periods.[4]

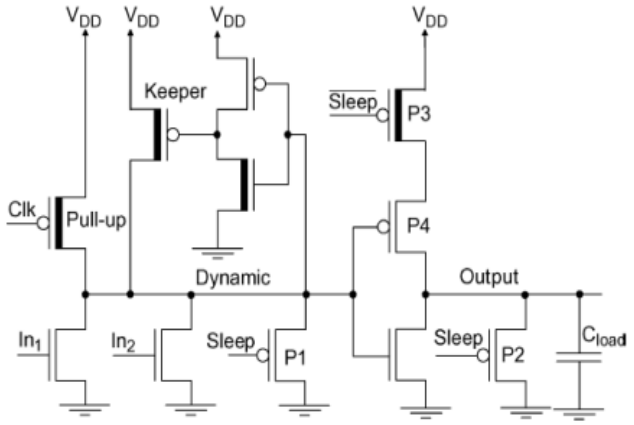

Fig.3.4. PMOS-Only Sleep Switch Dual-Threshold Voltage Domino Logic

3.5 Lector with Footed-Diode Inverter: a Technique for Leakage Reduction in Domino Circuits:

In this technique a modification in standard footerless domino logic is proposed. A lector is connected in between pull-up network and pull-down network is added(as shown in fig.5). Lector is a combination of a nmos and one pmos in which gate of each LCT is connected with the source of other. In standard footerless domino logic, the feedback keeper transistor is parallel with the precharge transistor, whose gate is biased with the output voltage to maintain the dynamic voltage against coupling noise, charge sharing problems, and sub-threshold leakage current. [5]

The proposed circuit technique effectively enhances the reduction of sub-threshold and gate oxide leakage simultaneously. The concept behind the approach is the reduction of leakage power using the effective stacking of transistors between the path from supply voltage to ground. which a state where only one transistor is OFF between the supply voltage and ground is more leaky than a state where more than one transistor is OFF in the path from supply voltage to ground.

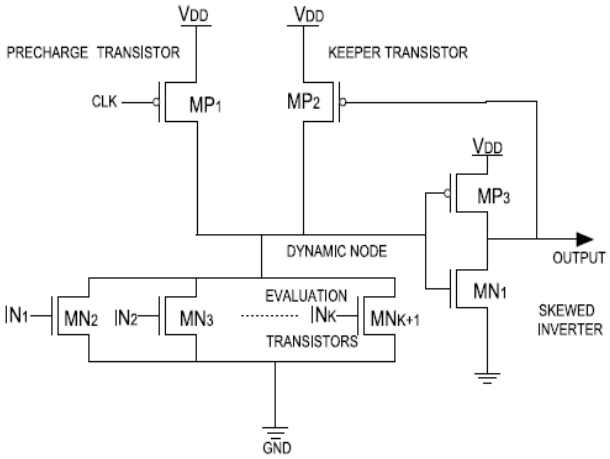

Fig.3.5.1: Standard Footerless Domino logic Circuit

Leakage control transistors (LCTs), are introduced between the precharge and the evaluation network and the gates of these transistors are controlled by each other's source. The drain nodes of MP4 and MN2 are connected to form the input of the inverter. In this configuration, transistor MP4 and MN2 switching will depend on the voltage potential at node N2 and N1, respectively. So, for any combination of inputs in the pull-down network, one of the LCTs will operate near its cut-off region and increase the resistance between V_{dd} and the ground rails, leading to a reduction of leakage current.

Both of the circuit are providing the voltage characteristics of a simple OR gate but with some leakage. Voltage waveform of two circuits is given below. But the leakage

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characteristics for both circuits ie: Conventional domino logic circuit and Lector based Domino Logic is different. Lector based Footed Diode Domino Logic Circuit is less leaky as compared to the Standard Footerless Domino logic circuits. As given in fig.3.5.3 and 3.5.4

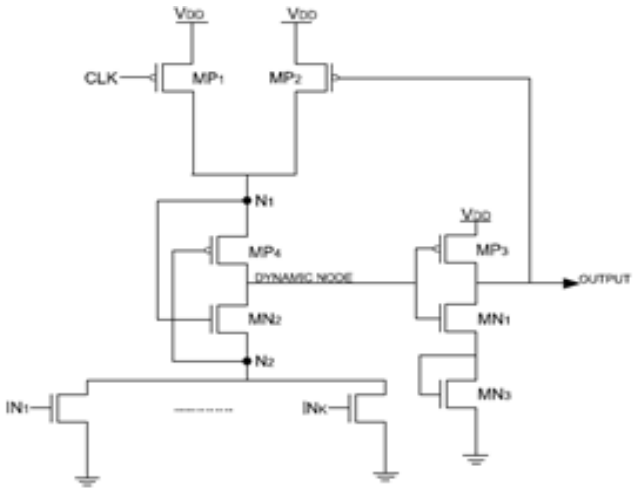

Fig.3.5.2: Lector based Footed Diode Domino Logic Based OR Gate

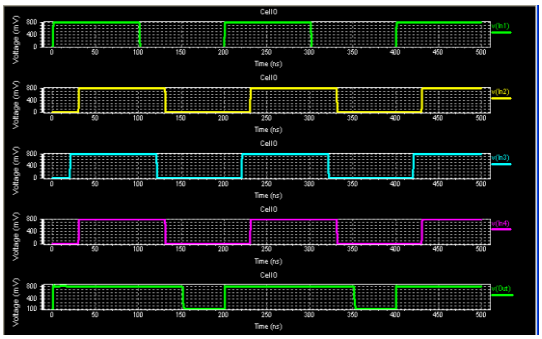

Fig.3.5.3: Output Voltage wave form fo4 4-bitOR gate

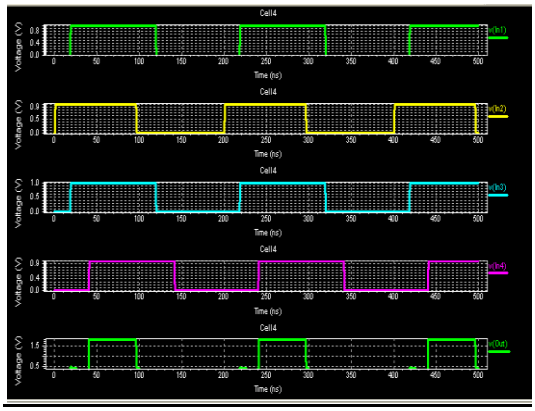

Fig.3.5.4: Output Voltage wave form for 4-bit AND gate

4. POWER DELAY COMPARISON FOR 2-BIT AND 4-BIT AND and OR GATES:

In the tables given below power delay and power delay product results for 2-bit and 4-bit AND and OR gates have been compared and from there analysis it is clear that the leakage of lector based circuit is less than that of conventional domino logic based circuits. But the delay of Lector based circuit is more than that of conventional domino logic based circuits.

TABLE 1: Avg Power and Delay comparison for 2-bit AND and OR Gates

	Power consumption	**Delay**	**Power Delay Product**
Std. OR2 Gate	1.02*10^-6	1.15*10^-7	1.181*10^-13
Lector Based OR2 Gate	4.52*10^-7	1.16*10^-7	5.243*10^-14
Results after Simulation	44.14% reduction	0.512% increase	40.369% reduction
Std. AND2 Gate	9.4*10^-5	6.61*10^-8	62.13*10^-13
Lector Based AND2 Gate	2.31*10^-7	6.63*10^-8	15.315*10^-15
Results after Simulation	19.245% reduction	.0302% increase	17.6% reduction

TABLE 2: Avg Power and Delay comparison for 4-bit AND and OR Gates

	Power consumption	Delay	Power Delay Product
Std. OR4 Gate	4.01*10^-8	1.65*10^-8	6.6165*10^-16
Lector Based OR4 Gate	1.53*10^-8	1.72*10^-8	2.6316*10^-16
Results after Simulation	38.15% reduction	4.24% increase	37.76% reduction
Std. AND4 Gate	1.98*10^-7	2.014*10^-7	3.98772* 10^-14
Lector Based AND4 Gate	1.028*10^-7	2.02*10^-7	2.07656*10^-14
Results after Simulation	51.91%	0.29% increase	50.0738%

5. COMPARISON OF ALL TECHNIQUES :

In the table given below comparison of leakage reduction techniques for Domino logic based circuits has been shown. Parameters of comparison are supply voltage, technology at which the technique is implemented, speed which is inversely proportional to the delay, leakage and area.

TABLE 3: Comparison of all techniques

Technique	Year of publication	Analysis of result				
		Supply voltage Vdd	Technology used	Speed	Leakage	Area
High-speed domino logic	1995	1V	0.5um	15-25% increase	Reduced	increase
Leakage control with efficient use of transistor stacks	2000	1.8V	0.5um	5-64% reduction	35-80% reduction	----
Sleep switch dual threshold voltage domino logic	2004	1.2V	0.18 um	14.6% reduction	20% reduction	-----
Pmos-only sleep switch dual-threshold voltage domino logic	2007	0.8V	65nm	decreases	77% reduction	increase
Lector with footed-diode inverter	2013	0.8V	45nm	decreases	79.4% reduction	14% increase

6. CONCLUSION

All of the techniques explained above are suitable for leakage reduction but they show trade-off with delay. Therefore there is no considerable reduction in power delay product. But if we introduce a high Vt NMOS with a separate sleep signal at the dynamic node of lector Footed Diode Based Domino Logic and one pmos-switch at the output of the circuit , we can get significant reduction in leakage but there will be no effect on delay, thus power delay product will also decrease. But the area of the circuit will increase, we can further work on area as well as delay.

REFERENCES:

[1] M.W. Allam, M.H. Anis, M.I. Elmasry, "High-speed dynamic logic styles for scaled-down CMOS and MTCMOS technologies", *in Proc. of the IEEE/ACM International Symposium on Low Power Electronics and Design, pp. 145–160 (2000).*

[2] M.C. Johnson, D. Somasekhar, L.Y. Chiou, K. Roy, Leakage control with efficient use of transistorstacks in single threshold CMOS. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 10, 1–5 (2002).*

[3] V. Kursun, E.G. Friedman, Sleep switch dual threshold voltage domino logic with reduced standby leakage current. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* ***12****(5), 485–496 (2004).*

[4] Z. Liu, V. Kursun, PMOS-only sleep dual-threshold voltage domino logic in sub-65-nm CMOS technology. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* ***15****(12), 1311–1319 (2007)*

[5] Tarun K. Gupta, Kavita Khare, Lector with Footed-Diode Inverter: A Technique for Leakage Reduction in Domino Circuits. *Circuits Syst Signal Process,Springer Science & Business Media New York 2707-2722 (2013).*