Low Power Design for D-Flip Flop

Aditi Mehta
Student, Department of Information Technology
Dronacharya College of Engineering,Gurgaon
aditi.16512@ggnindia.dronacharya.info

Riya Jain
Student, Department of Information Technology
Dronacharya College of Engineering,Gurgaon
riya.16548@ggnindia.dronacharya.info

Vaishali Yadav
Student, Department of Information Technology
Dronacharya College of Engineering,Gurgaon
vaishali.16558@ggnindia.dronacharya.info

Mrs. Ashu Soni
Associate Professor, Department of ECE
Dronacharya College of Engineering,Gurgaon
soniashu.14@gmail.com

*Abstract :*This paper enumerates the low power, high speed D-flip flop based on comparison between the various techniques i.e. Double Edge Triggering Flip Flop, Low Swing Double Edge Flip Flop, Multi Threshold CMOS and Conditional Data Mapping Flip Flop. In this paper, various designs are presented by connecting limited number of transistors and as the transistors used have small area and low power consumption, they can be used in buffers, registers, microprocessors, etc. The comparison is based on number of factors like leakage current, short circuit current, data activity, etc.

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Introduction :

A flip flop or latch is a circuit that has two stable states and can be used to store state information. They are fundamental building blocks of electronics system used in computers, communications and many other systems. They are used for storage of states. When used for infinite storage machines the output and the next state depends not only on current inputs, but also on current state, it can be used for counting pulses, and for synchronizing variably-timed input signals to some reference timing signal.

A flip flop generally consists of two inputs, a clock generator or a clocking signal and two outputs. One being the normal value of the output and the other is complement value of bit stored in it.

The output of flip flop is either logic 0 or logic 1.

D-flip flop: The D-flip flop tracks the input, making transitions with match those of the input D. The D stands for "data". This flip flop stores the value that is on the data line. It can be thought of as a basic memory cell.

D flip-flops are by far the most common type of flip-flops and some devices are made entirely from D flip-flops. They are also commonly used for shift-registers and input synchronization.

Power consumption plays an important role in any integrated circuit. In any integrated circuit, clock distribution network and flip -flop consumes large amount of power as they make maximum number of internal transitions.

Here various techniques for implementing flip-flops with low power clocking system are analyzed. Among those techniques, Conditional Data Mapping Flip Flops (CDMFF), Conditional Discharge Flip Flops (CDFF) and Conventional Double Edge Triggered Flip Flops (DEFF) are studied. Multi-Threshold voltage Complementary Metal-Oxide Semiconductor (MTCMOS) technique reduces the power consumption by approximately 20% to 70%.

Power consumption in a semiconductor depends upon a number of factors like frequency f, supply voltage v, capacitance c, leakage, short circuit current and data activity α.

The expression can be written as,

$$P = P_{dynamic} + P_{short\ circuit} + P_{leakage}$$

Here, $P_{dynamic}$ is also known as the switching power and is given by

$$P_{dynamic} = \alpha CV^2 f$$

$P_{short\ circuit}$ is the short circuit power which is given by

$$P_{short\ circuit} = I_{short\ circuit} V_{dd}$$

It is the maximum power that the network can provide to an installation during a fault.

$P_{leakage}$ is the leakage power. When the supply voltage decreases, the threshold voltage also decreases in order to maintain performance of the device. Leakage power is given by

$$P_{leakage} = I_{leakage} Vdd$$

Based on the above factors, various methods and designs for flip flops have been introduced so as to minimize the power consumption. Some of them are listed below:

1. **Double Edge Triggering Flip Flop**: Power depends on the frequency of the device. By reducing the frequency to half, power consumption simultaneously reduced to half. For this purpose, we use double edge triggering flip flop. The state equations for positive and negative-sensitive latch in a double edge triggering flip flop can be expressed as

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$$Q' = D.CLK + Q. CLK' \qquad - (1)$$

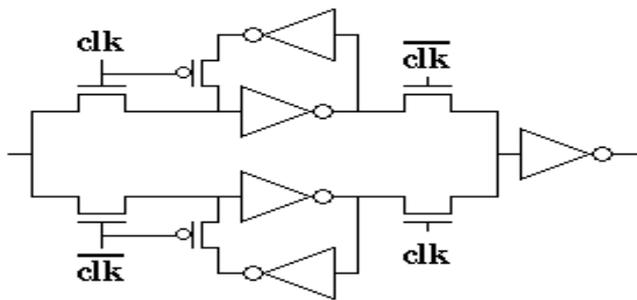$$Q' = D.CLK' + Q. CLK \qquad - (2)$$

Fig 1 : Double Edge Triggering Flip-flop

Equation (1) describes a latch which passes the input data when CLK= 1 and stores it when CLK = 0. Inversely, Equation (2) describes a latch which passes the input data

when CLK = 0 and stores it when CLK = 1. Double Edge Triggering method reduces the power consumption by reducing the frequency f in above equations.

2. As we know that power is a quadratic function of voltage. So by using a low swing voltage on the clock distribution, power can also be significantly reduced. This can be done by using a **Low Swing Double Edge Flip Flop (LSDEFF).** Low swing double edge flip flop uses a double edge operation as well as a low swing clock. To prevent performance degradation of the LSDFF due to low-swing clock, low Vt transistors are used for the clocked transistors without significant leakage current problems. Low swing method minimizes the power consumption by reducing the voltage.
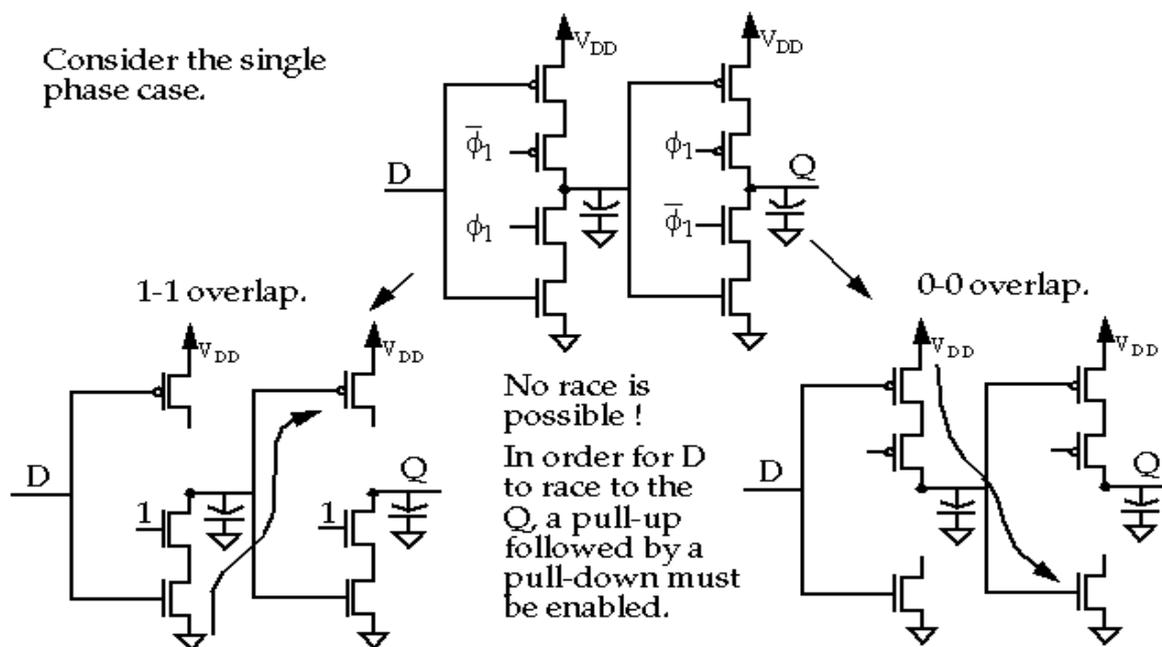

Fig 2 : Single phase case

3. **Multi-Threshold CMOS** technique reduces the leakage power. The high threshold mode in MTCMOS technique controls the leakage power and low threshold mode increases the speed performance. To reduce leakage power in MTCMOS circuits, sleep and sleep bar transistors are operated with high threshold voltages. When sleep input is OFF and sleep bar input is ON, there is no current flowing in the low threshold voltage circuit. When sleep is ON and sleep bar is OFF then the circuit works in normal mode.
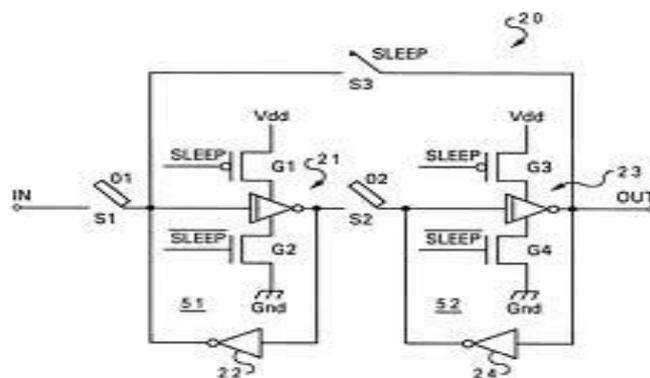

Fig 3: Multi-Threshold CMOS Technique

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4. Reducing capacity of Clock Load: A large part of power is consumed by the clock drivers. So by minimizing the number of clocked transistors, capacity of clock load can be reduced. E.g.: **Conditional Discharge Flip flop (CDFF)** uses 15 clocked transistors and conditional capture flip flop (CCFF) uses 14 clocked transistors. But **Conditional Data Mapping Flip Flop (CDMFF)** uses only 7 transistors which results in less power consumption in CDMFF than CDFF and CCFF.
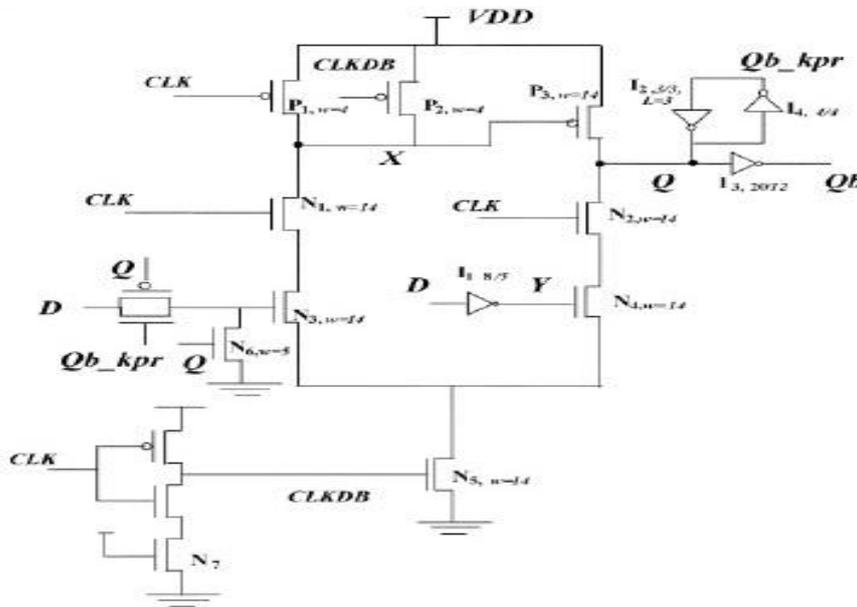

Fig 4 : Reducing capacity of clock load

Conclusion:

In this paper, analyzed various methods for reducing power consumption. After analysis, it can be concluded that MTCMOS technique is comparatively more effective than rest of the techniques discussed. This is so because MTCMOS D flip flop uses only 7 clocked transistors which reduced the consumption of power by about 50%. Hence from results, power consumption decreases and propagation delay increases. We presented a broad idea of different proposed techniques for low power D flip flops in the paper and based on the given facts we conclude that circuits using MTCMOS technique are suitable for higher performances.

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