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1.6V Wide Linear Range Subthreshold OTA Using 130nm CMOS Technology

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Abstract –This paper presents a low-power, low-voltage CMOS operational transconductance amplifier (OTA) operating in weak inversion region with a wide input range of -0.8 to 0.8V. It allows the use of very small current for low-power and low-voltage features. A pseudo resistive divider is used in the input section to ensure operation in subthreshold region. The linear operating region is selected to fix the input range for transistors operating in weak inversion region as 0.345 to 0.375V. Aspect ratios of pseudo resistive dividers are chosen such that the output voltage range is linear for the 1.6V wide input voltage. Pseudo resistive dividers are used to translate the input voltage range of -0.8 to 0.8V into 0.345 to 0.375V. The performances are examined through LTSPICE simulations using 130nm CMOS Technology. The power consumption is about 240nW at 1.2V supply with a 200nA bias current.

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I. INTRODUCTION

Operational transconductance amplifier (OTA) is the one of the most important analog building block with very large number of applications. There has been much effort to reduce the supply voltage of due to the demand for portable and battery-powered equipment. Subthreshold operation of OTA will lead to lower power consumption resulting from the low value of quiescent drain current. Since a low-voltage operating circuit becomes necessary, the operation of MOS devices in weak-inversion region is ideally suited for this purpose. Weak inversion operation of CMOS OTA is very popular in biomedical applications due to the high transconductance per drain current ratio, which yields more power efficiency [5].

Recently, a large number of the OTAs using this technique have been proposed. But there is a serious drawback, limited linear range. For a total harmonic distortion (THD) of -40dB, an OTA is designed [4] with traditional gate-driven differential pair operating in weak inversion region. It attains a linear input range of ten millivolts, which will not be sufficient for most biomedical applications. When the input voltage is applied directly to the transistor operating in weak inversion region then it will limit the linearity of the DC transfer characteristics into a range of -100 to 100mV[1].

In the context of low-voltage and low-power design, one of the suitable structures is the bulk-driven differential pair[3], which allows an input signal swing of -600 to 600mV which is significantly higher than the range achievable using a standard differential pair. An OTA has been proposed [6] with bulk-differential pairs and gate controlled asymmetry for linear range enhancement. The asymmetric gate voltage on the differential pairs causes a g_m curve shifting, which allows a much wider input range of 400mV.

To further improve the input range in this paper an ultra-low power, low voltage OTA with 1.6V wide input range is presented. 1.6V wide linear range is achieved using pseudo resistive dividers in the input section. First the characteristics of MOSFET under weak inversion region are analyzed. The linear operating region is selected to fix the input range for transistors operating in weak inversion region as 0.345 to 0.375V. When we apply an input voltage in the range -0.8 to 0.8V directly to the transistor it cannot operate in weak inversion mode. Aspect ratios of pseudo resistive dividers are chosen such that the output voltage range is linear and below V_{on} (0.408). Pseudo resistive dividers are used to translate the input voltage range of -0.8 to 0.8V into 0.345 to 0.375V. The output of pseudo resistive divider is fed to the input of OTA. The bias current is fixed as 200nA. Performance of the proposed OTA is analyzed using 130nm CMOS technology.

This paper is organized as follows: in Sect. 2, the configuration of proposed OTA is presented. Detailed simulation results that verify the proper operation of the simulated OTA are provided in Sect. 3. Finally, conclusions are provided in Sect. 4.

II. CIRCUIT CONFIGURATION

A. *Basic Concept of OTA*

An OTA is a voltage controlled current source, more specifically the term operational comes from the fact that it takes the difference of two voltages as the input for the current conversion. An ideal OTA has infinite input and output impedances. The proportionality factor between output current and input differential voltage is called transconductance. The output current of an OTA is given by

$$I_{o_+} = g_{m^+}(V_1 - V_2) \quad (1)$$

$$I_{o_-} = g_{m^-}(V_2 - V_1) \quad (2)$$

Where g_{m+} and g_{m-} are the positive and the negative transconductances of the operational transconductance amplifier.

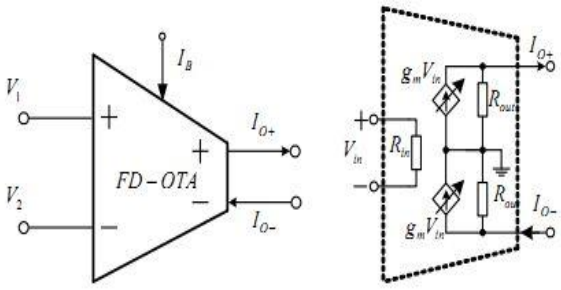

Fig 1: OTA (a) Symbol (b) Equivalent circuit

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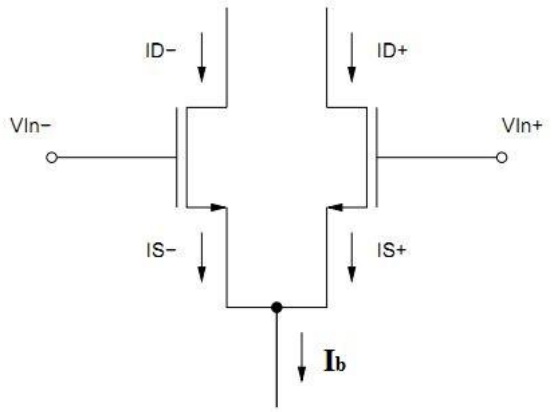

Fig 2: FET Differential Pair

The most simple OTA consists of a differential pair i.e. two matched transistors with sources joined together and biased by a constant current source for converting the input voltage difference into two currents I_{0+} and I_{o-}. These two currents are then mirrored to the output so that their difference becomes the output of the OTA, while the rest of the OTA is made up of bias circuitry. The tail current, which is a necessary part of the biasing, can be used to control the transconductance.

B. Operation of MOS Device in Weak-Inversion Region

The point at which transistor enters weak inversion region can be approximated as

$$V_{gs} < V_T + n\frac{KT}{q} \qquad (3)$$

$$V_{ds} > \frac{3kT}{q} \qquad (4)$$

I_d for weak inversion region is given as

$$I_D = I_{D0}\frac{W}{L}e^{\frac{V_{gs}-V_{th}}{nU_T}}(1-e^{\frac{V_{ds}}{nU_T}}) \qquad (5)$$

U_T is the thermal voltage which is 25.9mV, V_{th} is the threshold voltage, n is the subthreshold slope factor and it s value is greater than 1 and less than 3 and I_{D0} is process dependent parameter(dependes on V_{sb} and V_{th}). A simple model for weak inversion is given as

$$I_D = \frac{W}{L}I_{D0}exp\frac{V_{GS}}{n(KT/q)} \qquad (6)$$

From the above equation transconductance can be derived as

$$g_m = \frac{I_D}{nKT/q} \qquad (7)$$

There is a linaer relationship between transconductance and current instead of a square law relationship as in the case of strong inversion operation. Here transconductance is independent of device geometry instead of having a linear relationship.

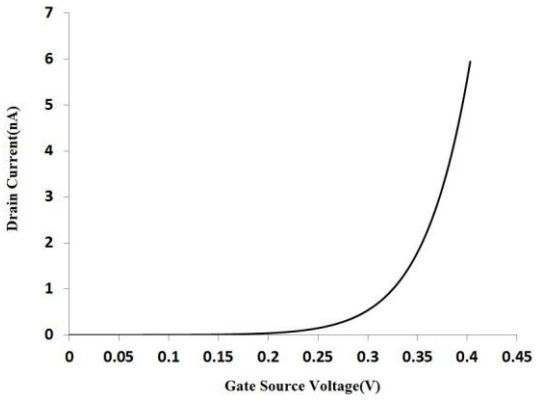

Fig 3: I_d - V_{gs} characteristics of NMOS for weak inversion operation

C. Bulk driven technique

The concept of a bulk-driven MOS transistor was first proposed by Guzinski et al.[1987] as active components in an OTA differential input stage.

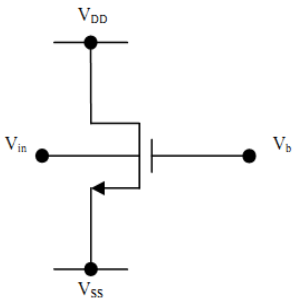

Fig 4: Bulk-driven MOSFET symbol

Generally the substrate potential in a MOSFET is equal to the source potential, i.e., V_{sb} (source to substrate voltage) = 0. But in some cases, the source potential of an NMOS can be larger than the substrate potential. This results in a positive source-to-substrate voltage, i.e., $V_{sb} > 0$. In such a case, threshold voltage V_T includes the substrate bias terms and can be defined as

$$V_t = V_{to} + \gamma(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}) \qquad (8)$$

Where, V_{TO} is the threshold voltage when V_{sb} =0, γ is the bulk threshold parameter and ϕ_F is the strong inversion surface potential. Substituting this value of V_T in the conventional drain current equation of the n-channel MOSFET in saturation region. The channel conductance of the bulk-to-source junctions g_{mbs} is defined as:

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$$g_{mbs} = \frac{\partial I_D}{\partial V_{DS}} \qquad (9)$$

Where, g_m is the channel transconductance of the gate-to-source junctions. The gate-source potential is taken to a dc voltage that is sufficient to turn-on the MOSFET. The drain is connected normally and the signal is applied between the bulk and the source.

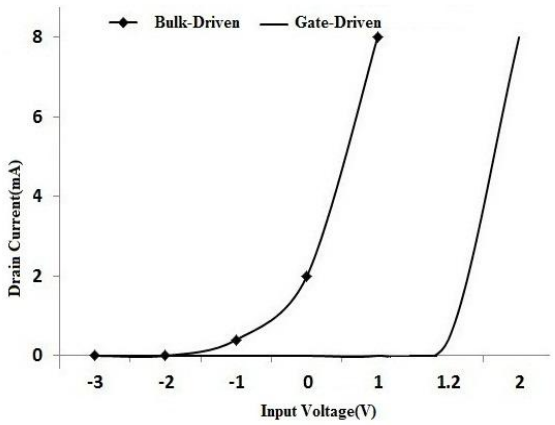

Fig 5: Characteristics plotted for Gate driven and Bulk-driven n channel MOSFET

Bulk-driven differential pairs in OTAs significantly improve the Input Common-Mode Range (ICMR) since a bulk-driven device allows an extension in its input range on the negative side, as illustrated in Fig 5. With proper design of the bulk-driven differential pair, the devices can remain saturated over the entire rail-to-rail ICMR. The transconductance of the bulk-driven MOS transistor g_{mb} is less than the transconductance of the conventional gate-driven MOS transistor g_m(g_m and g_{mb} are the slopes of its drain current versus its input voltage at the bias point). Therefore utilizing a bulk-driven differential pair for OTA design introduces a challenge in achieving high open-loop gain. The $\frac{g_{mb}}{g_m}$ ratio, η is typically 0.2 to 0.4.

D. Pseudo Resistive Divider[2]

MOSFET can be used as a resistor in it's active and saturation operation modes. As there is a current flow inside the device in it's saturation and active mode of operation, the device have some internal resistive effect as voltage is not zero in either of the operating modes. Pseudo ohm law can be formulated for a MOSFET as

$$I_d = \frac{V_d - V_g}{R} \qquad (10)$$

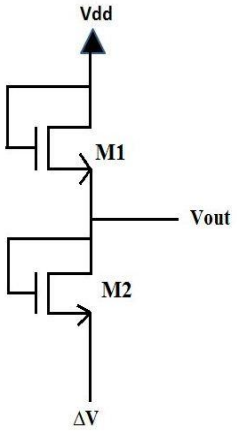

Fig 6 : Basic Pseudo Resistive Divider

A diode connected Mosfet can be used as a resistor in the saturation region. If V_{dd} and ΔV are applied across the source of M_1 and Drain of M_2 then output voltage V_{out} across the pseudo voltage divider circuit is given by

$$V_{out} = \frac{V_{dd} + \delta V(1 + \frac{R_1^*}{R_2^*})}{1 + \frac{R_1^*}{R_2^*}} \qquad (11)$$

where $R^* = \frac{1}{g_m}$. If and M_1 and M_2 are having same W/L ratios then the transconductances offered by them are the same. So they can act as a resistive divider element. The output voltage V_{out} will be

$$V_{out} = \frac{V_{dd} + \delta V}{2} \qquad (12)$$

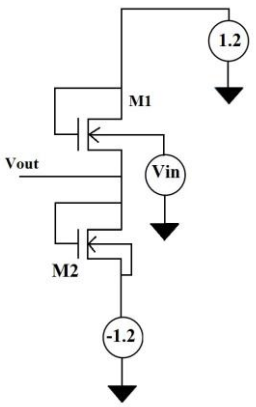

Fig 7: Pseudo Resistive Divider used for design

Pseudo resistive divider used in this work to map the wide input voltage range is shown in Fig 7. V_{in} is applied to the bulk of M_1. Upto an input voltage range of -0.8 to0.8V the output voltage is linear. The aspect ratios of M_1 and M_2 are selected to get a linear output voltage variation.

III. PROPOSED OTA

M_1 and M_2 are operating in weak inversion region. A pseudo resistive divider is used in the input section to map the wide input voltage range. A simple differential pair amplifier is employed to achieve simpler circuit description of the proposed OTA as shown in Fig. 8. M1 and M2 function as a differential amplifier to convert an input voltage to an output current and are biased to work in weak-inversion region. I_{D3} is the bias current.

When input voltage is applied, this makes I_1 and I_2 flowing through M_1 and M_2, respectively. M_1 and M_2 are operating in weak inversion region when $V_{in} < V_{on}$ (0.408). The pseudo resistive divider element will map the input voltage range -0.8 to 0.8 into the range 0.345 to 0.375 so that M_1 and M_2 are operating in weak inversion (subthreshold) region.

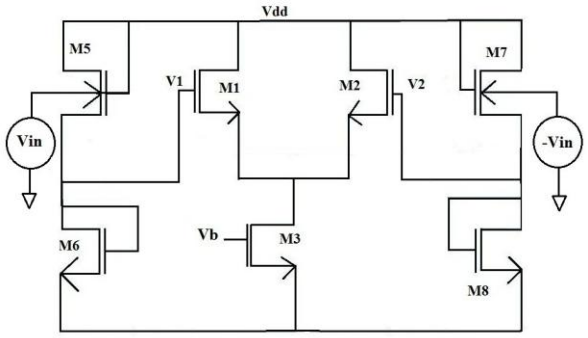

Fig 8: Proposed OTA with two pseudo resistive divider elements

Simulation Parameters	Values
V_{DD}/V_t	1.2V/230mV
Power consumption	240nW
Input bias range	200nA
$(W/L)_1, (W/L)_2$	10
$(W/L)_3$	40
$(W/L)_4$	10
$(W/L)_5, (W/L)_7$	30
$(W/L)_6, (W/L)_8$	100

Table 1: Proposed OTA parameters

IV. SIMULATION RESULTS

The proposed OTA circuit was simulated in LTSPICE using standard 130 nm CMOS technology. The circuit is operated with V_{dd} of 1.2 V. The dimensions of the various transistors and biasing conditions are listed in Table 1. Linear output voltage variation of pseudo resistive divider for a 1.6V wide input range is plotted in Fig. 9. From the result output is linear in the range 0.345 to 0.375V.

The DC transconductance of the circuit was analyzed by sweeping the differential input voltage from 800 to -800 mV and the results are plotted in Fig. 9. The proposed circuit has a better linear DC transfer characteristics. The variation of output currents over a wide range of input differential voltages are examined and plotted in Fig. 10. From the results it is evident that the circuit exhibits better linearity of output current over a wide range of input voltage.

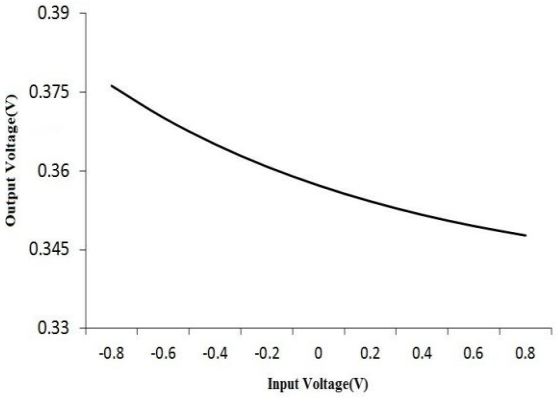

Fig 9: Output voltage of pseudo resistive divider

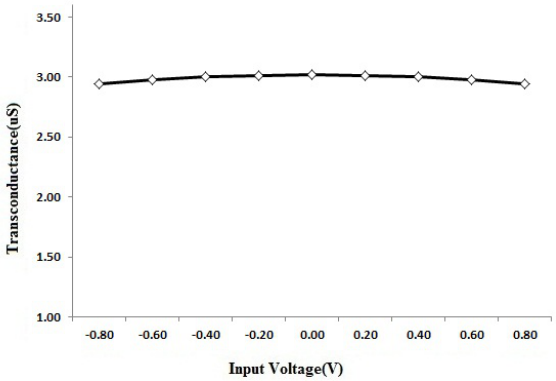

Fig 10: DC transfer characteristics

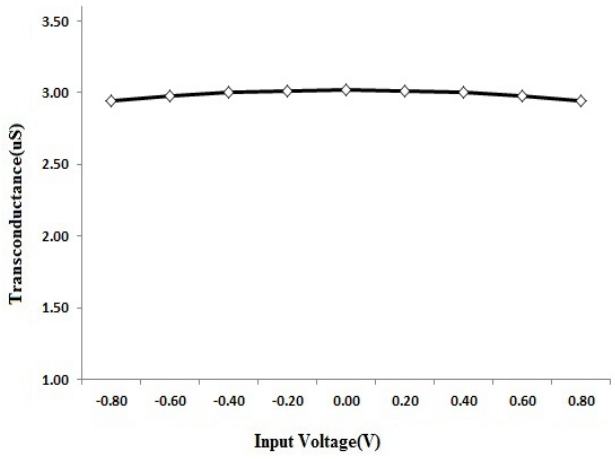

Fig 11: Transconductance variation (DC) with differential input voltage

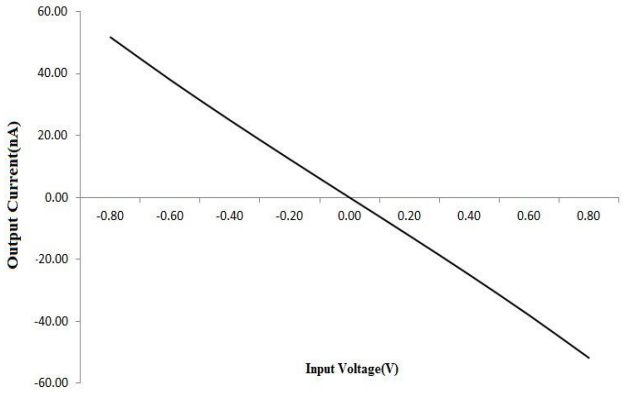

Fig 12: Output Current variation (DC) with differential input voltage

V. CONCLUSION

A new method is suggested to improve the input voltage range for an OTA operating in the weak inversion region. The design of this OTA with pseudo resistive dividers in the input section is done. Simulations are done using 130nm CMOS technology in LTSPICE. Power consumption is only 240nW with a 1.2V supply and it has a wide input voltage range of -0.8 to 0.8V.

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