VLSI Implementation of Encoder and Decoder for Advanced Communication Systems

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***Abstract*—**Forward Error Correction (FEC) schemes are an essential component of wireless communication systems.Present wireless standards such as Third generation (3G) systems, GSM, 802.11A, 802.16 utilize some configuration of convolutional coding. Convolutional encoding with Viterbi decoding is a powerful method for forward error correction. The Viterbi algorithm is the most extensively employed decoding algorithm for convolutional codes which comprises of minimum path and value calculation and retracing the path. The efficiency of error detection and correction increases with constraint length. In this paper the convolutional encoder and viterbi decoder are implemented on FPGA for constraint length of 9 and bit rate ½.

Keywords *– forward error correction, convolutional encoder, viterbi decoder, constraint length and FPGA*

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I. INTRODUCTION

Forward error correction (FEC) codes have long been a powerful tool in the advancement of information storage and transmission. By introducing meaningful redundancy into a stream of information, systems gain the ability not only to detect data errors, but also to correct them. Convolution coding is a popular error-correcting coding method used in digital communications. It is used in communications such as satellite and space communication to improve communication efficiency.

To detect and correct errors occurred while transmitting digital data through a noisy channel, the original data is convolutionally encoded by using convolutional encoder. The encoder adds some redundancy to the information and then transmits through a noisy channel. The transmitted data is received at the receiver and is given to viterbi decoder. The viterbi decoder evaluates the corrupted data and corrects the errors in the bit streams occurred during transmission. The block diagram of a system with convolutional encoder and viterbi decoder is as shown in fig. 1.

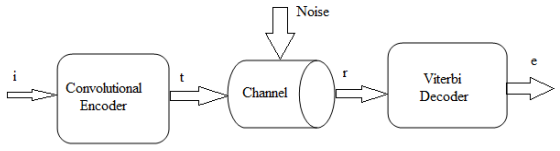

Fig.1. Basic communication system with encoder and decoder

The viterbi decoder uses viterbi algorithm for error correction which is a popular method used to decode convolutionally coded messages. The algorithm tracks down the most likely state sequences the encoder went through in encoding the message and uses this information to determine the original message. Instead of estimating a message based on each individual sample in the signal, this system works on sequential data and produces error free data.

The convolution codes are used mostly for the channel encoding of data to achieve low-error-rate in latest wireless communication standards like 3GPP, GSM and WLAN. All communication channels are subject to the additive whiteGaussian noise (AWGN) around the environment. Convolutional Encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN.

The efficiency of error detection and correction increases with constraint length. In this paper, the convolutional encoder and viterbi decoder are implemented on FPGA for a constraint length of 9 and bit rate ½.

The remainder of this paper is organized as follows. Section II gives the information about forward error correction techniques. Section III describes the convolutional encoder and its working process. Section IV gives information about viterbi decoder.

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II. FORWORD ERROR CORRECTION

Forward Error Correction is a process of error control for data transmission by adding some redundant symbols to the transmitted information to facilitate error detection and error correction at receiver end. Forward Error Correction (FEC) in digital communication system improves the error detection as well as error correction capability of the system at the cost of increased system complexity. Using FEC the need for retransmission of data can be avoided. Hence, it is applied in situations where applied in situations where retransmissions are relatively costly or impossible.

FEC codes can be classified into two categories namely block codes and convolution codes. Block codes work on fixed size blocks of bits where as convolution codes work on sequential and as well as blocks of data. In this, the encoding operation may be viewed as discrete time convolution of input sequence with the impulse response of the encoder. Error detection and correction or error control is a technique that enables reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to the receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data.

III. CONVOLUTIONAL ENCODER

Convolution codes are better codes of error controlling performance. The convolutional encoder is comprised of a shift register, adders and multiplexer with predefined connections between them. The basic convolutional encoder is as shown in fig. 2.

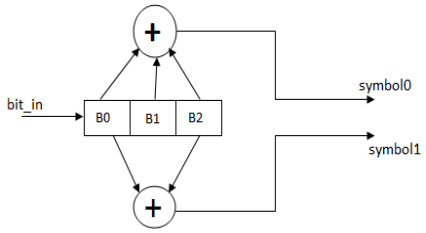

Fig.2. Basic Convolutional Encoder

The message stream to be encoded is continuously shifted into shift register bit by bit and then a set of output bits are produced based on logical operations carried out on the contents of the register memory. This process is often referred to as convolution encoding. The encoder introduces redundancy into the output code, producing more output bits than input bits shifted into its memory. As a bit is shifted along the register it becomes part of other output symbols sent. Thus the present output bit that is observed by the viterbi algorithm (VA) has information about previous input bits so that if one of these symbols becomes corrupted then the VA can still decode the original bits by using information from the previous and subsequent observation symbols.

One important parameter that decides the performance of the error detection and correction of this system is constraint length. Constraint length is defined as the number of shifts over which a single message bit can influence the encoder output. In other words it is equal to the size of shift register used in the construction of encoder. The error detection and correction capability increases with the increase in constraint length.

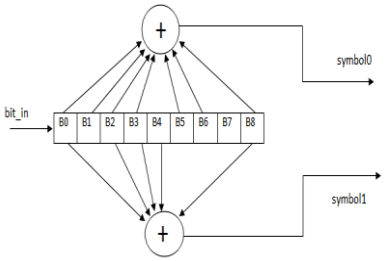

Fig.3. Proposed convolutional encoder

In this paper, the convolutional encoder and viterbi decoder are developed for a constraint length 9 and at a bit rate ½. The considered convolutional encoder is shown in fig. 3. This convolutional encoder has a shift register of size 9 and 2 XOR gates with predefined connections between shift register bits and XOR gates.

Transition table, state diagram and trellis diagram:

The k-1 LSB bits of the k bit shift register are called state. The relationship between inputs, outputs and states for a basic convolutional encoder can be described using a transition table which is shown below.

input	Register contents			output	
	B0	B1	B2	S0	S1
0	0	0	0	0	0
1	1	0	0	1	1
0	0	0	1	1	1
1	1	0	1	0	0
0	0	1	0	1	0
1	1	1	0	0	1
0	0	1	1	0	1
1	1	1	1	1	0

Table1. Transition table

In the table, B1 and B2 represent the state. The input bit is shifted into the B0 position of the shift register.

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The output bits S0 and S1 are generated by performing the logical operations on the register contents.

The structural properties of the convolutional encoder can be portrayed by using state diagram. For the convolutional encoder shown in the fig. 2, the state diagram is as shown in fig. 4.

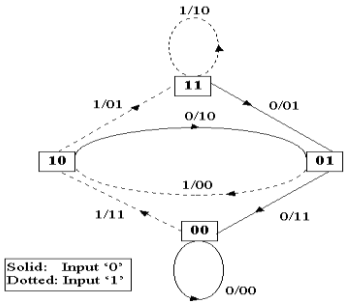

Fig.4. State Table

In the state diagram, square boxes are the states and the indicators of the states are written inside the boxes. Arrows are the state transitions according to input values. The state transition for input 0 is represented by thick line and for input 1 is represented by dashed arrow. Value after slash on the arrows corresponds to the output of the encoder.

Another way for representing the structural properties of convolutional encoder in graphical form is trellis diagram. The trellis diagram for basic convolutional encoder is shown in fig. 5.

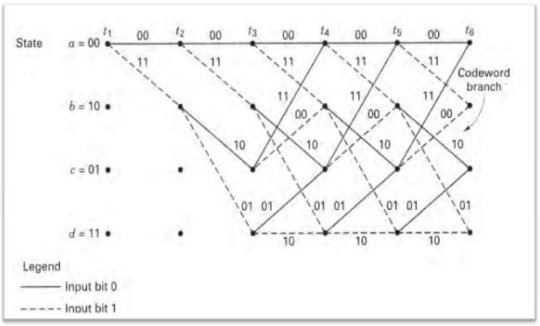

Fig. 5 Trellis Diagram

In the trellis diagram, the four states are referred as a, b, c and d. the state transition for input 0 is shown with thick line and for input 1 it is shown with dashed line. The outputs are written above the lines.

Design of state diagram and trellis diagram for a proposed architecture on paper is cumbersome because, for a convolutional encoder with constraint length 9, the is represented by 8 bits. So, the number of states is 256. It will be time consuming, clumsy and confusing to show them on paper. Hence, this paper is explained by considering basic convolutional encoder but final results are shown for an efficient system with constraint length 9.

IV. VITERBI DECODER

The basic units of viterbi decoder are branch metrics, Add compare select and Survivor management unit. Figure 1 shows the general structure of a Viterbi decoder.

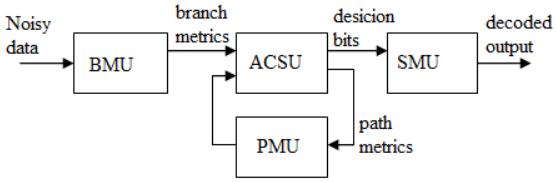

Fig.5. Block diagram of viterbi decoder

It consist of four blocks: the branch metric unit (BMU), which computes metrics, the path metric unit (PMU), which computes the path metric, the add–compare–select unit (ACSU), which selects the survivor paths for each trellis state, also finds the minimum path metric of the survivor paths and the survivor management unit (SMU), that is responsible for selecting the output based on the minimum path metric. The received data bits are given to the branch metric block which calculates the possible branch metrics at that particular state.

Any state from stage three in the trellis diagram can be reached from two possible previous states thus two error metrics are obtained. The Add compare select unit finds both the path metrics and compares, whichever is minimum that path metric is chosen as the new path metrics. The new path metrics are stored in path metric unit. Above two steps are repeated until the trellis ends and the entire path metric and next state metrics are obtained. Using these above metrics the survivor path traces the optimum path from last values of the next state matrix and then the data is decoded.

V. RESULTS

For verifying the error detecting and correcting capability of this system, a 32 bit data is serially given to the convolutional encoder. This data is encoded and is given to noise generating block which adds some errors to the data. This erroneous data is given to the viterbi decoder which extracts the originally transmitted data. Finally the inputs and outputs are compared.

The RTL Schematic of encoder block generated in Xilinx ISE is as shown below:

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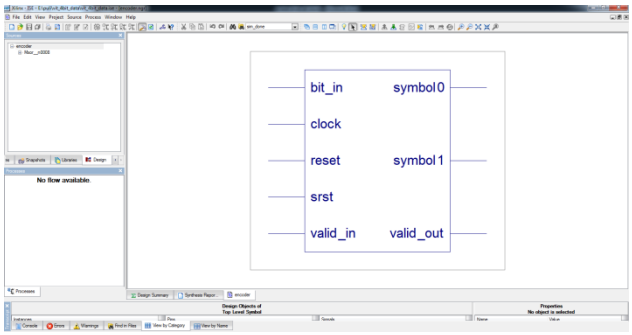


Fig.6. RTL Schematic of convolutional encoder

The internal structure of encoder block generated using Xilinx ISE is shown below:

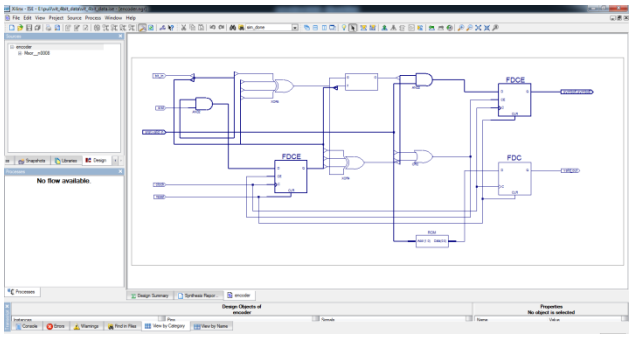


Fig.7. Internal structure of convolutional encoder

The RTL Schematic of decoder block generated in Xilinx ISE is as shown below:

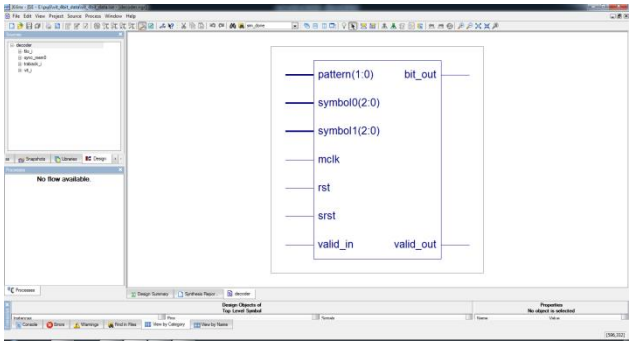


Fig.8. RTL Schematic of viterbi decoder

The internal structure of encoder block generated using Xilinx ISE is shown below:

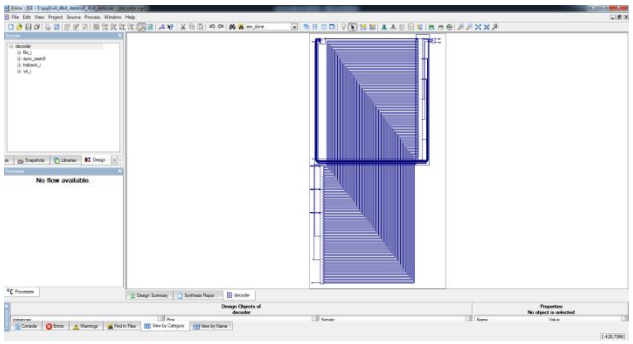
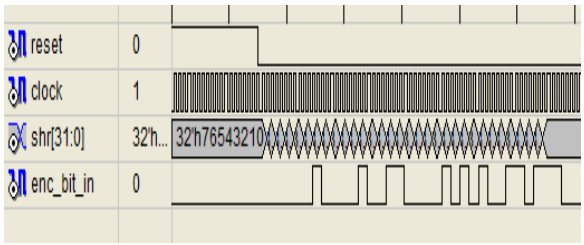


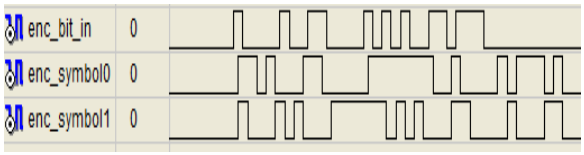
Fig.8. Internal structure of viterbi decoder

Applying 32- bit data to encoder:



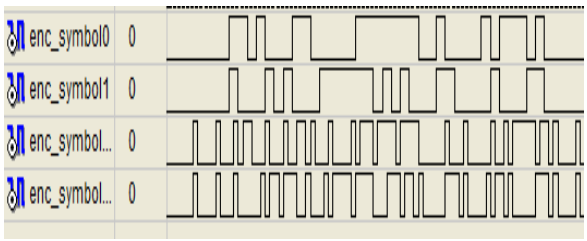
(A)

Encoder inputs and outputs:



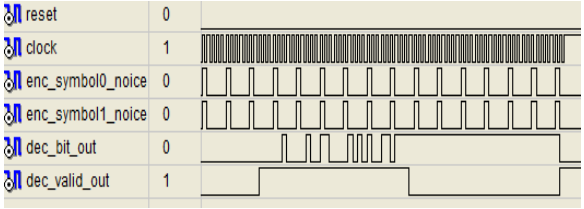
(B)

Noise generator inputs and outputs:



(C)

Viterbi decoder output:



(D)

Accumulating decoder output into a register:

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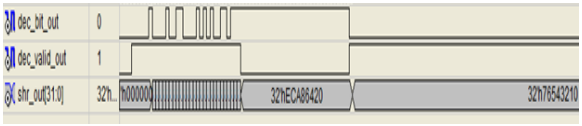
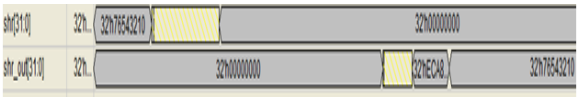


(E)

Comparison of final input and outputs:



(F)

Fig.9. Results of encoder and decoder

VI. CONCLUSION

Viterbi Algorithm allows safe data transmission via error correction and original message can be recovered accurately without any noise. Convolution encoder and Viterbi decoder for constraint length 9 and bit rate 1/2 is implemented using VHDL and simulated using XILINX ISE tools. Synthesis is done using Xilinx ISE Design Suit 14.3 tool. The working of the design is cross verified for many trials by introducing errors.

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