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Reversible Logic Circuit Based Twiddle Factor Generation

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Abstract-An efficient hardware implementation of FFT algorithm become essential one in signal analysis domain, more specifically the twiddle factor calculation in FFT computation plays important role in the speed and efficiency of the complete process. World of computation needs the fast and efficient tools to match the need of present scenario, even though there are many methods proposed the Reversible Logic design became the promising area for improvement of speed and reduces the power consumption to a larger extent. In this paper a reversible logic based implementation of twiddle factor generation is proposed.

Key words: *Fast Fourier Transform, Reversible Logic, Twiddle factor*

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1. Introduction

The world of Signal analysis the domain transfer of signal from time to frequency or frequency to time is unavoidable. Whatever may be the transform technique for domain transfer it needs the use of twiddle factorW_N^{kn}. FFT is one among them which uses the twiddle factor to a larger extend when it is implemented in butterfly structure. The required twiddle factor for FFT is generally stored in the memory and whenever it is needed for calculation it is taken form their and used in the FFT calculation process, this results an very large size memory bank to store all the twiddle factor most of the time the memory need for this purpose is more than it needed for core FFT processing element data memory. Therefore, an efficient, high speed, low power consuming and small area twiddle factor generator is essential. There are many techniques already proposed by different researchers based on generation of simple trigonometric function, DDFS, CORDIC [1], pipelined CORDIC architecture [2],[3] and polynomial based DDFS[5]-[11]. In this paper two techniques adopted to provide the most efficient twiddle factor generator, one is by means of using recursive sine function generator with compensation for error propagation second thing is by implementing the whole system using reversible logic gates which intern reduces the power consumption and increases the speed of calculation.

2. Twiddle Factor Generation

In the proposed technique the sine function generator is used to generate the real and imaginary part of twiddle factor, let's generate imaginary part generation using sine function

$$X(n) = [\ \sin(n\theta)\ ]u(n)$$

By taking Z-transform for the above expression, we get,

$$X(z) = \frac{sin\theta\ z^{-1}}{1 - 2\ (cos\theta)z^{-1} + \ z^{-2}}\ , |z| > 1$$

Its difference equation representation is,

$$X(z) - 2\ cos\theta\ X(z)z^{-1} - X(z)z^{-2} = sin\theta\ z^{-1}$$

Therefore,

$$sinn\theta = 2cos\theta\ \times \sin(n-1)\,\theta - \sin(n-2)\theta$$

$$cosn\theta = 2cos\theta\ \times \cos(n-1)\,\theta - \cos(n-2)\theta$$

This equation contain past output terms to generate present output which cause the propagation of error. The error introduced in the process is compensated by predefined error correction table to find the word length we analyze the upper bound and the maximum error of the computed $\overline{sinm\theta}$ is bounded by

$$max\left|2^{-1}[\sin(n-1)\theta \pm cos\theta \pm 2^{-1} \pm 2^{-(n+1)}]\right| < 2^{-(n-2)}$$

From this, it is concluded that an error correction word of three-bit long per output point is needed, hence in every iteration, the 3 LSB's of output is replaced with bits from correction table.

3. Reversible System

This section introduces the basics of reversible logic gates and various reversible logic gate proposed. Reversible logic has received significant attention in recent years. It has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology. It is not possible to construct quantum circuits without reversible logic gates. Synthesis of reversible logic circuits is significantly more complicated than traditional irreversible logic circuits

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because in a reversible logic circuit, we are not allowed to use fan-out and feedback [4].

The performance of the reversible circuit based on the following parameters

1. Garbage output: The number of unused outputs present in the reversible logic circuit.
2. Number of reversible logic gates: Total number of reversible logic gates used in the circuit.
3. Delay: Maximum number of unit delay gates in the path of propagation of inputs to outputs.
4. Constant inputs: The number of input which are maintained constant at 0 or 1 in order to get the required function.

Existing reversible logic gates are listed below

1. Feynman gate
2. Toffoli gate
3. Fredkin gate
4. Peres gate
5. HNG gate
6. URG gate

Reversible logic gates: An nxn reversible gate can be represented as[8]:

IV = (A, B ,C,....)
OV = (P, Q, R ...)

Where IV and OV are input and output vectors respectively.

4. Proposed Reversible Recursive Twiddle Factor Generation

The realization of reversible recursive twiddle factor generator is shown in the figure 1.1 and there are two inputs given to the unit one as it is the $\overline{cos\theta}$ and another one from the output acting as a feedback path ie, $\overline{cosn\theta}$ to an reversible multiplexer. The output of the multiplexer unit is given to the delay unit where the output of the multiplexer is delayed by one time step and it is feeded to reversible multiplier and another delay unit.

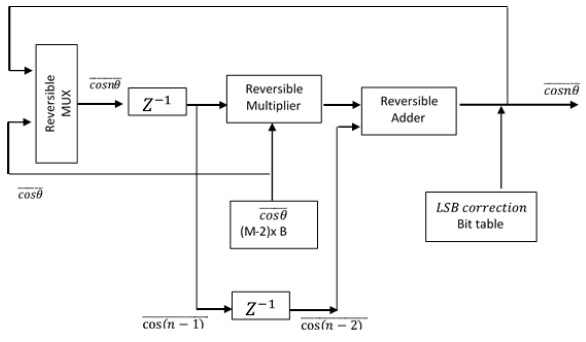

Fig 1: Realization of Reversible Recursive Twiddle Factor generator

In the multiplier block the delayed multiplexer outout and $\overline{cos\theta}$ functions are multiplied and the result sent to the reversible adder unit where it is added with the two time step delayed multiplexer output and finally taken as the output. But as discussed earlier the output contains the error that to be compensated so in the output of the reversible adder the 3 LSB bits are modified as per the LSB correction bit table and the error free output is taken at the final output.

5. Result & Discussion

The proposed method is simulated using VHDL software and the results are compared with the existing approaches. Fixed the word length as 8 bits and the experiment is conducted.

The total logical operation involved in the proposed reversible recursive twiddle factor generator circuit is calculated with the help of following logical assignments a = NOT logic, b = OR logic, c = AND logicfor example if T = 2a+3d then the circuit involves 2numbers of XOR logical operation and 3 numbers of OR logical operations. The performance of the design is based on the number of gate, number of garbage (unused terminals) and number of constants, in this proposed design the above said parameters are optimized to greater extent.

Table 1. PerformanceComparison of various methods of twiddle factor generation

	No. of Gates	Delay	No garbage's
RRTF (proposed)	2115	2.86	1305
CORDIC	9781	2.72	-
Polynomial	9125	4.12	-
Recursive	9879	2.89	-

6. Conclusion

This paper proposed and introduce a reversible logic circuit based generation of twiddle factor for FFT calculation. The proposed design achieve the lowest power consuming unit and also comparatively gives better speed. The reversible circuits are in the initial stage of development hence the availability of gates for implementation is less once the new reversible logic gates are developed it is possible to reduce the area and power consumed by the system further to larger extend. The proposed method is implemented and compared with other techniques with 8bit length if the Twiddle factor for FFT of length 16,64,256,512,1024,..is implemented with the proposed technique which shows better performance.

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