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Power Optimization of I/O Ports Using Clock Gating Technique

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***Abstract*—** This paper deals with the one of the application of clock gating techniques. As we all know that today power and switching speed optimization are the major areas on which vlsi designers are more concern about. Clock Gating Technique is one of the solutions to this major problem. So, here we are doing a kind of experiment on the applications of CGT e.g.UART and ADC. On the basis of this experiment we can have some clear views regarding efficiency of this technique. This paper provides the concept of reducing power consumption in IDLE state and enhances switching speed when the functional block is in running state. This modified instruction level clock gating reduces dynamic power by 19-25%.

Keywords- *CGT, ACG, DCG, Clock , UART, ADC etc*

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I. INTRODUCTION

Clock Gating Technique(CGT) is a well known method which can be used to reduce power dissipation while designing any VLSI circuit. Now a days, power consumption and switching speed are the areas for which vlsi designers are more concerned about. CGT is one of the technique which can optimize the power by 19-25% and can enhance the switching speed as well [3]. As we have two types of CGT: (i)DCG & (ii)ACG. To use Deterministic Clock Gating we should be perfect in system architecture designing, and should have the knowledge of pipelining. Whereas Adaptive Clock Gating first analyzes IP model which can be modeled as a finite state machine [3]. Here we are achieving the goal through ACG technique.

II. EXISTING ADC SYSTEM

In today's era everything is digitalized to make our lives easy and comfortable. Every single thing has been changed its state to be digital. As we know that there are so many drawbacks of analog signals , so , to overcome all these problems we switch over digital signal. To convert analog signal into digital form we require Analog to Digital Converter i.e. ADC. Here we will discuss the existing ADC system. As shown in fig. (1) ADC has different functional blocks in it. These functional blocks are as follows:

- A comparator.
- A Multiplexer.
- A successive approximation register.
- An output latch buffer.
- A sample and hold circuit (optional).

First of all we provide N-bit input signals to the Multiplexer, so , that it avoids congession to the inputs channels of ADC. Since multiplexer is nothing but a type of digital switch which produces only one output signal regardless of no. of inputs present. This output signal of multiplexer is given as one of the inputs to the comparator. Second input of comparator is the signal provided by the register tree. Register tree is nothing but the voltage divider circuit which is use to produce equivalent analog value i.e. Vref. Now the comparator will compare these two inputs available to it .

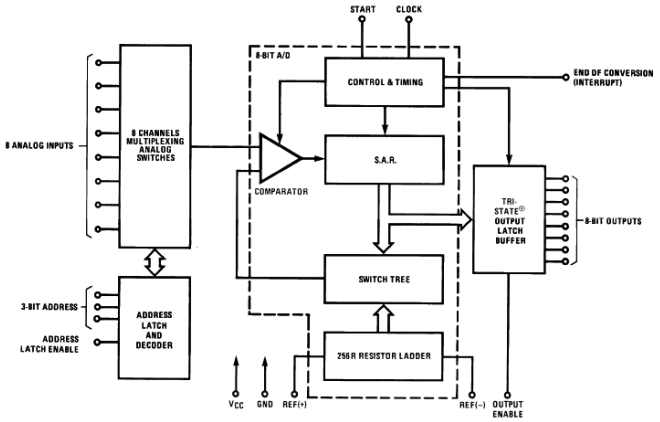

Fig. (1). Block Diagram of ADC

If (Vref > output of Mux) :
Then, Vout = '1'i.e. digital value of MSB.
If (Vref < Output of Mux) :
Then , Vout = '0' i.e. Digital value of MSB.

The output of the comparator is given to S.A.R unit to perform binary search for all bits available in SAR. The final digital codes available in SAR is the digitalized representation of analog signal. In this ways it produces digital signal out of analog inputs.

DRAWBACKS:

- ADC has comparator which is nothing but one of the application of Operational Amplifier (Op-Amp). As we know that op-amp consumes more power to compare Vref and output of Mux. It leads to more power dissipation.

- For comparator three major constraints are to be consider:

  (i) Comparator Trimming.

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(ii) Correction of Digital Output Data.

(iii) Selection of Optimal Set of Comparator.

- The points mentioned above are the reasons behind this experiment of power reduction of ADC by using Clock Gating Technique.

II. PROPOSED CLOCK GATING ARCHITECTURE

Modified instruction level Adaptive Clock Gating is the only method which can optimize dynamic power which deals with power consumption and switching activity. So, we use this technique to analyze IP model of FSM. For FSM there are five states: Idle, ready, Run, Wait and End. Usually we provide clock signal to each and every states of FSM to make a transition from one state to another. When an IP core finishes its work and enters to the idle state and stays there until system bus makes a request. Whenever any state of FSM enters the IDLE state ACG is being considered as shown in Fig. 2[3].
For output the control signals are generated in running staes, and combined with thw main FSM clock signal using modigfied instruction level clock gating. When not needed clock signal is diaabled. When output is active high, instructional ACG disables the IP clock otherwise, the clock is enabled. It reduces dynamic power consumption by 15-20%[1][3].

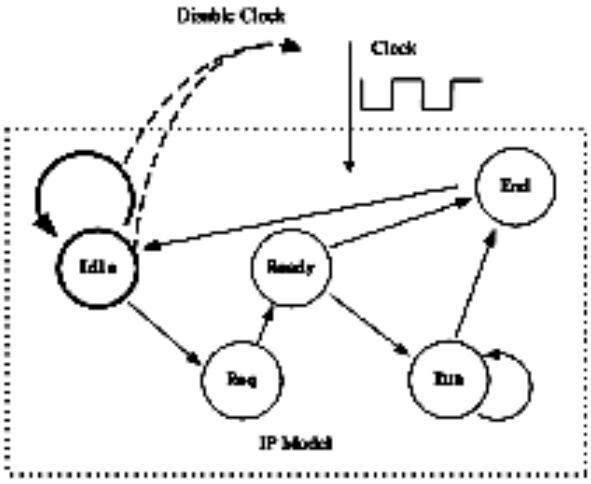

Fig. (2) ACG Principle for Low Power Design

A. APPICATION OF CLOCK GATING TECHNIQUE

Now a days Dynamic power management (DPM) has become very popular in low power vlsi design area. The concept of DPM is to minimize switching speed as much as possible, by using clock gating technique . Instruction level clock gating technique is being used to control the clock of Mux, SAR, Register tree. The basic procedure is shown in Fig. 3.

Where,
PORT I/O = I/O port operation,
ID = instruction decode operation,
IF = instruction fetch operation,
SIO = UART operation means transmission and reception
Port

Some of the instructions don't need this SIO operation but need PORT operation, such as IN SIO, OUT SIO instruction. By seeing this fig 3 We have a view that a power control logic is being used in different states of the FSM of PORT I/O functional block design flow. The control logic decide clock period for every instruction, and according to that the state of the clock to every component will be decide , whether it will be active mode or non active mode. This CGT efficiently reduces switching activity of the clock and register operation in the design flow of functional block. Some functional block enters in the IDLE state, which causes more reduction in the clock power consumption. Hence, the idea behind our proposed clock gating technique is to reduce switching speed of a functional block when they enter in IDLE state, and the power consumed by a functional block in running state as well.
The basic block diagram of a sample PORT I/O functional block is shown Fig.3 All operations need synchronization with the system clock, and both the edge of clock should be used. When Input of SIO MUX = 1, that means , PORT blocks are not being used but SIO block is being used. We adopt clock gating technique to the clock of PORT block. When the PORT blocks are in running state the clock becomes disable. Hence , it is easy to reduce power dissipation of the unused blocks.

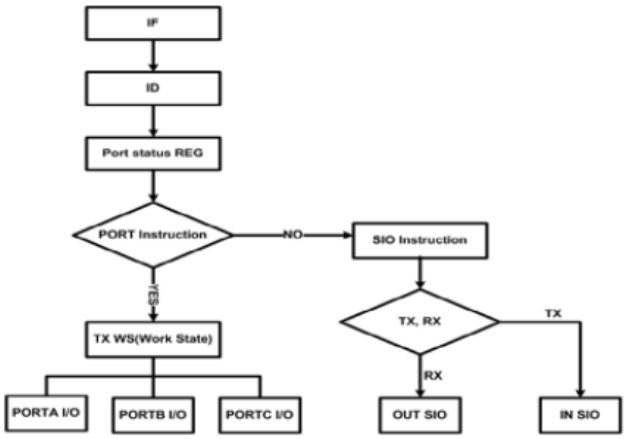

Fig. (2) Standard Design Flow

B. CLOCK GATED ADC ARCHITECTURE

The method of calibration is responsible to select an optimal set of comparators for this particular design and the reason behind this is the low power consumption of this method. The comparators are disabled by clock gating method to reduce the power consumption. Out of all clock gating here we use NAND gate as a local clock driver for all comparators as shown in Fig. 3.

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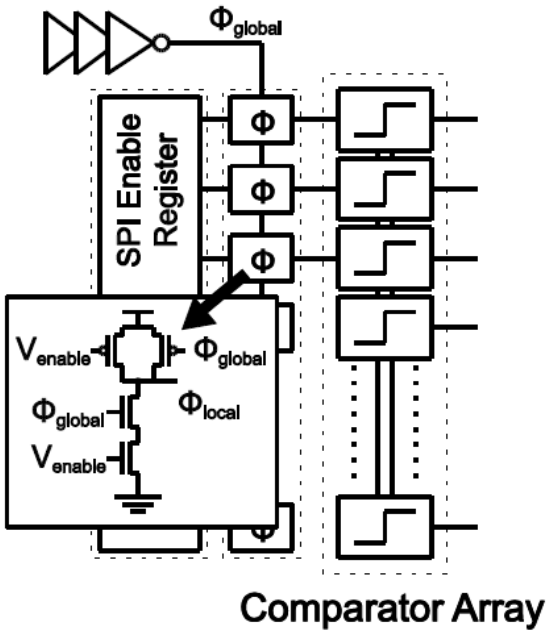

Fig. (3) Clock Gated Comparator

The NAND-gate is chosen to emphasize the rising edge of the clock at minimal clock load. When clock is disabled, the comparators will be go on the latching state i.e. in waiting state so that there will not be any effect of changes in the input signal or will not dissipate power due to switching. latched output has only two states either high i.e. '1' or low i.e. '0'. The enable signal is also used to reset the output signal in the subsequent latch to prevent the disabled comparator from biasing the final output. A serial-to-parallel-interface (SPI) is being used to program the enable signal register through an prt which is externally connect to it . It also leads to less power dissipation.

Vref to the comparators are generated by a voltage divider circuit known as resistor ladder. It also causes power dissipation , but the amount is very low so we can neglect it .

IV. METHODOLOGY

- FPGA board runs at 4-35Mhz and ADC runs at typical frequency of 650Khz.
- Using counter and clock divider we will divide main FPGA clock to get desired frequency. That frequency controller through AND gate will be sent out from FPGA on a port pin and given to ADC0808 IC.
- There will be a gating variable bit declared inside VHDL code. This bit and generated 650Khz frequency will be giben to AND gate. If that bit is high clock will be fed to ADC otherwise no clock.
- Now when program needs some external analog value to be read, it will activate the clock for ADC, ADS value is read inside by SC, OE and EOC, and 8 bit parallel data sequence mentioned in link above, and then clock is topped again. This will result into power saving.

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V. CONCLUSION AND FUTURE WORK

Here we have used clock gating techniques (ACG) in functional block designing of ADC. As it is mentioned above the drawbacks of existing ADC, so we are proposing the ACG, which is more efficient and easy for low power VLSI design for sequential as well as combinational circuits. It can also enhance switching speed along with reduction in power consumption by using same technique. We can reduce area as well, if we want to.

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