Implementation of a 4-Bit Direct Charge Transfer Switched Capacitor DAC and DWA DEM technique

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Abstract— The direct charge transfer switched capacitor DAC is one of the type of delta-sigma DAC which reduce capacitor mismatch effect. The switched capacitor DAC mainly suffers from mismatch among capacitors. Mismatches among the capacitor in DAC cause the nonlinearity between output and input. It also reduces Signal to Noise Distortion Ratio (SNDR). Dynamic Element Matching (DEM) technique is used to match the capacitors. According to element selection logic there are many types. In this paper Data Weighted Averaging (DWA) technique is used for mismatch shaping. In this paper the 4 bit DCT-SC-DAC and DWA-DEM technique is implemented using WINSPICE simulation software.

Index Terms—∑-Δ DAC, DCT-SC-DAC, mismatch shaping, DWA, DEM

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I. INTRODUCTION

The demand for high performance and linearity increases in audio digital to analog converter. The analog output is dependent on digital input and also analog reference voltage.

Oversampling DACs use quantization-noise-shaping to increase signal to noise ratio (SNR). The Δ-∑ DAC is the one of the popular type of oversampling DAC. Noise shaping requires that the DAC be clocked at a frequency much higher than the signal bandwidth.
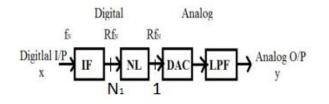

Fig.1. Block diagram of Delta-sigma DAC

The Fig.1 shows the block diagram of ∑-Δ DAC. In ∑-Δ DAC the difference between two signals is measured and used to get good conversion. The interpolation filter is used to increase the sampling ratio of the input data from the Nyquist rate f_N to Rf_N, where R is the oversampling ratio. Oversampling ratio is the ratio of the clock frequency to (twice) the signal bandwidth. The main function of noise-shaping loop (NL) is to reduce the word length of the signal from N_1 to a much lower value, often to 1. Mainly switched capacitor DAC is used in delta-sigma DAC as internal DAC. Low pass filter gives noise free analog output voltage [6].

II. A 4 BIT DCT-SC-DAC

The 16 level DCT-SC DAC is implemented in this paper. While converting the digital input into analog it also decreases noise and enhances power efficiency.

The circuit shown in Fig.2 is 4-bit DCT-SC DAC. As shown in figure operational amplifier is integral part of DCT-SC-DAC. There is very basic relationship between number of bits and levels (number of capacitors) given as $a=2^b$, where 'a' is levels and 'b' represents number of bits. The input word to the circuit is given by thermometer code as x_1 to x_{16}. If input word is 5, x_1 to x_5 will be 1 and rest are 0. When $\phi_1=1$ (reset phase) all the input capacitors are charged to V_{ref} and C_f is discharged. When $\phi_2=1$ (conversion phase) all the input capacitors (i.e. C_1 to C_m) are discharged into C_f, resulting in an output voltage

$$V_{out} = (mC/C_f) V_{ref} \tag{1}$$

Where m is integer value of the input word, C is value of input capacitor, C_f is feedback capacitor and V_{ref} is reference voltage to circuit [1].
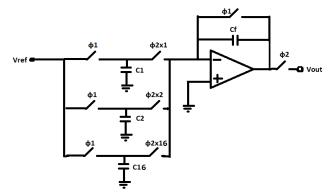

Fig.2. Circuit Diagram of 4-bit DCT-SC DAC

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A. Operational Amplifier

Operational amplifier is an integral part of analog and mixed signal systems. The Table 1 gives comparison between two main types of op-amp as 1) one-stage op-amp 2) two stage op-amp. Telescopic and Folded-cascade op-amp are the types of one-stage op-amp. By observing the table 1 it is seen that two stage op-amp gives high gain and high output swing as compared other types of op-amp. It also gives low noise and medium power dissipation as compared to other types, so two stage op-amp is suitable to use in DCT-SC-DAC [7].

Table.1. Comparison of performance of various op amp topologies

Type of op-amp	Gain	Output swing	Speed	Power dissipation	Noise
Telescopic	Medium	Medium	Highest	Low	Low
Folded-cascade	Medium	Medium	High	Medium	Medium
Two-stage op-amp	High	Highest	Low	Medium	Low

The Fig.3 shows the basic block diagram of two stage op-amp. As shown in figure it consists of mainly four blocks as differential amplifier, compensation circuit, second gain circuit and bias circuit. Differential amplifier provides the single ended output. The gain provided by this intermediate stage is not enough so the second gain stage is used. As name implies second gain circuit provides additional gain to the circuit. Compensation circuitry is used to lower the gain at higher frequencies and to achieve stable closed loop performance. Bias circuit is provided to establish the accurate operating point for each transistor in its quiescent state [11].
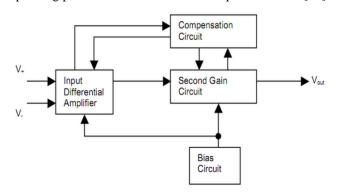

Fig.3 Block Diagram of Two Stage Op-amp

The internal circuit diagram of two stage op-amp is shown in Fig.4. The two stage op-amp consists of MOS transistors and also compensating and load capacitor are used [7]. This circuit is implemented using WINSPICE.
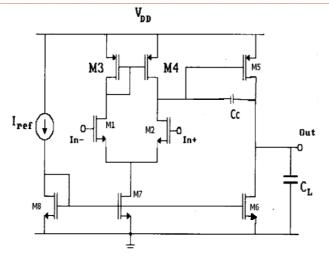

Fig.4. Circuit diagram of two stage op-amp

III. DWA-DEM MISMATCH SHAPING TECHNIQUE

Mismatch among any elements can be defined as difference is electric property even if physical layout is same. Mismatch causes the nonlinearity and also reduces the signal to noise plus distortion ratio (SNDR). There are mainly two types of sources of mismatch as 1) random error and 2) systematic error. Random error occurs due to variation in fabrication process and it cannot be predicted. Whereas systematic error occurs due to imperfect balancing in circuits and gradients and it can be predicted precisely [1].

Mainly two types of non-linearity error are caused due to mismatch as 1) integral nonlinearity and 2) Differential non-linearity. Integral non linearity (INL) is defined as the deviation of actual output from the ideal. Whereas differential nonlinearity is deviation between two analog values corresponding to adjacent input digital values.

Different mismatch shaping techniques are used to shape the noise. Dynamic element matching technique (DEM) groups the elements in such a manner that the DAC error is shaped to high frequency. According to the element selection logic Data weighted averaging (DWA), Individual level averaging (ILA), Butterfly shuffler, complex tree structure and vector based techniques are available.[12] In this paper data weighed averaging technique is implemented using WINSPICE .

A. DWA implementation

DWA technique is efficient technique. In this technique all the capacitors are used at maximum possible rate while ensuring that each capacitor is used the same number of times.
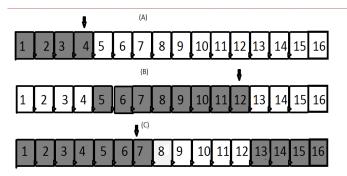
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Fig.5. DWA Element Selection for 4 Bit DAC with an Input Sequence of 0100, 1000 & 1011

Fig.5. explains the working of the Data weighted averaging technique. Fig.5 illustrates the concept for a 4-bit DAC with an input sequence of 0100, 1000, and 1011. Initially pointer will be at zero when first input is given as 4, the first four unused bits are selected as shown in Fig.5 (A) . In Fig.5 (B) input word 1000 so the next 8 unused elements are selected and pointer is set to 12. Again the input word in Fig.5 (C) is 1011 i.e. 13 so next 13 unused elements are selected and pointer is set to 7. The component selection will sequentially continue in this manner as the data is applied [8, 9].
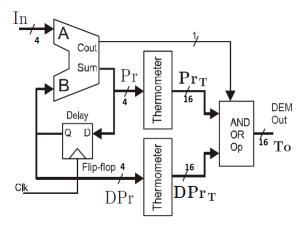

Fig.6. DWA technique

Basic block diagram of a DWA technique for 4 bit DAC is shown in Fig.6. As shown in figure 4 bit full adder, thermometer decoder, D flip flop and AND or OR operation are used. In represents 4 bit input, Pr is pointer which points the current element, DPr is delayed pointer which represents the previous pointer, Prt and DPr$_t$ are thermometer code of Pr and DPr respectively [2]. The output of DWA is then applied to DCT-SC-DAC.

B. SCOPE OF DWA TECHNIQUE

The data weighted averaging technique gives better performance compared to other mismatch shaping techniques. Using data weighted averaging technique (DWA) delta-sigma DACs can be fabricated with minimal impact upon chip area. By using DWA technique elements are used at maximum possible rate and DAC errors will quickly sum to zero by moving distortion to high frequencies. In this technique no

element is selected inordinate times, even in short and long time intervals. [3] [4]

IV.DESIGN EXAMPLE

The 4-bit DAC circuit containing 16 unit elements was simulated with WINSPICE using 180nm technology. The 4 bit DCT-SC-DAC circuit used C=1pf and C$_f$=16pf, C$_c$=3pf and C$_{L=}$10pf and W/L ratio of transistor are calculated to obtain gain of 7000v/v for two stage operational amplifier.

V.SIMULATION RESULTS

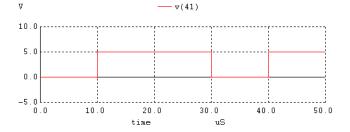Table.2. Simulation Output of 4-bit DCT-SC-DAC

Thermometer Code	Theoretical Output	Practical Output
0000000000000000	0v	60mv
0000000000000111	0.99v	1v
0000000000111111	2.31v	2v
0000000011111111	2.64v	2.4v

Table 2 shows the results of 4 bit DCT-SC-DAC. Theoretical outputs are calculated using equation (1).

Table 3 shows output at 16 pin of DWA circuit for different input combinations.

Table.3. Simulation result of data weighted averaging

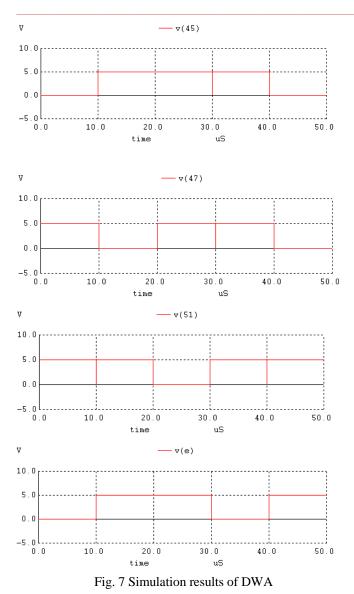| Input → Output pins ↓	1000	1110	1010	1100	1010
40	0	1	1	0	1
41	0	1	1	0	1
42	0	1	1	0	1
43	0	1	1	1	0
44	0	1	1	1	0
45	0	1	1	1	0
46	0	1	1	1	0
47	1	0	1	1	0
48	1	0	1	1	0
49	1	1	0	1	1
50	1	1	0	1	1
51	1	1	0	1	1
52	1	1	0	1	1
53	1	1	0	1	1
54	1	1	0	1	1
E	0	1	1	0	1

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Fig. 7 Simulation results of DWA

Fig. 7 shows the simulation results of DWA technique in WINSPICE software.

V.CONCLUSION

DCT-SC-DAC, generated analog output which matches with the theoretical values. A low complexity digital implementation of DEM-DWA is performed using WINSPICE in 180nm technology. As shown in table 3, outputs at pin 40-54 & e (16 bit) are "0000000111111110" for input 8(1000) & changes to "1111111001111111" for input 13 (1101). Thus, data weighted averaging technique uses all the capacitors at equal number of times.

REFERENCES

[1] Un-Ku Moon, Jos'e Silva, Jesper Steensgaard and Gabor C. Temes , "**A switched –capacitor DAC with analog mismatch correction**", Dept. of Electric and Computer Engineering, Owen Hall, Oregon State University, Corvallis, USA.

[2] Mohamed aboudina and Behzad Razavi, "**A new DAC mismatch shaping technique for Sigma Delta capacitors**", Computer systems Dept., Technical Univerrsity of Sofia

[3] Maria Bojidarova Stanoeva, Angel Nikolaev Popov, "**Investigation of a precise DAC based on two mismatched Modulator**", IEEE transactions on circuits and systems-II, VOL. 57, NO.12, December 2010.

[4] Jared Welz Ian Galton and Eric Fogleman "**Simplified Logic for First –order Mismatch Shaping Digital-to-analog Converter**", IEEE transactions on circuits and systems-II;analog and digital signal processing, VOL. 48, NO.11, November 2001.

[5] Ichiro Fujimori and Tetsuro Sugimoto, "**A 1.5, 4.1 mW Dual-Channel audio Delta-Sigma D/A converter**", IEEE journal of solid-state circuits. VOL.33, NO.12, December 1998.

[6] Liu Yuyu, Gao Jun Yang Xiaodong, "**24-bit low power low cost digital audio sigma-Delta DAC**", Tsinghua science and technology, VOL 16, NO. 1, February 2011.

[7] Phillip E. Allen and Douglas R. Holberg, "**CMOS Analog Circuit Design**", 2nd Edition, Oxford University Press, 2010.

[8] L. Gallin-Martel, D. Dzahini, J-Y Hostachy, F. Rarbi, and O. Rossetto, "**Design of high range digital to analog converters for the calibration of the CALICE Si-W Ecal readout electronics**",2003.

[9] Rex baird and Terri Feiz, "**Linearity enhancement of multi-bit ∑∆ A/D and D/A converters using data weighted averaging**", IEEE journal of solid-state circuits, VOL. 32, NO. 8, August 1997.

[10] Ramon Lopez-Holloway and Miguel García "**A Low-Complexity Data Weighted Averaging (DWA) Algorithm implementation**" National Institute of Astrophysics, Optics and Electronics , 2007

[11] Phillip E. Allen and Douglas R. Holberg, "**CMOS Analog Circuit Design**", 2nd Edition, Oxford University Press, 2010.

[12] Ali K. Nahar, "**Data Weighted Averaging Technique (DWA) with 1st order noise shaping to improve 6 bit Digital-to-Analog Converter (DAC) performance**", Journal of Babylon University, VOL.21,NO.5, 2013.

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