International Journal on Recent and Innovation Trends in Computing and Communication
Volume: 2 Issue: 6

ISSN: 2321-8169
1618 – 1622

Design of Testable ripple carry adder in Quantum Dot Cellular Automata

Ms.Punam Prabhakar Bhalerao
Department of Electronics Engineering, Patel Institute of Engineering and Science,
Bhopal, 462044, India

Sameena Zafar
H.O.D Department of Electronic Communication Engineering,
Patel College of science and Technology,
Bhopal 4620044, India

***Abstract*—** This paper provide an Outline of two test vectors testable sequential circuit based on conservative logic gate with the help of logic gate testability .In proposed work Two test vectors (all 1's and all 0's) are used to test classical unidirectional stuck at faults of any sequential circuit. By using two test vectors i.e. 1's and 0's All Reverse sequential circuits completely testable any stuck-at fault. We found that parity mismatch occurs between the input and the output due to the fault in the molecular QCA implementation Otherwise input parity is same as Output parity. We are presenting a new conservative logic gate in proposed work called multiplexer conservative (MX-QCA) logic gate with reversible DET flip-flop based on properties as the fredking gate and completely testable sequential circuit using two vector . The proposed MX-cqca gate provide less complexity of operation (the number of majority voters) high speed and small area as compare to fredking gate.

Keywords- Quantum-dot Cellular automata, conservative logic, Fredkin gate, , reversible logic**.**

*****

I .INTRODUCTION

QUANTUM dot cellular automata (QCA) are a nanotechnology with the small feature size, high clock frequency, and ultra low-power consumption advantages. Quantum dot cellular automata (QCA) not only gives a solution at nano scale, but also it offers a new method of computation and information transformation [1]. In this Synthesis and deposition phases defect can occur in the manufacturing of QCA. The logic states ("0" and "1") are defined by the positions of the electrons in QCA alternative way [1] [7]. .Some studies has been reported that QCA can be used to design general-purpose computational and memory circuits QCA that has recently been recognized as one of the top six emerging technologies with potential applications in future computers [2]. Due to the significant error rates in nano-scale manufacturing and nanotechnologies, including the QCA, there is a critical need to maintain extremely low device error rates [1].

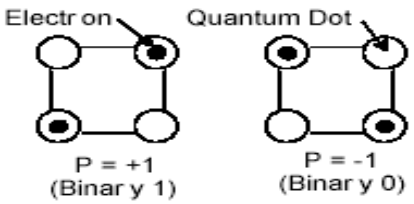
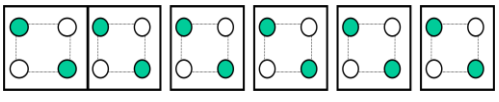


Fig 1(a)



Input Output

Fig 1(b)

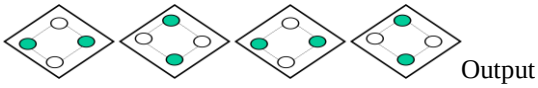


Fig 1(c)

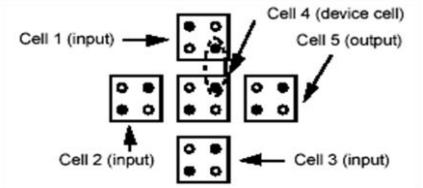


Fig. 1. QCA cell and basic QCA devices. (a) QCA 4 Dots. QCA cell as logic "1," and logic "0."(b) Binary wires (c)inverse chain . (d) MV.

QCA cell structure is a square pattern in this structure four dot is present in square pattern .The quantum dots capable to provide number of controllable 3D electrons In QCA cell [3], These electrons are able to tunnel between dots if the potential barrier separates the dots is low that binary information is encoded by the configuration of electrical charges in a QCA cell. When barrier is low, the electrons can located on any dot and the Null state occurs and when the barrier is raised, the cell is polarized and the other two states can occur. These two states are shown as P = +1 and P = −1 in Fig 1(a) [4]. Moreover, power dissipation in QCA circuits is ultra low compared with conventional CMOS circuits. QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates [2], [3]. In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell as illustrated in Fig. 1(b). Thus, when the bit is flipped from 1 to 0 there is no capacitor get discharging as in conventional CMOS. Hence, during transition QCA does not have to dissipate all its signal energy..QCA has provide some advantage compared to CMOS technology in terms of power dissipation .QCA and other nanotechnologies used to reducing device error rates .

In this paper, we propose the design of testable sequential circuits based on conservative logic gates MX-QCA based on fredking gate. Circuit perform operation in normal mode when there is no movement of electrons from one QCA cell to the other cell, there is no current flow . However, in order to detect faults in the test mode, The proposed technique

is extended toward the design of two vectors testable master-slave flip-flops and double edge triggered, (DET) flip-flops .we identified the QCA devices in the QCA layout of the Fredkin gate that can be replaced with fault tolerant components to provide the 100% fault coverage

.

II BACKGROUND

A conservative logic gate is a one to one multiple-output logic element in which the number of 1s at the inputs is equal to that of the corresponding output A conservative logic network can be work as non-reversible in nature if one-to-one mapping is not preserved. Researchers proved that: 1) in the event of unidirectional stuck-at-faults in a conservative logic network, either the number of 1s in its output set will differ from the number of 1s in its input set, or the output set is correct and 2) in a conservative logic network the two vector test sets, all 1s and all 0s, provide 100% coverage for unidirectional stuck-at faults [5]. Any stuck-at-1 fault in the conservative logic circuit can be detected by setting all inputs to 0s followed by subsequent checking of the outputs for the presence of any 1s. Any stuck-at-0 faults can be detected by setting all inputs to 1s followed by subsequent checking of outputs for the presence of any 0s. The comprehensive proofs can be referred in [2],[5] .

A. Conservative Reversible Fredkin Gate

Fig(2). shows the 3×3 reversible gate called Fredkin gate or swap gate. It has three inputs (A, B, C) and three outputs (P, Q, and R). The outputs are defined by to (P=A, Q=A'B +AC , R=AB+A'C) [6] . The truth

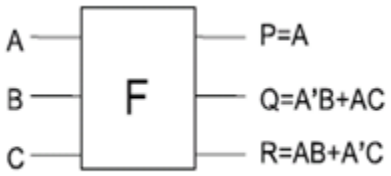


Fig (2)

table of the Fredkin gate demonstrates that Fredkin gate is swapping output or reversible output and conservative in nature, that is, it has unique input and output mapping and also has the same number of 1s in the outputs as in the inputs as. shown in fig 2 (a)

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig 2(a) Truth Table of Fredking gate

B. Basics of QCA Computing

In this paper, we propose a class of new designs for the implementation of testable sequential circuits form molecular QCA based on a special type of reversible logic called conservative reversible logic [7] . A QCA cell is a coupled dot system in which four dots are at the vertices of a square. The cell has two extra electrons that occupy the diagonals within the cell due to electrostatic repulsion. Fig. 1(a) and (b) shows the four quantum dots in a QCA cell, and the implementation of logic "0" and logic "1" in a QCA cell, respectively. The basic QCA device is the MV or majority gates or voters, which is represented as F = AB + BC + AC, where F is the majority of the inputs A, B, and C. Another important gate in QCA is the INV. There can be many ways of designing the QCA INV, In QCA computing, the clock helps in the synchronization of circuits and provides the power required for functionality.QCA clocking consists of four phases: switch, hold, release, and relax. In QCA computing, signal transfer is made through wires that are of two types: 1) binary wire and 2) INV chain. The binary wire is shown in Fig. 1(e). The INV chain . In QCA, there is no interaction between the binary wire &INV when crosses wire over each other,; hence, the signals in the INV chain and binary wire can pass over each other

C. Related Work

To the best of our knowledge, the offline testing of faults in reversible sequential circuits is not addressed in the literature. Any nanotechnology having applications of reversible logic. The testing of QCA was addressed for the first time in a seminal work reported [7]. The research on reversible logic is expanding towards both design and synthesis. Several researches have proposed reversible circuits in terms of garbage output, number of gate, power Dissipation [8] and other Several researchers have been exploring techniques for synthesis of reversible logic circuits and many interesting contributions have been made .such as based on nano-CMOS devices ,low power molecular QCA computing ,all are susceptible to high error rates due to transient faults. With respect to this paper on reversible sequential circuits. In this paper, we present the design and test of Digital circuits that can be tested by only two test vectors, all 0s and all 1s, for any unidirectional stuck-at-faults. Further ,the approach of fault testing based on conservative logic is extended toward the design of non reversible sequential circuits based on MX-cqca. based on conservative logic is extended toward the design of non reversible sequential circuits based on MX-cqca.

III. DESIGN OF TESTABLE REVERSIBLE LATCHES

D-latch is a sequential circuit The characteristic equation of the D latch can be written as $Q+ = D \cdot E + .E \cdot Q$. The equation can be mapped onto the Fredkin gate. [8],[7],[5] Fig.(3) shows the realization of the reversible D latch using the Fredkin gate. Thus the frequency of DET flip-flop is reduced to half of the master slave flip-flop because of DET flip-flop using reversible concept is proposed for sampling and storing the data at both the edge of the clock cycle [9] . It perform the operation in two mode 1) normal mode 2)Test mode In the proposed work, enable (E) refers to the clock and

 ISSN: 2321-8169
1618 – 1622

is used interchangeably in place of clock. When the enable signal (clock) is 1, the value of the input D is reflected at the output that is Q+ = D. While, when E = 0 the latch maintains its previous state, that is Q+ = Q. The

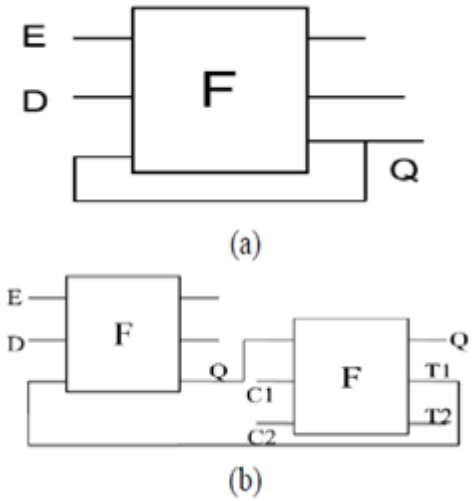


Fig (3)

1) Normal Mode: The normal mode is shown in Fig.3 in which we will have C1C2 = 01 and we will have the design working as a D latch without any fan-out problem.

2) Test Mode: In test mode, When C1C2 = 11 , the output T1 will become 1 and the design will become testable with all 1s input vectors for any stuck-at-0 fault when C1C2 = 00. it will make the design testable with all 0s input vectors as output T1 will become 0 resulting in making it testable with all 0s input vectors. Thus, any stuck-at-1 fault can be detected.. It can seen from above that C1 and C2 will disrupt the feedback in test mode, and in normal mode will take care of the fan out. Thus, our proposed design works as a reversible D latch and can be tested with only two test vectors, all 0s and all 1s, for any stuck-at fault by utilizing the inherent property of conservative reversible logic.

IV. DESIGN OF TESTABLE MASTER-SLAVE FLIP-FLOPS

In the existing literature, master-slave strategy design using one latch as a master and the other latch as a slave reversible flip-flops . In this paper, we proposed the design of testable flip-flops using the master slave strategy that can be tested for any stuck-at faults using only two test vectors, all 0s and all 1s. Fig. 4 shows the design of the master-slave D flip-flop. The testable reversible D flip-flops has four control signals mC1,mC2, sC1, and sC2. Out of this mC1 and mC2 control signals for the master latch, while sC1 and sC2 control signal for the slave latch. In the normal mode ,when the design is working as a master-slave flip-flop the values of the controls signals will be mC1 = 0 and mC2 = 1,sC1 = 0 and sC2 = 1 (as similar to values of the control signals C1 and C2 earlier described for the testable D latches).

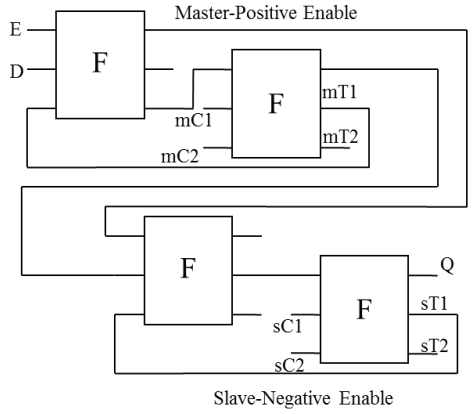


Fig (4)Fredkin gate-based testable reversible master-slave D flip-flop

Test mode.
1) To make the design testable vectors for any stuck-at-1 fault for all 0s input , the values of the controls signals will be mC1 = 0 and mC2 = 0, sC1 = 0 and sC2 = 0.This will make the outputs mT1 and sT1 as 0, which results in breaking the feedback and the design becomes testable with all 0s input vectors for any stuck-at-1 fault.2) To make the design for any stuck-at-0 fault for all 1s input vectors, the values of the control signals will be mC1 = 1 mC2 = 1, sC1 = 1, and sC2 = 1.This will result in outputs mT1 and sT 1 having a value of 1, breaking the feedback and resulting in the design testable with all 1s input vectors for any stuck-at-0 fault.

V .DESIGN OF TESTABLE REVERSIBLE DET FLIP-FLOP

The negative edge triggered master-slave flip-flop pass input data when value of E=1 while the slave latch maintains the previous state. When E = 0 , the master latch is in the storage state while the slave latch passes the output of the master latch to its output. Thus, the flip-flop does not sample the data at both the clock levels and waits for the next rising edge of the clock to latch the data at the master latch. The advantage of this design is that the data rate can be maintained and frequency is reduced to half when compared with the master slave flip-flop [10]. The DET flip-flop is designed by connecting the two latches, the positive enable and the negative enable in parallel rather than in The advantage of this design is that the data rate can be maintained and frequency is reduced to half when series The 2:1 MUX at the output transfer the output from one of these latches which is in the storage state.

1) Normal Mode:

The normal mode of the DET flip-flop is shown in fig where pC1 = 0, pC2 = 1, nC1 = 0, and nC2 = 1. The pC1 = 0, pC2 = 1 help in copying the output of the positive enable D latch thus avoiding the Fan out while the nC1 = 0 and nC2 = 1 help in copying the output of the negative, the master is designed using the positive enable T latch, while the slave is designed with the negative enable D latch.

2) Test Mode:

 ISSN: 2321-8169
1618 – 1622

There will be two test modes.

a) All 1s Test Vectors: This mode make the control signals value as pC1 = 1, pC2 = 1, nC1 = 1, and nC2 = 1. The pC1 = 1 and pC2 = 1 with the help of value of pC1, pC2 the positive enable D latch feedback break , while the nC1 = 1 and nC2 = 1 help in breaking the feedback of the negative enable D latch. This makes the design testable by all 1s test vector for any stuck-at-0 fault

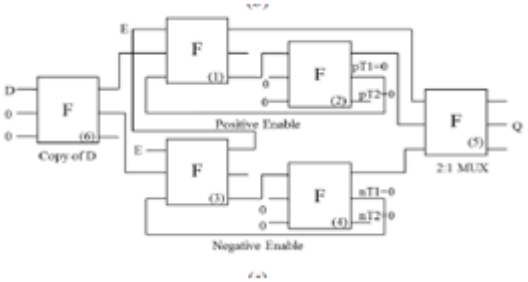


Fig 5(b)

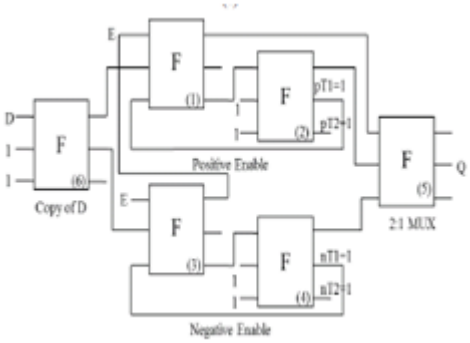
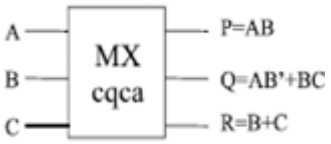


Fig 5(c)

b) All 0s Test Vectors: In this mode value of control signal is pC1 = 0, pC2 = 0, nC1 = 0, and nC2 = 0. The pC1 = 0 and pC2 = 0 help in breaking the feedback of the positive enable D latch, while the nC1 = 0 and nC2 = 0 help in breaking the feedback of the negative enable D latch. This makes the design testable by all 0s test vector for any stuck-at-1 fault.

VII. PROPOSED MULTIPLEXER CONSERVATIVE

. MX-cqca gate introduce to remove the disadvantages of fredking reversible sequential circuit. The proposed conservative logic gate is called multiplexer conservative QCA gate and has three inputs and three outputs. MX-cqca has one of its outputs act as a multiplexer this output help in mapping the sequential circuits based on it, while the other two outputs work as AND gate and OR gates, respectively. The mapping of the inputs to outputs of the MX-cqca is: P = AB; Q = AB′+BC; R = B + C, where A, B, and C are the inputs and P, Q, R are the outputs, respectively.QCA GATE For many of the designs, the designer could potentially be interested in using the testing advantages of conservative logic but saving the number of QCA cells. Thus, we propose a new conservative logic gate that is conservative in nature but is not reversible. The proposed conservative logic gate is called multiplexer conservative QCA gate



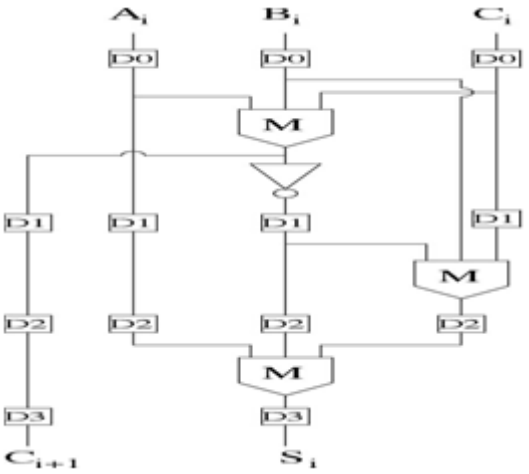
Input			Output		
A	B	C	P	Q	R
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	0	1
0	1	1	0	1	1
1	0	0	0	1	0
1	0	1	0	1	1
1	1	0	1	0	1

Truth Table

VIII. RIPPLE CARRY ADDER

The linear feedback shift register (LFSR) is commonly used as a test pattern generator (TPG) provide low overhead built-in self-test (BIST). This is due to the fact that an LFSR can be design used as a little area overhead not only as a TPG, This provides high fault coverage for a large class of circuits ,as well as output response analyzer. Test pattern generation is the process of generating a (minimal) set of input patterns to stimulate the inputs of a circuit, such that detectable faults can be sensitized and their effects can be propagated to the output. This test patterns are given to inputs of the ripple carry adder get the outputs according to the test patterns inputs. We will inject the faults based on struck at 0 and

Stuck at I fault



Fig(6)

Fig (7)

LFSR:
The most commonly used linear function of single bits is XOR. Thus, an LFSR is most often a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen
feedback function can produce a sequence of bits which appears at output line.

IX. CONCLUSION

This paper proposed work based on Design and Test of Digital Circuits by Quantum- Dot Cellular Automata that is testable for any unidirectional stuck-at faults using only two test vectors, all 0s and all 1s. The sequential circuits implemented using conventional classic gates do not provide inherited support for testability. Hence, a conventional sequential circuit needs modification in the original circuitry to provide the testing capability. the main advantage of the proposed conservative reversible sequential circuits compared to the conventional sequential circuit is the need of only two test vectors to test any sequential circuit irrespective of its complexity because sequential circuit increases the number of test vector required to test the sequential circuit also increases. For example, to test a complex sequential circuit thousand of test vectors are required to test all stuck-at-faults, while if the same sequential circuit is build using proposed reversible sequential building blocks it can be tested by only two test vectors, all 0s and all 1s. Thus,. The reduction in number of test vectors minimizes the overhead of test time for a reversible sequential circuit. The proposed work has the limitation that it cannot detect multiple stuck-at-faults as well as multiple missing/additional cell defects. In conclusion, this paper advances the state-of-the-art by minimizing the number of test vectors needed missing/additional cell defects.

REFERENCES

[1] Mehdi Baradaran Tahoori and Fabrizio Lombardi “Testing of Quantum Dot Cellular Automata Based Designs ieeexplore”1408 - 1409 Vol.2; ISSN : 1530-1591; Print ISBN: 0-7695-2085-5

[2] Himanshu Thapliyal, “Design of Testable Reversible Sequential Circuits,” IEEE Trans. Appl. Super-conduct., VOL. 21, NO. 7, JULY 2013.

[3] Anoop Vetteth, Konrad Walus, Vassil S. Dimitrov, Graham A. Jullien “Quantum-Dot Cellular Automata Carry-Look Ahead Adder And Barrel Shifter,” conf.2005

[4] Zahra Mohammadi , Majid Mohammadi , Mahdi Hasani “ Designing of Testable Reversible QCA Circuits Using a New Reversible MUX 2×1,” JACR Journal Vol. 3, No. 1, February 2012.

[5] M.Arthi anushalakshmi, R.Anandh, “QUANTUM-STUCK AT FAULT TESTING USING REVERSIBLE SEQUENTIAL CIRCUITS,” sequential circuit” IJISER Journal Vol 1 Issue 5 MAY 2014.

[6] Pradeep Singla , Naveen Kr. Malik “ A Cost- Effective Design of Reversible Programmable Logic Array” International Journal of Computer Applications (0975 – 8887) Volume 41– No.15, March 2012

[7] Himanshu Thapliyal, “Reversible Logic-Based Concurrently Testable Latches for Molecular QCA,” IEEE Trans. Appl. Super-conduct., VOL. 9, NO. 1, JANUARY 2010

[8] M.K.Nigesh praveen kumar, A.Arul Rex “Design of Stuck at Fault Testable Conservative Logic based Flip-Flops and its Application Circuits” International Journal of Computer Science Engineering (IJCSE) : 2319-7323 Vol. 3 No.02 Mar 2014.

[9] M.K.Nigesh praveen kumar, A.Arul Rex “Efficient Design of Conservative Logic Based Sequential Circuits” International Journal of Research in Advent Technology, ISSN: 2321-9637, Vol.2, No.2, February 2014.

[10] K.Rekhaswathi sri, M.Mano, G.Selvapriya “Reversible Gate Based Testable Sequential Circuits" ICGITC 3297: 2007 Certified Organization) Vol.2, Special Issue 1, March 2014