Review: PVT Variation and Power Consumption in Frequency Synthesizer

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***Abstract*—** In this paper; we have reviewed different type of frequency calibration and tuning design, independent from PVT variation. Almost every frequency synthesizer faces these natural process, voltage, and temperature (PVT) variation in modern application design. Generating an accurate frequency reference is desirable, and as it often require, minimum time to achieve optimal tuning frequency and less power consumption. Hence a frequency oscillator immune to PVT variation is extremely advantageous. Unfortunately, in small scale regime of CMOS world, CMOS technology becomes susceptible toward PVT variation.

Keywords- *Process, supply voltage, and temperature (PVT) compensation, voltage controlled oscillators (VCOs).*

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I. INTRODUCTION

The major design challenges of integrated circuit comprise of a) Macroscopic and b) Microscopic. Macroscopic issues are high level of abstraction, system on a chip and design complexity. Microscopic issues are power dissipation, noise, crosstalk, and clock distribution. The sensitivity of circuit, due to technology is shrinking to sub 100nm, and process, supply voltage, and temperature (PVT) variation hinder the circuit yield and performance. Deviation in the semiconductor fabrication process leads to process variation [1][2].This introduce variation in the transistor parameter such as threshold voltage. Due to process variation different size of same parameter transistor can exist in whole chip. As a consequence, Propagation delay different everywhere in a chip, because a smaller transistor have smaller propagation delay and faster speed. Current digital

One of the disadvantage of dual chamber pacemaker is that dual chamber pacemaker consumes more energy of the battery as compared to single chamber pacemakers. Since the pacemaker operate inside the body therefore is not possible to change the battery frequently. Also it is not safe too. Due to this problem, most of the patients have no other option to buy and implant single chamber pacemakers instead of dual chamber one [5].

Therefore an improvement in dual chamber pacemakers is required to make them compete with the single chamber pacemakers on the power consumption side so that patients are able to implant dual chamber pacemakers and have it advantageous[2]. CMOS system needs 5 volts supply voltage, while portable CMOS device using 1 to 3 volts battery power supply. Temperature variation, Battery condition or component tolerances all combine to change these nominal supply voltage [1][2]. An ambient temperature drastically hampers the CMOS performance [1].

The die temperature is specified as follow:-

$$tj = ta + \theta ja \times Pd$$

tj-Junction temperature in℃.

ta-Ambient temperature in ℃.

θja- Package thermal impedence.

Pd- The power distribution.

With the growing demand of small size of device a more reliable and accurate crystal oscillator has been not a predominant approach for frequency generation. The capability of quartz crystal to meet tight spectrum requirement under PVT variation cannot compare with other oscillator (LC, ring oscillator).But for on chip stable frequency generation circuit increases the demand of other oscillator.

On chip frequency references LC oscillators have been proposed for temperature compensated [3], but their consumption of power is relatively high (~1mW or higher). In contrast, RC oscillator provides low power consumption, wide tuning range, and small area making them appealing for size-constrained on-chip oscillator application. However, they are more susceptible to PVT variation [4]. The Ring oscillator based VCO exhibits low power consumption, wide tuning range, ease of integration, and small die area. Unfortunately, the ring oscillator suffers from impacts of increasing variability.

II. PVT COMPENSATION FOR VCO

We will discuss four types of PVT variation compensation built in calibration techniques have been proposed for VCOs. We will discuss it one by one. A) Closed-loop control voltage monitoring. B) Digital counter over fixed time. C) Analog time-to-voltage conversion. D) Analog frequency to voltage conversion.

A. *Closed-loop control voltage monitoring*

This PVT compensation proposed for wireless integrated network sensor (WINS) application and operate at the 902-928 MHz ISM band [5]. In this dual loop (Figure.1) PLL frequency synthesizer, for covering entire ISM band the switched capacitor (SC) coarse tuning loop first searches for the proper frequency curve. Once found the next step, CMOS varactor is tuned to synthesize the desirable channel in the main loop. The whole synthesizer including VCO consumes 7.5 mW power. In this configuration require continuous loop operation and long settling time.

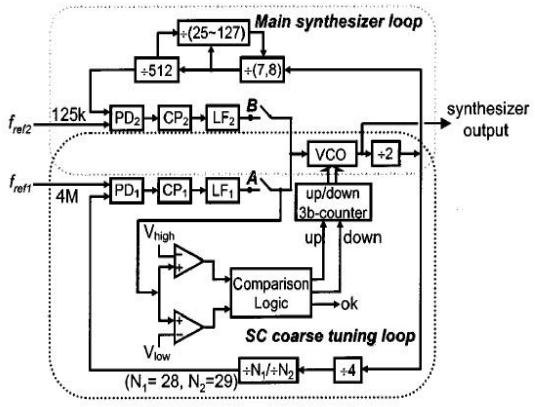

Figure 1. Frequency synthesizer schematic[5]

B. *Digital counter over fixed time*

This type of frequency synthesizer is capable of automatically adjusting the nominal center frequency of the VCO. The wide tuning range is realized by digital control (Figure 2). Process variability managed through self-calibration [6].

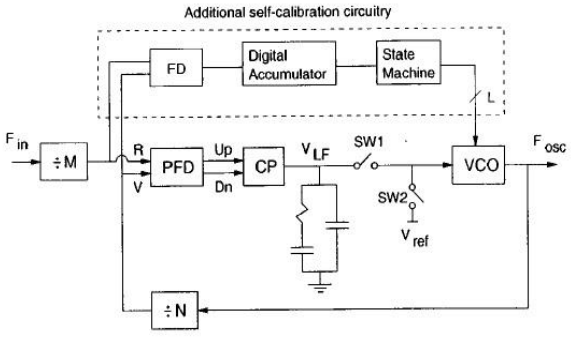

Figure 2. Self-calibrating PLL[6]

C. *Analog time-to-voltage conversion(TVC)*

This approach has the ability to track the frequency within several cycles of oscillation [7][8]. It is driven by current source Iref charging up a PF capacitor (Figure. 3). Clock is generated by a divider after the VCO, with external test controller in the measurement step. The design result show much improved PVT invariance with small power overhead. This system consume 46-µW VCO in the gigahertz range

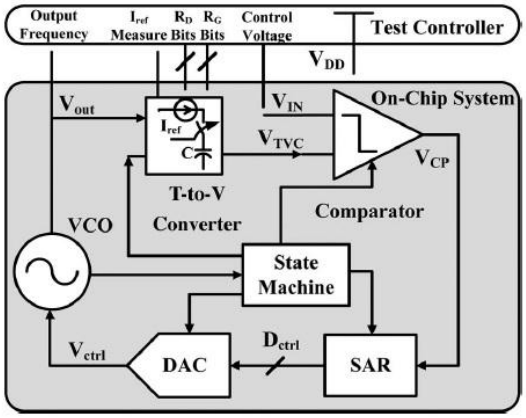

Figure 3 Self-calibrated VCO on-chip system[7]

D. *Analog frequency to voltage conversion*(FVC)

Above discuss systems are all PLL based PVT compensation system that require the use of phase detector, Low pass filter, and charge Pump. Usually, the low pass filter is not integrated on-chip but implemented externally in order to minimize the area of the on-chip PLL. To Overcome these design constraint frequency locked loop is proposed to allow the circuit fully integrated. FLL is similar to PLL that generate output signal which track input frequency instead of phase. Therefore FLL locking time would be short. Frequency comparison between two signal is completed using two FVC. The fast FVC that require small die is built upon charge redistribution (switched capacitor) and control signal are require that are derived from its inputs [9].

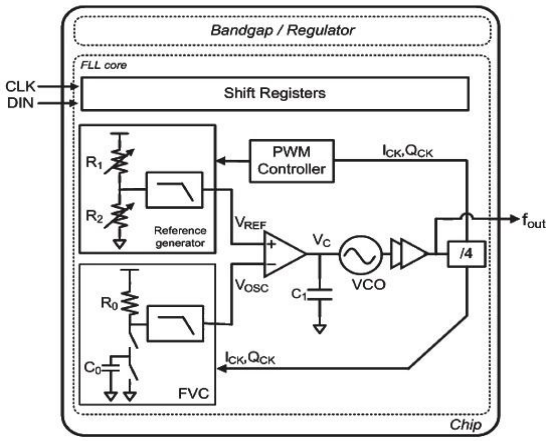

Figure 4. CMOS FLL[10]

Figure. 4 illustrates the schematic of the FVC. The switched circuit is formed by a capacitor and the transistor. The total power consumption of FLL including FVC is 325 µW at 1.2 V supply for tuning frequency range 310-420MHz[10].

III. CONCLUSION

Above discussion reveal PVT compensation is necessary for frequency synthesizer. A small variation in voltage controlled oscillator (VCO) can alter the whole time management of the chip. In addition, the oscillator must work under stringent power budget (< 100 µW) and without avoiding accurate calibration of clock frequency.

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