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Design of a CMOS Comparator using 0.18µm Technology

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Abstract- In Analog to digital convertor design converter, high speed comparator influences the overall performance of Flash/Pipeline Analog to Digital Converter (ADC) directly. This paper presents the schematic design of a CMOS comparator with high speed, low noise and low power dissipation. A schematic design of this comparator is given with 0.18µm TSMC Technology and simulated in cadence environment. Simulation results are presented and it shows that this design can work under high speed clock frequency 100MHz. The design has a low offset voltage 280.7mv, low power dissipation 0.37 mw and low noise 6.21µV.

Keywords: *CMOS Comparator, Low Power, Low Offset, High Speed clock frequency.*
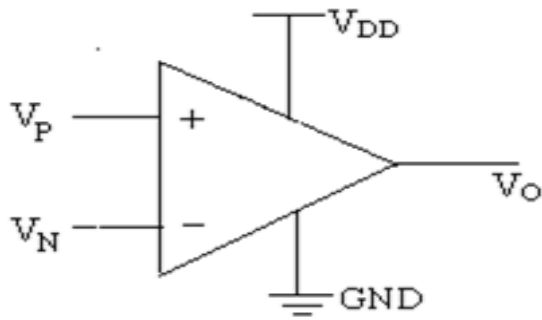
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Introduction

In ADCs, the comparator plays a main role on the overall performance. An accurate and fast comparator is a key element in any high-resolution and high speed data converter. As compared to other ADCs, pipelined ADC has merit of high speed, good precision and low power dissipation**.**

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signal to digital signals. In the analog to digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. If the + VP, the input of the comparator is at a greater potential than the –VN input, the output of the comparator is a logic 1, where as if the + input is at a potential less than the – input, the output of the comparator is at logic 0. [1-5]

In pipeline A/D converter, internal comparator must amplify small voltage into logic levels.

Depending on the algorithm use, encoding process can often be pipelined with the comparator function. Since the encoding process is faster than the comparator function, the maximum conversion rate for the ADC is limited by the response time of its comparators. Therefore, the design and optimization of the comparators is critically important [6-14]. The comparator is basically excluded from application to the high speed A/D converters with high resolution owning to its large offset voltage which significantly affects the resolution. As a consequence, the preamplifier-latch comparator topology in which an amplifier is added before a latched comparator, aiming at achieving small offset voltage and high speed, has been developed [7]. The preamplifier latch comparator, which combine of an amplifier and a latch comparator can obtain high speed and low power dissipation. Thus, by considering factor s of speed and power dissipation, preamplifier latch comparator is the choice for a pipeline ADC [8]. The proposed comparator in this paper is shown in the figure1.

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Fig.1-Comparator operation

Clock frequency and power dissipation

The clock frequency "*fc*" is defined as the reciprocal of the time interval *T*, as:

$$fc = 1/T$$

The clock frequency has to be equal or greater than twice of the frequency bandwidth of analog signals [10-11]. The power dissipated by comparator is simply the product of the sum of the current flowing in the current source with power supply voltage. We were primarily considering high speed and low voltage. Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by

$$p = fcv_{DD}{}^2$$

Where, f = output frequency,
V_{DD} = supply voltage
C = output capacitance

If a square pulse is applied to the input of the comparator with a period t and frequency *f,* the average amount of current that the comparator must pull from $V_{DD,}$ recalling the current is being supplied from V_{DD} only when p-channel is on. Notice that the power dissipation is a function of the clock frequency. A great deal of effort is put into reducing the power dissipation in CMOS circuits. One of the major advantages of dynamic logic is its power dissipation.

SCHEMATIC DESIGN OF COMPARATOR

We have implemented a Precision comparator and digital correction is applied to minimize offset error of comparator and get better output of ADC. In most cases comparators uses positive feedback to force a fast decision. The fundamental circuit often is a latch, which consists of two inverters, where each output is connected with the input of the other one (cross-coupled inverters). With a reset switch such a latch is forced into a meta stable state. When releasing reset the latch flips into one of the two stable states.

The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time. If the propagation delay time is determined by the slew rate of the comparator, then this time can be calculated as:

$$t_p = \Delta T = \frac{\Delta V}{SR} = \frac{V_{OH} - V_{OL}}{2SR}$$

Where, tp or ΔT = propagation delay
ΔV = Change of the voltage at the output of the comparator
SR = Slew rate
VOH = Upper limit of the comparator
VOL = Lower limit of the comparator

Slew rate is a large-signal behavior that sets the maximum rate of output change. It is limited by the output driving capability of the comparator. The propagation delay is inversely proportional to the input voltage applied. This means that applying a larger input voltage will improve the propagation delay, up to the limits set by the slew rate

Figure-2 presents the schematic view of the design comparator. The design can perform operation when clock (Clk) is low, the comparator is reset, and at this time Clk1 is high, comparator can receive the amplified signal of preamplifier. The use of a clock

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eliminates the need for an output buffer used in level shifting the output of the decision circuit. The discrepant voltage of loading in NM0 and NM6 compares the one of the loading in NM7 and NM5. Two ports produce different current, after the current passing through the common gate stage, which is connected two output of preamplifier, and produces a voltage difference (vout+, vout-), which is sent into of comparator. When clk is high, the comparator start to work, and the voltage difference (vout+, vout-) will be amplified by the crossing plus feedback loop, and later comparator will keep the state until clk becomes low.
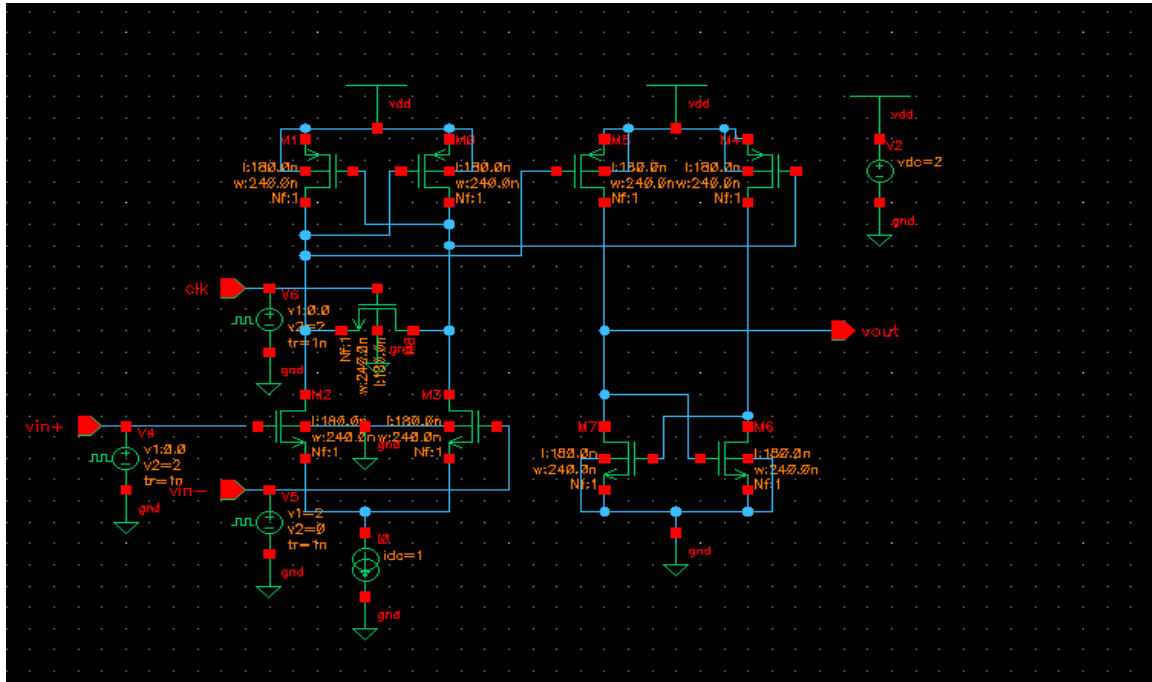

Figure2: Schematic view of CMOS comparator

SIMULATION RESULTS

Simulation of the present design has been done using the 0.18 μm CMOS technology under the 2V power supply by Cadence specter.

This design can directly used in an 8-bit pipeline ADCs, which first stage is a 1 bit switched capacitor pipeline ADC. Present results are included offset voltage, power dissipation, clock frequency and Gain calculation, which based on 0.18μm Technology. The circuit operates with a single 2.0 V power supply. From Fig.6 we can obtain that the offset voltage of comparator was reduced to approximate 280.7nV and power dissipation was 0.37 mW.

As the clock frequency of comparator is achieved 100MHz and clock period was 10ns can be used where Low power, high speed and Low offset voltage is the main requirements and it is very much useful for ADC designer. Finally simulation results of the comparator are shown in Fig. 3, Fig. 4 and 5 respectively. Table 1 has given the comparison of present work with earlier reported work and observed some improvement.

Table 1: Comparison of present results with earlier Reported work

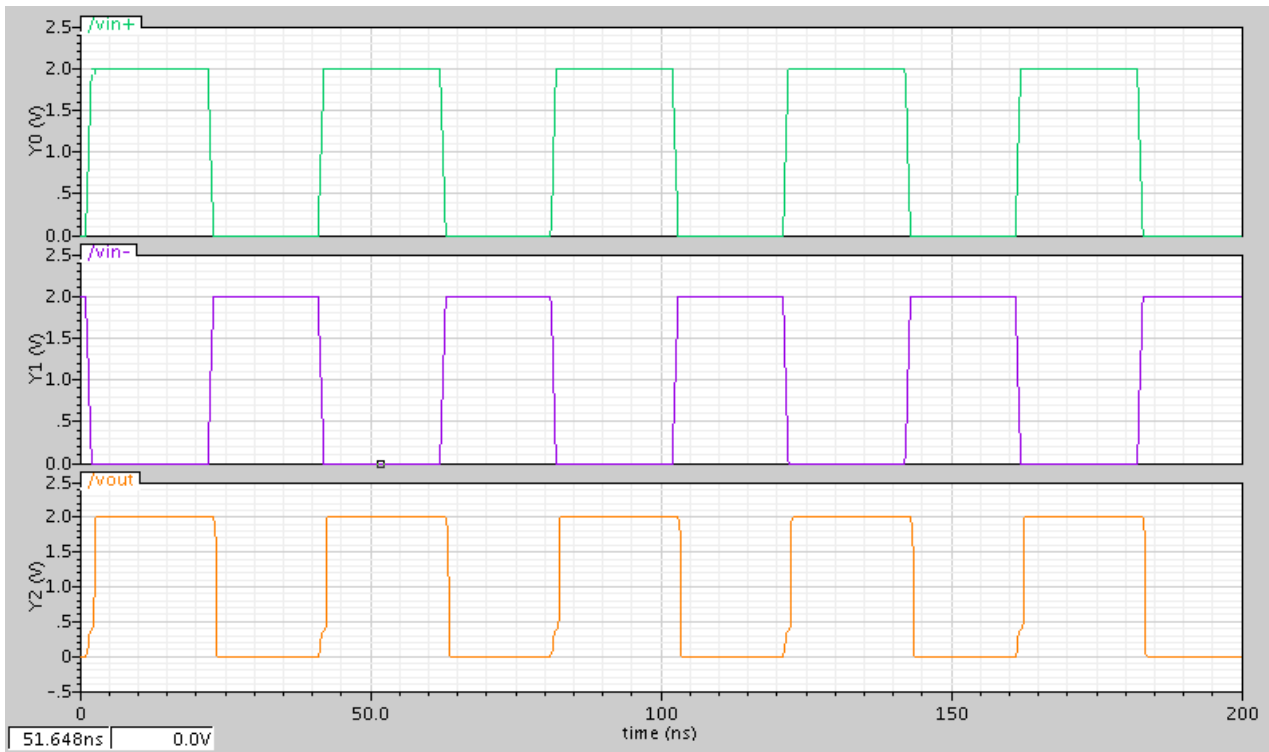| Parameters	Ref.[12]	Ref.[13]	This work
power supply	5V	2.5V	2V
Clock frequency	100MHz	10MHz	100MHz
Offset voltage	6.5 mV	280μV	280.7 mV
Power dissipation	0.49 mW	1.8mW	0.37 mW
Technology	0.35μm	1μm	0.18μm

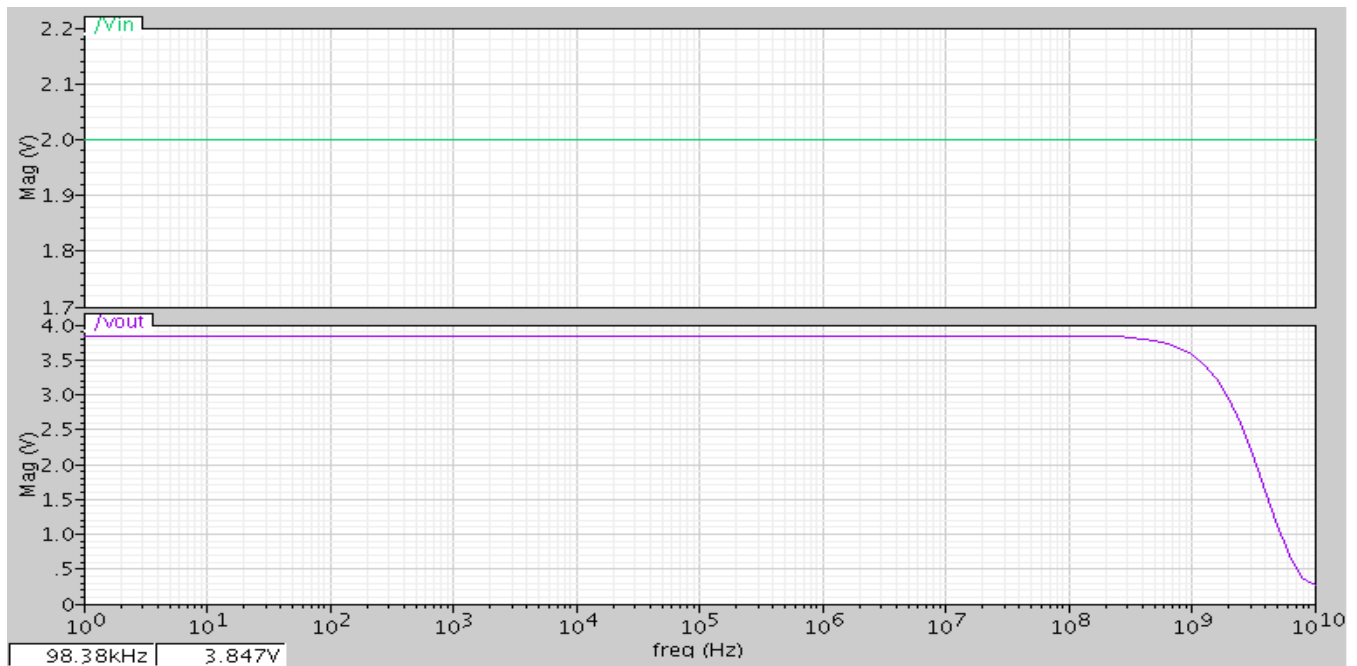**Figure3: Transient response of comparator**

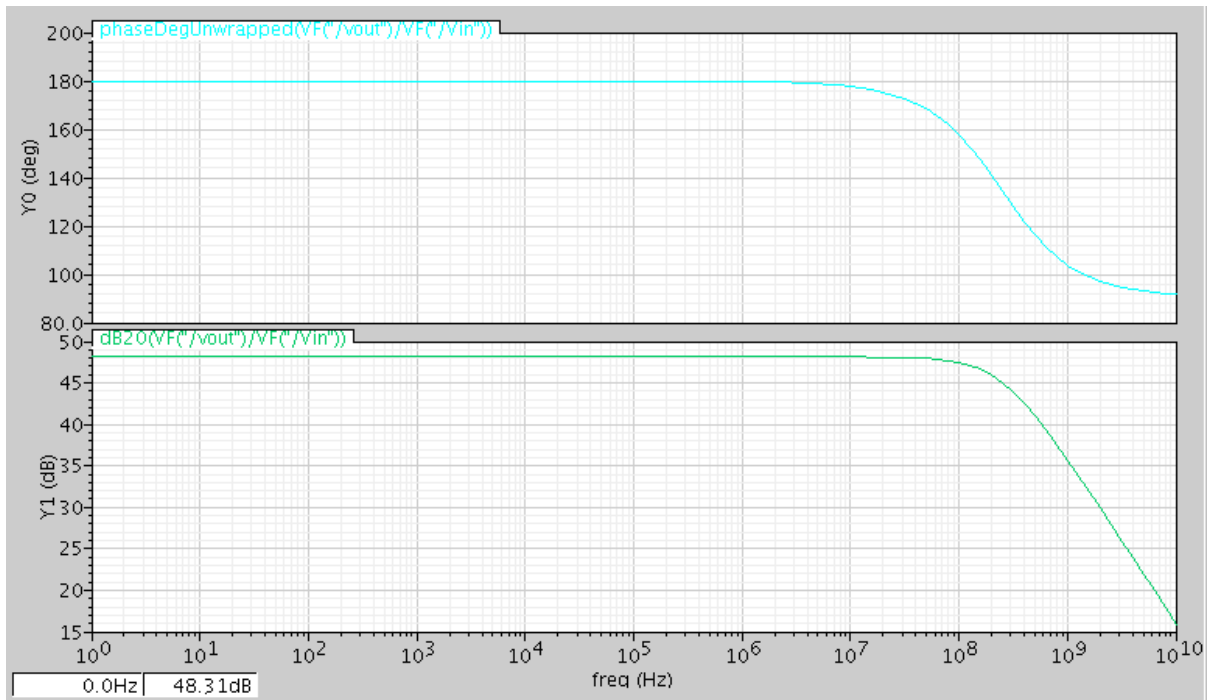**Figure4: AC response of comparator**
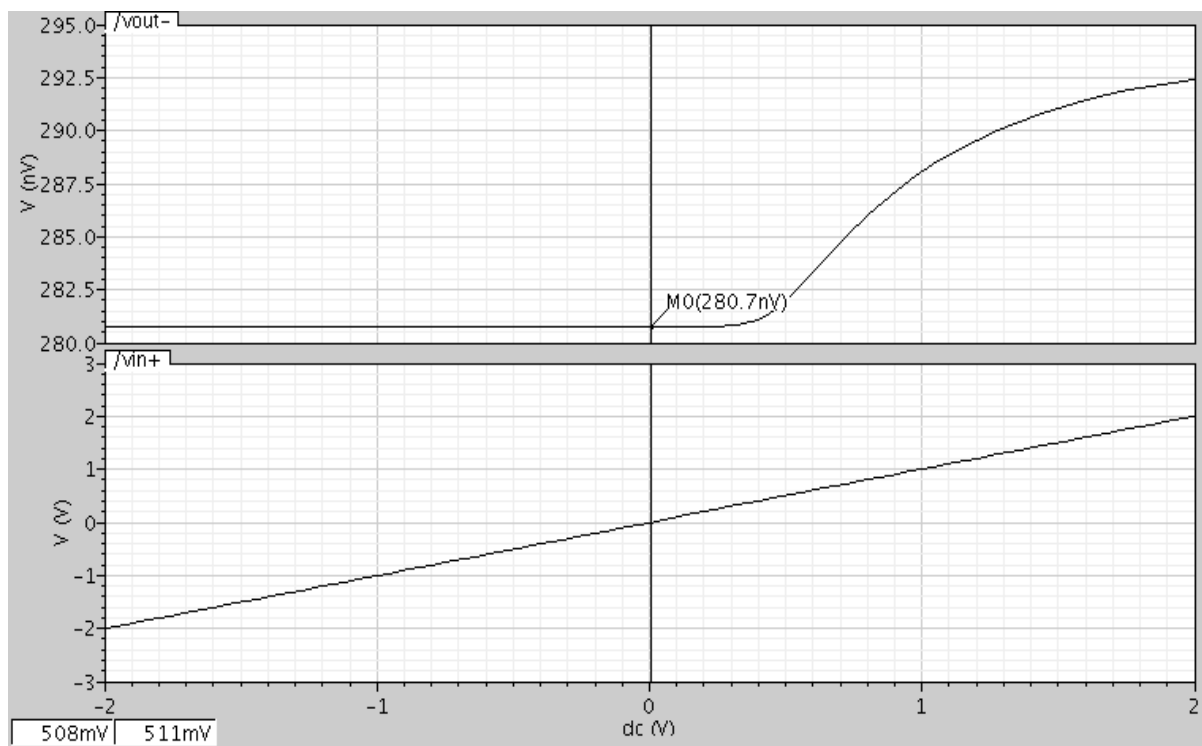
Figure5: Gain of comparator

Figure 6: Simulation results of offset voltage

CONCLUSION

A CMOS comparator design and optimized procedure has been developed for use in a pipeline ADC. A single comparator has been built and tested. It operated low power dissipation 0.37 mW.

The comparator is designed and simulated cadence spectre in 0.18μm CMOS Technology. Simulation results show that the circuit can work under as high clock frequency as 100MHz and its maximum offset voltage is

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about 280.7 nV. In this design we compare our results and observed that present results have improvement as shown in table 1. This design will be very beneficial for ADC designer & young researcher.

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